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AK4613

4/12-Channel Audio CODEC

GENERAL DESCRIPTION

The AK4613 is a single chip audio CODEC that includes four ADC channels and twelve DAC channels. The converters are designed with Enhanced Dual Bit architecture for the ADC's, and Advanced Multi-Bit architecture for the DAC, enabling very low noise performance. Fabricated on a low power process, the AK4613 operates off of a +3.3V analog supply and a +1.8V digital supply. The AK4613 supports both single-ended and differential inputs and outputs. A wide range of applications can be realized, including home theater, pro audio and car audio. The AK4613 is available in an 80-pin LQFP package.

FEATURES

1. 4channel 24bit ADC
- **128x Oversampling**
- **Linear Phase Digital Anti-Alias Filter**
- **Analog Anti-Alias Filter for Single-Ended Input and Differential Input**
- **ADC S/(N+D)**
  - **92dB: Single-Ended Input**
  - **97dB: Differential Input**
- **ADC DR, S/N**
  - **103dB: Single-Ended Input**
  - **104dB: Differential Input**
- **Digital HPF for offset cancellation**
- **I/F format: MSB justified, I^2S or TDM**
- **Overflow flag**

2. 12channel 24bit DAC
- **128x Oversampling**
- **Linear Phase 24bit 8 times Digital Filter**
- **Analog Smoothing Filter for Single-Ended Output**
- **DAC S/(N+D)**
  - **94dB: Single-Ended Output**
  - **100dB: Differential Output**
- **DAC DR, S/N**
  - **105dB: Single-Ended Output**
  - **108dB: Differential Output**
- **Individual channel digital volume with 256 levels and 0.5dB steps**
- **Soft mute**
- **De-emphasis for 32kHz, 44.1kHz and 48kHz**
- **Zero Detect Function**
- **I/F format: MSB justified, LSB justified (16bit, 20bit, 24bit), I^2S or TDM**

3. Sampling Frequency
- **Normal Speed Mode: 32kHz to 48kHz**
- **Double Speed Mode: 64kHz to 96kHz**
- **Quad Speed Mode: 128kHz to 192kHz**

4. Master / Slave mode

5. Master clock
- **Slave mode: 256fs, 384fs or 512fs (Normal Speed Mode: fs=32kHz ~ 48kHz)**
  256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
  128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)
- **Master mode: 256fs or 512fs (Normal Speed Mode: fs=32kHz ~ 48kHz)**
  256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
  128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)

6. 4-wire Serial and I^2C Bus µP I/F for mode setting

7. Power Supply
- **Analog Power Supply: AVDD1, AVDD2 = 3.0 ~ 3.6V**
- **Digital Power Supply: DVDD = 1.6 ~ 2.0V**
- **I/O Buffer Power Supply: TVDD1, TVDD2 = 1.6 ~ 3.6V**

8. Power Supply Current : 100mA (fs=48kHz)

9. Ta = -20 ~ 85°C (AK4613EQ), - 40 ~ 105°C (AK4613VQ)

10. Package: 80pin LQFP (0.5mm pitch)

■ Block Diagram

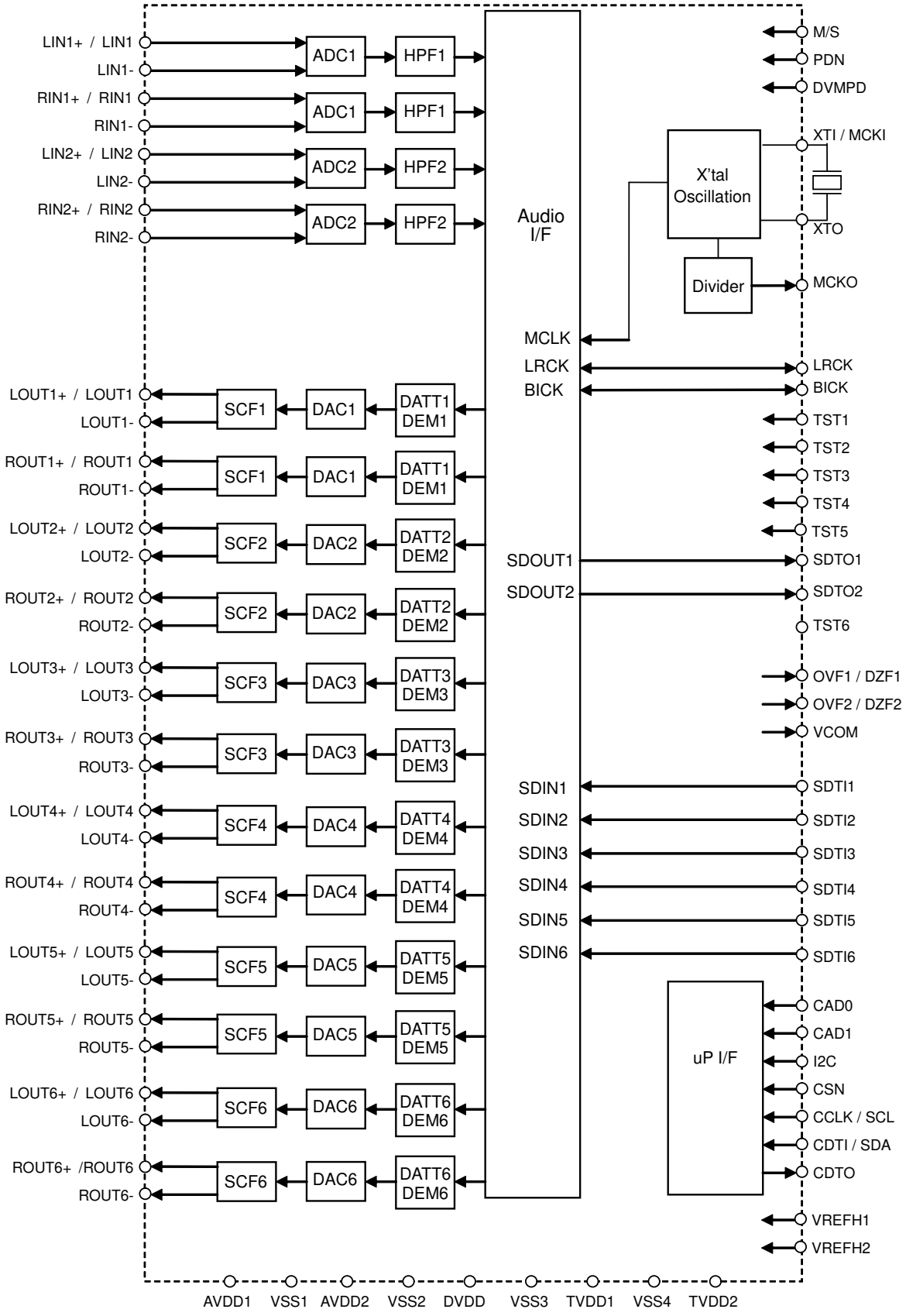

Figure 1. Block Diagram

■ Ordering Guide

AK4613EQ	-20 ~ +85°C	80pin LQFP(0.5mm pitch)
AK4613VQ	-40 ~ +105°C	80pin LQFP(0.5mm pitch)
AKD4613	Evaluation Board for AK4613	

■ Pin Layout

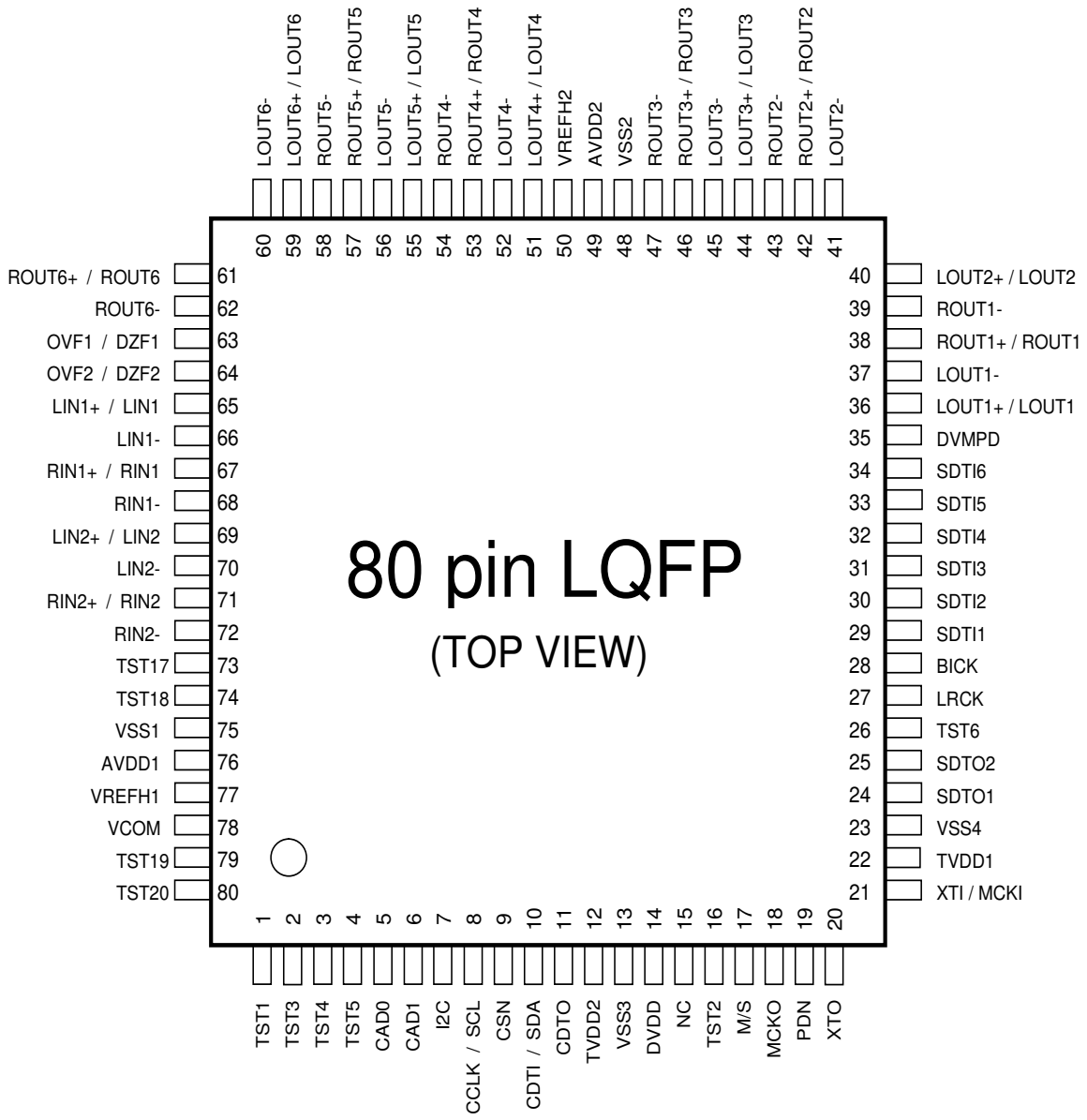

Figure 2. Pin Layout

■ Compatibility with AK4628

1. Functions

Function	AK4628	AK4613
Number of ADC channel	2-channel	4-channel
Number of DAC channel	8-channel	12-channel
Input	Single	Single or Diff
Output	Single	Single or Diff
I/F Format	I2S, LJ, RJ(20/24bit), TDM	I2S, LJ, RJ(16/20/24bit), TDM
TDM512	No	Fs=48kHz
XTAL OSC	No	Yes
Parallel / Serial Select Pin	Yes	No
Control Data Output Pin	No	Yes
Ta	-40 ~ +85°C	-40 ~ +105°C
Package	44pinLQFP	80pinLQFP

2. Power Supply

Voltage Name	AK4628	AK4613
AVDD	4.5 ~ 5.5V	No
AVDD1	No	3.0 ~ 3.6V
AVDD2	No	3.0 ~ 3.6V
DVDD	4.5 ~ 5.5V	1.6 ~ 2.0V
TVDD	2.7 ~ 5.5V	No
TVDD1	No	1.6 ~ 3.6V
TVDD2	No	1.6 ~ 3.6V

3. Specification

Parameter	AK4628	AK4613
Fs (AD/DA)	96k / 192k	192k / 192k
THD+N (AD/DA)	Single: 92 / 90 Differential : - / -	Single: 92 / 94 Differential : 97 / 100
S/N (AD/DA)	Single: 102 / 106 Differential : - / -	Single: 103 / 105 Differential: 104 / 108
Output DATT	128 level	256 level
µP I/F	100k I2C, 3wire	400k I2C, 4wire

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	TST1	I	Test Pin This pin must be connected to VSS4
2	TST3	I	Test Pin This pin must be connected to TVDD2.
3	TST4	I	Test Pin This pin must be connected to TVDD2.
4	TST5	I	Test Pin This pin must be connected to VSS4.
5	CAD0	I	Chip Address 0 Pin
6	CAD1	I	Chip Address 1 Pin
7	I2C	I	µP I/F Mode Select Pin "L": 4-wire Serial, "H": I^2C Bus
8	CCLK	I	Control Data Clock Pin in serial control mode I2C = "L": CCLK (4-wire Serial)
	SCL	I	Control Data Clock Pin in serial control mode I2C = "H": SCL (I^2C Bus)
9	CSN	I	Chip Select Pin in 4-wire serial control mode This pin must be connected to TVDD2 at I^2C bus control mode
10	CDTI	I	Control Data Input Pin in serial control mode I2C = "L": CDTI (4-wire Serial)
	SDA	I/O	Control Data Input Pin in serial control mode I2C = "H": SDA (I^2C Bus)
11	CDTO	O	Control Data Output Pin in 4-wire serial control mode
12	TVDD2	-	Input / Output Buffer Power Supply 1 Pin, 1.6V~3.6V
13	VSS3		Ground Pin, 0V
14	DVDD	-	Digital Power Supply Pin, 1.6V~2.0V
15	NC	-	No Connection. No internal bonding. This pin must be connected to the ground.
16	TST2	I	Test Pin This pin must be connected to VSS4.
17	M/S	I	Master Mode Select Pin "L": Slave Mode "H": Master Mode
18	MCKO	O	Master Clock Output Pin
19	PDN	I	Power-Down & Reset Pin When "L", the AK4613 is powered-down and the control registers are reset to default state. If the state of CAD1-0 changes, then the AK4613 must be reset by PDN.
20	XTO	O	X'tal Output Pin
21	XTI	I	X'tal Input Pin
	MCKI	I	External Master Clock Input Pin
22	TVDD1	-	Input / Output Buffer Power Supply 1 Pin, 1.6V~3.6V
23	VSS4	-	Digital Ground Pin, 0V
24	SDTO1	O	Audio Serial Data Output 1 Pin
25	SDTO2	O	Audio Serial Data Output 2 Pin
26	TST6	O	Test Pin This pin must be open.
27	LRCK	I/O	Input /Output Channel Clock Pin
28	BICK	I/O	Audio Serial Data Clock Pin
29	SDTI1	I	Audio Serial Data Input 1 Pin
30	SDTI2	I	Audio Serial Data Input 2 Pin
31	SDTI3	I	Audio Serial Data Input 3 Pin
32	SDTI4	I	Audio Serial Data Input 4 Pin
33	SDTI5	I	Audio Serial Data Input 5 Pin
34	SDTI6	I	Audio Serial Data Input 6 Pin

No.	Pin Name	I/O	Function
35	DVMPD	I	DAC output VCOM voltage power down pin "L": DAC outputs are VCOM voltage "H": DAC outputs are Hi-Z.
36	LOUT1+	O	Lch Analog Positive Output 1 Pin (DOE1 bit = "H")
	LOUT1	O	Lch Analog Output 1 Pin (DOE1 bit = "L")
37	LOUT1-	O	Lch Analog Negative Output 1 Pin (When DOE1 bit = "L", this pin must be open.)
38	ROUT1+	O	Rch Analog Positive Output 1 Pin (DOE1 bit = "H")
	ROUT1	O	Rch Analog Output 1 Pin (DOE1 bit = "L")
39	ROUT1-	O	Rch Analog Negative Output 1 Pin (When DOE1 bit = "L", this pin must be open.)
40	LOUT2+	O	Lch Analog Positive Output 2 Pin (DOE2 bit = "H")
	LOUT2	O	Lch Analog Output 2 Pin (DOE2 bit = "L")
41	LOUT2-	O	Lch Analog Negative Output 2 Pin (When DOE2 bit = "L", this pin must be open.)
42	ROUT2+	O	Rch Analog Positive Output 2 Pin (DOE2 bit = "H")
	ROUT2	O	Rch Analog Output 2 Pin (DOE2 bit = "L")
43	ROUT2-	O	Rch Analog Negative Output 2 Pin (When DOE2 bit = "L", this pin must be open.)
44	LOUT3+	O	Lch Analog Positive Output 3 Pin (DOE3 bit = "H")
	LOUT3	O	Lch Analog Output 3 Pin (DOE3 bit = "L")
45	LOUT3-	O	Lch Analog Negative Output 3 Pin (When DOE3 bit = "L", this pin must be open.)
46	ROUT3+	O	Rch Analog Positive Output 3 Pin (DOE3 bit = "H")
	ROUT3	O	Rch Analog Output 3 Pin (DOE3 bit = "L")
47	ROUT3-	O	Rch Analog Negative Output 3 Pin (When DOE3 bit = "L", this pin must be open.)
48	VSS2	-	Ground Pin, 0V
49	AVDD2	-	Analog Power Supply Pin, 3.0V~3.6V
50	VREFH2	I	Positive Voltage Reference Input Pin, AVDD2
51	LOUT4+	O	Lch Analog Positive Output 4 Pin (DOE4 bit = "H")
	LOUT4	O	Lch Analog Output 4 Pin (DOE4 bit = "L")
52	LOUT4-	O	Lch Analog Negative Output 4 Pin (When DOE4 bit = "L", this pin must be open.)
53	ROUT4+	O	Rch Analog Positive Output 4 Pin (DOE4 bit = "H")
	ROUT4	O	Rch Analog Output 4 Pin (DOE4 bit = "L")
54	ROUT4-	O	Rch Analog Negative Output 4 Pin (When DOE4 bit = "L", this pin must be open.)
55	LOUT5+	O	Lch Analog Positive Output 5 Pin (DOE5 bit = "H")
	LOUT5	O	Lch Analog Output 5 Pin (DOE5 bit = "L")
56	LOUT5-	O	Lch Analog Negative Output 5 Pin (When DOE5 bit = "L", this pin must be open.)
57	ROUT5+	O	Rch Analog Positive Output 5 Pin (DOE5 bit = "H")
	ROUT5	O	Rch Analog Output 5 Pin (DOE5 bit = "L")
58	ROUT5-	O	Rch Analog Negative Output 5 Pin (When DOE5 bit = "L", this pin must be open.)
59	LOUT6+	O	Lch Analog Positive Output 6 Pin (DOE6 bit = "H")
	LOUT6	O	Lch Analog Output 6 Pin (DOE6 bit = "L")
60	LOUT6-	O	Lch Analog Negative Output 6 Pin (When DOE6 bit = "L", this pin must be open.)
61	ROUT6+	O	Rch Analog Positive Output 6 Pin (DOE6 bit = "H")
	ROUT6	O	Rch Analog Output 6 Pin (DOE6 bit = "L")
62	ROUT6-	O	Rch Analog Negative Output 6 Pin (When DOE6 bit = "L", this pin must be open.)
63	OVF1	O	Analog Input Overflow Detect 1 Pin (Note 1) This pin goes to "H" if the analog input of Lch or Rch overflows.
	DZF1	O	Zero Input Detect 1 Pin (Note 2) When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". And when RSTN bit is "0", PMDAC bit is "0", this pin goes to "H".
64	OVF2	O	Analog Input Overflow Detect 2 Pin (Note 1) This pin goes to "H" if the analog input of Lch or Rch overflows.
	DZF2	O	Zero Input Detect 2 Pin (Note 2) When the input data of the group 2 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". And when RSTN bit is "0", PMDAC bit is "0", this pin goes to "H".
65	LIN1+	I	Lch Analog Positive Input 1 Pin (DIE1 bit = "H")
	LIN1	I	Lch Analog Input 1 Pin (DIE1 bit = "L")
66	LIN1-	-	Lch Analog Negative Input 1 Pin (When DIE1 bit = "L", this pin must be open.) (Note 3)

No.	Pin Name	I/O	Function
67	RIN1+	I	Rch Analog Positive Input 1 Pin (DIE1 bit = "H")
	RIN1	I	Rch Analog Input 1 Pin (DIE1 bit = "L")
68	RIN1-	-	Rch Analog Negative Input 1 Pin (When DIE1 bit = "L", this pin must be open.) (Note 3)
69	LIN2+	I	Lch Analog Positive Input 2 Pin (DIE2 bit = "H")
	LIN2	I	Lch Analog Input 2 Pin (DIE2 bit = "L")
70	LIN2-	-	Lch Analog Negative Input 2 Pin (When DIE2 bit = "L", this pin must be open.) (Note 3)
71	RIN2+	I	Rch Analog Positive Input 2 Pin (DIE2 bit = "H")
	RIN2	I	Rch Analog Input 2 Pin (DIE2 bit = "L")
72	RIN2-	-	Rch Analog Negative Input 2 Pin (When DIE2 bit = "L", this pin must be open.) (Note 3)
73	TST17	I	Test Pin This pin must be open.
74	TST18	I	Test Pin This pin must be open.
75	VSS1	-	Ground Pin, 0V
76	AVDD1	-	Analog Power Supply Pin, 3.0V~3.6V
77	VREFH1	I	Positive Voltage Reference Input Pin, AVDD1
78	VCOM	O	Common Voltage Output Pin, AVDD1x1/2 Large external capacitor around 2.2µF is used to reduce power-supply noise.
79	TST19	I	Test Pin This pin must be open.
80	TST20	I	Test Pin This pin must be open.

Note 1. This pin becomes OVF pin when OVFE bit is set to "1".
Note 2. This pin becomes DZF pin when OVFE bit is set to "0".
Note 3. This pin becomes analog negative input pin in differential input mode, and becomes output pin invert the positive input pin in single-end input mode. This pin must be open in single-end input mode.
Note 4. All digital input pins except for pull-down must not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4=0V; Note 5)

Parameter		Symbol	min	max	Unit
Power Supplies	Analog	AVDD1,2	-0.3	4.2	V
	Digital	DVDD	-0.3	2.2	V
	Output buffer	TVDD1,2	-0.3	4.2	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD1,2+0.3	V
Digital Input Voltage (TST2,M/S,PDN,XTI/MCKI,LRCK,BICK, SDTI1,SDTI2,SDTI3,SDTI4,SDTI5,SDTI6, DVMPD pins)		VIND1	-0.3	TVDD1+0.3	V
(TST1,TST3,TST4,TST5,CAD0,CAD1,I2C, CCLK/SCL,CSN,CDTI/SDA pins)		VIND2	-0.3	TVDD2+0.3	V
Ambient Temperature (power applied)	AK4613EQ	Ta	-20	85	°C
	AK4613VQ	Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 5. All voltages with respect to ground. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog ground plane. AVDD1 and AVDD2 must be the same voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=0V; Note 5)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 6)	Analog	AVDD1,2	3.0	3.3	3.6	V
	Digital	DVDD	1.6	1.8	2.0	V
	I/O buffer 1 (Stereo Mode & Normal Speed Mode)	TVDD1	DVDD	3.3	3.6	V
	I/O buffer 1 (Except Stereo Mode & Normal Speed Mode)	TVDD1	3.0	3.3	3.6	V
	I/O buffer 2	TVDD2	DVDD	3.3	3.6	V

Note 6. The power up sequence between AVDD1, AVDD2, DVDD, TVDD1 and TVDD2 is not critical. Each power supplies should be powered up during the PDN pin = "L". The PDN pin should be "H" after all power supplies are powered up. All power supplies should be powered on, only a part of these power supplies cannot be powered off. (Power off means power supplies equal to ground or power supplies are floating.) Do not turn off only the AK4613 under the condition that a surrounding device is powered on and the I2C bus is in use.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD1=AVDD2=TVDD1=TVDD2=3.3V, DVDD =1.8V; VSS1=VSS2=0V; VREFH1=AVDD1, VREFH2=AVDD2; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at 48kHz, 20Hz~40kHz at fs=96kHz, 20Hz~40kHz at fs=192kHz; unless otherwise specified)

Parameter			min	typ	max	Unit
ADC Analog Input Characteristics (single inputs)						
Resolution					24	Bits
S/(N+D)	fs=48kHz BW=20kHz	-1dBFS	84	92		dB
		-60dBFS		40		
	fs=96kHz BW=40kHz	-1dBFS	83	91		dB
		-60dBFS		37		
	fs=192kHz BW=40kHz	-1dBFS		91		
		-60dBFS		37		
DR	(-60dBFS with A-weighted)		95	103		dB
S/N	(A-weighted)		95	103		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				40	-	ppm/°C
Input Voltage	AIN=0.65xVREFH1		1.94	2.15	2.37	Vpp
Input Resistance			7	9		kΩ
Power Supply Rejection		(Note 7)		50		dB
ADC Analog Input Characteristics (differential inputs)						
S/(N+D)	fs=48kHz BW=20kHz	-1dBFS	88	97		dB
		-60dBFS		40		dB
	fs=96kHz BW=40kHz	-1dBFS	86	94		
		-60dBFS		37		
	fs=192kHz BW=40kHz	-1dBFS		94		
		-60dBFS		37		
DR	(-60dBFS with A-weighted)		96	104		dB
S/N	(A-weighted)		96	104		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				40	-	ppm/°C
Input Voltage	AIN=0.65xVREFH1	(Note 8)	±1.94	±2.15	±2.37	Vpp
Input Resistance			11	13		kΩ
Power Supply Rejection		(Note 7)		50		dB
Common Mode Rejection Ratio (CMRR)		(Note 9)	74			dB
DAC Analog Output Characteristics (single outputs)						
Resolution					24	Bits
S/(N+D)	fs=48kHz BW=20kHz	0dBFS	84	94		dB
		-60dBFS		44		
	fs=96kHz BW=40kHz	0dBFS	86	92		
		-60dBFS		41		
	fs=192kHz BW=40kHz	0dBFS		92		
		-60dBFS		41		
DR	(-60dBFS with A-weighted)		97	105		dB
S/N	(A-weighted)		97	105		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				20	-	ppm/°C
Output Voltage	AOUT=0.63xVREFH2		1.87	2.08	2.29	Vpp
Load Resistance		(AC Load)	5			kΩ
Load Capacitance					30	pF
Power Supply Rejection		(Note 7)		50		dB

DAC Analog Output Characteristics (differential outputs)						
S/(N+D)	fs=48kHz BW=20kHz	0dBFS	90	100		dB
		-60dBFS		45		
	fs=96kHz BW=40kHz	0dBFS	88	98		
		-60dBFS		42		
	fs=192kHz BW=40kHz	0dBFS		98		
		-60dBFS		42		
DR (-60dBFS with A-weighted)			100	108		dB
S/N (A-weighted)			100	108		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20	-	ppm/°C
Output Voltage	AOUT=0.63xVREFH2 (Note 8)		±1.87	±2.08	±2.29	Vpp
Load Resistance (Note 10)			2			kΩ
Load Capacitance					30	pF
Power Supply Rejection (Note 7)				50		dB

Note 7. PSR is applied to AVDD1, AVDD2, DVDD, TVDD1 and TVDD2 with 1kHz, 50mVpp. VREFH1 and VREFH2 pins are held a constant voltage +3.3V.

Note 8. This value is (LIN+) – (LIN-) and (RIN+) – (RIN-). The voltage is proportional to VREFH1, VREFH2 voltage.

Note 9. VREFH1 and VREFH2 are held +3.3V, the input bias voltage is set to AVDD1, 2 x 0.5. The 1kHz, 0.96Vpp signal is applied to LIN- and LIN+ with same phase (e.g. shorted) or RIN- and RIN+. The CMRR is measured as the attenuation level from 0dB = -7dBFS (since the normal 0.96Vpp = -7dBFS). This value is guaranteed but not tested.

Note 10. For AC-load. In the case of DC-load is 5kΩ.

Note 11. This value is Load Capacitance for output pin to GND. In differential mode, this value should be estimated to be twice, because Load Capacitance exists to GND and between the differential pin.

Parameter		min	typ	max	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
AVDD1+AVDD2	fs=48kHz, 96kHz, 192kHz		80.0	125.0	mA
DVDD	fs=48kHz		14.0	24.0	mA
	fs=96kHz		20.0	35.0	mA
	fs=192kHz		33.0	55.0	mA
TVDD1+TVDD2	fs=48kHz		6.0	8.0	mA
	fs=96kHz		7.0	9.5	mA
	fs=192kHz		7.0	9.5	mA
Power-down mode					
(PDN pin = "L", DVMPD = " L") (Note 12)					
AVDD1+AVDD2+DVDD+TVDD1+TVDD2			300	550	µA
(PDN pin = "L", DVMPD = " H") (Note 12)					
AVDD1+AVDD2+DVDD+TVDD1+TVDD2			10	200	µA

Note 12. In the power-down mode, all digital input pins including clock pins are held VSS3 (TST1, TST3, TST4, TST5, CAD0, CAD1, I2C, CSN, CCLK, CDTI pins), VSS4 (TST2, M/S, MCKI, LRCK, BICK, SDTI1, SDTI2, SDTI3, SDTI4,SDTI5, SDTI6).

FILTER CHARACTERISTICS (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD1=AVDD2=3.0~ 3.6V, DVDD=1.6~ 2.0V, TVDD1=TVDD2=1.6~ 3.6V; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 13)	±0.1dB	PB	0	-	18.9	kHz
	−0.2dB		-	20.0	-	kHz
	−3.0dB		-	23.0	-	kHz
Stopband (Note 13)		SB	28	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	16	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 13)	−3dB	FR	-	1.0	-	Hz
	−0.1dB		-	6.5	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 13)	±0.06dB	PB	0	-	21.8	kHz
	−6.0dB		-	24.0	-	kHz
Stopband (Note 13)		SB	26.2	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	22	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response (Note 15)	20kHz	FR	-	-0.1	-	dB

FILTER CHARACTERISTICS (fs=96kHz)

(Ta= -40 ~ +105°C; AVDD1=AVDD2=3.0~ 3.6V, DVDD=1.6~ 2.0V, TVDD1=TVDD2=1.6~ 3.6V; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 13)	±0.1dB	PB	0	-	37.8	kHz
	−0.2dB		-	40.0	-	kHz
	−3.0dB		-	46.0	-	kHz
Stopband (Note 13)		SB	56	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	16	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 13)	−3dB	FR	-	2.0	-	Hz
	−0.1dB		-	13.0	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 13)	±0.06dB	PB	0	-	43.6	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 13)		SB	52.4	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	22	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response (Note 15)	40kHz	FR	-	-0.3	-	dB

FILTER CHARACTERISTICS (fs=192kHz)

(Ta= -40 ~ +105°C; AVDD1=AVDD2=3.0~ 3.6V, DVDD=1.6~ 2.0V, TVDD1=TVDD2=1.6~ 3.6V; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 13)	±0.1dB	PB	0	-	56.6	kHz
	−0.2dB		-	57.0	-	kHz
	−3.0dB		-	90.3	-	kHz
Stopband (Note 13)		SB	112	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	16	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 13)	−3dB	FR	-	4.0	-	Hz
	−0.1dB		-	26.0	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 13)	±0.06dB	PB	0	-	87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 13)		SB	104.9	-	-	kHz
Passband Ripple		PR	-	-	±0.06	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	22	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response (Note 15)	80kHz	FR	-	-1	-	dB

Note 13. The passband and stopband frequencies scale with fs (sampling frequency). For example, ADC: Passband (±0.1dB) = 0.39375 x fs (@ fs=48kHz), DAC: Passband (±0.06dB) = 0.45412 x fs.

Note 14. The calculated delay time is resulting from digital filtering. For the ADC, this time is from the input of an analog signal to the setting of 24bit data for both channels to the ADC output register. For the DAC, this time is from setting the 24 bit data both channels at the input register to the output of an analog signal.

Note 15. The reference frequency is 1kHz.

DC CHARACTERISTICS

(Ta=-40°C~+105°C; AVDD1=AVDD2=3.0~3.6; DVDD=1.6~2.0V; TVDD1=TVDD2=1.6~3.6V)

Parameter	Symbol	min	typ	max	Unit
TVDD1,TVDD2 ≤2.2V					
High-Level Input Voltage					
(TST2, M/S, PDN, MCKI, LRCK, BICK, SDTI1, SDTI2, SDTI3, SDTI4,SDTI5, SDTI6, DVMPD pins)	VIH	80%TVDD1	-	-	V
(TST1,TST3,TST4,TST5,CAD0,CAD1,I2C, CSN,CCLK, CDTI pins)	VIH	80%TVDD2	-	-	V
Low-Level Input Voltage					
(TST2, M/S, PDN, MCKI, LRCK, BICK, SDTI1, SDTI2, SDTI3, SDTI4,SDTI5, SDTI6, DVMPD pins)	VIL	-	-	20%TVDD1	V
(TST1,TST3,TST4,TST5,CAD0,CAD1,I2C, CSN,CCLK, CDTI pins)	VIL	-	-	20%TVDD2	V
TVDD1,TVDD2 > 2.2V					
High-Level Input Voltage					
(TST2, M/S, PDN, MCKI, LRCK, BICK, SDTI1, SDTI2, SDTI3, SDTI4,SDTI5, SDTI6, DVMPD pins)	VIH	70%TVDD1	-	-	V
(TST1,TST3,TST4,TST5,CAD0,CAD1,I2C, CSN,CCLK, CDTI pins)	VIH	70%TVDD2	-	-	V
Low-Level Input Voltage					
(TST2, M/S, PDN, MCKI, LRCK, BICK, SDTI1, SDTI2, SDTI3, SDTI4,SDTI5, SDTI6, DVMPD pins)	VIL	-	-	30%TVDD1	V
(TST1,TST3,TST4,TST5,CAD0,CAD1,I2C, CSN,CCLK, CDTI pins)	VIL	-	-	30%TVDD2	V
High-Level Output Voltage					
(SDTO1,SDTO2,TST6, LRCK, BICK, MCKO pins: Iout=-100μA)	VOH	TVDD1-0.5	-	-	V
(CDTO pin: Iout=-100μA)	VOH	TVDD2-0.5	-	-	V
(DZF1/OVF1, DZF2/OVF2 pins: Iout=-100μA)		AVDD2-0.5			V
Low-Level Output Voltage					
(SDTO1,SDTO2,TST6, LRCK, BICK, MCKO, CDTO, DZF1, DZF2/OVF pins: Iout= 100μA)	VOL	-	-	0.5	V
(SDA pin, 2.0V≤TVDD2≤3.6V Iout= 3mA)	VOL	-	-	0.4	V
(SDA pin, 1.6V≤TVDD2<2.0V Iout= 3mA)	VOL			20%TVDD2	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=-40~+105°C; AVDD1=AVDD2=3.0~3.6; DVDD=1.6~2.0V; TVDD1=1.6~3.6V, TVDD2=1.6~3.6V; C_L=20pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
Crystal Resonator					
Frequency	fXTAL	11.2896		24.576	MHz
MCKO Output					
Frequency (TVDD1 ≥3.0V)	fMCK	5.6448		24.576	MHz
Duty	dMCK	40	50	60	%
External Clock					
256fsn:	fCLK	8.192		12.288	MHz
Pulse Width Low	tCLKL	32			ns
Pulse Width High	tCLKH	32			ns
384fsn:	fCLK	12.288		18.432	MHz
Pulse Width Low	tCLKL	22			ns
Pulse Width High	tCLKH	22			ns
512fsn, 256fsd, 128fsq:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
MCKO Output					
Frequency	fMCK	4.096		12.288	MHz
(TVDD1 ≥3.0V)	fMCK	12.288		24.576	MHz
Duty (Note 16)	dMCK	40	50	60	%
LRCK Timing (Slave mode)					
Stereo mode **(TDM1 bit = "0", TDM0 bit = "0")**					
Normal Speed Mode	fsn	32		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	45		55	%
TDM512 mode (Note 17) **(TDM1 bit = "0", TDM0 bit = "1")**					
LRCK frequency	fsn	32		48	kHz
"H" time	tLRH	1/512fs			ns
"L" time	tLRL	1/512fs			ns
TDM256 mode (Note 18) **(TDM1 bit = "1", TDM0 bit = "0")**					
LRCK frequency	fsd	64		96	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM128 mode (Note 19) **(TDM1 bit = "1", TDM0 bit = "1")**					
LRCK frequency	fsq	128		192	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns

Parameter	Symbol	min	typ	max	Unit
LRCK Timing (Master Mode)					
Stereo mode					
(TDM1 bit = "0", TDM0 bit = "0")					
Normal Speed Mode	fsn	32		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	-	50	-	%
TDM512 mode (Note 17)					
(TDM1 bit = "0", TDM0 bit = "1")					
LRCK frequency	fsn	32		48	kHz
"H" time (Note 20)	tLRH		1/16fs		ns
TDM256 mode (Note 18)					
(TDM1 bit = "1", TDM0 bit = "0")					
LRCK frequency	fsd	64		96	kHz
"H" time (Note 20)	tLRH		1/8fs		ns
TDM128 mode (Note 19)					
(TDM1 bit = "1", TDM0 bit = "1")					
LRCK frequency	fsq	128		192	kHz
"H" time (Note 20)	tLRH		1/4fs		ns

Note 16. Except the case of DIV bit = "0".
Note 17. Please use for Normal Speed mode. Master clock should be input the 512fs in Master mode.
Note 18. Please use for Double Speed mode.
Note 19. Please use for Quad Speed mode.
Note 20. If the format is I^2S, it is "L" time.

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Slave mode)					
Stereo mode (TDM1 bit = "0", TDM0 bit = "0")					
(TVDD1= 1.6V~3.6V)					
BICK Period	tBCK	324			ns
BICK Pulse Width Low	tBCKL	130			ns
Pulse Width High	tBCKH	130			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	20			ns
LRCK to SDTO(MSB) (Except I^2S mode)	tLRS			80	ns
BICK "↓" to SDTO	tBSD			80	ns
SDTI Hold Time	tSDH	50			ns
SDTI Setup Time	tSDS	50			ns
(TVDD1= 3.0V~3.6V)					
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	33			ns
Pulse Width High	tBCKH	33			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	23			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	23			ns
LRCK to SDTO(MSB) (Except I^2S mode)	tLRS			23	ns
BICK "↓" to SDTO	tBSD			23	ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM512 mode (TDM1 bit = "0", TDM0 bit = "1")					
(TVDD1= 3.0V~3.6V) (Note 17)					ns
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	10			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM256 mode (TDM1 bit = "1", TDM0 bit = "0")					
(TVDD1= 3.0V~3.6V) (Note 18)					
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	10			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM128 mode (TDM1 bit = "1", TDM0 bit = "1")					
(TVDD1= 3.0V~3.6V) (Note 19)					
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 21)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	10			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Master mode)					
Stereo mode (TDM1 bit = "0", TDM0 bit = "0")					
(TVDD1= 1.6V~3.6V)					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–40	-	40	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
(TVDD1= 3.0V~3.6V)					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–23	-	23	ns
BICK "↓" to SDTO	tBSD	–23	-	23	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
TDM512 mode (TDM1 bit = "0", TDM0 bit = "1")					
(TVDD1= 3.0V~3.6V) (Note 17)					
BICK Frequency	fBCK	-	512fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	-10		10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
TDM256 mode (TDM1 bit = "1", TDM0 bit = "0")					
(TVDD1= 3.0V~3.6V) (Note 18)					
BICK Frequency	fBCK	-	256fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
TDM128 mode (TDM1 bit = "1", TDM0 bit = "1")					
(TVDD1= 3.0V~3.6V) (Note 19)					
BICK Frequency	fBCK	-	128fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns

Note 21. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (4-wire Serial mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
CDTO Delay	tDCD			50	ns
CSN "↑" to CDTO Hi-Z	tCCZ			70	ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 22)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 23)	tPD	150			ns
PDN "↑" to SDTO valid (Note 24)	tPDV		518		1/fs

Note 22. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 23. The AK4613 can be reset by setting the PDN pin to "L" upon power-up.
Note 24. These cycles are the numbers of LRCK rising from the PDN pin rising.
Note 25. I^2C-bus is a trademark of NXP B.V.

■ Timing Diagram

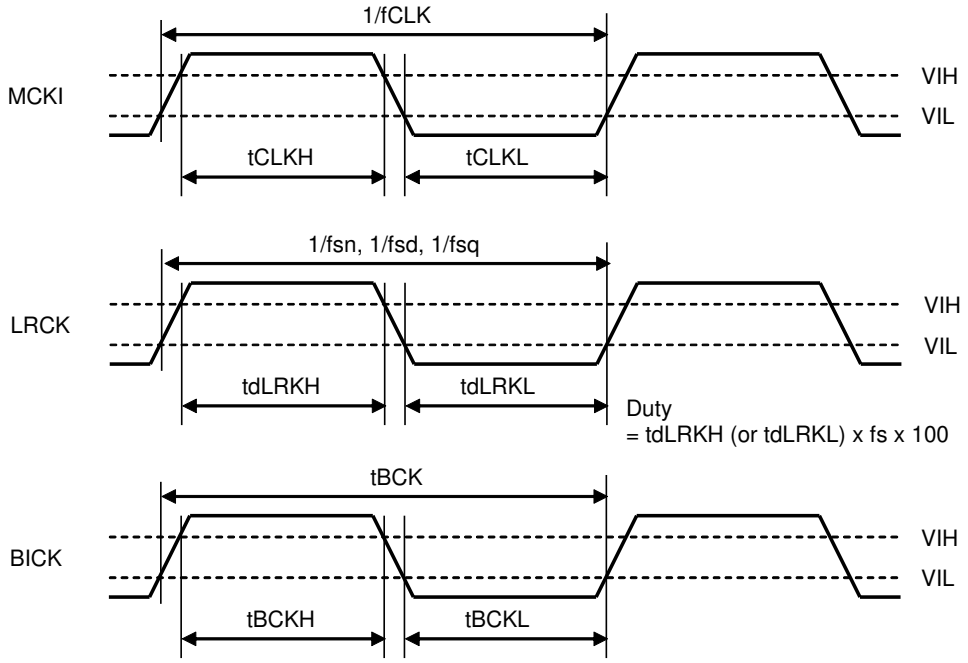

Figure 3. Clock Timing (TDM1/0 bit = "00" & Slave mode)

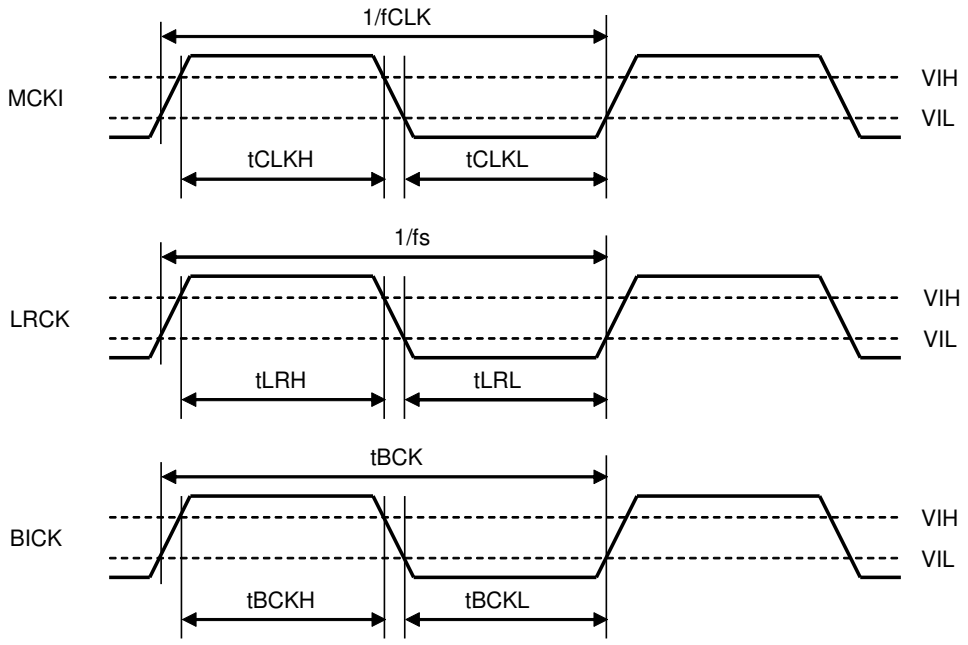

Figure 4. Clock Timing (Except TDM1/0 bit = "00" & Slave mode)

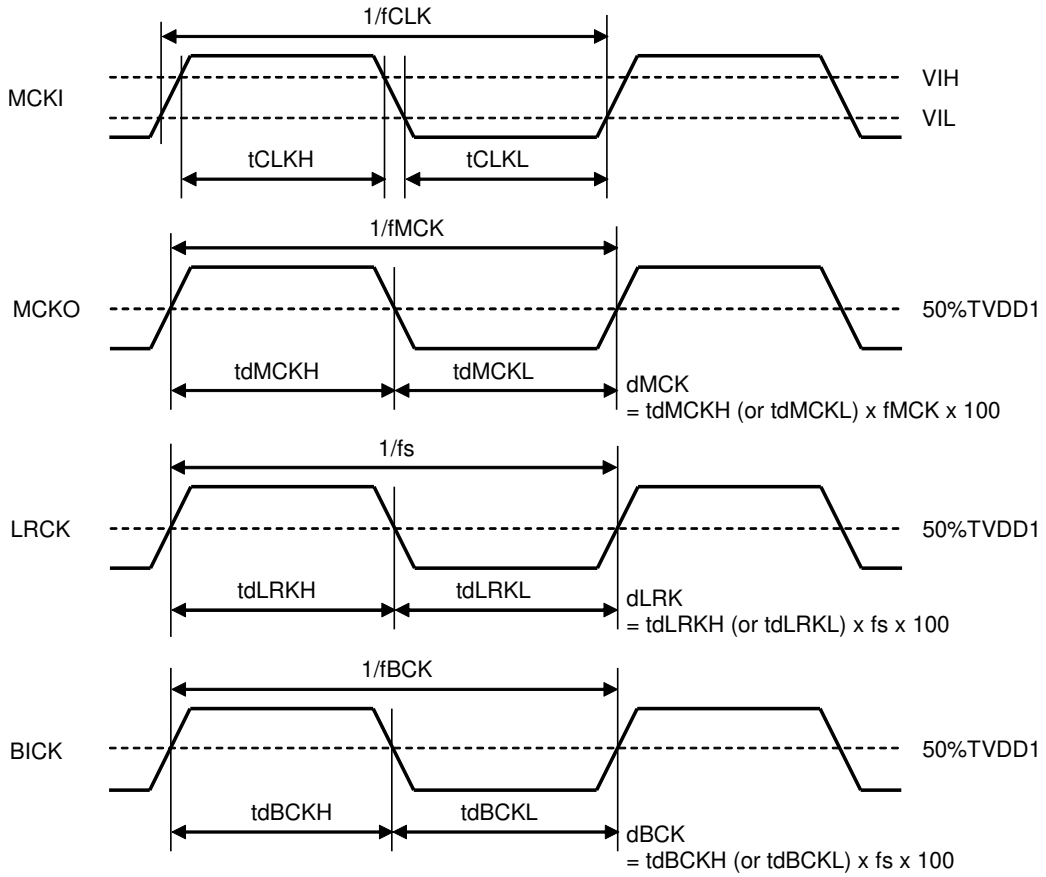

Figure 5. Clock Timing (TDM1/0 bit = "00" & Master mode)

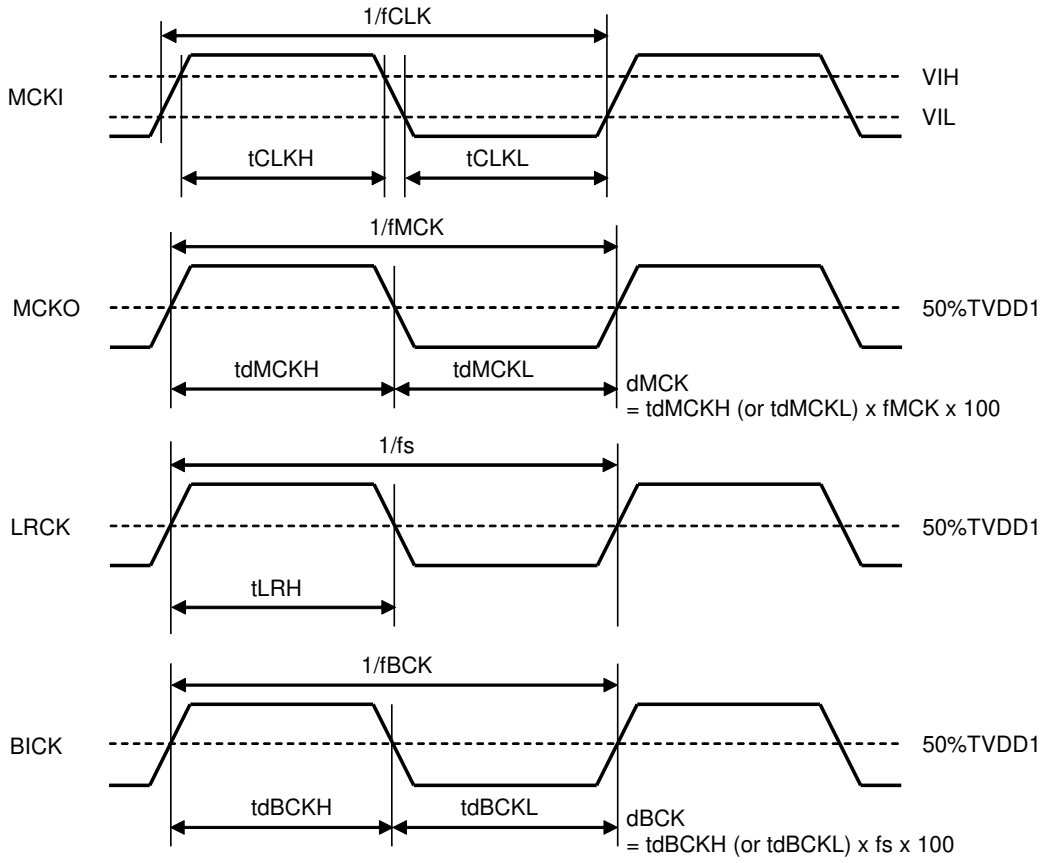

Figure 6. Clock Timing (Except TDM1/0 bit = "00" & Master mode)

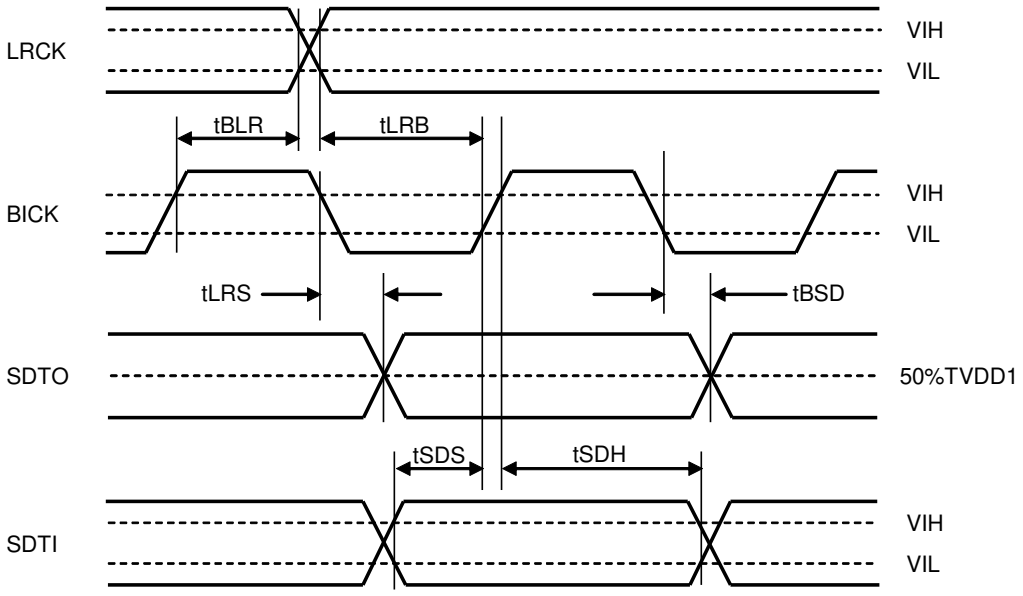

Figure 7. Audio Interface Timing (TDM1/0 bit = "00" & Slave mode)

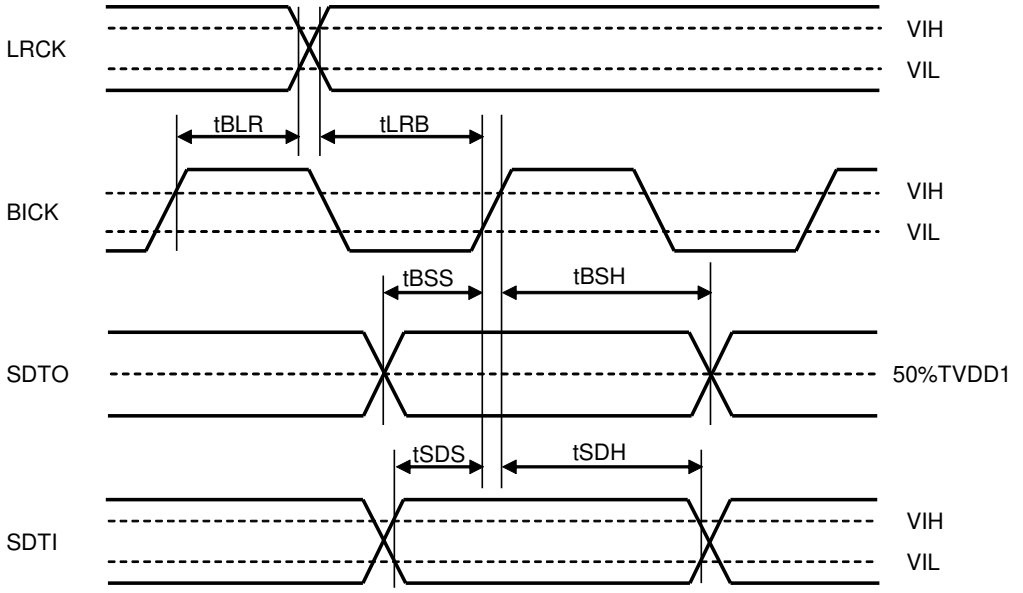

Figure 8. Audio Interface Timing (Except TDM1/0 bit = "00" & Slave mode)

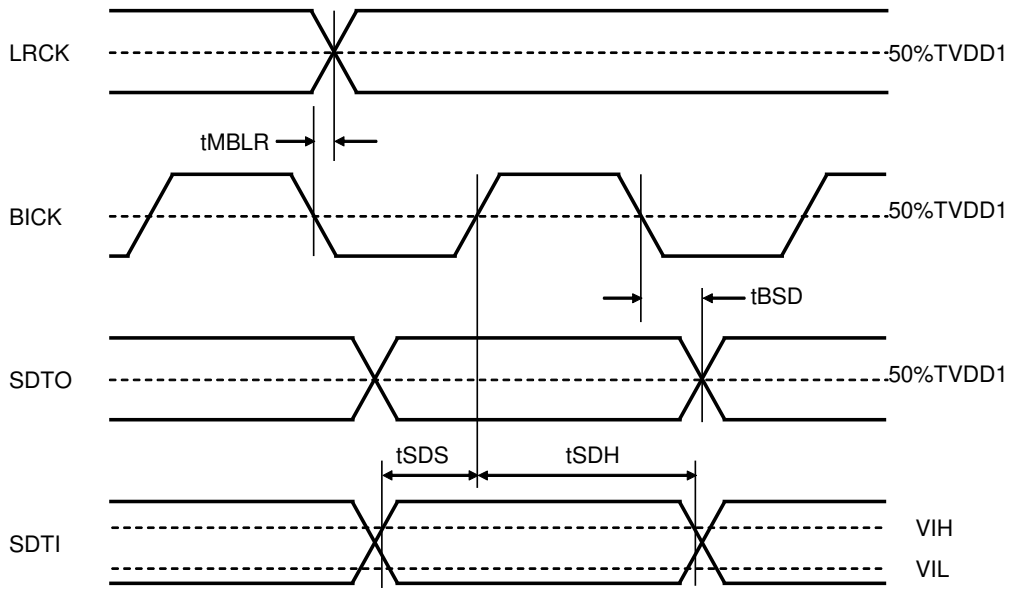

Figure 9. Audio Interface Timing (TDM1/0 bit = "00" & Master mode)

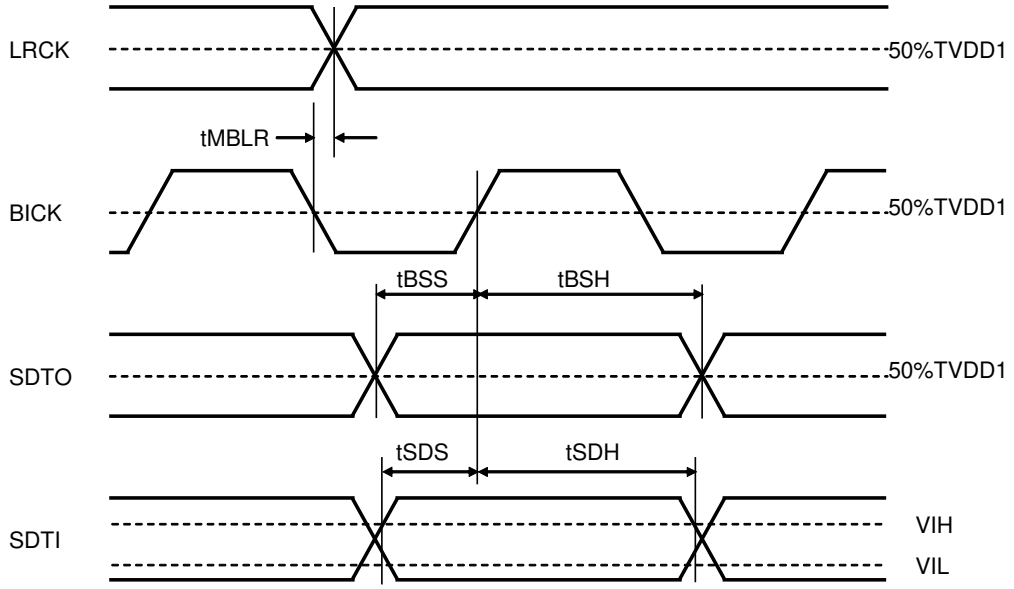

Figure 10. Audio Interface Timing (Except TDM1/0 bit = "00" & Master mode)

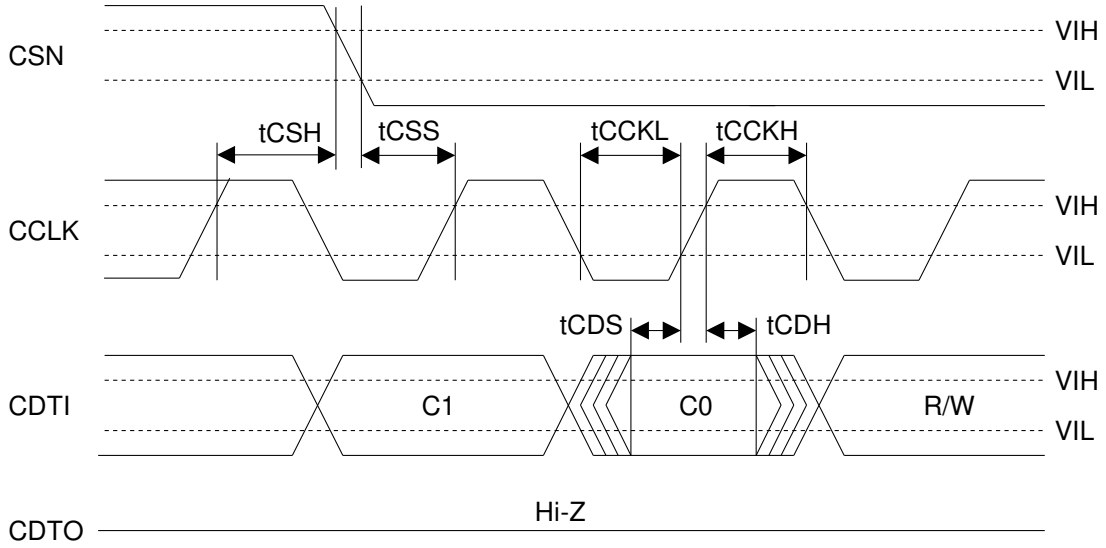

Figure 11. WRITE Command Input Timing (4-wire Serial mode)

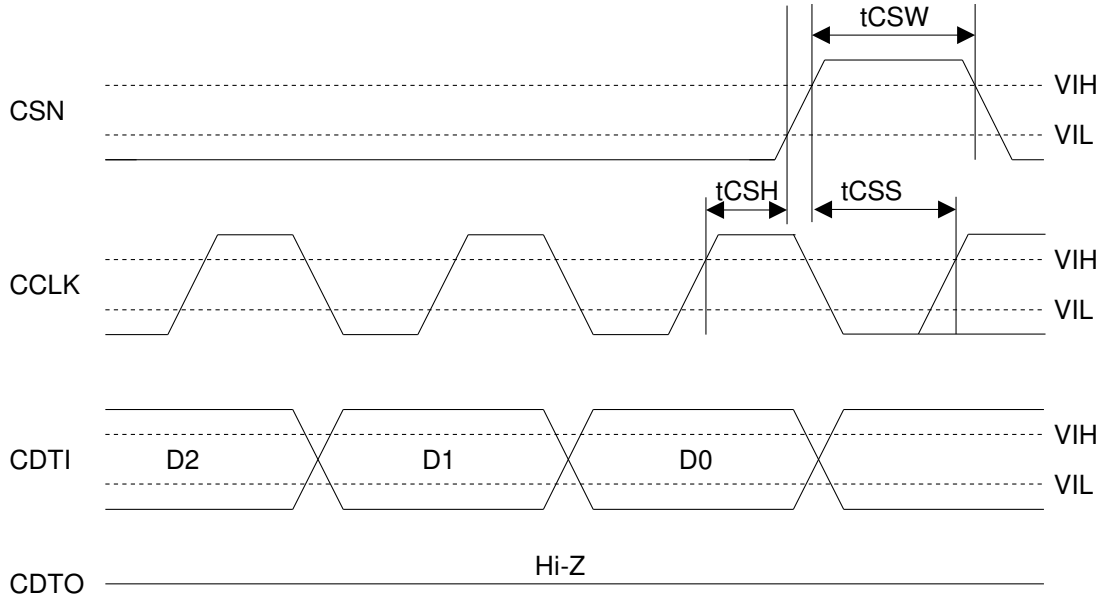

Figure 12. WRITE Data Input Timing (4-wire Serial mode)

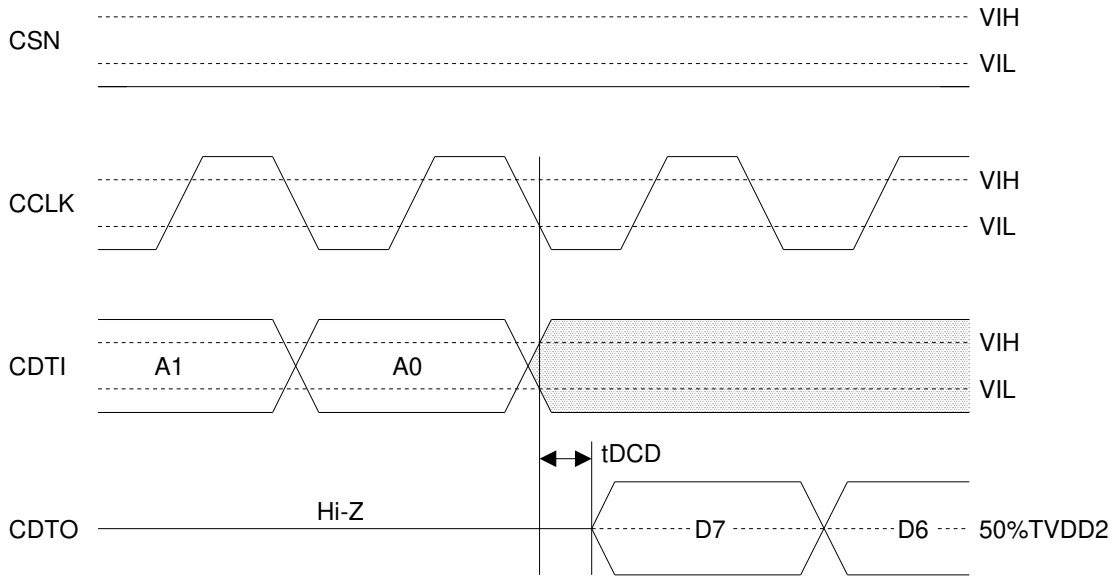

Figure 13. Read Data Output Timing1(4-wire Serial mode)

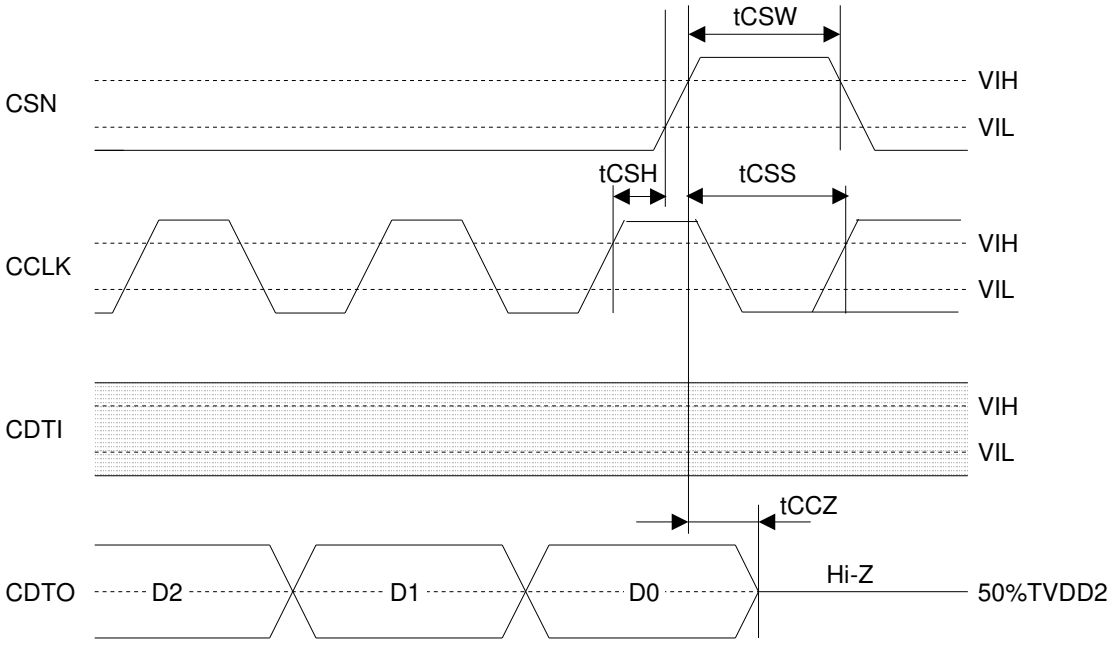

Figure 14. Read Data Output Timing2(4-wire Serial mode)