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AK4617

192kHz 24-bit 2ch/12ch Audio CODEC

1. General Description

The AK4617 is a single chip audio CODEC that includes 2-channel ADC and 12-channel DAC. The stereo ADC supports differential/single-ended analog inputs. The high performance 12-channel DAC integrates full-range digital volume control and achieves 106dB dynamic range. A car audio system can be easily designed with an audio DSP and the AK4617. The AK4617 is housed in a space saving 48-pin LQFP package.

2. Features

- **2ch ADC**
  - **Sampling Frequency: 8kHz~48kHz**
  - **ADC S/N: 97dB, S/ (N+D): 87dB**
  - **I/F format: MSB justified, I^2S or TDM**
- **12ch DAC**
  - **Sampling Frequency: 8kHz~192kHz**
  - **DAC S/N: 106dB, S/ (N+D): 85dB**
  - **I/F format: MSB justified, LSB justified (16bit, 24bit), I^2S or TDM**
- **Channel Independent Digital Attenuator (Linear 256 steps)**
- **Master / Slave mode**
- **Master clock**
  - **Slave mode: 256fs, 384fs or 512fs (Normal Speed Mode: fs=8kHz ~ 48kHz)**
    256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
    128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)
  - **Master mode: 256fs, 384fs or 512fs (Normal Speed Mode: fs=8kHz ~ 48kHz)**
    256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
    128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)
- **µP I/F: I^2C or 3-wire**
- **Power supply**
  - **Analog Power Supply: 3.0V ~ 3.6V (typ.3.3V)**
  - **Digital I/O Power Supply: 3.0V ~ 3.6V (typ.3.3V)**
- **Operating temperature range: -40°C ~ 105°C**
- **Package: 48pin LQFP**

3. Table of Contents

4. Block Diagram and Functions

■ Block Diagram

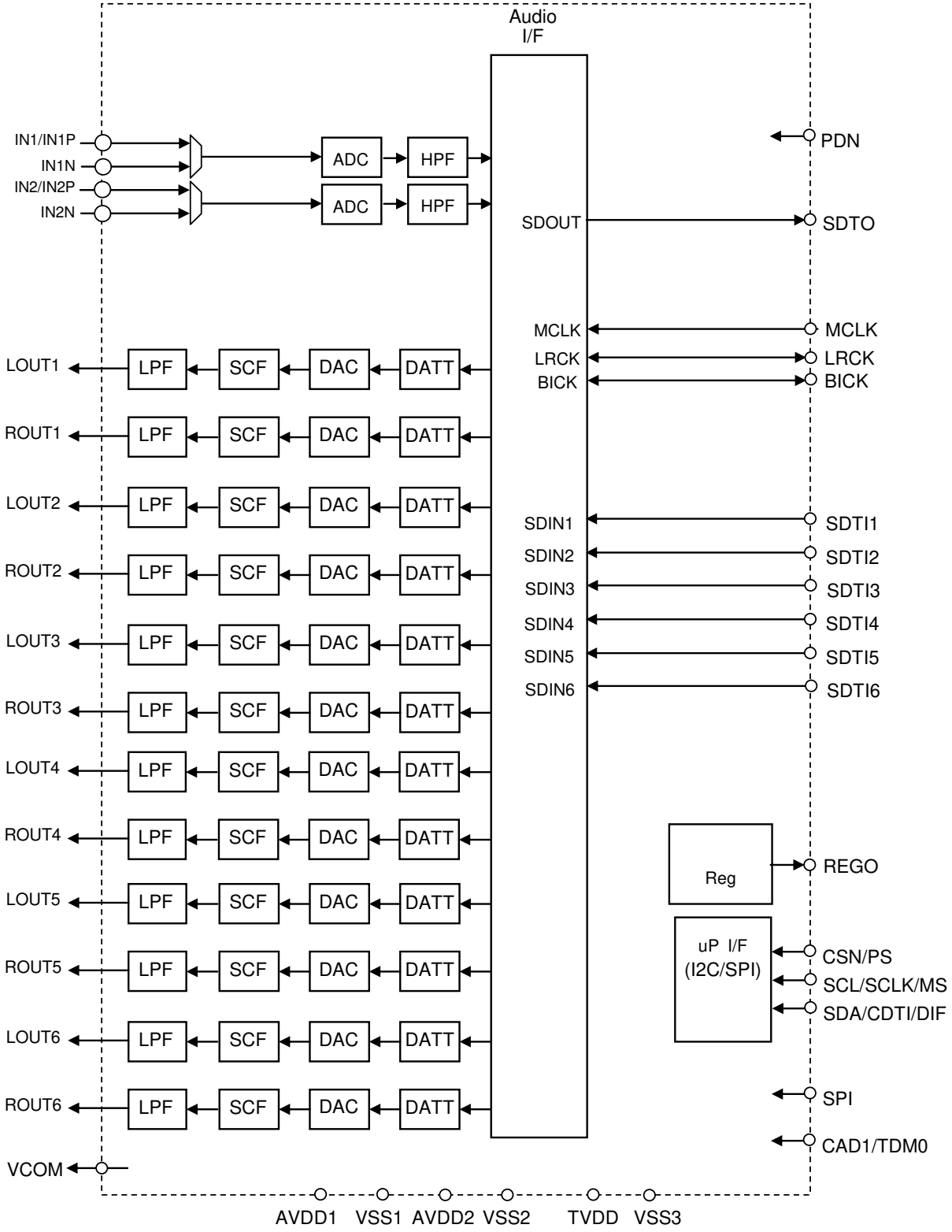
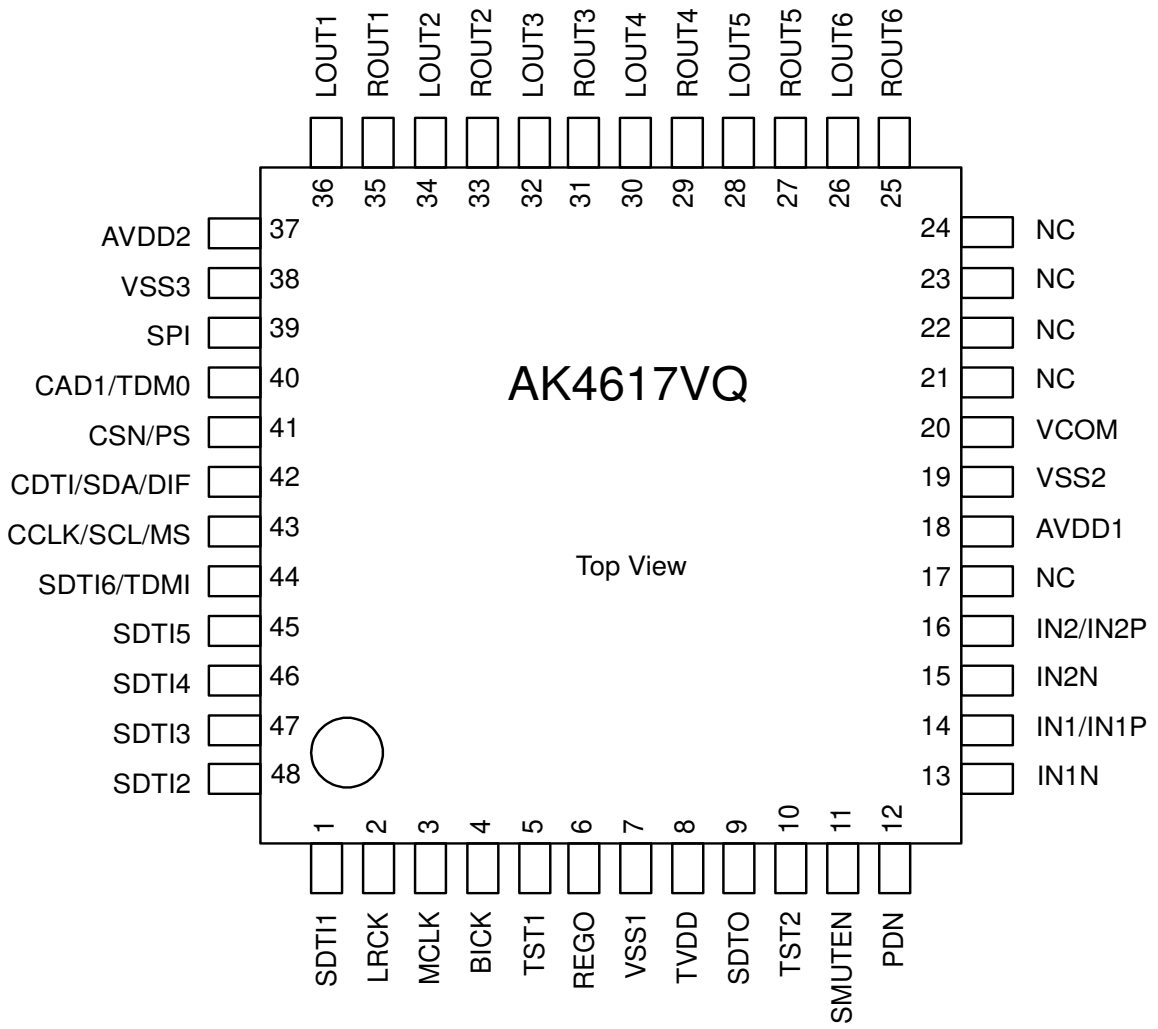


Figure 1. Block Diagram

■ Ordering Guide

AK4617VQ	–40 ~ +105°C	48pin LQFP (0.5mm pitch)
AKD4617	Evaluation Board for AK4617	

■ Pin Layout



■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	IN1/IN1P, IN1N, IN2/IN2P, IN2N	Open
	LOUT1-6, ROUT1-6	Open
Digital	SDTI1-6	Connect to VSS1
	SDTO	Open

5. Pin Configurations and Functions

No.	Pin Name	I/O	Function
1	SDTI1	I	Audio Serial Data Input 1 Pin
2	LRCK	I/O	Input Channel Clock Pin
3	MCLK	I	External Master Clock Input Pin
4	BICK	I/O	Audio Serial Data Clock Pin
5	TST1	I	This pin must be connected to ground.
6	REGO	O	Regulator Output Pin This pin should be connected to ground with 1.0uF.
7	VSS1	-	Ground Pin, 0V
8	TVDD	-	Digital Power Supply Pin, 3.0V~3.6V
9	SDTO	O	Audio Serial Data Output Pin
10	TST2	O	This pin must be open.
11	SMUTEN	I	All Analog Outputs Soft Mute Pin L: Mute H: Normal Operation
12	PDN	I	Power-Down & Reset Pin When "L", the AK4617 is powered-down and the control registers are reset to default state.
13	IN1N	I	(MDIE1 bit = "1") Differential Analog Negative input 1 pin
14	IN1	I	(MDIE1 bit = "0") Single-ended Analog Input 1 pin
	IN1P	I	(MDIE1 bit = "1") Differential Analog Positive input 1 pin
15	IN2N	I	(MDIE2 bit = "1") Differential Analog Negative input 2 pin
16	IN2	I	(MDIE2 bit = "0") Single-ended Analog Input 2 pin
	IN2P	I	(MDIE2 bit = "1") Differential Analog Positive input 2 pin
17	NC	-	This pin must be open.
18	AVDD1	-	Analog Power Supply Pin, 3.0V~3.6V
19	VSS2	-	Ground Pin, 0V
20	VCOM	O	Common Voltage Output Pin, AVDD1x1/2 Large external capacitor around 1μF is used to reduce power-supply noise.
21	NC	-	This pin must be open.
22	NC	-	This pin must be open.
23	NC	-	This pin must be open.
24	NC	-	This pin must be open.
25	ROUT6	O	Rch Analog Output 6 Pin
26	LOUT6	O	Lch Analog Output 6 Pin
27	ROUT5	O	Rch Analog Output 5 Pin
28	LOUT5	O	Lch Analog Output 5 Pin
29	ROUT4	O	Rch Analog Output 4 Pin
30	LOUT4	O	Lch Analog Output 4 Pin
31	ROUT3	O	Rch Analog Output 3 Pin
32	LOUT3	O	Lch Analog Output 3 Pin
33	ROUT2	O	Rch Analog Output 2 Pin
34	LOUT2	O	Lch Analog Output 2 Pin
35	ROUT1	O	Rch Analog Output 1 Pin

36	LOUT1	O	Lch Analog Output 1 Pin
37	AVDD2	-	Analog Power Supply Pin, 3.0V~3.6V
38	VSS3	-	Ground Pin, 0V
39	SPI	I	Control Mode Select Pin "L": I^2C Bus or Parallel control mode, "H": 3-wire serial control mode
40	CAD1	I	(SPI pin = "H") (SPI pin = "L", PS pin= "L") Chip Address Pin in serial control mode
	TDM0	I	(SPI pin = "L", PS pin= "H") TDM I/F Format Mode 0 Pin in parallel control mode "L": Normal mode, "H": TDM mode
41	CSN	I	(SPI pin = "H") Chip Select Pin in 3-wire serial control mode
	PS	I	(SPI pin = "L") Control Mode Select Pin "L": I^2C Bus serial control mode, "H": Parallel control mode
42	CDTI	I	(SPI pin = "H") Control Data Input Pin in 3-wire serial control mode
	SDA	I/O	(SPI pin = "L", PS pin= "L") Control Data Input Pin in I^2C Bus Serial control mode
	DIF	I	(SPI pin = "L", PS pin= "H") Audio Data Interface Format Pin in parallel control mode "L":24bit, Left justified, "H": 24bit, I^2S
43	CCLK	I	(SPI pin = "H") Control Data Clock Pin in 3-wire serial control mode
	SCL	I	(SPI pin = "L", PS pin= "L") Control Data Clock Pin in I^2C Bus serial control mode
	MS	I	(SPI pin = "L", PS pin= "H") Master Mode Select Pin "L": Slave Mode "H": Master Mode
44	SDTI6	I	(TDM1-0 bit = "00") Audio Serial Data Input 6 Pin/
	TDMI	I	(TDM1-0 bit = "01" or "10") TDM Data Input Pin
45	SDTI5	I	Audio Serial Data Input 5 Pin
46	SDTI4	I	Audio Serial Data Input 4 Pin
47	SDTI3	I	Audio Serial Data Input 3 Pin
48	SDTI2	I	Audio Serial Data Input 2 Pin

Note 1. All digital input pins must not be allowed to float.

6. Absolute Maximum Ratings

(VSS1 ~ 3 = 0V; Note 2)

Parameter		Symbol	min	max	Unit
Power Supplies	Analog1	AVDD1,	-0.3	6.0	V
	Analog2	AVDD2	-0.3	6.0	V
	Digital1	TVDD	-0.3	6.0	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD1+0.3	V
Digital Input Voltage (SDTI1-6, SPI, CSN/PS, CCLK/ SCL/MS, CDTI/SDA/DIF, CAD1/TDM0, PDN pins)		VIND	-0.3	TVDD+0.3	V
Ambient Temperature (power applied)(Note 3)		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground. VSS1 ~ 3 must be connected to the same analog ground plane.
Note 3. In case that PCB wiring density is 100%.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1 ~ 3 = 0V; Note 2)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 4)	Analog	AVDD1, AVDD2	3.0	3.3	3.6	V
	Digital	TVDD	3.0	3.3	3.6	V
	Difference	AVDD1, AVDD2 – TVDD	-0.1	0	+0.1	V

Note 4. The power up sequence between AVDD1, AVDD2 and TVDD is not critical. Each power supplies should be powered up during the PDN pin = "L". The PDN pin should be "H" after all power supplies are powered up. All power supplies should be powered on, only a part of these power supplies cannot be powered off. (Power off means power supplies equal to ground or power supplies are floating.) Do not turn off only the AK4617 under the condition that a surrounding device is powered on and the I^2C bus is in use. AVDD1 and AVDD2 must be connected with the same power supply.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Analog Characteristics

(Ta=25ºC; AVDD1, AVDD2=TVDD=3.3V, VSS1 ~ 3 =0V, BICK=64fs; Signal frequency 1kHz; Measurement frequency = 20Hz~20kHz @fs=48kHz, 20Hz~40kHz at fs=96kHz, 20Hz~40kHz at fs=192kHz; Unless otherwise specified.)

Parameter			min	typ	max	Unit
ADC Analog Input Characteristics(Single-ended inputs)						
Resolution					24	bit
S/(N+D)	(-1dBFS)		77	87		dB
DR (-60dBFS with A-weighted)			87	97		dB
S/N	(A-weighted)		87	97		dB
Interchannel Isolation				110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20	-	ppm/°C
Input Voltage	Single-ended (AIN=0.81x AVDD1)		2.40	2.67	2.94	Vpp
Power Supply Rejection		(Note 5)		60		dB
DAC Analog Output Characteristics (Single-ended outputs)						
Resolution					24	bit
S/(N+D)	(0dBFS)	fs=48kHz BW=20kHz	85	95		dB
		fs=96kHz BW=40kHz		93		
		fs=192kHz BW=40kHz		93		
DR	(-60dBFS with A-weighted)		100	106		dB
S/N	(A-weighted)		100	106		dB
Interchannel Isolation				100		dB
Interchannel Gain Mismatch		(Note 6)		0	0.7	dB
Gain Drift				20	-	ppm/°C
Output Voltage	AOUT=0.76 x AVDD2		2.25	2.51	2.77	Vpp
Load Resistance	(AC Load)		5			kΩ
Load Capacitance					30	pF
Power Supply Rejection		(Note 5)		60		dB

Note 5. PSR is applied to AVDD1, AVDD2 and TVDD with 1kHz, 50mVpp.
Note 6. Channel gain mismatch between all output channels (LOUT1-6, ROUT1-6).

Parameter		min	typ	max	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
AVDD1+AVDD2	fs=48kHz		45	59	mA
AVDD1+AVDD2	fs=96kHz, 192kHz		40		mA
TVDD	fs=48kHz		6	8	mA
TVDD	fs=96kHz		7		mA
TVDD	fs=192kHz		9		mA
Power-down mode (PDN pin = "L") (Note 7)					
AVDD1+AVDD2+TVDD			10	200	µA

Note 7. In the power-down mode, all digital input pins including clock pins are held VSS1.

9. ADC Filter Characteristics (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF): SHARP ROLL-OFF(SD_AD bit="0")						
Passband (Note 8)	±0.16dB	PB	0	-	18.8	kHz
	–0.28dB		-	20.0	-	kHz
	–3.0dB		-	22.8	-	kHz
Stopband(Note 8)		SB	28.4	-	-	kHz
Stopband Attenuation		SA	71	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	15.5	-	1/fs
ADC Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER(SD_AD bit="1")						
Passband (Note 8)	±0.16dB	PB	0	-	18.8	kHz
	–0.28dB		-	20.0	-	kHz
	–3.0dB		-	22.8	-	kHz
Stopband (Note 8)		SB	28.4		-	-
Stopband Attenuation		SA	72		-	-
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	2.4	1/fs
Group Delay (Note 10)		GD	-	5.5	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response	–3.0dB	FR	-	3.7	-	Hz
(Note 8)	–0.5dB		-	10.9	-	Hz
	–0.1dB		-	24.0	-	Hz

10. DAC Filter Characteristics (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF): SHARP ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	21.4	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR	-	-0.1	-	dB
DAC Digital Filter (LPF): SLOW ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	 22.5	9.8 -	kHz kHz
Stopband		SB	40.1			kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		9.0		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR		-4.0		dB
DAC Digital Filter (LPF): SHORT DELAY SHARP ROLL-OFF (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	8.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR		-0.1		dB
DAC Digital Filter (LPF): SHORT DELAY SLOW ROLL-OFF FILTER (DEM=OFF; SD_DA bit="1"; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	- 22.5	9.8 -	kHz kHz
Stopband		SB	40.1	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0~20.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	7.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR	-	-4.0	-	dB

11. DAC Filter Characteristics (fs=96kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF): SHARP ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 48.0	43.6 -	kHz kHz
Stopband		SB	52.4	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	21.4	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR	-	-0.3	-	dB
DAC Digital Filter (LPF): SLOW ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	 45.0	19.6 -	kHz kHz
Stopband		SB	80.2			kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		9.0		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR		-4.2		dB
DAC Digital Filter (LPF): SHORT DELAY SHARP ROLL-OFF (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 48.0	43.6 -	kHz kHz
Stopband		SB	52.4	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	8.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR		-0.3		dB
DAC Digital Filter (LPF): SHORT DELAY SLOW ROLL-OFF FILTER (DEM=OFF; SD_DA bit="1" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	- 45.0	19.6 -	kHz kHz
Stopband		SB	80.2	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	7.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR	-	-4.2	-	dB

12. DAC Filter Characteristics (fs=192kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF): SHARP ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 96.0	87.2 -	kHz kHz
Stopband		SB	104.8	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	21.4	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR	-	-1.0	-	dB
DAC Digital Filter (LPF): SLOW ROLL-OFF(DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	 90.0	39.2 -	kHz kHz
Stopband		SB	160.4			kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		9.0		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR		-5.0		dB
DAC Digital Filter (LPF): SHORT DELAY SHARP ROLL-OFF (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 96.0	87.2 -	kHz kHz
Stopband		SB	104.8	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	8.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR		-1.0		dB
DAC Digital Filter (LPF): SHORT DELAY SLOW ROLL-OFF FILTER (DEM=OFF; SD_DA bit="1" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	- 90.0	39.2 -	kHz kHz
Stopband		SB	160.4	-	-	kHz
Passband Ripple (Note 12)		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	7.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR	-	-5.0	-	dB

Note 8. The passband and stopband frequencies scale with fs (sampling frequency). For example, ADC: Passband (±0.1dB) = 0.375 x fs, DAC: Passband (±0.06dB) = 0.454 x fs.

Note 9. The passband and stopband frequencies scale with fs (sampling frequency). For example, DAC: Passband (±0.06dB) = 0.204 x fs.

Note 10. The calculated delay time is resulting from digital filtering. For the ADC, this time is from the input of an analog signal to the setting of 24bit data for both channels to the ADC output register. For the DAC, this time is from setting the 24 bit data both channels at the input register to the output of an analog signal.
Note 11. The reference frequency is 1kHz.
Note 12. It is the gain amplitude in passband.

13. DC Characteristics

(Ta=-40~+105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage (MCLK, LRCK, BICK, SDTI1-6/TDMI, SPI, CSN/PS, CCLK/SCL/MS, CDTI/SDA/DIF, CAD1/TDM0, PDN pins)	VIH	70% TVDD	-	-	V
Low-Level Input Voltage (MCLK, LRCK, BICK, SDTI1-6/TDMI, SPI, CSN/PS, CCLK/SCL/MS, CDTI/SDA/DIF, CAD1/TDM0, PDN pins)	VIL	-	-	30% TVDD	V
High-Level Output Voltage (LRCK, BICK, SDTO pins: Iout=-100µA)	VOH	TVDD-0.5	-	-	V
Low-Level Output Voltage (LRCK, BICK, SDTO pins: Iout= 100µA)	VOL		-	0.5	V
(SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	µA

14. Switching Characteristics

(Ta=-40~+105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V; C_L=20pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
External Clock					
256fsn:	fCLK	2.048		12.288	MHz
Pulse Width Low	tCLKL	32			ns
Pulse Width High	tCLKH	32			ns
384fsn:	fCLK	3.072		18.432	MHz
Pulse Width Low	tCLKL	22			ns
Pulse Width High	tCLKH	22			ns
512fsn:	fCLK	4.096		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
256fsd, 128fsq:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
LRCK Timing (Slave mode)					
Stereo mode (Figure 2)					
(TDM1-0 bit = "00")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	45		55	%
TDM512 mode (Figure 3),(Note 13)					
(TDM1-0 bit = "01")					
LRCK frequency	fsn	8		48	kHz
"H" time	tLRH	1/512fs			ns
"L" time	tLRL	1/512fs			ns
TDM256 mode (Figure 3),(Note 14)					
(TDM1-0 bit = "10")					
LRCK frequency	fsn	8		48	kHz
	fsd	64		96	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM128 mode (Figure 3),(Note 15)					
(TDM1-0 bit = "11")					
LRCK frequency	fsq	128		192	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns

LRCK Timing (Master Mode)					
Stereo mode (Figure 4)					
(TDM1-0 bit = "00")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	-	50	-	%
TDM512 mode (Figure 5),(Note 13)					
(TDM1-0 bit = "01")					
LRCK frequency	fsn	8		48	kHz
"H" time (Note 16)	tLRH		1/16fs		ns
TDM256 mode (Figure 5),(Note 14)					
(TDM1-0 bit = "10")					
LRCK frequency	fsn	8		48	kHz
	fsd	64		96	kHz
"H" time (Note 16)	tLRH		1/8fs		ns
TDM128 mode (Figure 5),(Note 15)					
(TDM1-0 bit = "11")					
LRCK frequency	fsq	128		192	kHz
"H" time (Note 16)	tLRH		1/4fs		ns

Note 13. Please use for Normal Speed mode. Master clock should be input the 512fs in Master mode.
Note 14. Please use for Normal Speed mode, Double Speed mode. Master clock should be input the 256fs or 512fs in Master mode.
Note 15. Please use for Quad Speed mode. Master clock should be input the 128fs in Master mode.
Note 16. If the format is I^2S, it is "L" time.

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Slave mode)					
Stereo mode (TDM1-0 bit = "00") for Normal Speed mode (Figure 2, Figure 6)					
BICK Period	tBCK	324			ns
BICK Pulse Width Low	tBCKL	130			ns
Pulse Width High	tBCKH	130			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	20			ns
LRCK to SDTO(MSB) (Except I^2S mode)	tLRS			80	ns
BICK "↓" to SDTO	tBSD			80	ns
SDTI Hold Time	tSDH	50			ns
SDTI Setup Time	tSDS	50			ns
Stereo mode (TDM1-0 bit = "00") for Double and Quad Speed mode (Figure 2, Figure 6)					
BICK Period	tBCK	81			ns
BICK Pulse Width Low	tBCKL	33			ns
Pulse Width High	tBCKH	33			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	23			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	23			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM512 mode (TDM1-0 bit = "01") (Note 13) (Figure 3, Figure 7)					ns
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	10			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM256 mode (TDM1-0 bit = "10") (Note 14) (Figure 3, Figure 7)					ns
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	10			ns
SDTO Setup time BICK "↑"	tBSS	6			ns
SDTO Hold time BICK "↑"	tBSH	5			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
TDM128 mode (TDM1-0 bit = "11") (Note 15) (Figure 3, Figure 7)					
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 17)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 17)	tBLR	10			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Master mode)					
Stereo mode (TDM1-0 bit = "00") for Normal Speed mode (Figure 4, Figure 8)					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–80	-	80	ns
BICK "↓" to SDTO	tBSD	–80	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Stereo mode (TDM1-0 bit = "00") for Double and Quad Speed mode (Figure 4, Figure 8)					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty (Table 17)	dBCK	-	50	-	%
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
TDM512 mode (TDM1-0 bit = "01") (Note 13) (Figure 5, Figure 9)					
BICK Frequency	fBCK	-	512fs	-	Hz
BICK Duty (Table 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	-10		10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI Hold Time	tSDH	5	-	-	ns
SDTI Setup Time	tSDS	6	-	-	ns
TDM256 mode (TDM1-0 bit = "10") (Note 14) (Figure 5, Figure 9)					
BICK Frequency	fBCK	-	256fs	-	Hz
BICK Duty (Table 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	--	ns
SDTI Hold Time	tSDH	5	-	-	ns
SDTI Setup Time	tSDS	6	-		ns
TDM128 mode (TDM1-0 bit = "11") (Note 15) (Figure 5, Figure 9)					
BICK Frequency	fBCK	-	128fs	-	Hz
BICK Duty (Table 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns

Note 17. BICK rising edge must not occur at the same time as LRCK edge.
Note 18. In the case that the duty of MCLK is 50%.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (3-wire Serial mode):					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	40			ns
CDTI Hold Time	tCDH	40			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 19)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 20)	tPD	150			ns
PDN "↑" to SDTO valid (Note 21)	tPDV		32768/MCLK +1059/fs		s

Note 19. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 20. The AK4617 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 150ns for a certain reset. The AK4617 is not reset by the "L" pulse less than 30ns.

Note 21. These cycles are the numbers of MCLK and LRCK rising from the PDN pin rising.

Note 22. I^2C is a trademark of NXP B.V.

■ Timing Diagram

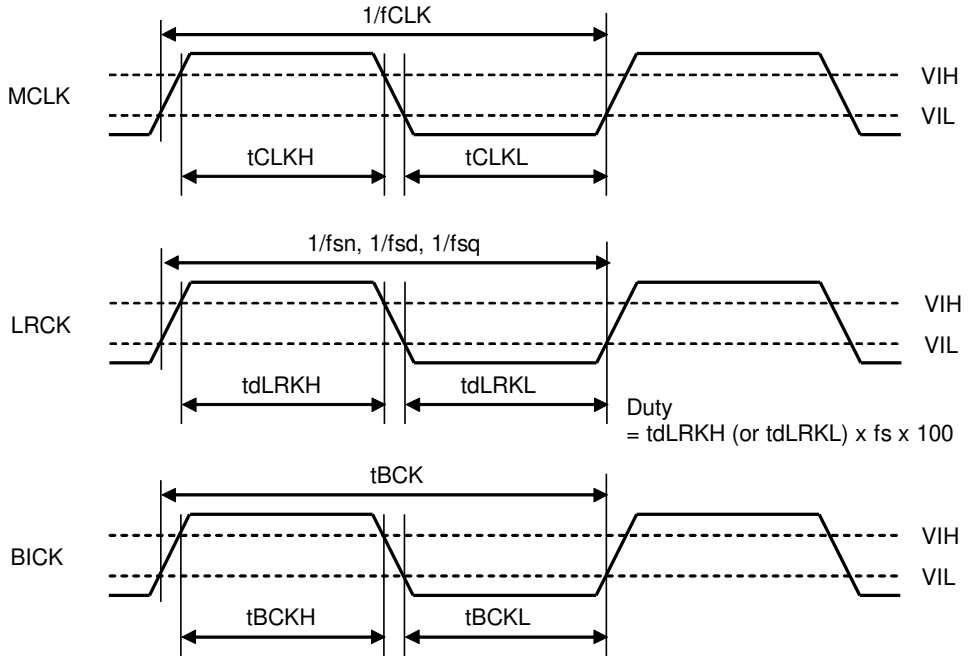


Figure 2. Clock Timing (TDM1-0 bit = "00" & Slave mode)

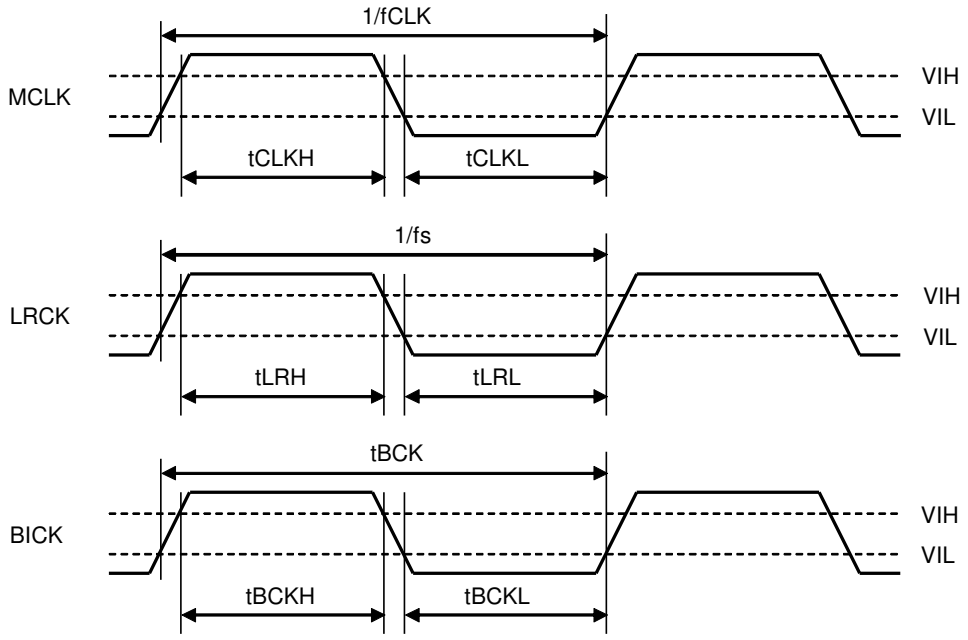


Figure 3. Clock Timing (Except TDM1-0 bit = "00" & Slave mode)

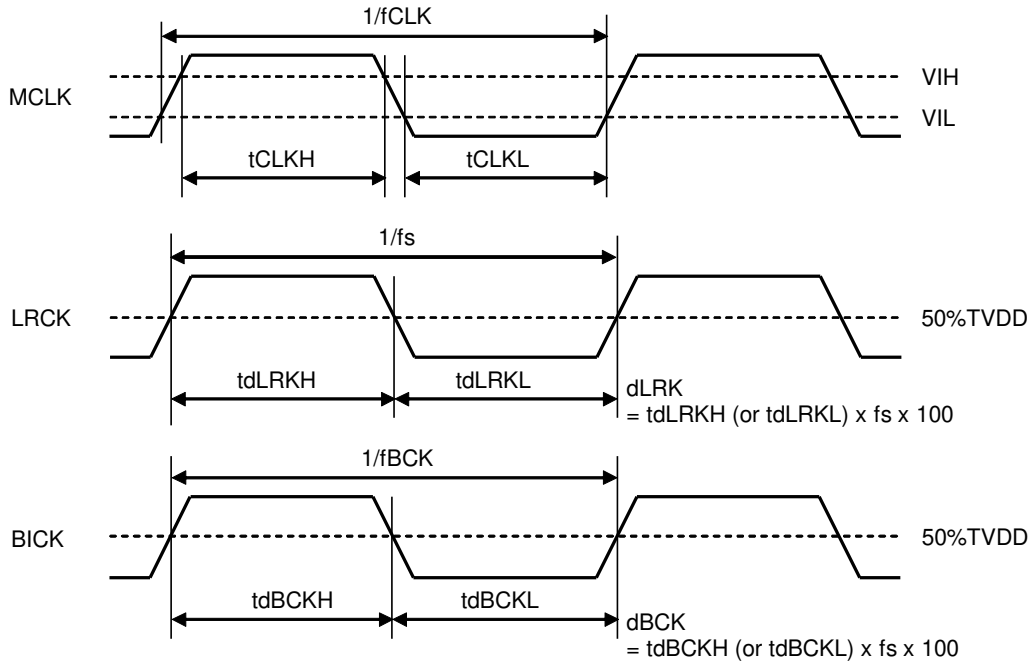


Figure 4. Clock Timing (TDM1-0 bit = "00" & Master mode)

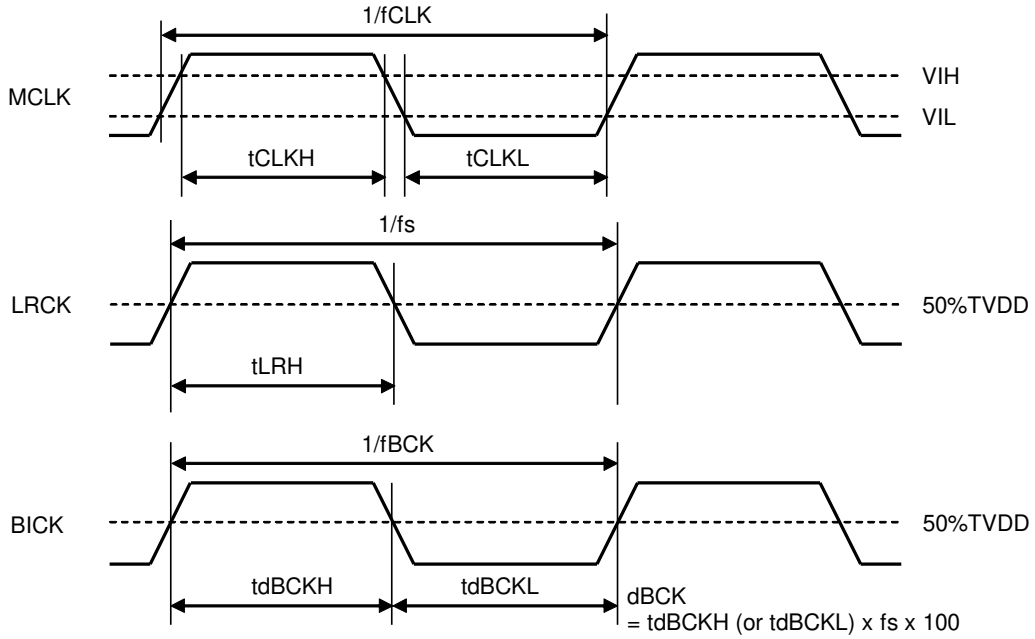


Figure 5. Clock Timing (Except TDM1-0 bit = "00" & Master mode)

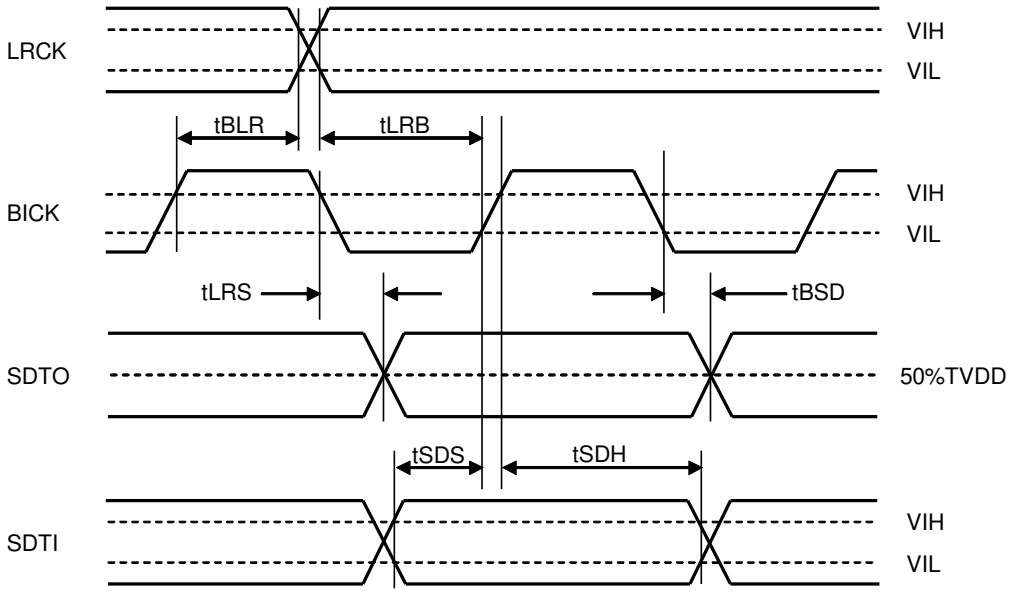


Figure 6. Audio Interface Timing (TDM1-0 bit = "00" & Slave mode)

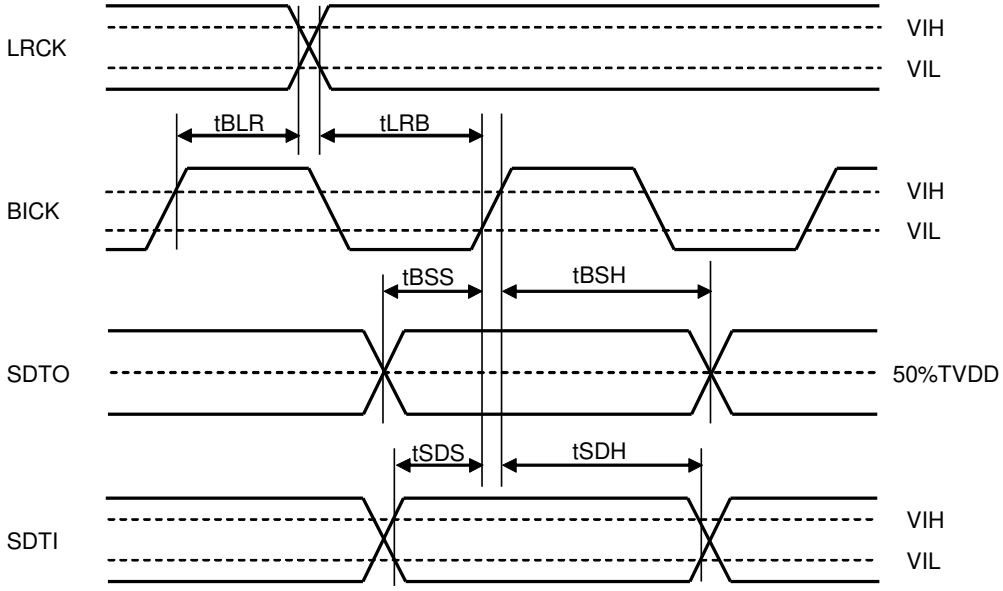


Figure 7. Audio Interface Timing (Except TDM1-0 bit = "00" & Slave mode)

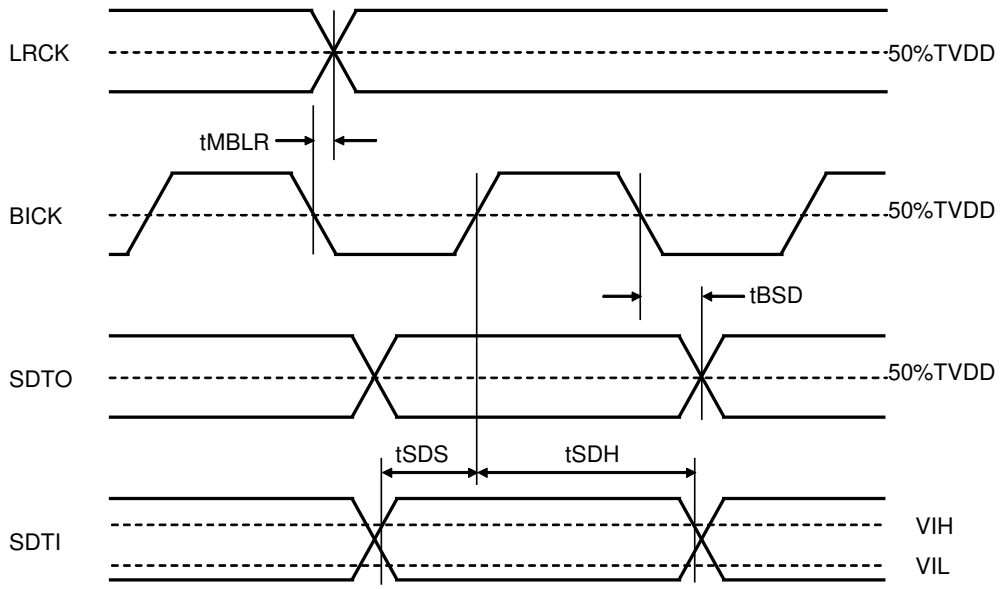


Figure 8. Audio Interface Timing (TDM1-0 bit = "00" & Master mode)

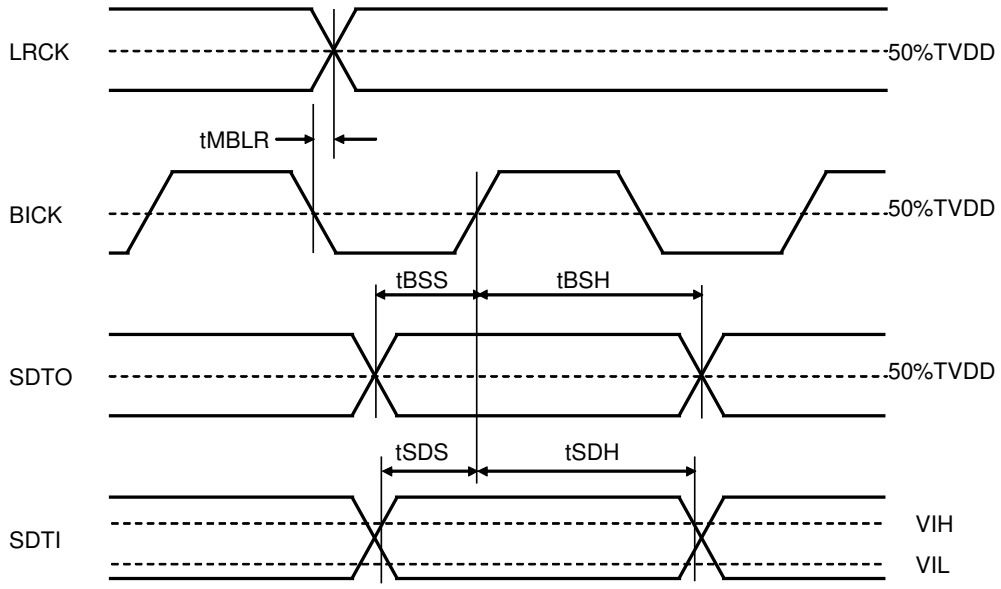


Figure 9. Audio Interface Timing (Except TDM1-0 bit = "00" & Master mode)

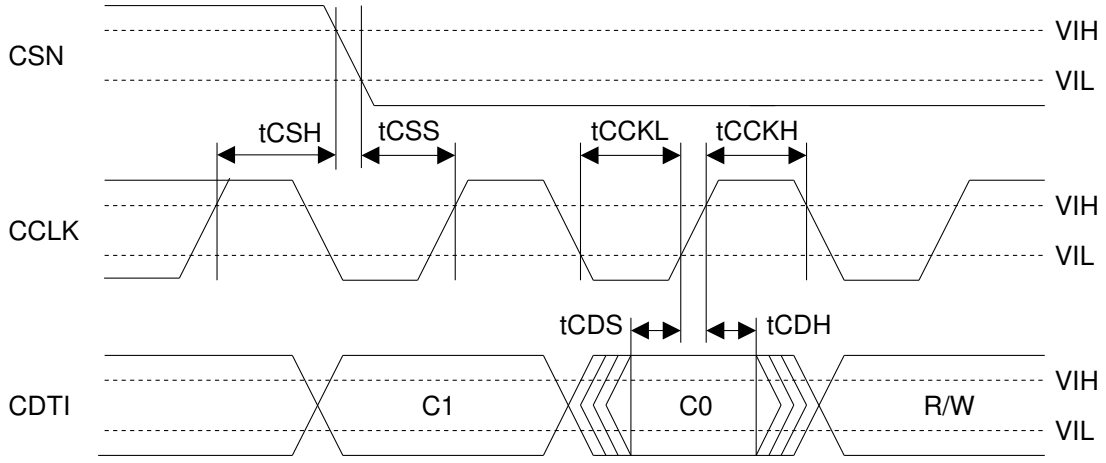


Figure 10. WRITE Command Input Timing (3-wire Serial mode)

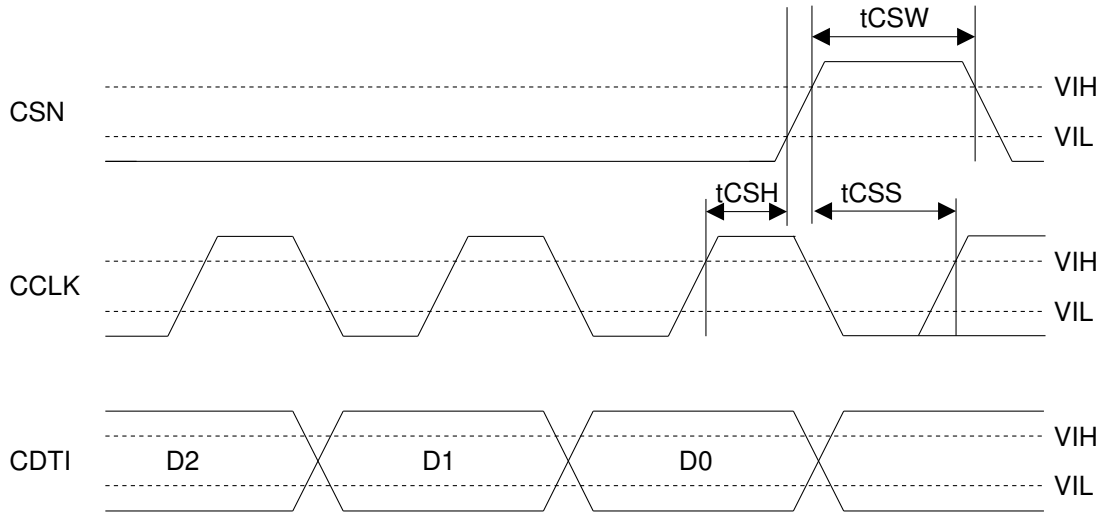


Figure 11. WRITE Data Input Timing (3-wire Serial mode)

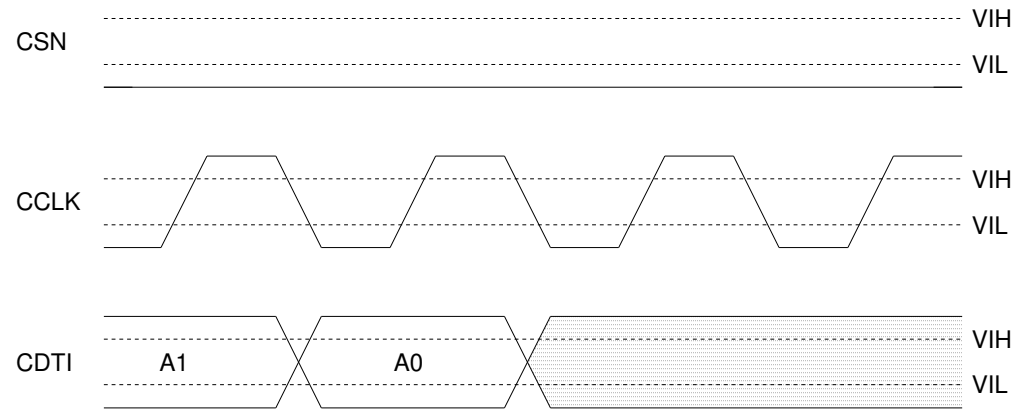


Figure 12. Read Data Output Timing1(3-wire Serial mode)

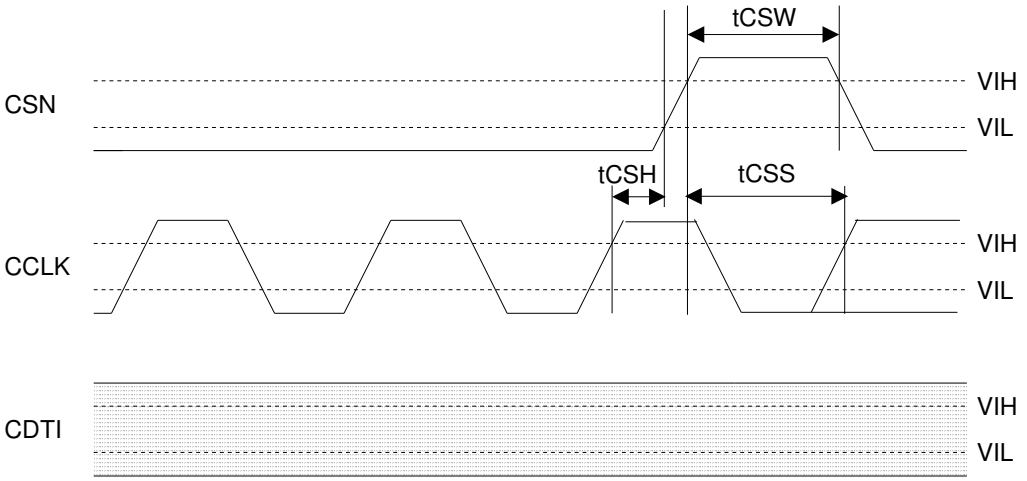


Figure 13. Read Data Output Timing2(3-wire Serial mode)

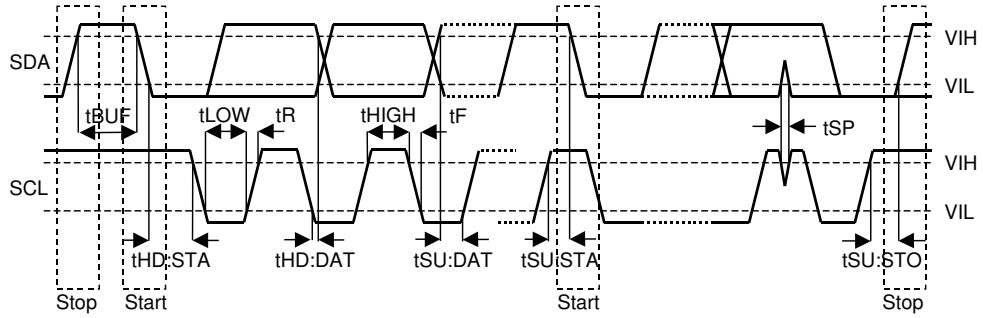


Figure 14. I^{2}C Bus mode Timing

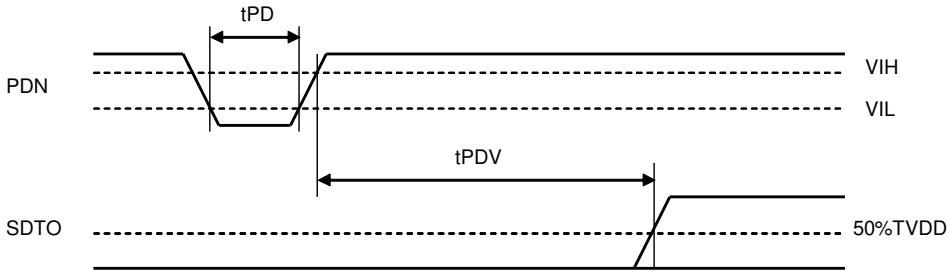


Figure 15. Power-down & Reset Timing