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AK4618

192kHz 24-bit 6ch/12ch Audio CODEC with Microphone Interface

GENERAL DESCRIPTION

The AK4618 is a single chip audio CODEC that includes 6-channel ADC and 12-channel DAC. The 6-channel ADC supports differential/single-ended analog inputs. The high performance 12-channel DAC integrates full-range digital volume control and achieves 106dB dynamic range. A car audio system can be easily designed with an audio DSP and the AK4618. The AK4618 is housed in a space saving 48-pin LQFP package.

FEATURES

- ☐ **6ch ADC**
  - **Sampling Frequency: 8KHz~48KHz**
  - **ADC S/N: 98dB, S/ (N+D): 87dB**
  - **I/F format: MSB justified, I^2S or TDM**
- ☐ **12ch DAC**
  - **Sampling Frequency: 8KHz~192KHz**
  - **DAC S/N: 106dB, S/ (N+D): 92dB**
  - **I/F format: MSB justified, LSB justified (16bit, 24bit), I^2S or TDM**
  - **Channel Independent Digital Attenuator (Linear 256 steps)**
- ☐ **Microphone Interface**
  - **Single-ended/Differential Input Select**
  - **Programmable Gain (+33dB ~ +15dB and 0dB, 3dB step)**
  - **Low Noise Microphone Bias**
- ☐ **Master / Slave mode**
- ☐ **Master clock**
  - **Slave mode: 256fs, 384fs or 512fs (Normal Speed Mode: fs=8kHz ~ 48kHz)**
    256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
    128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)
  - **Master mode: 256fs, 384fs or 512fs (Normal Speed Mode: fs=8kHz ~ 48kHz)**
    256fs (Double Speed Mode: fs=64kHz ~ 96kHz)
    128fs (Quad Speed Mode: fs=128kHz ~ 192kHz)
- ☐ **µP I/F: I^2C**
- ☐ **Power supply**
  - **Analog Power Supply: 3.0V ~ 3.6V (typ.3.3V)**
  - **Digital I/O Power Supply: 3.0V ~ 3.6V (typ.3.3V)**
- ☐ **Operating temperature range: -40°C ~ 105°C**
- ☐ **Package: 48pin LQFP**

■ Block Diagram

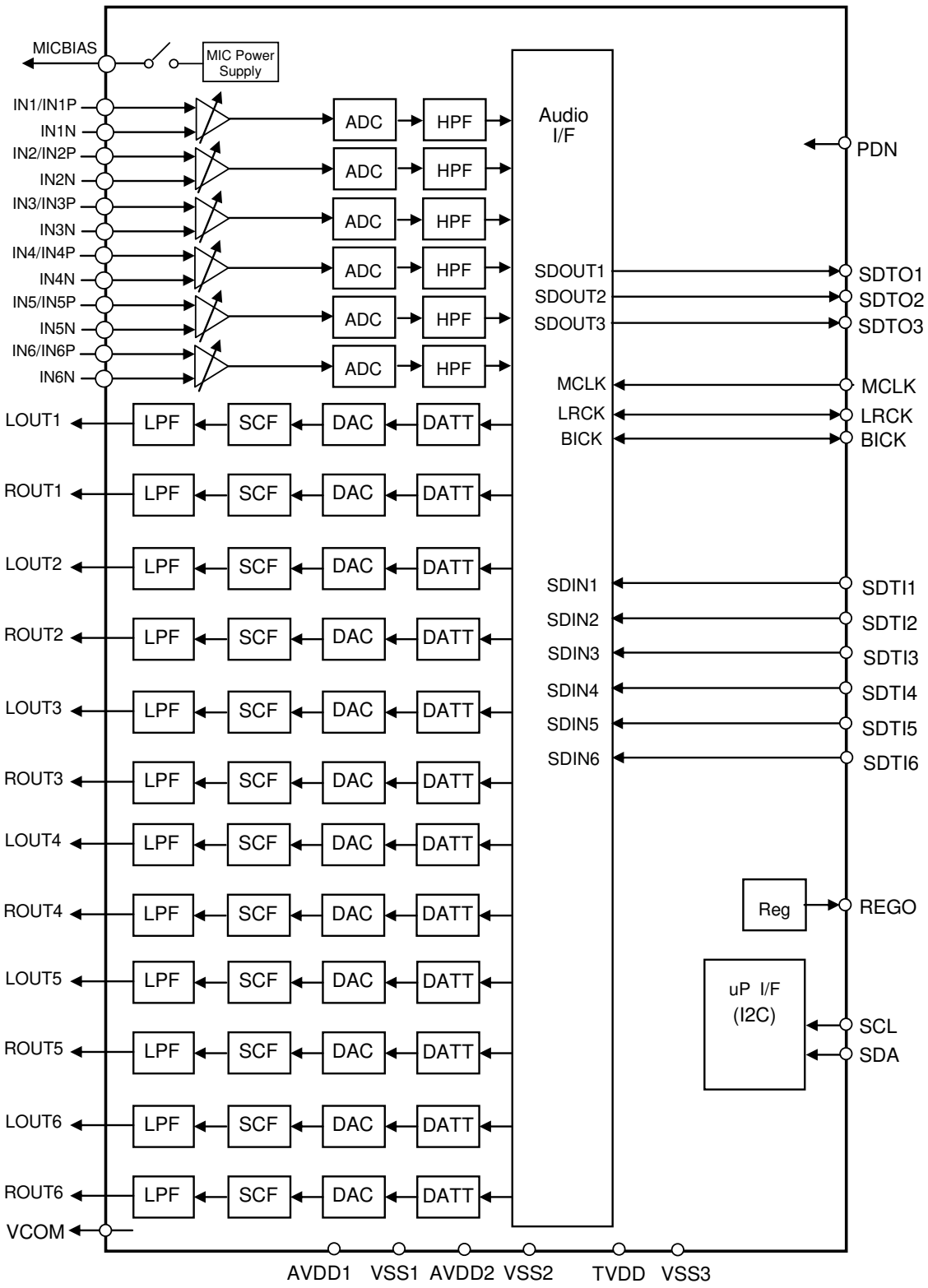
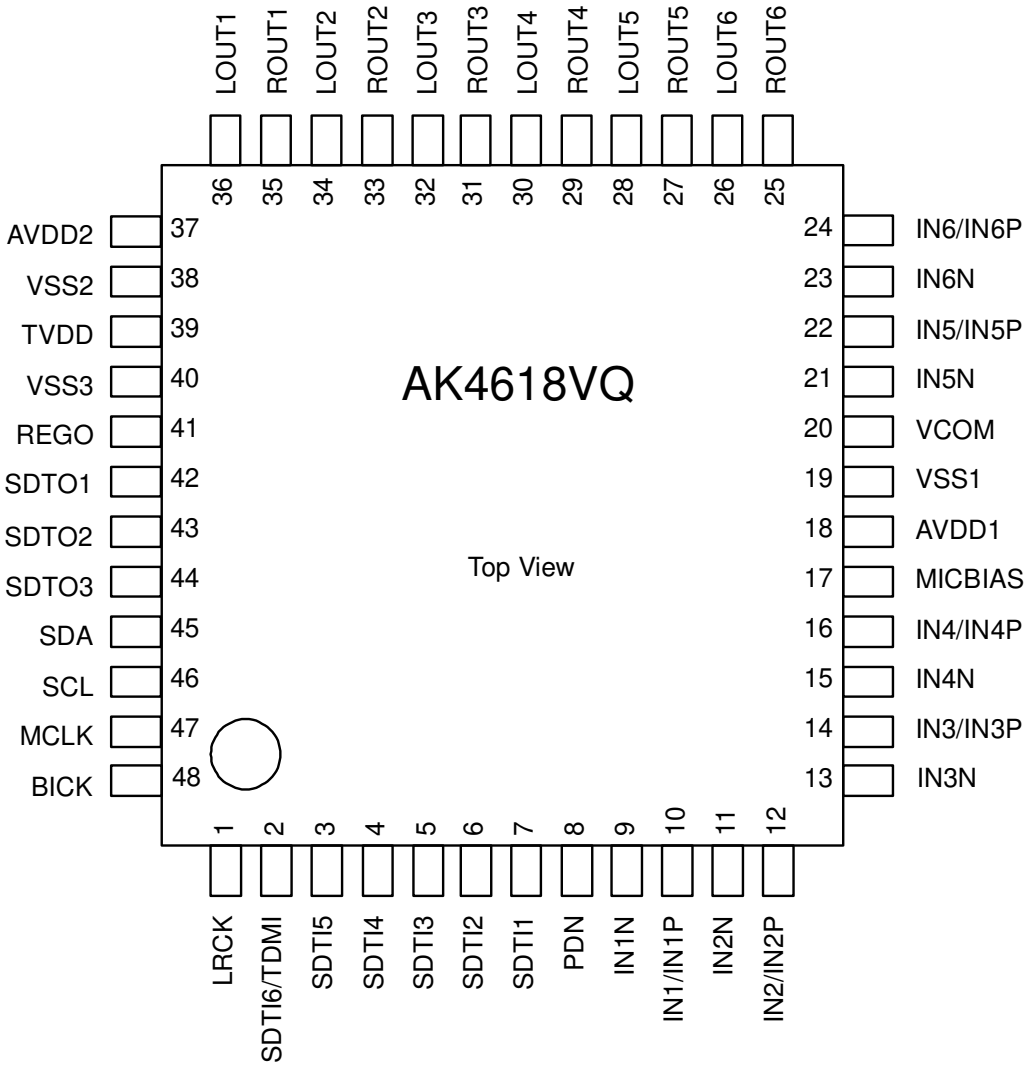


Figure 1. Block Diagram

■ Ordering Guide

AK4618VQ	–40 ~ +105°C	48pin LQFP (0.5mm pitch)
AKD4618	Evaluation Board for AK4618	

■ Pin Layout



■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	IN1/IN1P, IN1N, IN2/IN2P, IN2N, IN3/IN3P, IN3N, IN4/IN4P, IN4N, IN5/IN5P, IN5N, IN6/IN6P, IN6N	Open
	MICBIAS	Open
	LOUT1-6, ROUT1-6	Open
Digital	SDTI1-6	Connect to VSS3
	SDTO1-3	Open

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LRCK	I/O	Input Channel Clock Pin
2	SDTI6	I	(TDM1-0 bits = "00") Audio Serial Data Input 6 Pin
	TDMI	I	(TDM1-0 bits = "01" or "10") TDM Data Input Pin
3	SDTI5	I	Audio Serial Data Input 5 Pin
4	SDTI4	I	Audio Serial Data Input 4 Pin
5	SDTI3	I	Audio Serial Data Input 3 Pin
6	SDTI2	I	Audio Serial Data Input 2 Pin
7	SDTI1	I	Audio Serial Data Input 1 Pin
8	PDN	I	Power-Down & Reset Pin When "L", the AK4618 is powered-down and the control registers are reset to default state.
9	IN1N	I	(MDIE1 bit = "1") Differential Analog Negative input 1 pin
10	IN1	I	(MDIE1 bit = "0") Single-ended Analog Input 1 pin
	IN1P	I	(MDIE1 bit = "1") Differential Analog Positive input 1 pin
11	IN2N	I	(MDIE2 bit = "1") Differential Analog Negative input 2 pin
12	IN2	I	(MDIE2 bit = "0") Single-ended Analog Input 2 pin
	IN2P	I	(MDIE2 bit = "1") Differential Analog Positive input 2 pin
13	IN3N	I	(MDIE3 bit = "1") Differential Analog Negative input 1 pin
14	IN3	I	(MDIE3 bit = "0") Single-ended Analog Input 1 pin
	IN3P	I	(MDIE3 bit = "1") Differential Analog Positive input 1 pin
15	IN4N	I	(MDIE4 bit = "1") Differential Analog Negative input 2 pin
16	IN4	I	(MDIE4 bit = "0") Single-ended Analog Input 2 pin
	IN4P	I	(MDIE4 bit = "1") Differential Analog Positive input 2 pin
17	MICBIAS	O	Microphone bias pin.
18	AVDD1	-	Analog Power Supply Pin, 3.0V~3.6V
19	VSS1	-	Ground Pin, 0V
20	VCOM	O	Common Voltage Output Pin, AVDD1x1/2 Large external capacitor around 1μF is used to reduce power-supply noise.
21	IN5N	I	(MDIE5 bit = "1") Differential Analog Negative input 1 pin
22	IN5	I	(MDIE5 bit = "0") Single-ended Analog Input 1 pin
	IN5P	I	(MDIE5 bit = "1") Differential Analog Positive input 1 pin
23	IN6N	I	(MDIE6 bit = "1") Differential Analog Negative input 2 pin
24	IN6	I	(MDIE6 bit = "0") Single-ended Analog Input 2 pin
	IN6P	I	(MDIE6 bit = "1") Differential Analog Positive input 2 pin
25	ROUT6	O	Rch Analog Output 6 Pin
26	LOUT6	O	Lch Analog Output 6 Pin

27	ROUT5	O	Rch Analog Output 5 Pin
28	LOUT5	O	Lch Analog Output 5 Pin
29	ROUT4	O	Rch Analog Output 4 Pin
30	LOUT4	O	Lch Analog Output 4 Pin
31	ROUT3	O	Rch Analog Output 3 Pin
32	LOUT3	O	Lch Analog Output 3 Pin
33	ROUT2	O	Rch Analog Output 2 Pin
34	LOUT2	O	Lch Analog Output 2 Pin
35	ROUT1	O	Rch Analog Output 1 Pin
36	LOUT1	O	Lch Analog Output 1 Pin
37	AVDD2	-	Analog Power Supply Pin, 3.0V~3.6V
38	VSS2	-	Ground Pin, 0V
39	TVDD	-	Digital Power Supply Pin, 3.0V~3.6V
40	VSS3	-	Ground Pin, 0V
41	REGO	O	Regulator Output Pin This pin should be connected to ground with 1.0uF.
42	SDTO1	O	Audio Serial Data Output Pin1
43	SDTO2	O	Audio Serial Data Output Pin2
44	SDTO3	O	Audio Serial Data Output Pin3
45	SDA	I/O	Control Data Input Pin in I^2C Bus Serial control mode
46	SCL	I	Control Data Clock Pin in I^2C Bus serial control mode
47	MCLK	I	External Master Clock Input Pin
48	BICK	I/O	Audio Serial Data Clock Pin

Note 1. All digital input pins must not be allowed to float.

ABSOLUTE MAXIMUM RATINGS

(VSS1 ~ 3 = 0V; Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog1	AVDD1	-0.3	6.0	V
	Analog2	AVDD2	-0.3	6.0	V
	Digital1	TVDD	-0.3	6.0	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD1+0.3	V
Digital Input Voltage (MCLK, LRCK, BICK, SDTI1-6/TDMI, SCL, SDA, PDN pins)		VIND	-0.3	TVDD+0.3	V
Ambient Temperature (power applied)(Note 3)		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground. VSS1 ~ 3 must be connected to the same analog ground plane.
Note 3. In case that PCB wiring density is 100%.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1 ~ 3 = 0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 4)	Analog	AVDD1, AVDD2	3.0	3.3	3.6	V
	Digital	TVDD	3.0	3.3	3.6	V
	Difference	AVDD1, AVDD2 – TVDD	-0.1	0	+0.1	V

Note 4. The power up sequence between AVDD1, AVDD2 and TVDD is not critical. Each power supplies should be powered up during the PDN pin = "L". The PDN pin should be "H" after all power supplies are powered up. All power supplies should be powered on, only a part of these power supplies cannot be powered off. (Power off means power supplies equal to ground or power supplies are floating.) Do not turn off only the AK4618 under the condition that a surrounding device is powered on and the I2C bus is in use. AVDD1 and AVDD2 must be connected with the same power supply.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25ºC; AVDD1, AVDD2=TVDD=3.3V, VSS1 ~ 3 =0V, BICK=64fs; Signal frequency 1kHz; Measurement frequency = 20Hz~20kHz @fs=48kHz, 20Hz~40kHz at fs=96kHz, 20Hz~40kHz at fs=192kHz; Unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
MIC AMP						
Input Resistance			40			kΩ
Gain	MGAIN[2:0]bits=0h			0		dB
	MGAIN[2:0]bits=1h			15		dB
	MGAIN[2:0]bits=2h			18		dB
	MGAIN[2:0]bits=3h			21		dB
	MGAIN[2:0]bits=4h			24		dB
	MGAIN[2:0]bits=5h			27		dB
	MGAIN[2:0]bits=6h			30		dB
	MGAIN[2:0]bits=7h			33		dB
MIC BIAS						
Bias Output Voltage	Load current = 0mA			2.40		V
	Load current = 6mA			2.40		V
Load Resistance			0.4			kΩ
Load Capacitance					30	pF
ADC Analog Input Characteristics(Differential inputs)						
Resolution					24	Bits
S/(N+D) (-1dBFS)	MGAIN[2:0]bits=0h(0dB)		77	87		dB
	MGAIN[2:0]bits=3h(+21dB)			80		dB
DR (-60dBFS with A-weighted)	MGAIN[2:0]bits=0h(0dB)		88	98		dB
	MGAIN[2:0]bits=3h(+21dB)			85		dB
S/N (A-weighted)	MGAIN[2:0]bits=0h(0dB)		88	98		dB
	MGAIN[2:0]bits=3h(+21dB)			85		dB
Interchannel Isolation				110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20		ppm/°C
Input Voltage	Single-ended (AIN=0.81x AVDD1)			2.67		Vpp
	Differential (AIN=±0.81x AVDD1)			±2.67		Vpp
Power Supply Rejection Ratio (Note 5)				60		dB
DAC Analog Output Characteristics						
Resolution					24	Bits
S/(N+D) (0dBFS)	fs=48kHz	BW=20kHz	82	92		dB
	fs=96kHz	BW=40kHz		90		dB
	fs=192kHz	BW=40kHz		90		dB
DR (-60dBFS with A-weighted)			100	106		dB
S/N (A-weighted)			100	106		dB
Interchannel Isolation				100		dB
Interchannel Gain Mismatch (Note 6)				0	0.7	dB
Gain Drift				20		ppm/°C
Output Voltage	AOUT=0.86x AVDD2		2.54	2.83	3.12	Vpp
Load Resistance (AC Load)			5			kΩ
Load Capacitance					30	pF
Power Supply Rejection (Note 5)				60		dB

Note 5. PSRR is applied to AVDD1, AVDD2 and TVDD with 1kHz, 50mVpp.
Note 6. Channel gain mismatch between all output channels (LOUT1-6, ROUT1-6).

Parameter		Min.	Typ.	Max.	Unit
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")					
AVDD1+AVDD2	fs=48kHz		55	77	mA
AVDD1+AVDD2	fs=96kHz, 192kHz		40		mA
TVDD	fs=48kHz		8	12	mA
TVDD	fs=96kHz		7		mA
TVDD	fs=192kHz		10		mA
Power-down mode (PDN pin = "L") (Note 7)					
AVDD1+AVDD2+TVDD			10	200	μA

Note 7. In the power-down mode, all digital input pins including clock pins are held VSS3.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF): Sharp roll-off mode (SD_AD bit = "0")						
Passband (Note 8)	±0.16dB	PB	0	-	18.8	kHz
	–0.28dB		-	20.0	-	kHz
	–3.0dB		-	22.8	-	kHz
Stopband (Note 8)		SB	28.4	-	-	kHz
Stopband Attenuation		SA	71	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	15.5	-	1/fs
ADC Digital Filter (Decimation LPF): Short delay Sharp roll-off mode (SD_AD bit = "1")						
Passband (Note 8)	±0.16dB	PB	0	-	18.8	kHz
	–0.28dB		-	20.0	-	kHz
	–3.0dB		-	22.8	-	kHz
Stopband (Note 8)		SB	28.4		-	-
Stopband Attenuation		SA	72		-	-
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	2.4	1/fs
Group Delay (Note 10)		GD	-	5.5	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	–3.0dB	FR	-	3.7	-	Hz
	–0.5dB		-	10.9	-	Hz
	–0.1dB		-	24.0	-	Hz

FILTER CHARACTERISTICS (fs=48kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	19.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR	-	-0.1	-	dB
DAC Digital Filter (LPF): Slow roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	 22.5	9.8 -	kHz kHz
Stopband		SB	40.1			kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		6.8		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR		-4.0		dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 24.0	21.8 -	kHz kHz
Stopband		SB	26.2	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	6.2	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR		-0.1		dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode (DEM=OFF; SD_DA bit="1" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	- 22.5	9.8 -	kHz kHz
Stopband		SB	40.1	-	-	kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0 ~ 20.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 20.0kHz (Note 11)		FR	-	-4.0	-	dB

FILTER CHARACTERISTICS (fs=96kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 48.0	43.6 -	kHz kHz
Stopband		SB	52.4	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	19.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR	-	-0.3	-	dB
DAC Digital Filter (LPF): Slow roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	 45.0	19.6 -	kHz kHz
Stopband		SB	80.2			kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		6.8		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR		-4.2		dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 48.0	43.6 -	kHz kHz
Stopband		SB	52.4	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	6.2	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR		-0.3		dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode (DEM=OFF; SD_DA bit="1" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	- 45.0	19.6 -	kHz kHz
Stopband		SB	80.2	-	-	kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0 ~ 40.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 40.0kHz (Note 11)		FR	-	-4.2	-	dB

FILTER CHARACTERISTICS (fs=192kHz)

(Ta= -40 ~ +105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF): Sharp roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 96.0	87.2 -	kHz kHz
Stopband		SB	104.8	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 10)		GD	-	19.3	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR	-	-1.0	-	dB
DAC Digital Filter (LPF): Slow roll-off mode (DEM=OFF; SD_DA bit="0" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	 90.0	39.2 -	kHz kHz
Stopband		SB	160.4			kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50			dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD		0		1/fs
Group Delay (Note 10)		GD		6.8		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR		-5.0		dB
DAC Digital Filter (LPF): Short delay Sharp roll-off mode (DEM=OFF; SD_DA bit="1"; SLOW bit="0")						
Passband (Note 8)	±0.06dB −6.0dB	PB	0 -	- 96.0	87.2 -	kHz kHz
Stopband		SB	104.8	-	-	kHz
Passband Ripple		PR	-0.06		+0.06	dB
Stopband Attenuation		SA	52	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	-	1.7	1/fs
Group Delay (Note 10)		GD	-	6.2	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR		-1.0		dB
DAC Digital Filter (LPF): Short delay Slow roll-off mode (DEM=OFF; SD_DA bit="1" ; SLOW bit="1")						
Passband (Note 9)	±0.06dB −6.0dB	PB	0 -	- 90.0	39.2 -	kHz kHz
Stopband		SB	160.4	-	-	kHz
Passband Ripple		PR	-4.0		+0.06	dB
Stopband Attenuation		SA	50	-	-	dB
Group Delay Distortion 0 ~ 80.0kHz		ΔGD	-	-	0.5	1/fs
Group Delay (Note 10)		GD	-	5.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response 0 ~ 80.0kHz (Note 11)		FR	-	-5.0	-	dB

Note 8. The passband and stopband frequencies scale with fs (sampling frequency). For example, ADC: Passband (±0.1dB) = 0.375 x fs, DAC: Passband (±0.06dB) = 0.454 x fs (@ fs=48kHz).

Note 9. The passband and stopband frequencies scale with fs (sampling frequency). For example, DAC: Passband (±0.06dB) = 0.204 x fs (@ fs=48kHz).

Note 10. The calculated delay time is resulting from digital filtering. For the ADC, this time is from the input of an analog signal to the setting of 24bit data for both channels to the ADC output register. For the DAC, this time is from setting the 24 bit data both channels at the input register to the output of an analog signal.

Note 11. The reference frequency is 1kHz.

DC CHARACTERISTICS

(Ta=-40°C~+105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage (MCLK, LRCK, BICK, SDTI1-6/TDMI, SCL, SDA, PDN pins)	VIH	70% TVDD	-	-	V
Low-Level Input Voltage (MCLK, LRCK, BICK, SDTI1-6/TDMI, SCL, SDA, PDN pins)	VIL	-	-	30% TVDD	V
High-Level Output Voltage (LRCK, BICK, SDTO1-3 pins: Iout=-100µA)	VOH	TVDD-0.5	-	-	V
Low-Level Output Voltage (LRCK, BICK, SDTO1-3 pins: Iout= 100µA)	VOL		-	0.5	V
(SDA pin: Iout= 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta=-40~+105°C; AVDD1, AVDD2= TVDD=3.0~ 3.6V; C_L=20pF; unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock Timing					
External Clock					
256fsn:	fCLK	2.048		12.288	MHz
Pulse Width Low	tCLKL	32			ns
Pulse Width High	tCLKH	32			ns
384fsn:	fCLK	3.072		18.432	MHz
Pulse Width Low	tCLKL	22			ns
Pulse Width High	tCLKH	22			ns
512fsn:	fCLK	4.096		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
256fsd, 128fsq:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	16			ns
Pulse Width High	tCLKH	16			ns
LRCK Timing (Slave mode)					
Stereo mode					
(TDM1-0 bits = "00")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	45		55	%
TDM512 mode (Note 12)					
(TDM1-0 bits = "01")					
LRCK frequency	fsn	8		48	kHz
"H" time	tLRH	1/512fs			ns
"L" time	tLRL	1/512fs			ns
TDM256 mode (Note 13)					
(TDM1-0 bits = "10")					
LRCK frequency	fsn	8		48	kHz
	fsd	64		96	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM128 mode (Note 14)					
(TDM1-0 bits = "11")					
LRCK frequency	fsq	128		192	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns
LRCK Timing (Master Mode)					
Stereo mode					
(TDM1-0 bits = "00")					
Normal Speed Mode	fsn	8		48	kHz
Double Speed Mode	fsd	64		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	-	50	-	%
TDM512 mode (Note 12)					
(TDM1-0 bits = "01")					
LRCK frequency	fsn	8		48	kHz
"H" time (Note 15)	tLRH		1/16fs		ns
TDM256 mode (Note 13)					
(TDM1-0 bits = "10")					
LRCK frequency	fsn	8		48	kHz
	fsd	64		96	kHz
"H" time (Note 15)	tLRH		1/8fs		ns

TDM128 mode (Note 14) **(TDM1-0 bits = "11")**						
LRCK frequency		fsq	128		192	kHz
"H" time	(Note 15)	tLRH		1/4fs		ns

Note 12. Please use for Normal Speed mode. Master clock should be input the 512fs in Master mode.
Note 13. Please use for Normal Speed mode, Double Speed mode. Master clock should be input the 256fs or 512fs in Master mode.
Note 14. Please use for Quad Speed mode. Master clock should be input the 128fs in Master mode.
Note 15. If the format is I^2S, it is "L" time.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Slave mode)						
Stereo mode (TDM1-0 bits = "00") **for Normal Speed mode**						
BICK Period		tBCK	324			ns
BICK Pulse Width Low		tBCKL	130			ns
Pulse Width High		tBCKH	130			ns
LRCK Edge to BICK "↑"	(Note 16)	tLRB	20			ns
BICK "↑" to LRCK Edge	(Note 16)	tBLR	20			ns
LRCK to SDTO(MSB) (Except I^2S mode)		tLRS			80	ns
BICK "↓" to SDTO		tBSD			80	ns
SDTI Hold Time		tSDH	50			ns
SDTI Setup Time		tSDS	50			ns
Stereo mode (TDM1-0 bits = "00") **for Double and Quad Speed mode**						
BICK Period		tBCK	81			ns
BICK Pulse Width Low		tBCKL	33			ns
Pulse Width High		tBCKH	33			ns
LRCK Edge to BICK "↑"	(Note 16)	tLRB	23			ns
BICK "↑" to LRCK Edge	(Note 16)	tBLR	23			ns
SDTI Hold Time		tSDH	10			ns
SDTI Setup Time		tSDS	10			ns
TDM512 mode (TDM1-0 bits = "01") (Note 12)						ns
BICK Period		tBCK	40			ns
BICK Pulse Width Low		tBCKL	16			ns
Pulse Width High		tBCKH	16			ns
LRCK Edge to BICK "↑"	(Note 16)	tLRB	10			ns
BICK "↑" to LRCK Edge	(Note 16)	tBLR	10			ns
SDTO Setup time BICK "↑"		tBSS	6			ns
SDTO Hold time BICK "↑"		tBSH	5			ns
SDTI/TDMI Hold Time		tSDH	5			ns
SDTI/TDMI Setup Time		tSDS	6			ns
TDM256 mode (TDM1-0 bits = "10") (Note 13)						ns
BICK Period		tBCK	40			ns
BICK Pulse Width Low		tBCKL	16			ns
Pulse Width High		tBCKH	16			ns
LRCK Edge to BICK "↑"	(Note 16)	tLRB	10			ns
BICK "↑" to LRCK Edge	(Note 16)	tBLR	10			ns
SDTO Setup time BICK "↑"		tBSS	6			ns
SDTO Hold time BICK "↑"		tBSH	5			ns
SDTI/TDMI Hold Time		tSDH	5			ns
SDTI/TDMI Setup Time		tSDS	6			ns

TDM128 mode (TDM1-0 bits = "11") (Note 14)					
BICK Period	tBCK	40			ns
BICK Pulse Width Low	tBCKL	16			ns
Pulse Width High	tBCKH	16			ns
LRCK Edge to BICK "↑" (Note 16)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 16)	tBLR	10			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Master mode)					
Stereo mode (TDM1-0 bits = "00") for Normal Speed mode					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–80	-	80	ns
BICK "↓" to SDTO	tBSD	–80	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Stereo mode (TDM1-0 bits = "00") for Double and Quad Speed mode					
BICK Frequency	fBCK	-	64fs	-	Hz
BICK Duty (Note 17)	dBCK	-	50	-	%
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns
TDM512 mode (TDM1-0 bits = "01") (Note 12)					
BICK Frequency	fBCK	-	512fs	-	Hz
BICK Duty (Note 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	-10		10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	-	ns
SDTI/TDMI Hold Time	tSDH	5	-	-	ns
SDTI/TDMI Setup Time	tSDS	6	-	-	ns
TDM256 mode (TDM1-0 bits = "10") (Note 13)					
BICK Frequency	fBCK	-	256fs	-	Hz
BICK Duty (Note 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTO Setup time BICK "↑"	tBSS	6	-	-	ns
SDTO Hold time BICK "↑"	tBSH	5	-	--	ns
SDTI/TDMI Hold Time	tSDH	5	-	-	ns
SDTI/TDMI Setup Time	tSDS	6	-		ns
TDM128 mode (TDM1-0 bits = "11") (Note 14)					
BICK Frequency	fBCK	-	128fs	-	Hz
BICK Duty (Note 17)	dBCK	-	50	-	%
BICK "↓" to LRCK	tMBLR	–10	-	10	ns
SDTI Hold Time	tSDH	10	-	-	ns
SDTI Setup Time	tSDS	10	-	-	ns

Note 16. BICK rising edge must not occur at the same time as LRCK edge.
Note 17. The case that duty of MCLK is 50%.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 18)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 19)	tPD	150			ns
PDN "↑" to SDTO valid (Note 20)	tPDV		32768/MCLK +1059/fs		1/fs

Note 18. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 19. The AK4618 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 150ns for a certain reset. The AK4618 is not reset by the "L" pulse less than 30ns.

Note 20. These cycles are the numbers of MCLK and LRCK rising from the PDN pin rising.

Note 21. I^2C-bus is a trademark of NXP B.V.

■ Timing Diagram

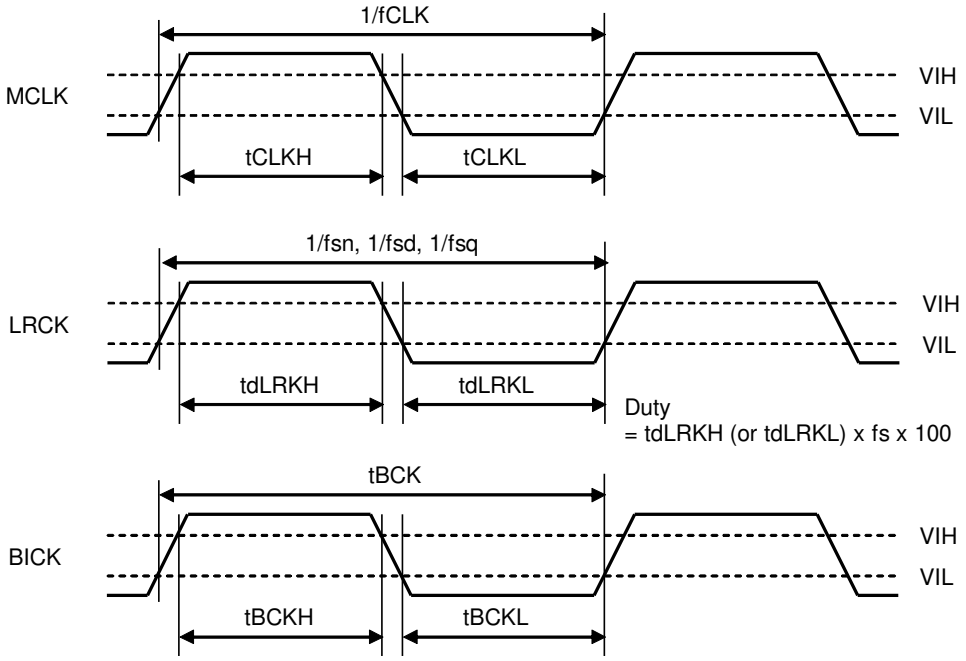


Figure 2. Clock Timing (TDM1-0 bits = "00" & Slave mode)

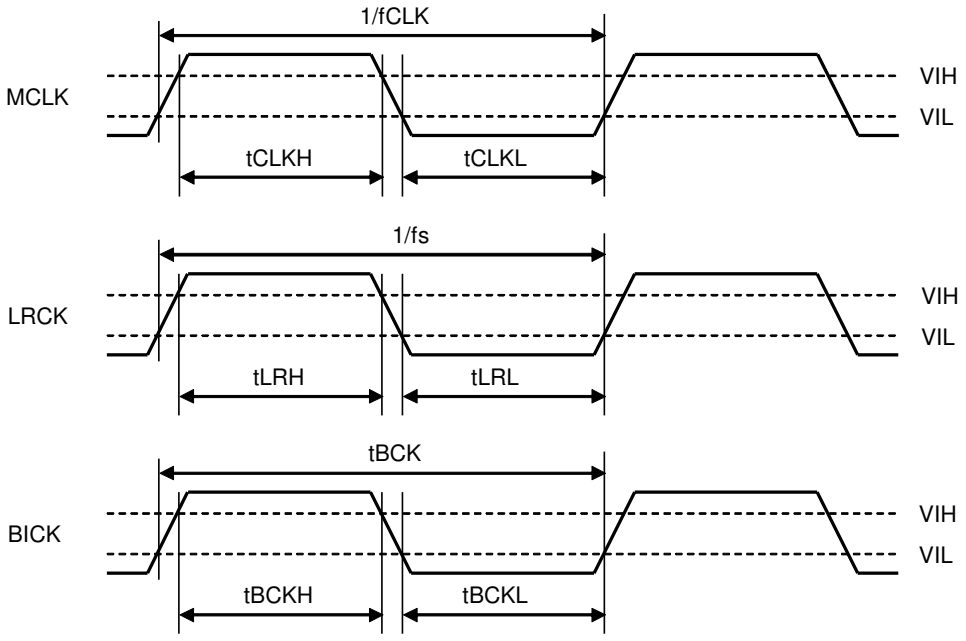


Figure 3. Clock Timing (Except TDM1-0 bits = "00" & Slave mode)

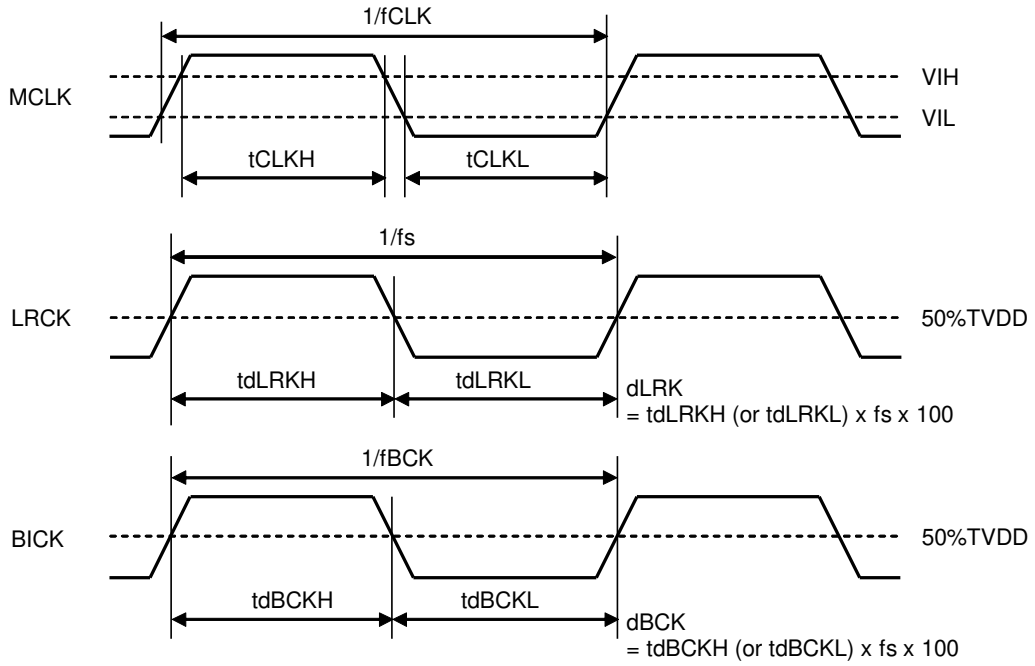


Figure 4. Clock Timing (TDM1-0 bits = "00" & Master mode)

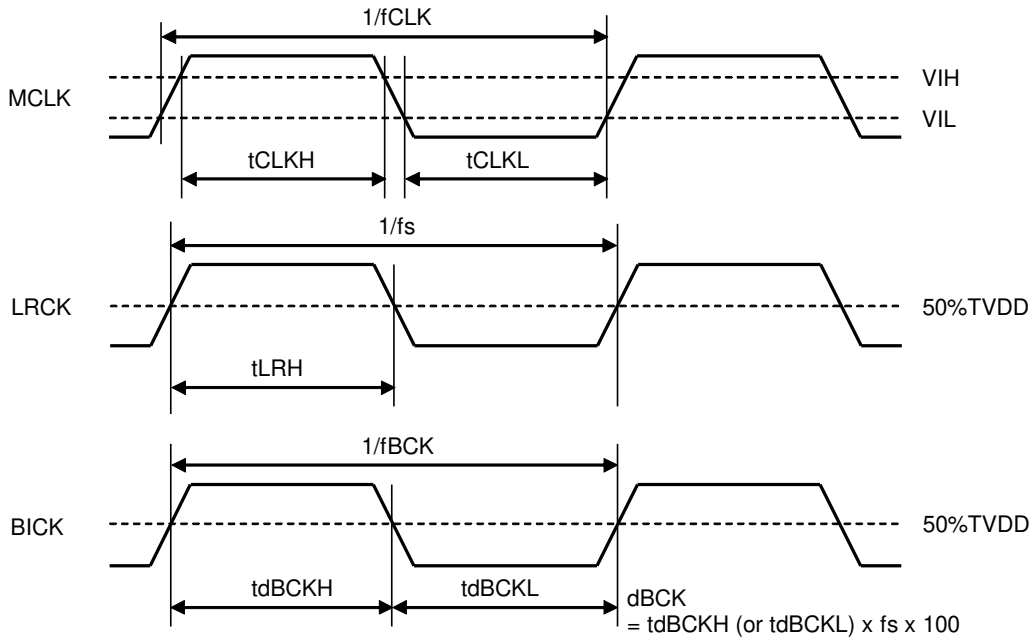


Figure 5. Clock Timing (Except TDM1-0 bits = "00" & Master mode)

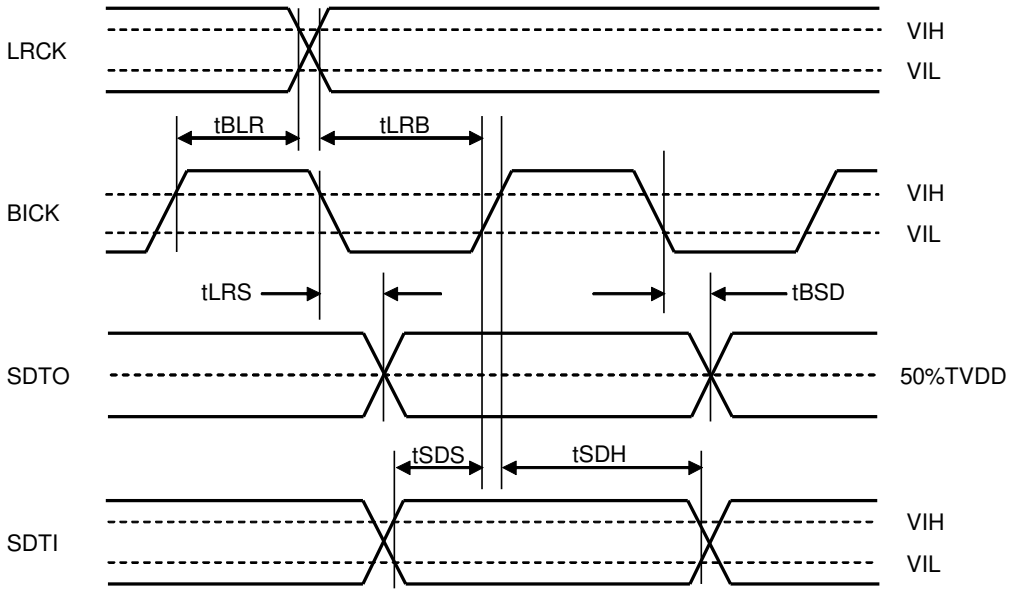


Figure 6. Audio Interface Timing (TDM1-0 bits = "00" & Slave mode)

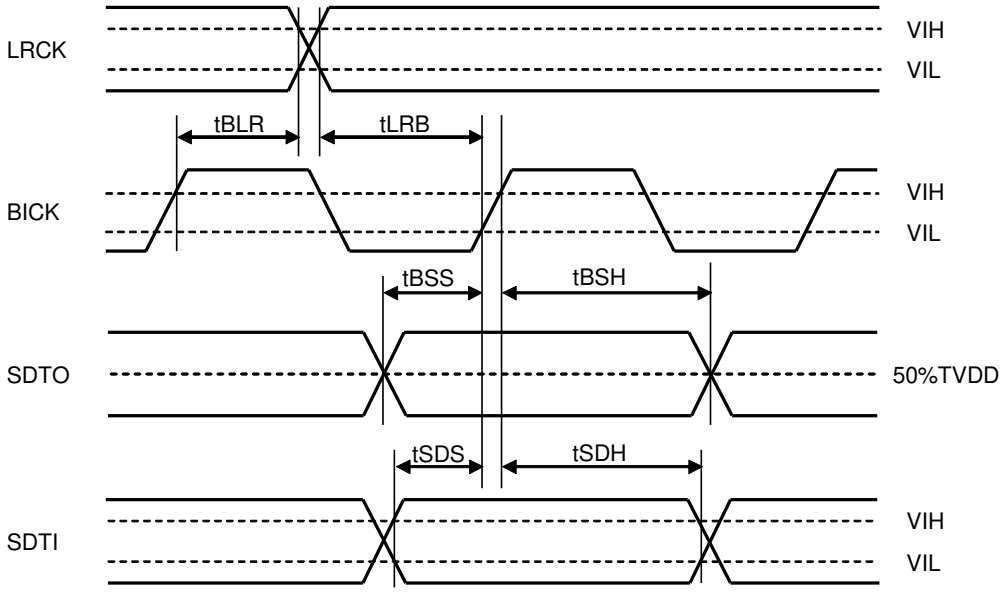


Figure 7. Audio Interface Timing (Except TDM1-0 bits = "00" & Slave mode)

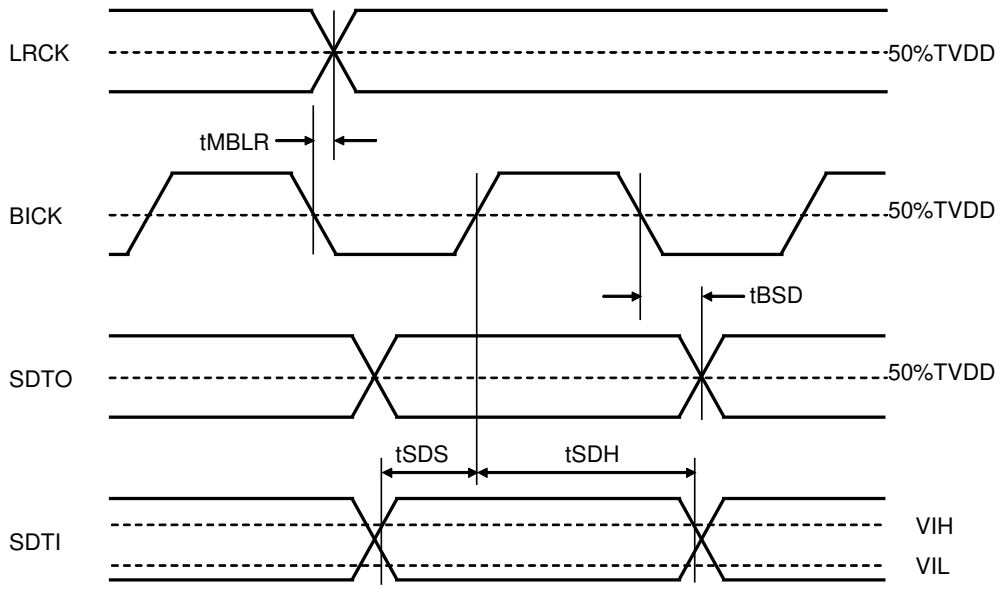


Figure 8. Audio Interface Timing (TDM1-0 bits = "00" & Master mode)

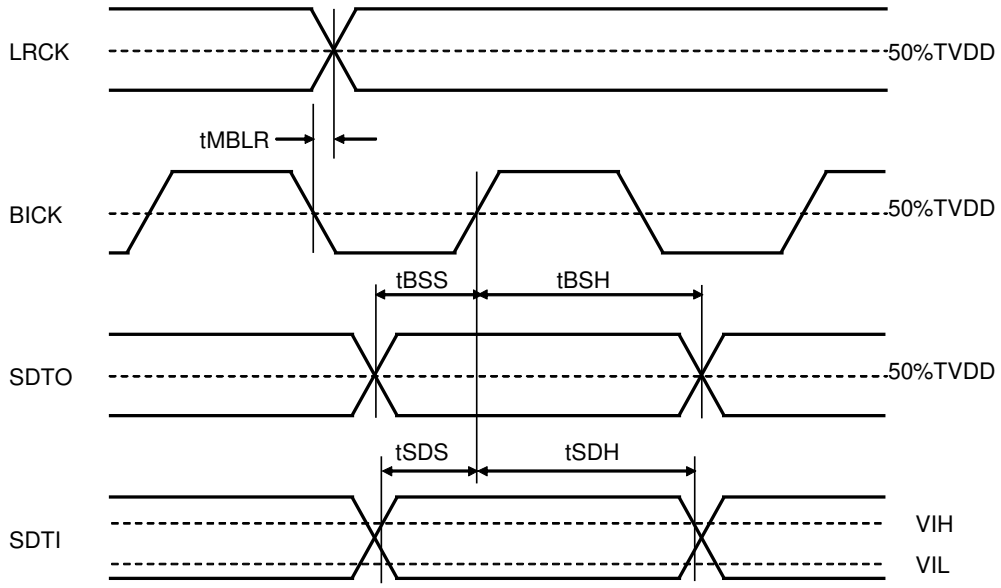


Figure 9. Audio Interface Timing (Except TDM1-0 bits = "00" & Master mode)

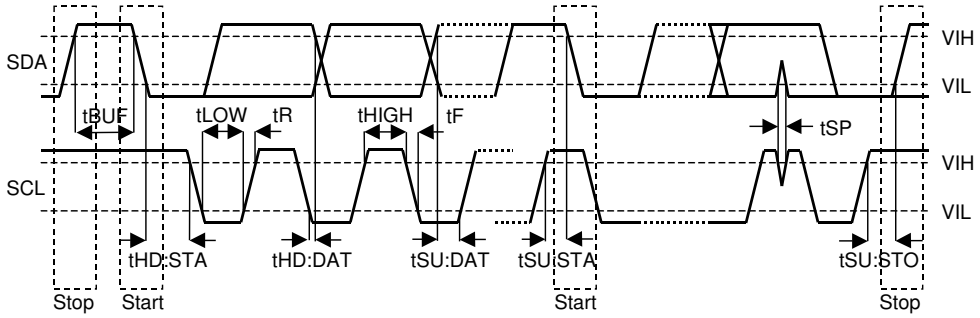


Figure 10. I^{2}C Bus mode Timing

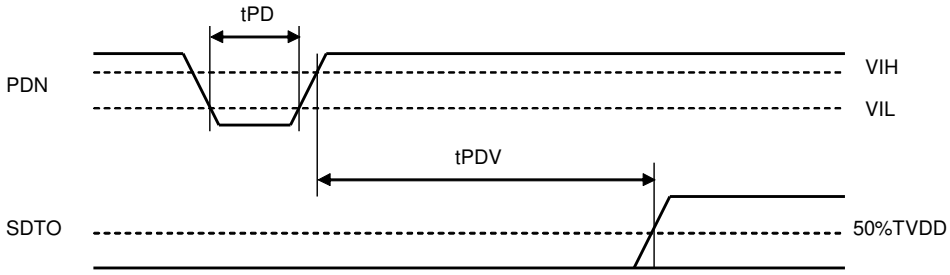


Figure 11. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks which are required to operate the AK4618 in slave mode are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK but the phase is not critical. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit= "0": Default), the sampling speed is set by DFS0, DFS1 (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 3, Table 4, Table 5). In Auto Setting Mode (ACKS bit= "1"), as MCLK frequency is detected automatically (Table 6) and the internal master clock attains the appropriate frequency (Table 7), so it is not necessary to set DFS.

In master mode, only MCLK is required. Master Clock Input Frequency should be set with the CKS1-0 bits, and the sampling speed should be set by the DFS1-0 bits. The frequencies and the duties of the clocks (LRCK, BICK) are not stabile immediately after setting CKS1-0 bits and DFS1-0 bits up.

After exiting reset at power-up in slave mode, the AK4618 is in power-down mode until MCLK and LRCK are input.

If the clock is stopped, click noise occurs when restarting the clock. Mute the digital output externally if the click noise influences system applications.

Note: ADC is automatically powered-down in Doble Speed Mode and Quad Speed Mode.

DFS1	DFS0	Sampling Speed Mode (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	(default)
0	1	Double Speed Mode	64kHz~96kHz	
1	0	Quad Speed Mode	128kHz~192kHz	
1	1	N/A	-	

(N/A: Not available)

Table 1. Sampling Speed (Manual Setting Mode)

CKS1	CKS0	Normal Speed Mode	Double Speed Mode	Quad Speed Mode	
0	0	256fs	256fs	128fs	
0	1	384fs	256fs	128fs	
1	0	512fs	256fs	128fs	(default)
1	1	512fs	256fs	128fs	

Table 2. Master Clock Input Frequency Select (Master Mode)
Note: In Normal Speed Mode, TDM mode (TDM1-0 bits ="01) can be used when CKS1 bit = "1".

LRCK	MCLK (MHz)			BICK (MHz)
fs	256fs	384fs	512fs	64fs
32.0kHz	8.1920	12.2880	16.3840	2.0480
44.1kHz	11.2896	16.9344	22.5792	2.8224
48.0kHz	12.2880	18.4320	24.5760	3.0720

Table 3. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)	BICK (MHz)
fs	256fs	64fs
88.2kHz	22.5792	5.6448
96.0kHz	24.5760	6.1440

Table 4. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK (MHz)	BICK (MHz)
fs	128fs	64fs
176.4kHz	22.5792	11.2896
192.0kHz	24.5760	12.2880

Table 5. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK	Sampling Speed Mode
512fs	Normal Speed Mode
256fs	Double Speed Mode
128fs	Quad Speed Mode

Table 6. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)			Sampling Speed Mode
fs	128fs	256fs	512fs	
32.0kHz	-	-	16.3840	Normal Speed Mode
44.1kHz	-	-	22.5792	
48.0kHz	-	-	24.5760	
88.2kHz	-	22.5792	-	Double Speed Mode
96.0kHz	-	24.5760	-	
176.4kHz	22.5792	-	-	Quad Speed Mode
192.0kHz	24.5760	-	-	

Table 7. System Clock Example (Auto Setting Mode)

■ De-emphasis Filter

The AK4618 has a digital de-emphasis filter (tc=50/15μs) by an IIR filter. The de-emphasis filter supports only Normal Speed Mode. This filter corresponds to three sampling frequencies (32kHz, 44.1kHz, 48kHz). De-emphasis of each DAC can be set individually by registers, DAC1(SDTI1), DAC2(SDTI2), DAC3(SDTI3), DAC4(SDTI4), DAC5(SDTI5), DAC6(SDTI6).

Mode	Sampling Speed Mode	DEM11 (DEM61-21)	DEM10 (DEM60-20)	DEM	
0	Normal Speed Mode	0	0	44.1kHz	
1	Normal Speed Mode	0	1	OFF	(default)
2	Normal Speed Mode	1	0	48kHz	
3	Normal Speed Mode	1	1	32kHz	

Table 8. De-emphasis Control

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 3.7Hz at fs=48kHz and scales with the sampling rate (fs).

■ Master Mode and Slave Mode

Master Mode and Slave Mode are selected by setting the MS bit.
LRCK and BICK pins are outputs in Master Mode (MS bit= “1”)
LRCK and BICK pins are inputs in Slave Mode (MS bit= “0”)

The BICK and LRCK pins are in Hi-z state before an internal power up and MS bit = "1".
When a problem is occurred by this, pulldown BICK and LRCK pins by external resistance(ex. 100kohm).

PDN	MS bit	LRCK pin	BICK pin
L	0	Input	Input
	1	Hi-z	Hi-z
H	0	Input	Input
	1	Output	Output

Table 9. LRCK and BICK pins