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AK4620B

24-Bit 192kHz Audio CODEC with IPGA

GENERAL DESCRIPTION

The AK4620B is a high performance 24-bit CODEC that supports up to 192kHz record and playback. The on-board analog-to-digital converter has a high dynamic range due to AKM's Enhanced Dual-Bit architecture. The DAC utilizes AKM's Advanced Multi-Bit architecture that achieves low out-of-band noise and high jitter tolerance through the use of Switched Capacitor Filter (SCF) technology. The AK4620B has an input Programmable Gain Amplifier and is ideal for Pro Audio sound cards, Digital Audio Workstations, DVD-R, hard disk, CD-R recording/playback systems, and musical instrument recording.

FEATURES

- **24-bit 2-channel ADC**
  - **Selectable Single-ended or Differential Input**
  - **High Performance Linear Phase Digital Anti-Alias Filter**
    - **Passband: 0 ~ 20.25kHz (@fs=44.1kHz)**
    - **Ripple: ± 0.005dB**
    - **Stopband Attenuation: 100dB**
  - **S/(N+D): 90dB (single-ended)**
    100dB (differential)
  - **S/N: 110dB (single-ended)**
    113dB (differential)
  - **Digital High-pass Filter for Offset Cancellation**
  - **Input PGA: 0dB to +18dB, 0.5dB/step (for single-ended input)**
  - **Input Digital Attenuator: 0dB to – 63dB, 0.5dB/step**
  - **Overflow Flag**
  - **Audio Interface Format: MSB justified or I^2S**

- **24-bit 2-channel DAC**
  - **24-bit 8 times Oversampling Linear Phase Digital Filter**
    - **Ripple: ±0.005dB**
    - **Stopband Attenuation: 75dB**
  - **Switched-cap Low Pass Filter**
  - **Differential Outputs**
  - **S/(N+D): 97dB**
  - **S/N: 115dB**
  - **De-emphasis for 32kHz, 44.1kHz, 48kHz Sampling**
  - **Output Digital Attenuator: Linear 255 steps**
  - **Soft Mute**
  - **Zero Detection Function**
  - **Audio interface format: MSB justified, LSB justified, I^2S, or DSD**

- **High Jitter Tolerance**
- **Sampling Rate: Up to 216kHz**
- **μP Interface: 3-wire Serial Interface**
- **Master Clock**
  - **128fs/192fs/256fs/384fs/512fs/768fs/1024fs**
- **Power Supply: 5V ± 5%(Analog), 3V~3.6V with 5V tolerant I/O(Digital)**
- **Small 30-pin VSOP package**
- **Ta: -10 to 70 °C**

■ Block Diagram

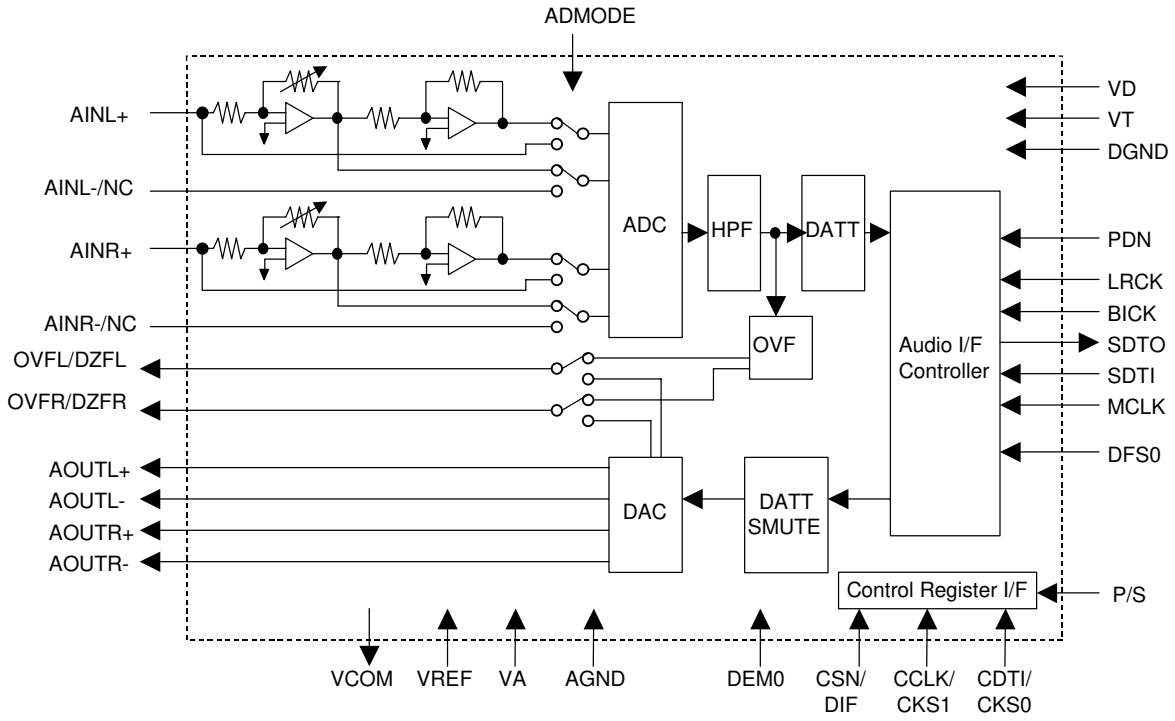


Figure 1. Block Diagram

- **Compatibility with AK4528 / AK4524**

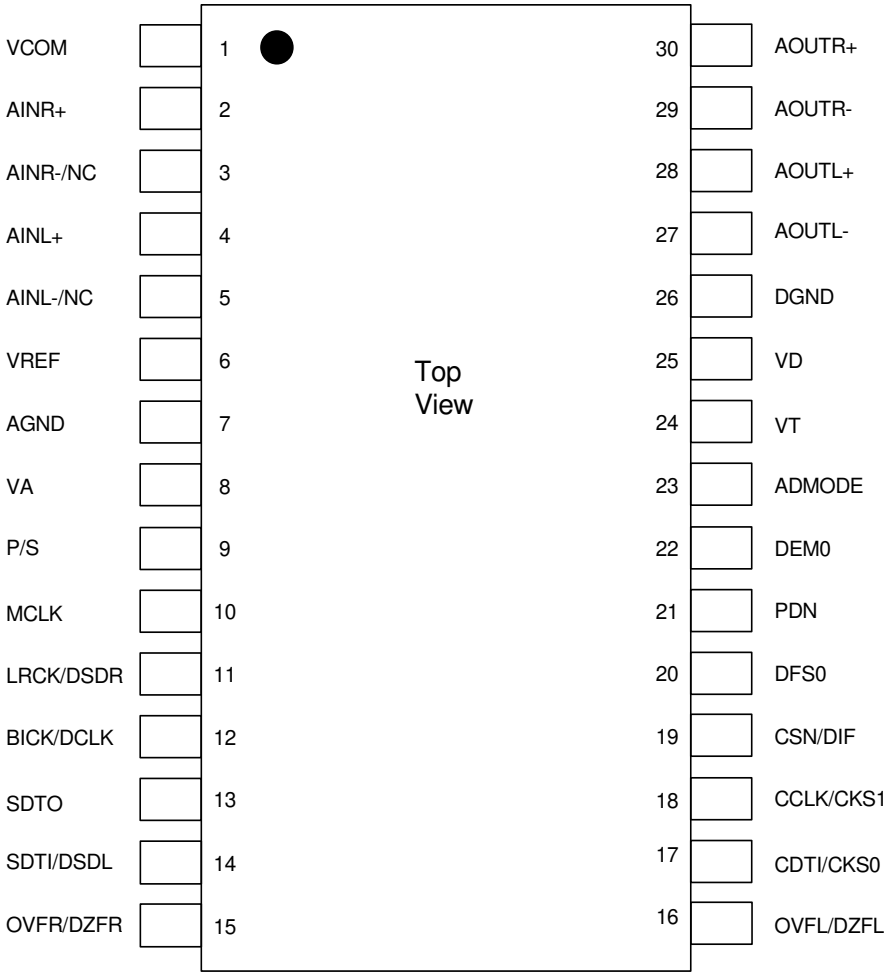
Function	AK4524	AK4528	AK4620B	
Max fs	96kHz	108kHz	216kHz	
ADC Inputs	Single-ended	Differential	Single-ended	Differential
Input analog PGA	0dB ~ +18dB 0.5dB/step	-	0 ~ +18dB 0.5dB/step	-
Input digital ATT	Mute, -72dB ~ 0dB Pseudo-log step	Mute, -72dB ~ 0dB Pseudo-log step	Mute,-63.5dB ~ 0dB 0.5dB/step	Mute,-63.5dB ~ 0dB 0.5dB/step
ADC S/(N+D)	90dB	94dB	90dB	100dB
ADC DR, S/N	100dB	108dB	110dB	113dB
ADC Digital Filter SA	75dB	75dB	100dB	
ADC Overflow detection	-	-	X	
DAC S/(N+D)	94dB	94dB	97dB	
DAC DR, S/N	110dB	110dB	115dB	
Output digital Attenuator	Mute, -72dB ~ 0dB Pseudo-log step	Mute, -72dB ~ 0dB Pseudo-log step	Mute, -48dB ~ 0dB Linear 256 steps	Mute, -48dB ~ 0dB Linear 256 steps
DAC DSD mode	-	-	X	
DAC Zero-data detection	-	-	X	
X'tal Oscillating Circuit	X	-	-	
Master Mode	X	-	-	
Parallel Mode	-	X	X	

X: Available, -: NOT available

■ Ordering Guide

AK4620BVF	-10~+70°C	30pin VSOP (0.65mm pitch)
AKD4620B	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin, VA/2 Bias voltage of ADC inputs and DAC outputs.
2	AINR+	I	Rch Positive Input Pin
3	AINR-	I	Rch Negative Input Pin (when ADMODE pin="H")
		I	No Connect pin (when ADMODE pin="L") No internal bonding. This pin should be open.
4	AINL+	I	Lch Positive Input Pin
5	AINL-	I	Lch Negative Input Pin (when ADMODE pin="H")
		I	No Connect pin (when ADMODE pin="L") No internal bonding. This pin should be open.
6	VREF	I	Voltage Reference Input Pin, VA Used as a voltage reference by ADC & DAC. VREF is connected externally to filtered VA.
7	AGND	-	Analog Ground Pin
8	VA	-	Analog Power Supply Pin, 4.75 ~ 5.25V
9	P/S	I	Parallel/Serial Mode Select Pin "L": Serial Mode, "H": Parallel Mode Do not change this pin during PDN pin = "H".
10	MCLK	I	Master Clock Input Pin
11	LRCK	I	Input/Output Channel Clock Pin (in Parallel mode or when D/P bit="0" in Serial Mode)
	DSDR	I	DSD Rch Data Input Pin (when D/P bit="1" in Serial Mode)
12	BICK	I	Audio Serial Data Clock Pin (in Parallel mode or when D/P bit="0" in Serial Mode)
	DCLK	I	DSD Clock Pin (when D/P bit="1" in Serial Mode)
13	SDTO	O	Audio Serial Data Output Pin
14	SDTI	I	Audio Serial Data Input Pin (in Parallel mode or when D/P bit="0" in Serial Mode)
	DSDL	I	DSD Lch Data Input Pin (when D/P bit="1" in Serial Mode)
15	OVFR	O	Rch Over Flow Flag Pin (in Parallel mode or when ZOS bit="0" in Serial Mode)
	DZFR	O	Rch Zero Detection Flag Pin (when ZOS bit="1" in Serial Mode)
16	OVFL	O	Lch Over Flow Flag Pin (in Parallel mode or when ZOS bit="0" in Serial Mode)
	DZFL	O	Lch Zero Detection Flag Pin (when ZOS bit="1" in Serial Mode)
17	CDTI	I	Control Data Input Pin (in Serial Mode)
	CKS0	I	Master Clock Select Pin (in Parallel Mode)
18	CCLK	I	Control Data Clock Pin (in Serial Mode)
	CKS1	I	Master Clock Select Pin (in Parallel Mode)
19	CSN	I	Chip Select Pin in Serial Mode (in Serial Mode)
	DIF	I	Digital Audio Interface Select Pin (in Parallel Mode) "L": 24bit MSB justified, "H": I^2S compatible
20	DFS0	I	Double Speed Sampling Mode Pin
21	PDN	I	Power-Down Mode Pin "L": Power down reset and initialize the control register, "H": Power up
22	DEM0	I	De-emphasis Control Pin
23	ADMODE	I	Analog Input Mode Select Pin "L": Single-ended Input & IPGA Enable "H": Differential Input & IPGA Bypass

PIN/FUNCTION (Continued)

24	VT	-	Input Buffer Tolerant Pin, 3.0 ~ 5.25V
25	VD	-	Digital Power Supply Pin, 3.0 ~ 3.6V
26	DGND	-	Digital Ground Pin
27	AOUTL-	O	Lch Negative Analog Output Pin
28	AOUTL+	O	Lch Positive Analog Output Pin
29	AOUTR-	O	Rch Negative Analog Output Pin
30	AOUTR+	O	Rch Positive Analog Output Pin

Note. Do not allow digital input pins (P/S, MCLK, LRCK/DSDR, BICK/DCLK, SDTI/DSDL, CDTI/CKS0, CCLK/CKS1, CSN/DIF, DFS0, PDN, DEM0 and ADMODE pins) to float.

■ Handling of Unused Pin

The unused I/O pin should be processed appropriately as below.

Classification	Pin Name	Setting
Analog Input	AINL+, AINL-/NC, AINR+, AINR+NC	These pins should be open when ADMODE pin = "L".
	AINL+, AINL-/NC	AINL+ pin is connected to AINL-/NC pin when ADMODE pin = "H".
	AINR+, AINR-/NC	AINR+ pin is connected to AINR-/NC pin when ADMODE pin = "H".
Analog Output	AOUTL+, AOUTL-, AOUTR+, AOUTR-	These pins should be open.
Digital Input	DEM0	This pin should be connected to DVSS.
Digital Output	OVFL/DZFL, OVFR/DZFR	These pins should be open.

ABSOLUTE MAXIMUM RATINGS

(AGND, DGND=0V;Note 1)

Parameter			Symbol	min	max	Units
Power Supplies:	Analog		VA	-0.3	6.0	V
	Digital		VD	-0.3	6.0	V
	Input Tolerant		VT	-0.3	6.0	V
	|AGND – DGND|	(Note 2)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies			IIN	-	±10	mA
Analog Input Voltage		(Note 3)	VINA	-0.3	VA+0.3	V
Digital Input Voltage		(Note 4)	VIND	-0.3	VT+0.3	V
Ambient Temperature (powered applied)			Ta	-10	70	°C
Storage Temperature			Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AGND and DGND must be connected to the same analog ground plane.
Note 3. AINL+, AINL-/NC, AINR+ and AINR-/NC pins
Note 4. P/S, MCLK, LRCK/DSDR, BICK/DCLK, SDTI/DSDL, CDTI/CKS0, CCLK/CKS1, CSN/DIF, DFS0, PDN, DEM0 and ADMODE pins.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND=0V;Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	VA	4.75	5.0	5.25	V
(Note 5)	Digital	VD	3.0	3.3	3.6	V
	Input Tolerant	VT	VD	5.0	5.25	V
Voltage Reference		VREF	3.0	-	VA	V

Note 5. The power up sequence among VA, VD and VT is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS (ADC: Single-ended Input)

(Ta=25°C; VA=5V, VD=3.3V, VT=5V; AGND=DGND=0V; VREF=VA; fs=44.1kHz; Signal Frequency =1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=44.1kHz, 40Hz ~ 40kHz at fs=96kHz, 40Hz ~ 40kHz at fs=192kHz; unless otherwise specified)

Parameter			min	typ	max	Units
Input PGA Characteristics:						
Input Voltage		(Note 6)	2.77	3.07	3.37	Vpp
Input Resistance		(Note 7)	0.7	5.1	-	kΩ
Step Size			0.2	0.5	0.8	dB
Gain Control Range			0		18	dB
ADC Analog Input Characteristics: IPGA=0dB						
Resolution					24	Bits
S/(N+D)	fs=44.1kHz	-1dBFS	80	90		dB
	BW=20kHz	-60dBFS	-	47		dB
	fs=96kHz	-1dBFS	-	90		dB
	BW=40kHz	-60dBFS	-	44		dB
	fs=192kHz	-1dBFS	-	90		dB
	BW=40kHz	-60dBFS	-	44		dB
Dynamic Range		(-60dBFS with A-weighted)	-	110		dB
S/N		(A-weighted)	101	110		dB
Interchannel Isolation			90	105		dB
Interchannel Gain Mismatch				0.2	0.5	dB
Gain Drift				150	-	ppm/°C
Power Supply Rejection		(Note 8)	-	50		dB

ANALOG CHARACTERISTICS (ADC: Differential Input)

(Ta=25°C; VA=5V, VD=3.3V, VT=5V; AGND=DGND=0V; VREF=VA; fs=44.1kHz; Signal Frequency =1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=44.1kHz, 40Hz ~ 40kHz at fs=96kHz, 40Hz ~ 40kHz at fs=192kHz; unless otherwise specified)

Parameter			min	typ	max	Units
ADC Analog Input Characteristics:						
Resolution					24	Bits
Input Voltage		(Note 9)	±2.62	±2.82	±3.02	Vpp
Input Resistance		fs=44.1kHz	8	14	-	kΩ
		fs=48kHz	-	13	-	kΩ
		fs=96kHz	-	13	-	kΩ
		fs=192kHz	-	13	-	kΩ
S/(N+D)	fs=44.1kHz	-1dBFS	90	100		dB
	BW=20kHz	-60dBFS	-	50		dB
	fs=96kHz	-1dBFS	-	100		dB
	BW=40kHz	-60dBFS	-	46		dB
	fs=192kHz	-1dBFS	-	100		dB
	BW=40kHz	-60dBFS	-	46		dB
Dynamic Range		(-60dBFS with A-weighted)	-	113		dB
S/N		(A-weighted)	103	113		dB
Interchannel Isolation			90	120		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				20	-	ppm/°C
Power Supply Rejection		(Note 8)	-	50		dB

Note 6. Full scale (0dB) of the input voltage at PGA=0dB.
This voltage is proportional to VREF. Vin(typ) = 3.07Vpp x VREF/5.
Note 7. These values become smaller when a gain of IPGA is large.
IPGA=0dB; typ. 5.1kΩ, IPGA=+18dB; typ. 1.18kΩ
Note 8. PSR is applied to VA, VD, VT with 1kHz, 50mVpp. VREF pin is held a constant voltage.
Note 9. Full scale (0dB) of the input voltage at 0dB. This voltage is proportional to VREF.
Vin (typ) = ±2.82Vpp x VREF/5.

ANALOG CHARACTERISTICS (DAC)

(Ta=25°C; VA=5V, VD=3.3V, VT=5V; AGND=DGND=0V; VREF=VA; fs=44.1kHz; Signal Frequency =1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=44.1kHz, 40Hz ~ 40kHz at fs=96kHz, 40Hz ~ 40kHz at fs=192kHz; unless otherwise specified)

DAC Analog Output Characteristics:						
Parameter			**min**	**typ**	**max**	**Units**
Resolution					24	Bits
Dynamic Characteristics						
S/(N+D)	fs=44.1kHz	0dBFS	87	97		dB
	BW=20kHz	–60dBFS	-	52		dB
	fs=96kHz	0dBFS	-	97		dB
	BW=40kHz	–60dBFS	-	49		dB
	fs=192kHz	0dBFS	-	97		dB
	BW=40kHz	–60dBFS	-	49		dB
Dynamic Range (–60dBFS with A-weighted) (Note 10, Note 11)			-	115		dB
S/N (A-weighted) (Note 11, Note 12)			107	115		dB
Interchannel Isolation (1kHz)			90	110		dB
DC Accuracy						
Interchannel Gain Mismatch				0.15	0.3	dB
Gain Drift (Note 13)				20	-	ppm/°C
Output Voltage (Note 14)			±2.6	±2.8	±3.0	Vpp
Load Capacitance					25	pF
Load Resistance (Note 15)			3			kΩ

Note 10. 100dB at 16bit data and 114dB at 20bit data.
Note 11. By Figure 19. External LPF Circuit Example 2 for PCM.
Note 12. S/N does not depend on input bit length.
Note 13. The voltage on VREF is held +5V externally.
Note 14. Full-scale voltage(0dB). Output voltage scales with the voltage of VREF.
AOUT (typ.@0dB) = (AOUT+) - (AOUT-) = 5.6Vpp x VREF/5.
Note 15. For AC-load.

Parameter	**min**	**typ**	**max**	**Units**
Power Supplies				
Power Supply Current				
Normal Operation (PDN pin = "H")				
VA: ADC Single-ended Mode		60	90	mA
ADC Differential Mode		55	83	mA
VD+VT (fs=44.1kHz)		11	-	mA
(fs=96kHz)		21	-	mA
(fs=192kHz)		27	41	mA
Power-down mode (PDN pin = "L") (Note 16)				
VA		10	100	μA
VD+VT		10	100	μA

Note 16. All digital input pins are held VT or DGND.

ADC FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta=25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V; Normal Speed Mode)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 17)	−0.005dB	PB	0		19.8	kHz
	−0.02dB		-	20.25	-	kHz
	−0.06dB		-	20.4	-	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 17)		SB	24.3			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 18)		GD		43.2		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 17)	−3dB	FR		0.9		Hz
	−0.1dB			6.0		Hz

ADC FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V; Double Speed Mode)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 17)	−0.005dB	PB	0		43.0	kHz
	−0.02dB		-	44.08	-	kHz
	−0.06dB		-	44.5	-	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 17)		SB	53.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 18)		GD		43.1		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 17)	−3dB	FR		2.0		Hz
	−0.1dB			13.0		Hz

FILTER CHARACTERISTICS (fs=192kHz)

(Ta=25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V; Quad Speed Mode)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 17)	−0.005dB	PB	0		86.0	kHz
	−0.02dB		-	88.18	-	kHz
	−0.06dB		-	89.0	-	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 17)		SB	106.0			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 18)		GD		38.2		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 17)	−3dB	FR		4.0		Hz
	−0.1dB			26.0		Hz

Note 17. The passband and stopband frequencies scale with fs. The reference frequency of these responses is 1kHz.
Note 18. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

DAC SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta = 25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V; fs = 44.1kHz; Normal Speed Mode; DEM = OFF; SLOW = "0")

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband	±0.01dB	(Note 19)	PB	0		20.0	kHz
	-6.0dB			-	22.05	-	kHz
Stopband		(Note 19)	SB	24.1			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	75			dB
Group Delay		(Note 20)	GD	-	28	-	1/fs
Digital Filter + SCF							
Frequency Response: 0 ~ 20.0kHz				-	± 0.2	-	dB

DAC SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta = 25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V; fs = 96kHz; Double Speed Mode; DEM = OFF; SLOW = "0")

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband	±0.01dB	(Note 19)	PB	0		43.5	kHz
	-6.0dB			-	48.0	-	kHz
Stopband		(Note 19)	SB	52.5			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	75			dB
Group Delay		(Note 20)	GD	-	28	-	1/fs
Digital Filter + SCF							
Frequency Response: 0 ~ 40.0kHz				-	± 0.3	-	dB

DAC SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta = 25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V; fs = 192kHz; Quad Speed Mode; DEM = OFF; SLOW = "0")

Parameter			symbol	min	typ	max	Units
Digital Filter							
Passband	±0.01dB	(Note 19)	PB	0		87.0	kHz
	-6.0dB			-	96.0	-	kHz
Stopband		(Note 19)	SB	105			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	75			dB
Group Delay		(Note 20)	GD	-	28	-	1/fs
Digital Filter + SCF							
Frequency Response: 0 ~ 80.0kHz				-	+0/-1	-	dB

Note 19. The passband and stopband frequencies scale with fs.
For example, PB = 0.4535×fs (@±0.01dB), SB = 0.546×fs.

Note 20. Delay time caused by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

DAC SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta = 25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V; fs = 44.1kHz; Normal Speed Mode; DEM = OFF; SLOW = "1")

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband	±0.04dB	(Note 21)	PB	0		8.1	kHz
	-3.0dB			-	18.2	-	kHz
Stopband		(Note 21)	SB	39.2			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	72			dB
Group Delay		(Note 20)	GD	-	28	-	1/fs
Digital Filter + SCF							
Frequency Response: 0 ~ 20.0kHz				-	+0/-5	-	dB

DAC SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta = 25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V; fs = 96kHz; Double Speed Mode; DEM = OFF; SLOW = "1")

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband	±0.04dB	(Note 21)	PB	0		17.7	kHz
	-3.0dB			-	39.6	-	kHz
Stopband		(Note 21)	SB	85.3			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	72			dB
Group Delay		(Note 20)	GD	-	28	-	1/fs
Digital Filter + SCF							
Frequency Response: 0 ~ 40.0kHz				-	+0/-4	-	dB

DAC SLOW ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta = 25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V; fs = 192kHz; Quad Speed Mode; DEM = OFF; SLOW = "1")

Parameter			Symbol	min	typ	max	Units
Digital Filter							
Passband	±0.04dB	(Note 21)	PB	0		35.5	kHz
	-3.0dB			-	79.1	-	kHz
Stopband		(Note 21)	SB	171			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	72			dB
Group Delay		(Note 20)	GD	-	28	-	1/fs
Digital Filter + SCF							
Frequency Response: 0 ~ 80.0kHz				-	+0/-5	-	dB

Note 21. The passband and stopband frequencies scale with fs.
For example, PB = 0.185×fs (@±0.04dB), SB = 0.888×fs.

DIGITAL CHARACTERISTICS

(Ta=25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	VT	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage (Iout=-100μA)	VOH	VD-0.5	-	-	V
Low-Level Output Voltage (Iout=100μA)	VOL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; VA=4.75 ~ 5.25V; VD=3.0 ~ 3.6V, VT=3.0 ~ 5.25V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing					
Frequency	fCLK	8.192		55.296	MHz
Pulse Width Low	tCLKL	0.4/fCLK			ns
Pulse Width High	tCLKH	0.4/fCLK			ns
LRCK Frequency (Note 22)					
Normal Speed Mode (DFS0="0", DFS1="0")	fsn	32		54	kHz
Double Speed Mode (DFS0="1", DFS1="0")	fsd	54		108	kHz
Quad Speed Mode (DFS0="0", DFS1="1")	fsq	108		216	kHz
Duty Cycle		45		55	%
PCM Audio Interface Timing					
BICK Period					
Normal Speed Mode	tBCK	1/128fsn			ns
Double Speed Mode	tBCK	1/64fsd			ns
Quad Speed Mode	tBCK	1/64fsq			ns
BICK Pulse Width Low	tBCKL	33			ns
Pulse Width High	tBCKH	33			ns
LRCK Edge to BICK "↑" (Note 23)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 23)	tBLR	20			ns
LRCK to SDTO (MSB) (Except I^2S mode)	tLRS			20	ns
BICK "↓" to SDTO	tBSD			20	ns
SDTI Hold Time	tSDH	20			ns
SDTI Setup Time	tSDS	20			ns
DSD Audio Interface Timing					
DCLK Period	tDCK	1/64fs			ns
DCLK Pulse Width Low	tDCKL	160			ns
Pulse Width High	tDCKH	160			ns
DCLK Edge to DSDL/R (Note 24)	tDDD	-20		20	ns

Note 22. When the normal/double/quad speed modes are switched, the AK4620B should be reset by PDN pin or RSTN bit.

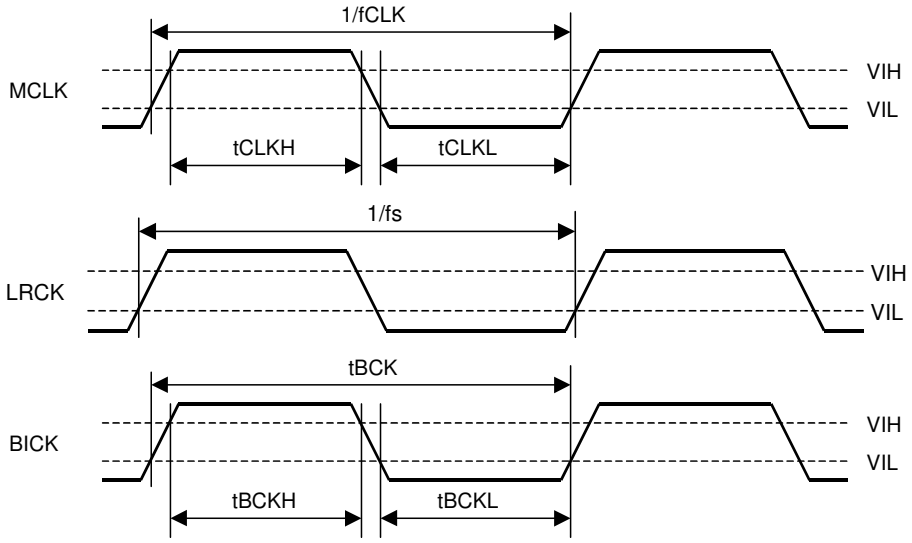
Note 23. BICK rising edge must not occur at the same time as LRCK edge.

Note 24. DSD data transmitting device must meet this time.

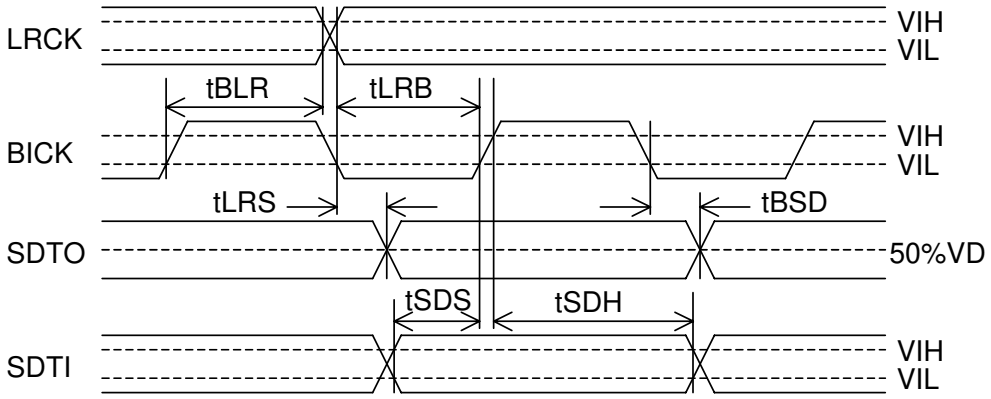
Parameter	Symbol	min	typ	max	Units
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
Reset Timing					
PDN Pulse Width (Note 25)	tPD	150			ns
RSTAD "↑" to SDTO valid (Note 26)	tPDV		516		1/fs

Note 25. The AK4620B can be reset by bringing PDN pin "L".
Note 26. These cycles are the number of LRCK rising from RSTAD bit.

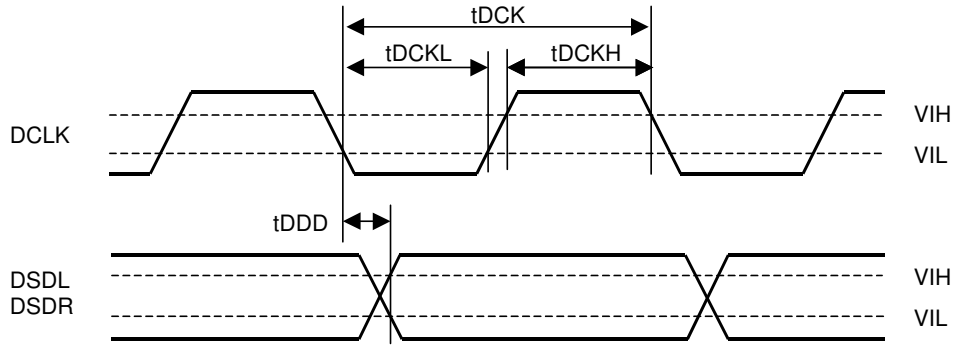
■ Timing Diagram



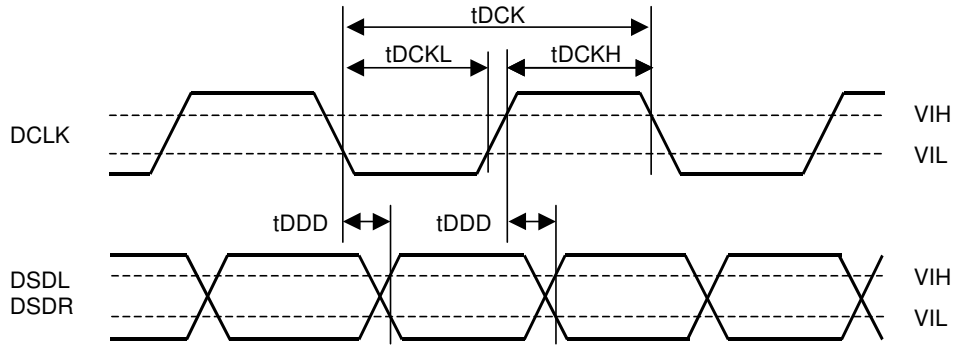
Clock Timing



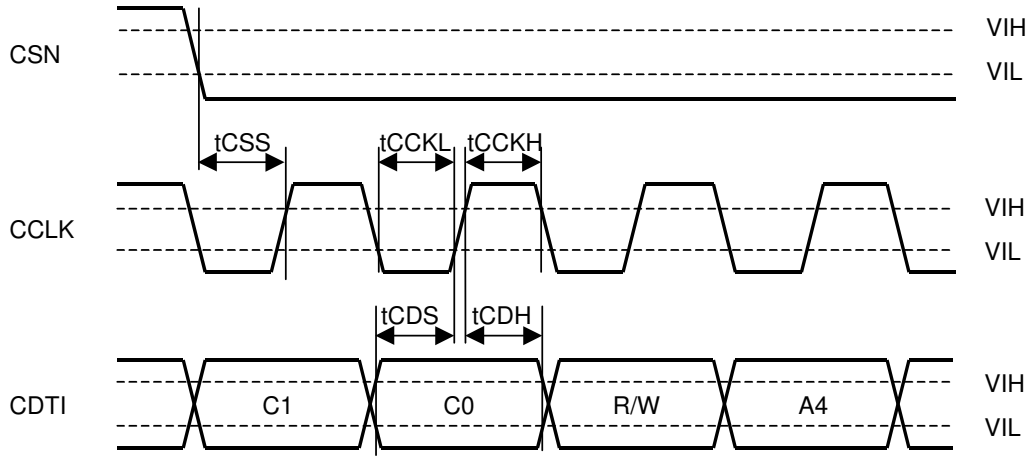
Audio Interface Timing (PCM mode)



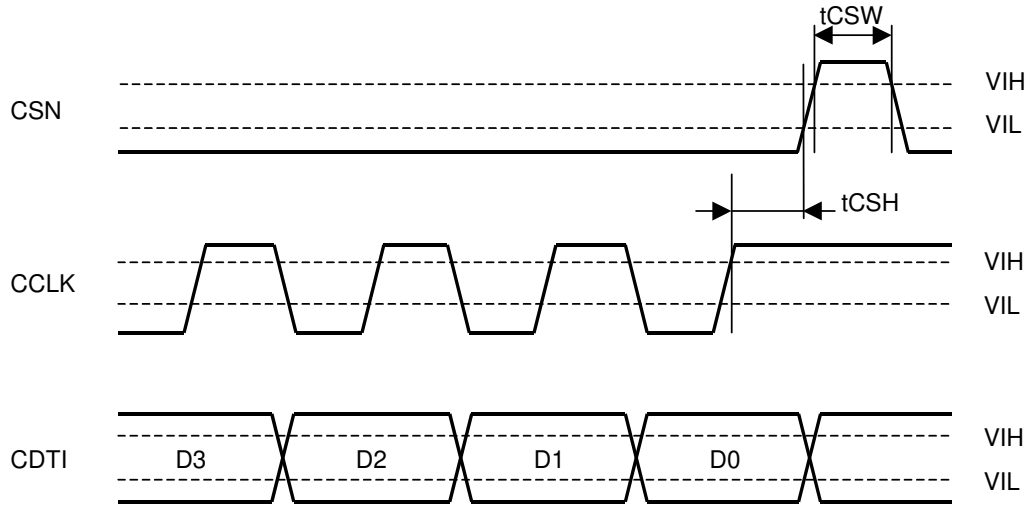
Audio Serial Interface Timing (DSD Normal Mode, DCKB bit = "0")



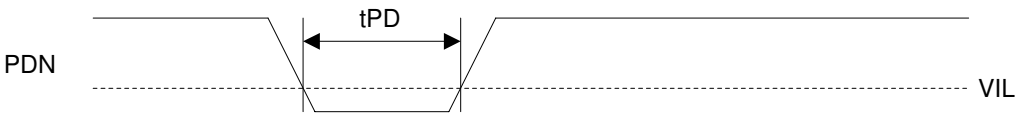
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB bit = "0")



WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing

OPERATION OVERVIEW

■ D/A Conversion Mode

In serial mode, the AK4620B can digitize either PCM data or DSD data. The P/D bit controls PCM/DSD mode. When DSD mode, DSD data input occurs on DCLK, DSDL and DSDR pins. The ADC and IPGA are in power down mode. In PCM mode, PCM data input occurs on BICK, SDTI and LRCK pins. When PCM/DSD mode changes (D/P bit), the AK4620B should be reset by setting RSTAD and RSTDA bits to "0" or by grounding the PDN pin. It takes from 2/fs to 3/fs to change the mode. In parallel mode, AK4620B can only process PCM data.

D/P bit	DAC mode	ADC mode
0	PCM	PCM
1	DSD	Power down

Table 1. DSD/PCM Mode Control

■ System Clock Input

1. PCM Mode

AK4620B requires MCLK, BICK and LRCK external clocks. MCLK should be synchronized with LRCK but the phase is not critical. External clocks (MCLK, BICK and LRCK) should always be present whenever the AK4620B is in normal operation mode (PDN pin = "H" and either the ADC and DAC is in normal operation mode). If these clocks are not provided, the AK4620B may draw excess current due to dynamic refresh of internal logic. If the external clocks are not present, the AK4620B should be in the power-down mode (PDN pin = "L" or power down both the ADC and DAC by the register). After exiting reset (PDN pin = "L" → "H") at power-up etc., the AK4620B is in power-down mode until MCLK and LRCK are provided.

As the AK4620B includes the phase detect circuit for LRCK, the AK4620B is reset automatically when the synchronization is out of phase by changing the clock frequencies.

1-1. Serial mode (P/S pin= "L")

As shown in Table 2, Table 3 and Table 4, select the MCLK frequency by setting CMODE, CKS0-1 and DFS0-1 (DFS0 bit and DFS0 pin are internally ORd). These registers are changed when RSTAD bit = RSTDA bit = "0".

DFS1 bit	OR of DFS0 bit / DFS0 pin	Mode	Sampling Rate	
0	0	Normal speed	32kHz-54kHz	Default
0	1	Double speed	54kHz-108kHz	
1	0	Quad speed	108kHz-216kHz	
1	1	N/A	-	

Table 2. Sampling speed in serial mode

CMODE bit	CKS1 bit	CKS0 bit	MCLK Normal Speed (DFS1-0 = "00")	MCLK Double Speed (DFS1-0 = "01")	MCLK Quad Speed (DFS1-0 = "10")	
0	0	0	256fs	N/A	N/A	Default
0	0	1	512fs	256fs	128fs	
0	1	0	1024fs	512fs	256fs	
0	1	1	N/A	Auto Setting Mode (*)	N/A	
1	0	0	384fs	N/A	N/A	
1	0	1	768fs	384fs	192fs	

Table 3. Master clock frequency in serial mode ("*": refer to Table 4)

The Auto Setting Mode detects MCLK/LRCK ratio and selects Normal/Double/Quad speed mode automatically.

MCLK/LRCK ratio	Mode	Sampling Rate
512 or 768	Normal speed	32kHz-54kHz
256 or 384	Double speed	54kHz-108kHz
128 or 192	Quad speed	108kHz-216kHz

Table 4. Auto Setting Mode in serial mode (DFS1-0 = "01", CMODE bit = "0", CKS1-0 bit = "11")

1-2. Parallel mode (P/S pin= "H")

As shown in Table 5, Table 6 and Table 7, select the MCLK frequency with the CKS0-1 and DFS0 pins. These pins should be changed when the PDN pin = "L".

DFS0 pin	Mode	Sampling Rate
L	Normal speed	32kHz-54kHz
H	Double speed	54kHz-108kHz

Table 5. Sampling speed in parallel mode

CKS1 pin	CKS0 pin	MCLK Normal Speed (DFS0 pin = "L")	MCLK Double Speed (DFS0 pin = "H")
L	L	256fs	N/A
L	H	512fs	256fs
H	L	384fs	Auto Setting Mode (*)
H	H	1024fs	512fs

Table 6. Master clock frequency in parallel mode ("*"; refer to Table 7.)

The Auto Setting Mode detects MCLK/LRCK ratio and selects Normal/Double/Quad speed mode automatically.

MCLK/LRCK ratio	Mode	Sampling Rate
512 or 768	Normal speed	32kHz-54kHz
256 or 384	Double speed	54kHz-108kHz
128 or 192	Quad speed	108kHz-216kHz

Table 7. Auto Setting Mode in parallel mode (DFS0 pin = "H", CKS1 pin = "H", CKS0 pin = "L")

MCLK (Normal speed)	fs=44.1kHz	fs=48kHz
256fs	11.2896MHz	12.288MHz
512fs	22.5792MHz	24.576MHz
1024fs	45.1584MHz	49.152MHz
384fs	16.9344MHz	18.432MHz
768fs	33.8688MHz	36.864MHz

MCLK (Double speed)	fs=88.2kHz	fs=96kHz
N/A	N/A	N/A
256fs	22.5792MHz	24.576MHz
512fs	45.1584MHz	49.152MHz
N/A	N/A	N/A
384fs	33.8688MHz	36.864MHz

MCLK (Quad speed)	fs=176.4kHz	fs=192kHz
128fs	22.5792MHz	24.576MHz
256fs	45.1584MHz	49.152MHz
192fs	33.8688MHz	36.864MHz

Table 8. Master clock frequency example

2. DSD Mode

The external clocks, which are required to operate the AK4620B, are MCLK and DCLK. The master clock (MCLK) should be synchronized with DSD clock (DCLK) but the phase is not critical. The frequency of MCLK is set by DCKS bit.

All external clocks (MCLK, DCLK) must be present whenever the AK4620B is in the normal operation mode (PDN pin = "H"). If these clocks are not provided, the AK4620B may draw excess current because the device utilizes dynamically refreshed logic. The AK4620B should be reset by PDN pin = "L" after these clocks are provided. If the external clocks are not present, the AK4620B should be in the power-down mode (PDN pin = "L"). After exiting reset (PDN pin = "↑") at power-up etc., the AK4620B is in the power-down mode until MCLK is provided.

■ Audio Serial Interface Format

1. PCM Mode

Five serial modes are supported and selected by the DIF2-0 bits in Serial Mode (two modes by DIF pin in Parallel Mode) as shown in Table 9 and Table 10. In all modes the serial data has MSB first, 2's complement format. The SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge. Mode2 can be used for 20 and 16 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTO	SDTI	LRCK	BICK	
0	0	0	0	24bit, MSB justified	16bit, LSB justified	H/L	≥ 48fs	
1	0	0	1	24bit, MSB justified	20bit, LSB justified	H/L	≥ 48fs	
2	0	1	0	24bit, MSB justified	24bit, MSB justified	H/L	≥ 48fs	Default
3	0	1	1	24bit, I^2S	24bit, I^2S	L/H	≥ 48fs	
4	1	0	0	24bit, MSB justified	24bit, LSB justified	H/L	≥ 48fs	

Table 9. Audio data format (Serial Mode)

Mode	DIF pin	SDTO	SDTI	LRCK	BICK
2	L	24bit, MSB justified	24bit, MSB justified	H/L	≥ 48fs
3	H	24bit, I^2S	24bit, I^2S	L/H	≥ 48fs

Table 10. Audio data format (Parallel Mode)

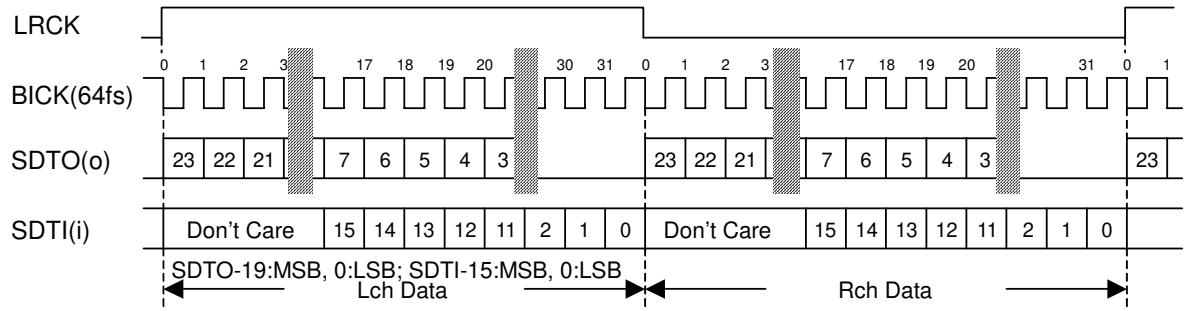


Figure 2. Mode 0 Timing

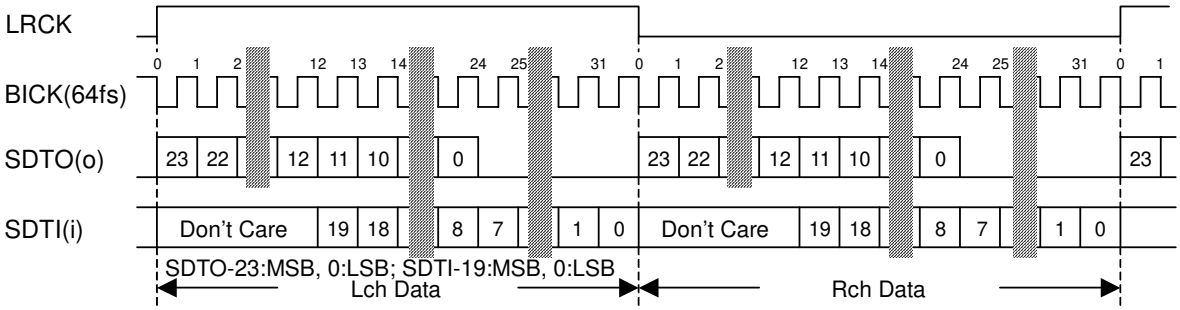


Figure 3. Mode 1 Timing

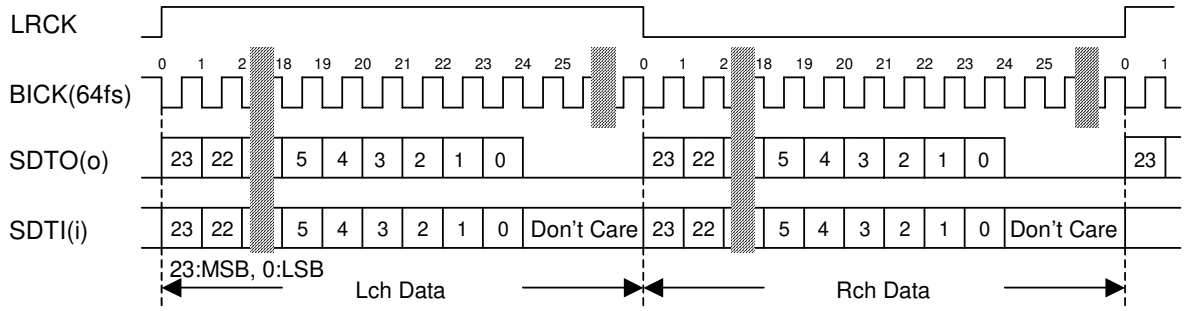


Figure 4. Mode 2 Timing

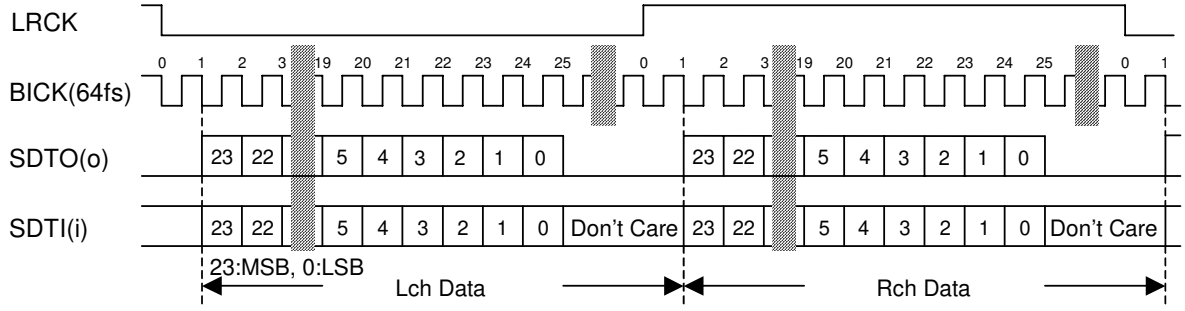


Figure 5. Mode 3 Timing

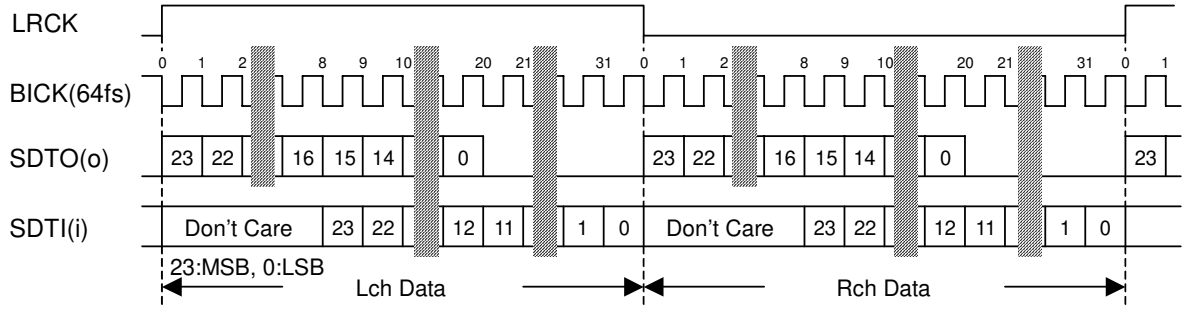


Figure 6. Mode 4 Timing

2. DSD Mode

In DSD mode, DIF0-2 is ignored. The frequency of DCLK is fixed at 64fs. The DCKB bit inverts the polarity of DCLK.

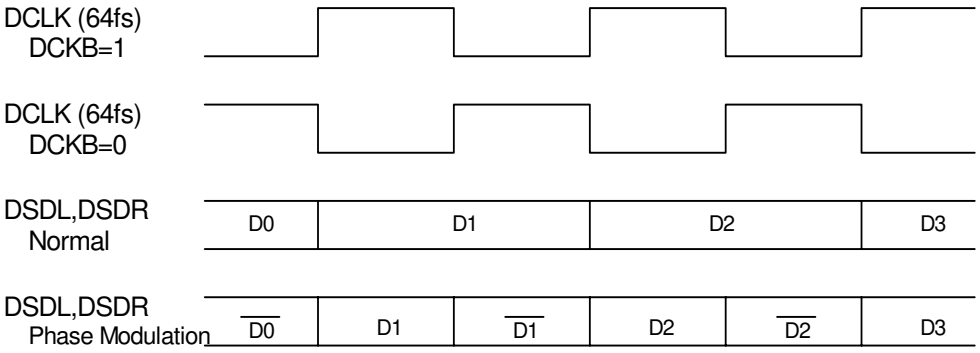


Figure 7. DSD Mode Timing

■ D/A conversion mode switching timing

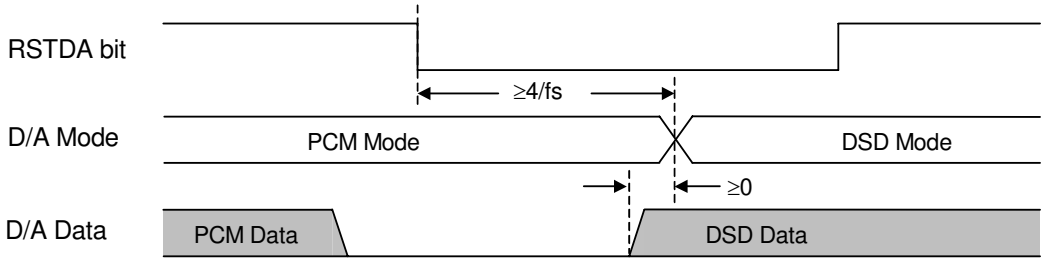


Figure 8. D/A Mode Switching Timing (PCM to DSD)

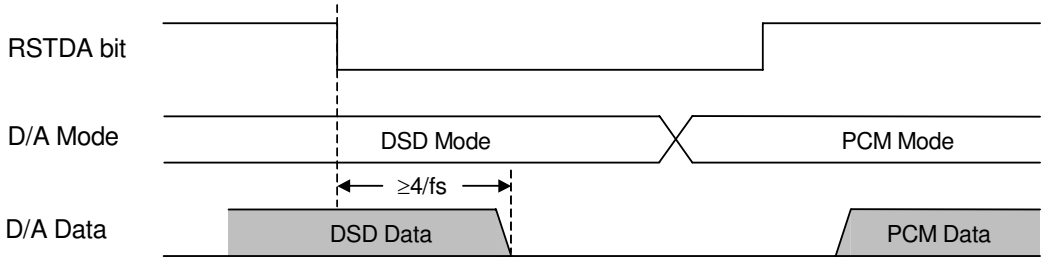


Figure 9. D/A Mode Switching Mode Timing (DSD to PCM)

Caution: In DSD mode, the signal level ranges from 25% to 75%. Peak levels of DSD signal above this range are not recommended by the SACD format book (Scarlet Book).

■ Input Volume

The AK4620B includes two channel-independent analog volumes (IPGA), each with 32 levels in 0.5dB increments. These are located in front of the ADC while digital volume controls (IATT) with 128 levels (including MUTE) are located after the ADC. Control of both of these volume settings is handled by the same register address. When the MSB of the register is "1", the IPGA changes and when the MSB = "0" the IATT changes.

The IPGA is an analog volume control that improves the S/N ratio compared with digital volume controls (Table 11). Level changes only occur during zero-crossings to minimize switching noise. Channel independent zero-crossing detection is used. If there are no zero-crossings, then the level will change after a time-out. The time-out period scales with fs. The periods of 256/fs, 512/fs, 1024/fs and 2048/fs are selected by ZTM1-0 bits in normal speed mode. If a new value is written to the IPGA register before the IPGA changes at the zero crossing or time-out, the previous value becomes invalid. The timer (channel independent) for time-out is reset and the timer restarts for the new IPGA value. ZCEI bits in the control register enable zero-crossing detection.

The IATT is a log volume that is linear-interpolated internally. When changing the level, the transition between ATT values has 29 levels and is done by soft changes, eliminating any switching noise.

	Input Gain Setting		
	0dB	+6dB	+18dB
fs=44.1kHz, A-weight	110dB	108dB	101dB

Table 11. IPGA+ADC S/N (typ.)

ZTM1	ZTM0	Normal speed	Double speed	Quad speed	
0	0	256/fs	512/fs	1024/fs	
0	1	512/fs	1024/fs	2048/fs	
1	0	1024/fs	2048/fs	4096/fs	Default
1	1	2048/fs	4096/fs	8192/fs	

Table 12. LRCK cycles for timeout period

■ Output Volume

The AK4620B includes channel independent digital output volumes (ATT) with 256 levels at linear steps including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to −48dB and mute. When changing levels, transitions are executed via soft changes, eliminating any switching noise. The transition time of 1 level and all 256 levels is shown in Table 13.

Sampling Speed	Transition Time	
	1 Level	255 to 0
Normal Speed Mode	4LRCK	1020LRCK
Double Speed Mode	8LRCK	2040LRCK
Quad Speed Mode	16LRCK	4080LRCK

Table 13. ATT Transition Time

■ Overflow Detection

The ADC has a channel independent overflow detection function. This function is enabled in the parallel control mode, or when the ZOS bit = ZOE bit = "0"in serial control mode. OVFL/R pins go to "H" if each Lch/Rch analog input overflows (exceeds -0.3dBFS). The output of each OVFL/R pin has same group delay as ADC against analog input. OVFL/R pin is "L" for 516/fs (=10.8ms @fs=48kHz) after PDN pin = "↑", and then overflow detection is enabled.

■ Zero detection

The DAC has a channel-independent zero detect function. The zero detect function is enabled when the ZOS bit = "1" and the ZOE bit = "0"in serial control mode. When the input data at both channels is continuously zero for 8192 LRCK cycles, the DZF pin of each channel goes to "H". The DZF pin of each channel immediately goes to "L" if the input data of each channel is not zero after DZF "H". If the RSTDA bit is "0", the DZF pins of both channels go to "H". DZF pins of both channels go to "L" at 4~5/fs after the RSTDA bit becomes "1". Zero detect function can be disabled by the ZOE bit. In this case, the DZF pins of both channels are always "L". The DZFB bit can invert the polarity of the DZF pin.

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 0.9Hz at fs=44.1kHz. The digital high pass filter cutoff frequency scales with the sampling rate (fs). In parallel mode, the HPF is always enabled. In serial mode, the HPF can control each channel by HPLN/HPRN bits.

■ De-emphasis Filter

The DAC includes a digital de-emphasis filter (tc=50/15μs) via an integrated IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz, 48kHz). This setting is done via control register (DEM1-0 bits). This filter is always OFF in double and quad speed modes. The DEM0 pin and DEM0 bit are OR'd in serial control mode. In parallel control mode, the DEM1 bit is fixed to "0" and only the DEM0 pin can be controlled (44.1kHz or OFF). When in DSD mode, DEM1-0 bits are ignored. The setting value is held even if PCM mode and DSD mode are switched.

No	DEM1	DEM0	Mode	
0	0	0	44.1kHz	
1	0	1	OFF	Default
2	1	0	48kHz	
3	1	1	32kHz	

Table 14. De-emphasis control (Normal Speed Mode)

■ ADC Single-ended/Differential Input Mode

The ADC has a selectable single-ended or differential input mode. This mode can be selected by ADMODE pin, AML bit and AMR bit. (See Table 15 and Table 16) In differential input mode, the IPGA is powered-down and bypassed. IATT can be controlled in differential mode.

ADMODE pin	Lch	Rch
L	Single-ended	Single-ended
H	Differential	Differential

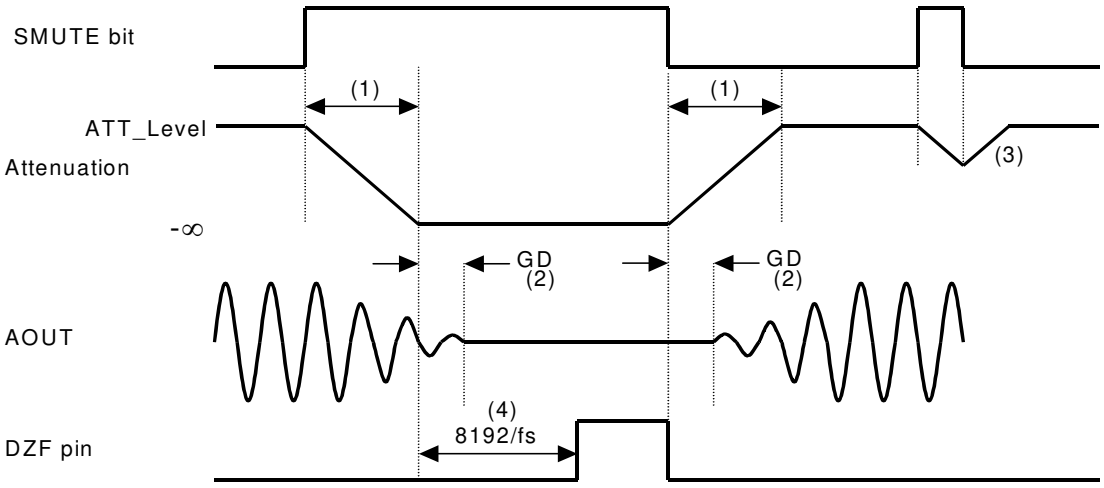
Table 15. ADC Input Mode in parallel mode

ADMODE pin	AML bit	AMR bit	Lch	Rch
L	0	0	Single-ended	Single-ended
	0	1	Single-ended	Differential
	1	0	Differential	Single-ended
	1	1	Differential	Differential
H	X	X	Differential	Differential

Table 16. ADC Input Mode in serial mode (X: Don't care)

■ Soft Mute Operation

Soft mute operation is performed in the digital domain of the DAC input. When the SMUTE bit goes to "1", the output signal is attenuated by −∞ during ATT_DATA × ATT transition time (Table 12) from the current ATT level. When SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time. If soft mute is cancelled before attenuating to −∞ after starting the operation, the attenuation is discontinued and returns to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA × ATT transition time (Table 12). For example, this time is 1020LRCK cycles (1020/fs) at ATT_DATA=255 in Normal Speed Mode.
(2) Analog output corresponding to digital input has group delay (GD).
(3) If the soft mute is cancelled before attenuating −∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.
(4) When the input data at each channel is continuously zero for 8192 LRCK cycles, DZF pin of each channel goes to "H". DZF pin immediately goes to "L" if input data are not zero after going DZF pin "H".

Figure 10. Soft Mute and Zero Detection