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AK4637

24bit Mono CODEC with MIC/SPK-AMP

1. General Description

The AK4637 is a low power 24-bit Mono CODEC with a microphone and speaker amplifiers.

The AK4637 supports sampling frequency from 8kHz to 48kHz. It is suitable for a wide range of application from speech signal processing for narrowband, wideband and super wideband to sound signal processing for audio band.

The input circuits include a microphone amplifier and a high performance digital ALC (automatic level control) circuit. In addition, the output circuits include a speaker amplifier with 1W output power. It is suitable for various products as well as portable applications with recording/playback function.

The AK4637 are available in a small 20-pin QFN (3mm x 3mm, 0.4mm pitch: AK4637EN) package saving mounting area on the board.

Application:

- **IP Camera**
- **Digital Camera**
- **MFP(Multi Function Printer)**

2. Features

1. **Recording Functions**
   - **Analog Input**
     1 Monaural Single-ended input or Differential input
   - **Microphone Amplifier: +30dB ~ 0dB, 3dB Step**
   - **Microphone Power Supply: 2.0V or 2.4V, Noise Level= –108dBV**
   - **Digital ALC (Automatic Level Control)**
     - Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute
   - **ADC Performance: S/(N+D): 83dB, DR, S/N: 88dB (MIC-Amp=+18dB)**
     S/(N+D): 84dB, DR, S/N: 95dB (MIC-Amp=0dB)
   - **Wind Noise Reduction Filter**
   - **5-Band Notch Filter: Include Dynamic Gain Control**
   - **Digital Microphone Interface**
2. **Playback Functions**
   - **Digital ALC (Automatic Level Control)**
     - Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute
   - **Sidetone Mixer & Volume Control (0dB ~ –18dB, 6dB Step)**
   - **Digital Volume Control**
     - +12dB ~ –89.5dB, 0.5dB Step & Mute
   - **Mono Speaker Amplifier (with Line Output Switch)**
     - Speaker Amplifier Porformance: S/(N+D): 75dB@250mW, S/N: 97 dB
     - BTL Output
     - Output Power: 400mW@8Ω (AVDD=3.3V), 1W@8Ω (AVDD=5V)
   - **Analog Mixing: BEEP Input**
3. **Power Management**

4. **Master Clock:**
   - **(1) PLL Mode**
     Frequencies: 11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin), 16fs, 32fs, 64fs (BICK pin)
   - **(2) External Clock Mode**
     Frequencies: 256fs, 384fs, 512fs or 1024fs (MCKI pin)
5. **Sampling Frequencies**
   - **PLL Master Mode:**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **PLL Slave Mode (BICK pin): 8kHz ~ 48kHz**
   - **EXT Master/Slave Mode:**
     8kHz ~ 48kHz (256fs, 384fs, 512fs), 8kHz ~ 24kHz (1024fs)
6. **Master/Slave Mode**
7. **Audio Interface Format: MSB First, 2's complement**
   - **ADC: DSP Mode, 16/24bit MSB justified, 16/24bit I^2S**
   - **DAC: DSP Mode, 16/24bit MSB justified, 16bit LSB justified, 16/24bit I^2S**
8. **μP I/F: I^2C Bus (Ver 1.0, 400kHz Fast-Mode)**
9. **Operating Temperature: Ta = –40 ~ 85°C**
10. **Power Supply**
    - **Analog Power Supply (AVDD): 2.8 ~ 5.5V**
    - **Digital Power Supply (DVDD): 1.6 ~ 1.98V**
    - **Digital I/O Power Supply (TVDD): 1.6 or (DVDD – 0.2) ~ 3.6V**
11. **Package:**
    - **20-pin QFN (3 x 3 mm, 0.4mm pitch)**

3. Table of Contents

4. Block Diagram

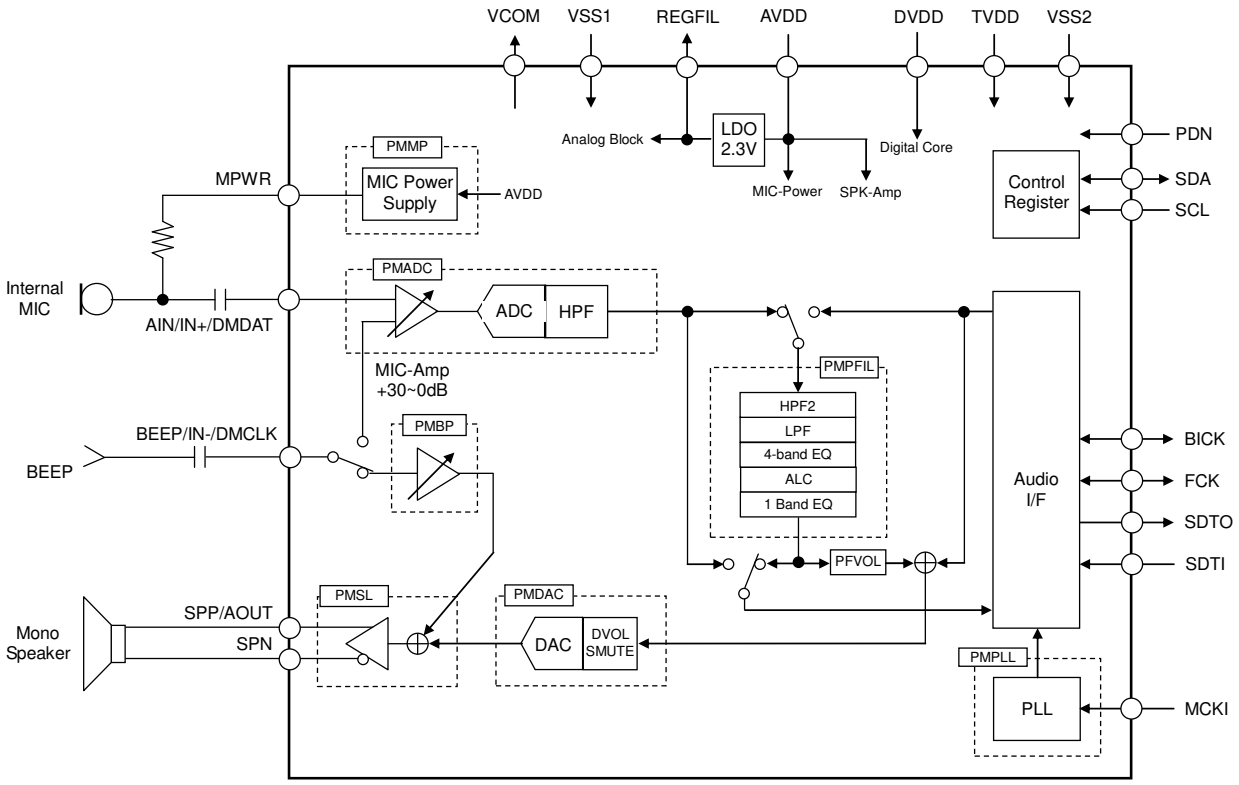


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Layout

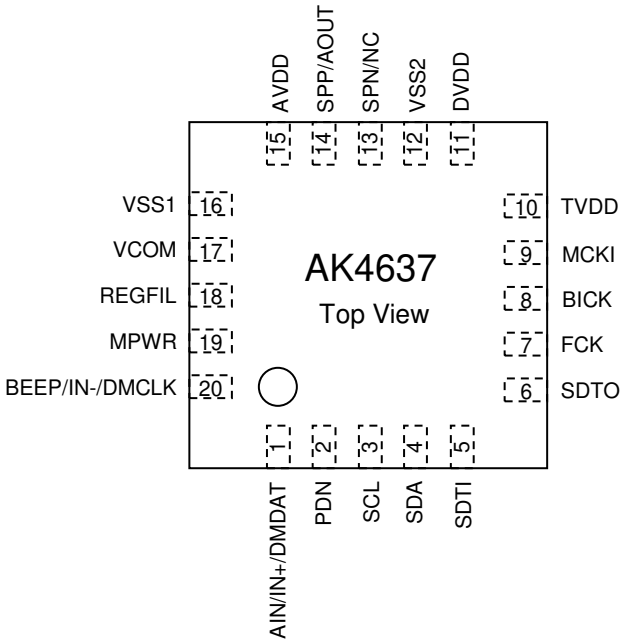


Figure 2. Pin Layout

■ Comparison Table of the AK4951EN

1. Function

Function	AK4951EN	AK4637EN
Stereo/Mono	Stereo	Mono
AVDD	2.8V ~ 3.5V	2.8V ~ 5.5V
SVDD	1.8V ~ 5.5V	-
DVDD	1.6V ~ 1.98V	←
TVDD	1.6V or (DVDD-0.2)V ~ 3.5V	1.6V or (DVDD-0.2)V ~ 3.6V
Differential Input	No	Yes
MIC Sensitivity Correction	Yes	No
Automatic Wind Noise Reduction	Yes	No
Stereo Separation Emphasis Circuit	Yes	No
Headphone Amplifier	Yes	No
Audio I/F Format	DSP Mode is Not Available	DSP Mode is Available
Package	32-pin QFN (4 x 4mm, 0.4mm pitch)	20-pin QFN (3 x 3mm, 0.4mm pitch)

2. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	0	LOSEL	PMDAC	~~PMADR~~	PMADC
01H	Power Management 2	~~PMOSC~~	0	~~PMHPR~~	~~PMHPL~~	M/S	PMPLL	PMSL	~~LOSEL~~
02H	Signal Select 1	SLPSN	MGAIN3	DACS	~~MPSEL~~	PMMP	MGAIN2	MGAIN1	MGAIN0
03H	Signal Select 2	SPKG1	SPKG0	0	MICL	~~INL1~~	~~INL0~~	~~INR1~~	MDIF
04H	Signal Select 3	LVCM1	LVCM0	DACL	0	~~PTS1~~	~~PTS0~~	~~MONO1~~	~~MONO0~~
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	~~BCKO~~	CKOFF	BCKO1	BCKO0
07H	Mode Control 3	TSDSEL	THDET	SMUTE	~~DVOLC~~	MSBS	BCKP	DIF1	DIF0
08H	Digital MIC	~~READ~~	0	~~PMDMR~~	PMDM	DCLKE	0	DCLKP	DMIC
0EH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0FH	BEEP Control	~~HPZ~~	BPVCM	BEEPS	~~BEEPH~~	BPLVL3	BPLVL2	BPLVL1	BPLVL0
10H	Digital Volume Control	DVOL7	DVOL6	DVOL5	DVOL4	DVOL3	DVOL2	DVOL1	DVOL0
11H	EQ Common Gain Select	0	0	0	EQC5	EQC4	EQC3	EQC2	0
12H	EQ2 Gain Setting	EQ2G5	EQ2G4	EQ2G3	EQ2G2	EQ2G1	EQ2G0	EQ2T1	EQ2T0
13H	EQ3 Gain Setting	EQ3G5	EQ3G4	EQ3G3	EQ3G2	EQ3G1	EQ3G0	EQ3T1	EQ3T0
14H	EQ4 Gain Setting	EQ4G5	EQ4G4	EQ4G3	EQ4G2	EQ4G1	EQ4G0	EQ4T1	EQ4T0
15H	EQ5 Gain Setting	EQ5G5	EQ5G4	EQ5G3	EQ5G2	EQ5G1	EQ5G0	EQ5T1	EQ5T0
16H	Digital Filter Select 1	0	0	0	0	0	HPFC1	HPFC0	HPFAD
17H	Digital Filter Select 2	~~GN1~~	~~GN0~~	~~EQ0~~	~~FIL3~~	0	0	LPF	HPF
18H	Digital Filter Mode	0	0	PFVOL1	PFVOL0	PFDAC1	PFDAC0	ADCPF	PFSDO
19H	HPF2 Co-efficient 0	F1A7	F1A6	F1A5	F1A4	F1A3	F1A2	F1A1	F1A0
1AH	HPF2 Co-efficient 1	0	0	F1A13	F1A12	F1A11	F1A10	F1A9	F1A8
1BH	HPF2 Co-efficient 2	F1B7	F1B6	F1B5	F1B4	F1B3	F1B2	F1B1	F1B0
1CH	HPF2 Co-efficient 3	0	0	F1B13	F1B12	F1B11	F1B10	F1B9	F1B8
1DH	LPF Co-efficient 0	F2A7	F2A6	F2A5	F2A4	F2A3	F2A2	F2A1	F2A0
1EH	LPF Co-efficient 1	0	0	F2A13	F2A12	F2A11	F2A10	F2A9	F2A8
1FH	LPF Co-efficient 2	F2B7	F2B6	F2B5	F2B4	F2B3	F2B2	F2B1	F2B0
20H	LPF Co-efficient 3	0	0	F2B13	F2B12	F2B11	F2B10	F2B9	F2B8

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
21H	Digital Filter Select 3	0	0	0	EQ5	EQ4	EQ3	EQ2	EQ1
22H	E1 Co-efficient 0	E1A7	E1A6	E1A5	E1A4	E1A3	E1A2	E1A1	E1A0
23H	E1 Co-efficient 1	E1A15	E1A14	E1A13	E1A12	E1A11	E1A10	E1A9	E1A8
24H	E1 Co-efficient 2	E1B7	E1B6	E1B5	E1B4	E1B3	E1B2	E1B1	E1B0
25H	E1 Co-efficient 3	E1B15	E1B14	E1B13	E1B12	E1B11	E1B10	E1B9	E1B8
26H	E1 Co-efficient 4	E1C7	E1C6	E1C5	E1C4	E1C3	E1C2	E1C1	E1C0
27H	E1 Co-efficient 5	E1C15	E1C14	E1C13	E1C12	E1C11	E1C10	E1C9	E1C8
28H	E2 Co-efficient 0	E2A7	E2A6	E2A5	E2A4	E2A3	E2A2	E2A1	E2A0
29H	E2 Co-efficient 1	E2A15	E2A14	E2A13	E2A12	E2A11	E2A10	E2A9	E2A8
2AH	E2 Co-efficient 2	E2B7	E2B6	E2B5	E2B4	E2B3	E2B2	E2B1	E2B0
2BH	E2 Co-efficient 3	E2B15	E2B14	E2B13	E2B12	E2B11	E2B10	E2B9	E2B8
2CH	E2 Co-efficient 4	E2C7	E2C6	E2C5	E2C4	E2C3	E2C2	E2C1	E2C0
2DH	E2 Co-efficient 5	E2C15	E2C14	E2C13	E2C12	E2C11	E2C10	E2C9	E2C8
2EH	E3 Co-efficient 0	E3A7	E3A6	E3A5	E3A4	E3A3	E3A2	E3A1	E3A0
2FH	E3 Co-efficient 1	E3A15	E3A14	E3A13	E3A12	E3A11	E3A10	E3A9	E3A8
30H	E3 Co-efficient 2	E3B7	E3B6	E3B5	E3B4	E3B3	E3B2	E3B1	E3B0
31H	E3 Co-efficient 3	E3B15	E3B14	E3B13	E3B12	E3B11	E3B10	E3B9	E3B8
32H	E3 Co-efficient 4	E3C7	E3C6	E3C5	E3C4	E3C3	E3C2	E3C1	E3C0
33H	E3 Co-efficient 5	E3C15	E3C14	E3C13	E3C12	E3C11	E3C10	E3C9	E3C8
34H	E4 Co-efficient 0	E4A7	E4A6	E4A5	E4A4	E4A3	E4A2	E4A1	E4A0
35H	E4 Co-efficient 1	E4A15	E4A14	E4A13	E4A12	E4A11	E4A10	E4A9	E4A8
36H	E4 Co-efficient 2	E4B7	E4B6	E4B5	E4B4	E4B3	E4B2	E4B1	E4B0
37H	E4 Co-efficient 3	E4B15	E4B14	E4B13	E4B12	E4B11	E4B10	E4B9	E4B8
38H	E4 Co-efficient 4	E4C7	E4C6	E4C5	E4C4	E4C3	E4C2	E4C1	E4C0
39H	E4 Co-efficient 5	E4C15	E4C14	E4C13	E4C12	E4C11	E4C10	E4C9	E4C8
3AH	E5 Co-efficient 0	E5A7	E5A6	E5A5	E5A4	E5A3	E5A2	E5A1	E5A0
3BH	E5 Co-efficient 1	E5A15	E5A14	E5A13	E5A12	E5A11	E5A10	E5A9	E5A8
3CH	E5 Co-efficient 2	E5B7	E5B6	E5B5	E5B4	E5B3	E5B2	E5B1	E5B0
3DH	E5 Co-efficient 3	E5B15	E5B14	E5B13	E5B12	E5B11	E5B10	E5B9	E5B8
3EH	E5 Co-efficient 4	E5C7	E5C6	E5C5	E5C4	E5C3	E5C2	E5C1	E5C0
3FH	E5 Co-efficient 5	E5C15	E5C14	E5C13	E5C12	E5C11	E5C10	E5C9	E5C8

These bits are added to the AK4637.
These bits are removed from the AK4637.
These bits are changed from the AK4637.

■ PIN/FUNCTION

No.	Pin Name	I/O	Function
1	AIN	I	Analog Input Pin (MDIF bit = "0": Single-ended Input, DMIC bit = "0": default)
	IN+	I	Positive Analog Input Pin (MDIF bit = "1": Full-differential Input, DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
2	PDN	I	Reset & Power-down Pin "L": Reset & Power-down, "H": Normal Operation
3	SCL	I	Control Data Clock Pin
4	SDA	I/O	Control Data Input/Output Pin
5	SDTI	I	Audio Serial Data Input Pin
6	SDTO	O	Audio Serial Data Output Pin
7	FCK	I/O	Frame Clock Pin
8	BICK	I/O	Audio Serial Data Clock Pin
9	MCKI	I	External Master Clock Input Pin
10	TVDD	-	Digital I/O Power Supply Pin, 1.6 or (DVDD-0.2) ~ 3.6V
11	DVDD	-	Digital Power Supply Pin, 1.6 ~ 1.98V
12	VSS2	-	Ground 2 Pin
13	SPN	O	Speaker-Amp Negative Output Pin (LOSEL bit = "0": default)
	NC	O	No Connect Pin (LOSEL bit = "1") This pin should be open.
14	SPP	O	Speaker-Amp Positive Output Pin (LOSEL bit = "0": default)
	AOUT	O	Line Output Pin (LOSEL bit = "1")
15	AVDD	-	Analog Power Supply Pin, 2.8 ~ 5.5V
16	VSS1	-	Ground 1 Pin
17	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 with 2.2μF±10% or 4.7μF±10% capacitor in series.
18	REGFIL	O	LDO Voltage Output pin for Analog Block (typ 2.3V) This pin must be connected to VSS1 with 2.2μF±10% capacitor in series.
19	MPWR	O	MIC Power Supply Pin
20	BEEP	I	Beep Signal Input Pin (MDIF bit="0": Single-ended Input, DMIC bit="0": default)
	IN-	I	Negative Analog Input Pin (MDIF bit = "1": Full-differential Input, DMIC bit="0")
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")

Note 1. All input pins except analog input pins (AIN/IN+, IN-/BEEP) must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	AIN/IN+/DMDAT, BEEP/IN-/DMCLK, MPWR, SPN, SPP/AOUT	Open
Digital	MCKI, SDTI	Connect to VSS2
	SDTO	Open

6. Absolute Maximum Ratings

(VSS1=VSS2=0V; Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog	AVDD	−0.3	6.0	V
	Digital	DVDD	−0.3	2.5	V
	Digital I/O	TVDD	−0.3	6.0	V
	Speaker-Amp	SVDD	−0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	−0.3	AVDD+0.3	V
Digital Input Voltage (Note 4)		VIND	−0.3	TVDD+0.3	V
Operating Temperature (powered applied)		Ta	−40	85	°C
Storage Temperature		Tstg	−65	150	°C
Maximum Power Dissipation (Note 5)		Pd	-	800	mW

Note 2. All voltages are with respect to ground.
VSS1 and VSS2 must be connected to the same analog ground plane.

Note 3. AIN/IN+ and BEEP/IN- pins

Note 4. PDN, SCL, SDA, SDTI, FCK, BICK and MCKI pins
Pull-up resistors at the SDA and SCL pins must be connected to a voltage in the range from TVDD or more to 6V or less.

Note 5. This power is the AK4637 internal dissipation that does not include power dissipation of externally connected speakers. The maximum junction temperature is 125°C and θja (Junction to Ambient) is 50°C/W at JESD51-9 (2p2s) for the AK4637. When Pd = 800mW and the θja is 50°C/W for the AK4637, the junction temperature does not exceed 125°C. In this case, the AK4637 will not be damaged by its internal power dissipation. Therefore, the AK4637 should be used in the condition of θja ≤ 50°C/W.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1=VSS2=0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 6)	Analog	AVDD	2.8	3.3	3.5	V
	Digital	DVDD	1.6	1.8	1.98	V
	Digital I/O (Note 7)	TVDD	1.6 or (DVDD-0.2)	1.8	3.5	V

Note 2. All voltages are with respect to ground.

Note 6. The power-up sequence between AVDD, DVDD, TVDD and SVDD is not critical. The PDN pin must be “L” upon power up, and should be changed to “H” after all power supplies are supplied to avoid an internal circuit error.

Note 7. The minimum value is higher voltage between DVDD-0.2 and 1.6V.

*** When TVDD is powered ON and the PDN pin is “L”, AVDD and DVDD can be powered ON/OFF. The PDN pin must be set to “H” after all power supplies are ON, when the AK4637EN is powered-up from power-down state.**

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

■ Analog Characteristics

(Ta=25°C; AVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=0V; fs=48kHz, BICK=64fs; Signal Frequency =1kHz; 24bit Data; Measurement Bandwidth=20Hz ~ 20kHz; unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
MIC Amplifier: AIN pin; MDIF bit = "0" (Single-ended input)						
Input Resistance (Note 8)			20	30	40	kΩ
Gain	Gain Setting		0	-	+30	dB
	Step Width		-	3	-	dB
MIC Power Supply: MPWR pin						
Output Voltage	MICL bit = "0"		2.2	2.4	2.6	V
	MICL bit = "1"		1.8	2.0	2.2	
Output Noise Level (A-weighted)			-	-108	-	dBV
Load Resistance			2.0	-	-	kΩ
Load Capacitance			-	-	30	pF
PSRR (f = 1kHz) (Note 9)			-	100	-	dB
ADC Analog Input Characteristics: AIN pins → ADC (Programmable Filter = OFF) → SDTO						
Resolution			-	-	24	Bits
Input Voltage (Note 10)		(Note 11)	-	0.261	-	Vpp
		(Note 12)	1.86	2.07	2.28	Vpp
S/(N+D) (-1dBFS)		(Note 11)	73	83	-	dBFS
		(Note 12)	-	84	-	dBFS
D-Range (–60dBFS, A-weighted)		(Note 11)	78	88	-	dB
		(Note 12)	-	95	-	dB
S/N (A-weighted)		(Note 11)	78	88	-	dB
		(Note 12)	-	95	-	dB
PSRR (f = 1kHz) (Note 9)			-	90	-	dB

Note 8. Full Differential Input: IN+=20kΩ(typ), IN-=57kΩ(typ)@MGAIN3-0 bits = "0000" (0dB),
IN+=16kΩ(typ), IN-=244kΩ(typ)@MGAIN3-0 bits = "0110" (+18dB)

Note 9. PSRR applied to AVDD with 500mVpp sine wave.

Note 10. Single-ended Input: Vin = 0.9 x 2.3Vpp (typ) @MGAIN3-0 bits = "0000" (0dB)
Full Differential Input: Vin = (IN+) – (IN–) = 0.9 x 2.3Vpp (typ)
IN+ = 0.45 x 2.3Vpp (typ), IN– = 0.45 x 2.3Vpp (typ)

Note 11. MGAIN3-0 bits = "0110" (+18dB)
Full Differential Input: S/(N+D) = 81dB、DR = S/N = 86dB

Note 12. MGAIN3-0 bits = "0000" (0dB)
Full Differential Input: S/(N+D) = 83dB、DR = S/N = 93dB

Parameter			Min.	Typ.	Max.	Unit
DAC Characteristics:						
Resolution			-	-	24	Bit
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=8Ω, BTL						
Output Voltage						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	1.79	-	Vrms
SPKG1-0 bits = "11", –0.5dBFS (Po=1000mW) (AVDD=5V)			-	2.83	-	Vrms
S/(N+D)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	80	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			40	75	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	20	-	dB
SPKG1-0 bits = "11", –0.5dBFS (Po=1000mW) (AVDD=5V)			-	20	-	dB
S/N (A-weighted)	SPKG1-0 bits = "01"		80	97	-	dB
Output Offset Voltage	SPKG1-0 bits = "01"		-30	0	+30	mV
Load Resistance			8	-	-	Ω
Load Capacitance			-	-	100	pF
PSRR (f = 1kHz) (Note 13)			-	60	-	dB
Line Output Characteristics: DAC → AOUT pin, ALC=OFF, IVOL=DVOL= 0dB, R_L=10kΩ, LVCM1-0 bits = "01"						
Output Voltage	(0dBFS)	LVCM0 bit = "0" AVDD=2.8V	-	2.26	-	Vpp
		LVCM0 bit = "1"	-	1.0	-	Vrms
	(-3dBFS)	LVCM0 bit = "0" AVDD=2.8V	1.44	1.6	1.76	Vpp
		LVCM0 bit = "1"	1.82	2.0	2.22	Vpp
S/(N+D)	(0dBFS)	LVCM0 bit = "0" AVDD=2.8V	-	80	-	dB
		LVCM0 bit = "1"	-	40	-	dB
	(-3dBFS)		75	85	-	dB
S/N (A-weighted)			82	94	-	dB
Load Resistance			10	-	-	kΩ
Load Capacitance			-	-	30	pF
Mono Input: BEEP pin (PMBP bit ="1", BPVCM bit = "0", BPLVL3-0 bits = "0000")						
Input Resistance			46	66	86	kΩ
Maximum Input Voltage (Note 14)			-	-	1.54	Vpp
Gain						
BEEP pin → SPP/SPN pins (Note 15)		SPKG1-0 bits = "00"	+4.4	+6.4	+8.4	dB
		SPKG1-0 bits = "01"	-	+8.4	-	dB
		SPKG1-0 bits = "10"	-	+11.1	-	dB
		SPKG1-0 bits = "11"	-	+14.9	-	dB
BEEP pin → AOUT pin		LVCM1-0 bits = "00"	-1	0	+1	dB
		LVCM1-0 bits = "01"	-	+2	-	dB
		LVCM1-0 bits = "10"	-	+2	-	dB
		LVCM1-0 bits = "11"	-	+4	-	dB

Note 13. PSRR applied to AVDD with 500mVpp sine wave.

Note 14. The maximum value is the smaller one of AVDD Vpp or 3.3Vpp when BPVCM bit = "1". However, a click noise may occur when the amplitude after BEEP-Amp is 0.5Vpp or more. (Set by BPLVL3-0 bits)

Note 15. This gain is an ideal gain when no load resistance.

Parameter	Min.	Typ.	Max.	Unit
Power Supplies:				
Power Up (PDN pin = "H", All Circuit Power Up)				
AVDD+DVDD+TVDD (Note 16)	-	6.6	10.2	mA
AVDD+DVDD+TVDD (Note 17)	-	5.6	-	mA
Power Down (PDN pin = "L")				
AVDD+DVDD+TVDD (Note 18)	-	0	10	μA

Note 16. When PLL Master Mode (MCKI=12MHz), PMADC=PMDAC=PMPFIL=PMSL=PMVCM=PMPLL =PMBP=PMMP=M/S=SLPSN bits = "1" and LOSEL bit = "0". In this case, the MPWR pin outputs 0mA. AVDD= 4.9mA (typ), DVDD= 1.5mA (typ), TVDD= 0.2mA (typ).

Note 17. When EXT Slave Mode (PMPLL=M/S bits ="0"), PMADC =PMDAC=PMSL=PMVCM=PMBP =PMMP=SLPSN bits = "1" and PMPFIL = LOSEL bits = "0". In this case, the MPWR pin outputs 0mA. AVDD= 4.6mA (typ), DVDD= 1.0mA (typ), TVDD= 0.02mA (typ).

Note 18. All digital input pins are fixed to TVDD or VSS2.

■ Power Consumption on Each Operation Mode

Conditions: Ta=25°C; AVDD= 3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=0V; fs=48kHz,
Programmable Filter=OFF, External Slave Mode, BICK=64fs; AIN input = No signal;
SDTI input = No data; Speaker output = No load.

Mode	Power Management Bit						AVDD [mA]	DVDD [mA]	TVDD [mA]	Total Power [mW]
	PMVCM	PMADC	PMDAC	LOSEL	PMSL	PMPFIL				
All Power-down	0	0	0	0	0	0	0	0	0	0
AIN → ADC	1	1	0	0	0	0	1.6	0.65	0.02	6.5
DAC → SPK	1	0	1	0	1	0	3.2	0.55	0.02	11.6
DAC → Line out	1	0	1	1	1	0	1.6	0.55	0.02	6.3
AIN → ADC & DAC → SPK	1	1	1	0	1	0	4.1	1.0	0.02	15.4
AIN → ADC & DAC → Line out	1	1	1	1	1	0	2.5	1.0	0.02	10.1

Table 1. Power Consumption on Each Operation Mode (typ)

■ Filter Characteristics

(Ta=25°C; fs=48kHz; AVDD=2.8~5.5V, DVDD=1.6~1.98V, TVDD=1.6 or (DVDD-0.2)~3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 19)	±0.16dB	PB	0	-	18.8	kHz
	−0.66dB		-	21.1	-	kHz
	−1.1dB		-	21.7	-	kHz
	−6.9dB		-	24.1	-	kHz
Stopband (Note 19)		SB	28.4	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 20)		GD	-	17	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	−3.0dB	FR	-	3.7	-	Hz
(Note 19)	−0.5dB		-	10.9	-	Hz
	−0.1dB		-	23.9	-	Hz
DAC Digital Filter (LPF):						
Passband	−0.006dB ~ +0.076dB	PB	0	-	21.9	kHz
(Note 19)	−6.0dB		-	24	-	kHz
Stopband (Note 19)		SB	26.2	-	-	kHz
Passband Ripple		PR	-0.006	-	+0.076	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 20)		GD	-	27	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 19. The passband and stopband frequencies scale with fs (sampling frequency).

Note 20. A calculating delay time which is induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the DAC, this time is from setting the 24-bit data of a channel from the input register to the output of analog signal. For the signal through the programmable filters (1st order HPF + 1st order LPF + 4-band Equalizer + ALC + 1-band Equalizer), the group delay is increased by 4/fs from the value above in both recording and playback modes if there is no phase change by the IIR filter.

■ DC Characteristics

(Ta=25°C; fs=48kHz; AVDD=2.8~5.5V, DVDD=1.6~1.98V, TVDD=1.6 or (DVDD-0.2)~3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface & Serial µP Interface (SDA, CSL, PDN, SDTI, BICK, FCK, MCKI pins Input)					
High-Level Input Voltage (TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
(TVDD < 2.2V)		80%TVDD	-	-	V
Low-Level Input Voltage (TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
(TVDD < 2.2V)		-	-	20%TVDD	V
Input Leakage Current	Iin1	-	-	±10	µA
Audio Interface & Serial µP Interface (SDA, BICK, FCK, SDTO pins Output)					
High-Level Output Voltage (Iout = −80µA)	VOH	TVDD−0.2	-	-	V
Low-Level Output Voltage					
(Except SDA pin: Iout = 80µA)	VOL1	-	-	0.2	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout = 3mA)	VOL2	-	-	0.4	V
(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Digital MIC Interface (DMDAT pin Input; DMIC bit = "1", AVDD=2.8~3.6V)					
High-Level Input Voltage	VIH2	65%AVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	35%AVDD	V
Input Leakage Current	Iin2	-	-	±10	µA
Digital MIC Interface (DMCLK pin Output; DMIC bit = "1" , AVDD=2.8~3.6V)					
High-Level Output Voltage (Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 80µA)	VOL3	-	-	0.4	V

■ Switching Characteristics

(Ta=25°C; fs=48kHz; C_L=20pF; AVDD=2.8~5.5V, DVDD=1.6~1.98V, TVDD=1.6 or (DVDD-0.2)~3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency	PLL3-0 bits = “0100”	fCLK	-	11.2896	-	MHz
	PLL3-0 bits = “0101”	fCLK	-	12.288	-	MHz
	PLL3-0 bits = “0110”	fCLK	-	12	-	MHz
	PLL3-0 bits = “0111”	fCLK	-	24	-	MHz
	PLL3-0 bits = “1100”	fCLK	-	13.5	-	MHz
	PLL3-0 bits = “1101”	fCLK	-	27	-	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
FCK Output Timing						
Frequency		fs	-	Table 8	-	Hz
DSP Mode: Pulse Width High		tFCKH	-	1/fBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Frequency	BCKO1-0 bit = “00”	fBCK	-	16fs	-	Hz
	BCKO1-0 bit = “01”	fBCK	-	32fs	-	Hz
	BCKO1-0 bit = “10”	fBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = BICK pin)						
FCK Input Timing						
Frequency	PLL3-0 bits = “0001”	fs	-	fBCK/16	-	Hz
	PLL3-0 bits = “0010”	fs	-	fBCK/32	-	Hz
	PLL3-0 bits = “0011”	fs	-	fBCK/64	-	Hz
DSP Mode: Pulse Width High		tFCKH	1/fBCK−60	-	1/fs−1/fBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Frequency	PLL3-0 bits = “0001”	fBCK	0.128	-	0.768	MHz
	PLL3-0 bits = “0010”	fBCK	0.256	-	1.536	MHz
	PLL3-0 bits = “0011”	fBCK	0.512	-	3.072	MHz
Pulse Width Low		tBCKL	0.4/fBCK	-	-	s
Pulse Width High		tBCKH	0.4/fBCK	-	-	s

Parameter		Symbol	Min.	Typ.	Max.	Unit
External Slave Mode						
MCKI Input Timing						
Frequency	CM1-0 bits = "00"	fCLK	-	256fs	-	Hz
	CM1-0 bits = "01"	fCLK	-	384fs	-	Hz
	CM1-0 bits = "10"	fCLK		512fs		Hz
	CM1-0 bits = "11"	fCLK	-	1024fs	-	Hz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
FCK Input Timing						
Frequency	CM1-0 bits = "00"	fs	8	-	48	kHz
	CM1-0 bits = "01"	fs	8	-	48	kHz
	CM1-0 bits = "10"	fs	8	-	48	kHz
	CM1-0 bits = "11"	fs	8	-	24	kHz
DSP Mode: Pulse Width High		tFCKH	1/fBCK−60	-	1/fs−1/fBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Frequency		fBCK	16fs	-	64fs	Hz
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	2.048	-	12.288	MHz
	384fs	fCLK	3.072	-	18.432	MHz
	512fs	fCLK	4.096	-	24.576	MHz
	1024fs	fCLK	8.192	-	24.576	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
FCK Output Timing						
Frequency	CM1-0 bits = "00"	fs	-	fCLK/256	-	Hz
	CM1-0 bits = "01"	fs	-	fCLK/384	-	Hz
	CM1-0 bits = "10"	fs	-	fCLK/512	-	Hz
	CM1-0 bits = "11"	fs	-	fCLK/1024	-	Hz
DSP Mode: Pulse Width High		tFCKH	-	1/fBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Frequency	BCKO1-0 bit = "00"	fBCK	-	16fs	-	Hz
	BCKO1-0 bit = "01"	fBCK	-	32fs	-	Hz
	BCKO1-0 bit = "10"	fBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (DSP Mode)					
Master Mode					
FCK "↑" to BICK "↑" (Note 21)	tDBF	0.5x1/fBCK−40	0.5x1/fBCK	0.5x1/fBCK+40	ns
FCK "↑" to BICK "↓" (Note 22)	tDBF	0.5x1/fBCK−40	0.5x1/fBCK	0.5x1/fBCK+40	ns
BICK "↑" to SDTO (BCKP bit ="0")	tBSD	−70	-	70	ns
BICK "↓" to SDTO (BCKP bit ="1")	tBSD	−70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
FCK "↑" to BICK "↑" (Note 21)	tFCKB	0.4x1/fBCK	-	-	ns
FCK "↑" to BICK "↓" (Note 22)	tFCKB	0.4x1/fBCK	-	-	ns
BICK "↑" to FCK "↑" (Note 21)	tBFCK	0.4x1/fBCK	-	-	ns
BICK "↓" to FCK "↑" (Note 22)	tBFCK	0.4x1/fBCK	-	-	ns
BICK "↑" to SDTO (BCKP bit ="0")	tBSD	-	-	80	ns
BICK "↓" to SDTO (BCKP bit ="1")	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Audio Interface Timing (Right/Left justified &I²S)					
Master Mode					
BICK "↓" to FCK Edge (Note 23)	tBFCK	−40	-	40	ns
FCK Edge to SDTO (MSB) (Except I²S mode)	tFCKD	−70	-	70	ns
BICK "↓" to SDTO	tBSD	−70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
FCK Edge to BICK "↑" (Note 23)	tFCKB	50	-	-	ns
BICK "↑" to FCK Edge (Note 23)	tBFCK	50	-	-	ns
FCK Edge to SDTO (MSB) (Except I²S mode)	tFCKD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Digital Audio Interface Timing; C_L=100pF					
DMCLK Output Timing					
Period	tSCK	-	1/(64fs)	-	s
Rising Time	tSRise	-	-	10	ns
Falling Time	tSFall	-	-	10	ns
Duty Cycle	dSCK	40	50	60	%
Audio Interface Timing					
DMDAT Setup Time	tDSDS	50	-	-	ns
DMDAT Hold Time	tDSDH	0	-	-	ns

Note 21. MSBS, BCKP bits = "00" or "11".
Note 22. MSBS, BCKP bits = "01" or "10".
Note 23. BICK rising edge must not occur at the same time as FCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I^2C Bus) (Note 24)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 25)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 26)	tAPD	200	-	-	ns
PDN Reject Pulse Width (Note 26)	tRPD	-	-	50	ns
PMADC "↑" to SDTO valid (Note 27)					
ADRST1-0 bits ="00"	tPDV	-	1059	-	1/fs
ADRST1-0 bits ="01"	tPDV	-	267	-	1/fs
ADRST1-0 bits ="10"	tPDV	-	531	-	1/fs
ADRST1-0 bits ="11"	tPDV	-	135	-	1/fs
VCOM Voltage					
Rising Time (Note 28)	tRVCM	-	0.6	2.0	ms

Note 24. I^2C Bus is a trademark of NXP B.V.

Note 25. Data must be held for sufficient time to bridge the 300ns transition time of SCL.

Note 26. The AK4637 can be reset by the PDN pin = "L". The PDN pin must be held "L" for more than 200ns for a certain reset. The AK4637 is not reset by the "L" pulse less than 50ns.

Note 27. This is the count of FCK "↑" from the PMADC bit = "1".

Note 28. All analog blocks including PLL block are powered up after the VCOM voltage (VCOM pin) rises up. An external capacitor of the VCOM pin is 2.2μF (AVDD ≤ 3.6V) or 4.7μF (AVDD > 3.6V) and the REGFIL pin is 2.2μF. The capacitance variation should be ±10%.

■ Timing Diagram

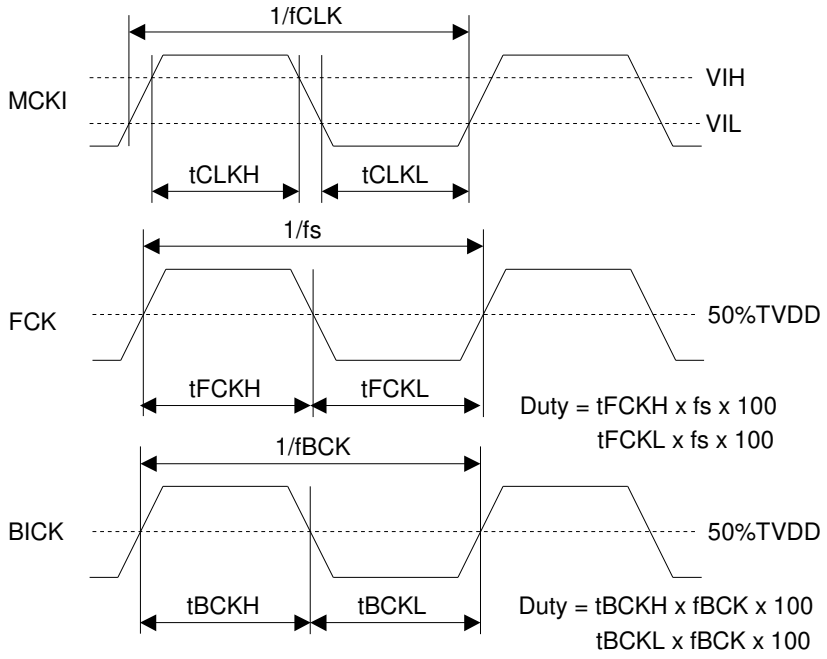


Figure 3. Clock Timing (PLL/EXT Master mode)

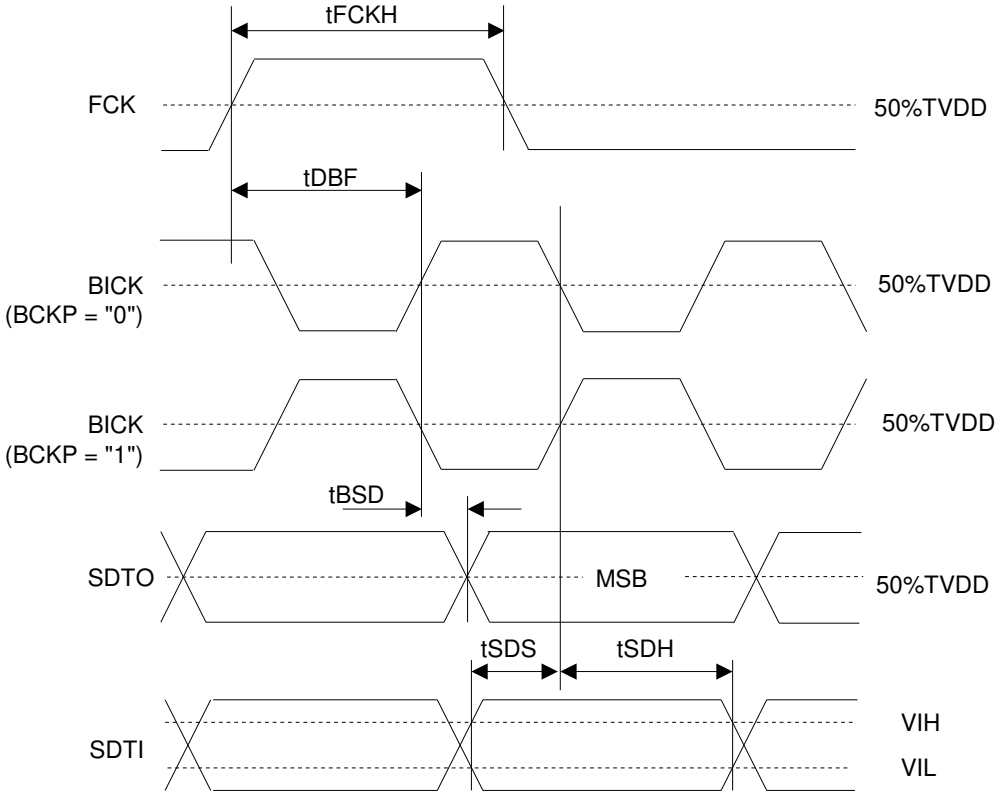


Figure 4. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS bit= “0”)

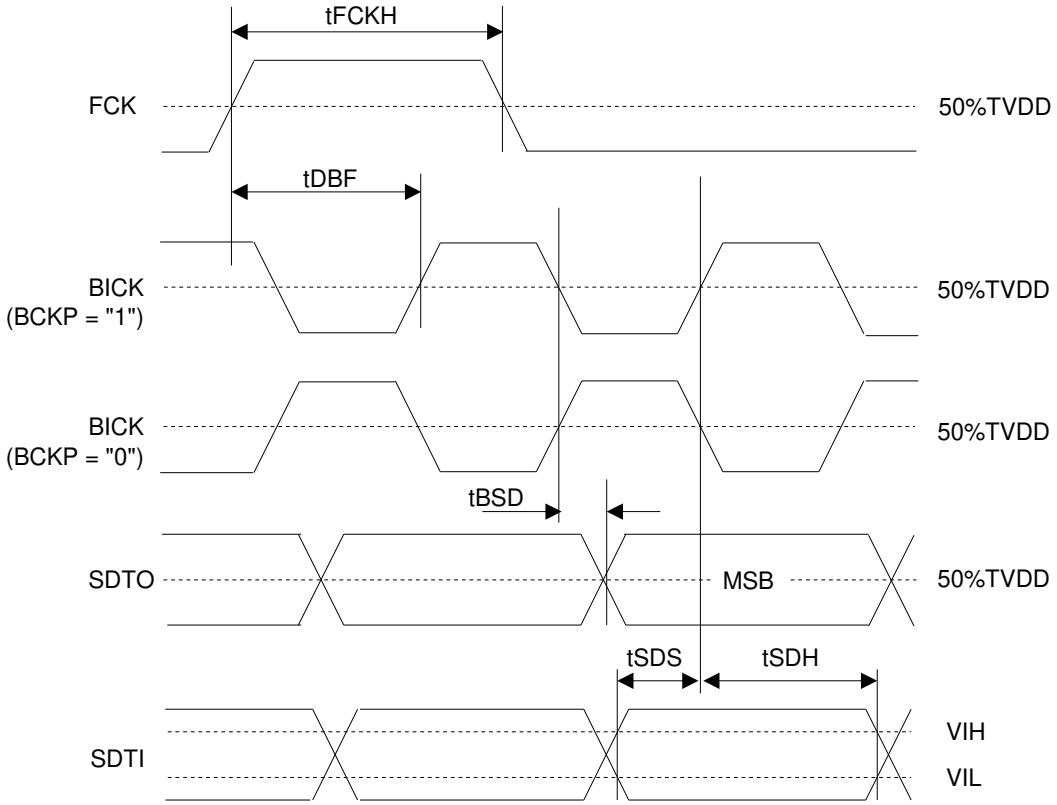


Figure 5. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS bit= “1”)

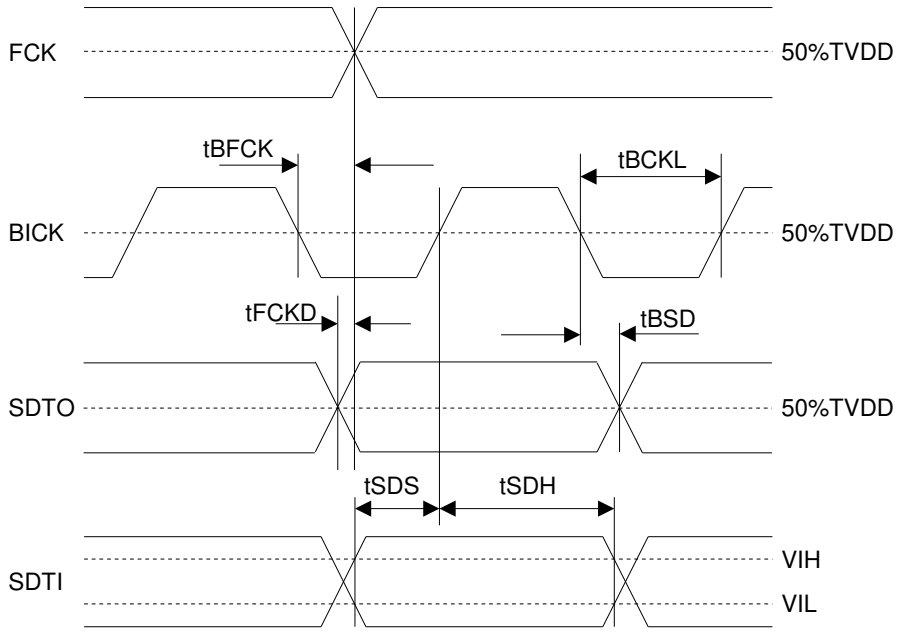


Figure 6. Audio Interface Timing (PLL/EXT Master mode; Except DSP mode)

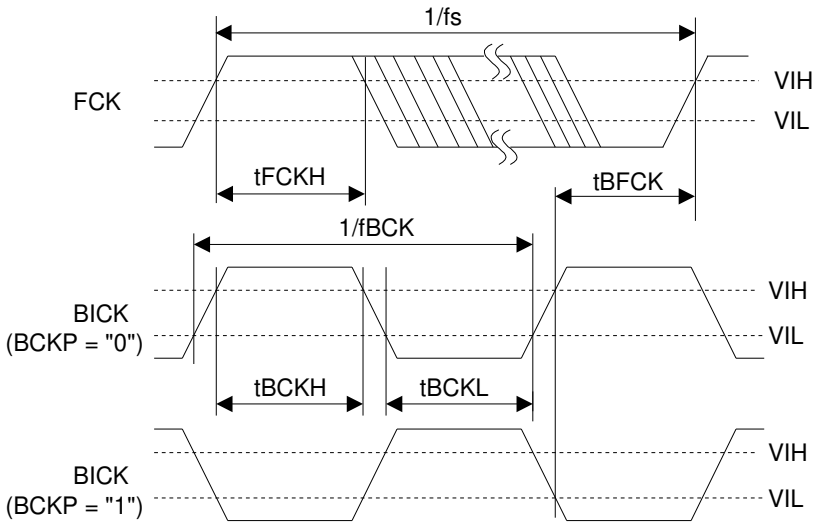


Figure 7. Clock Timing (PLL/EXT Slave mode; DSP mode, MSBS bit= “0”)

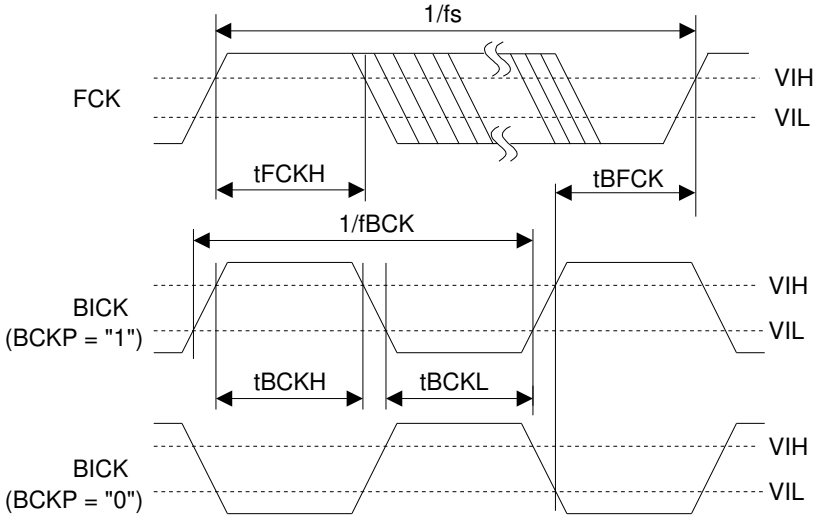


Figure 8. Clock Timing (PLL/EXT Slave mode; DSP mode, MSBS bit= “1”)

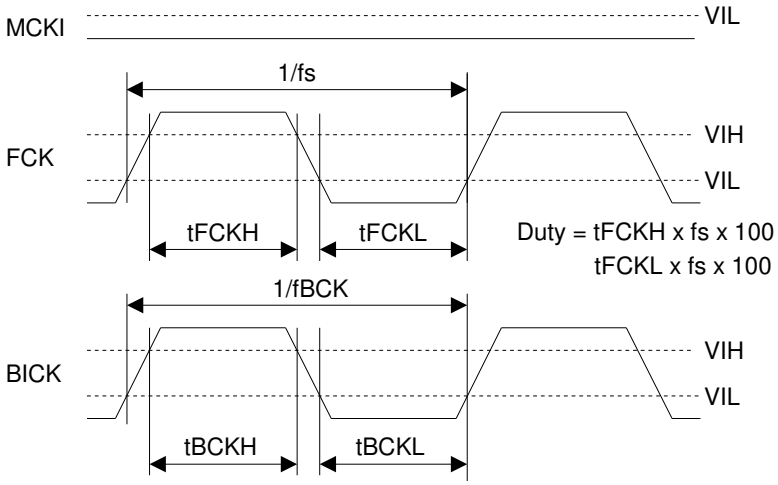


Figure 9. Clock Timing (PLL Slave mode; Except DSP mode)

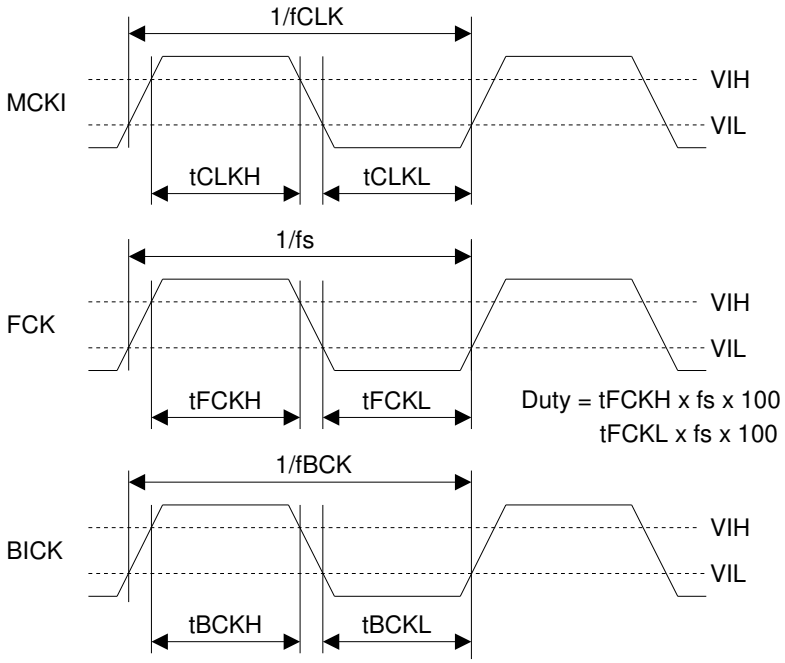


Figure 10. Clock Timing (EXT Slave mode)

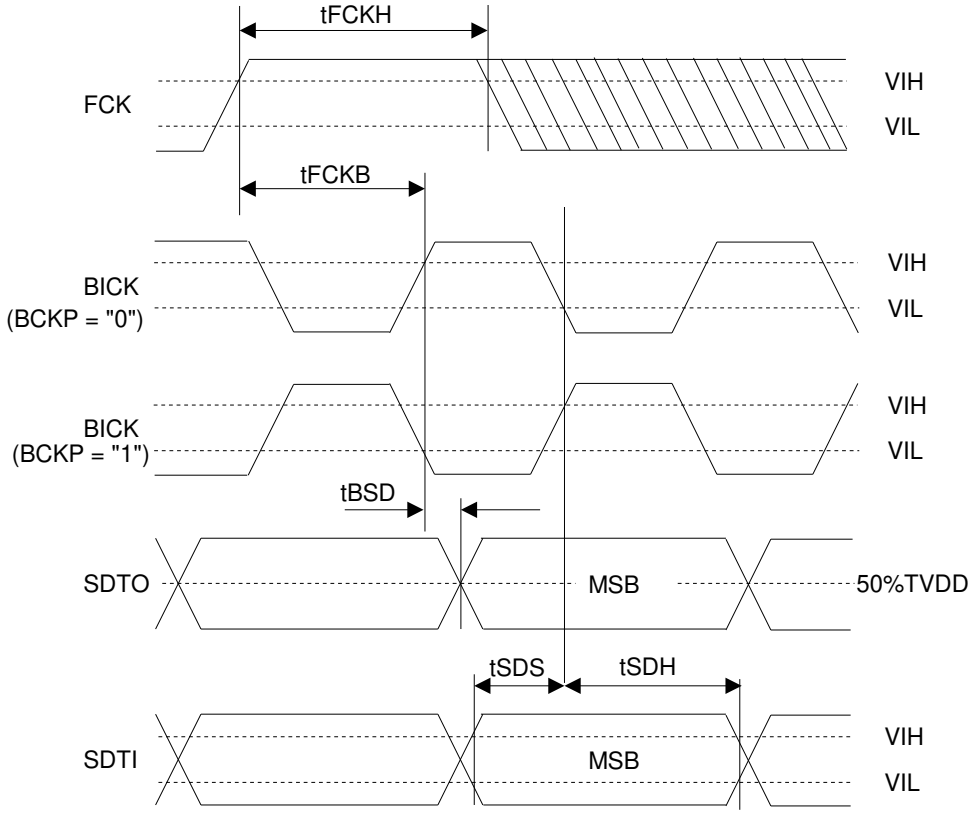


Figure 11. Audio Interface Timing (PLL/EXT Slave mode, DSP mode; MSBS bit= “0”)

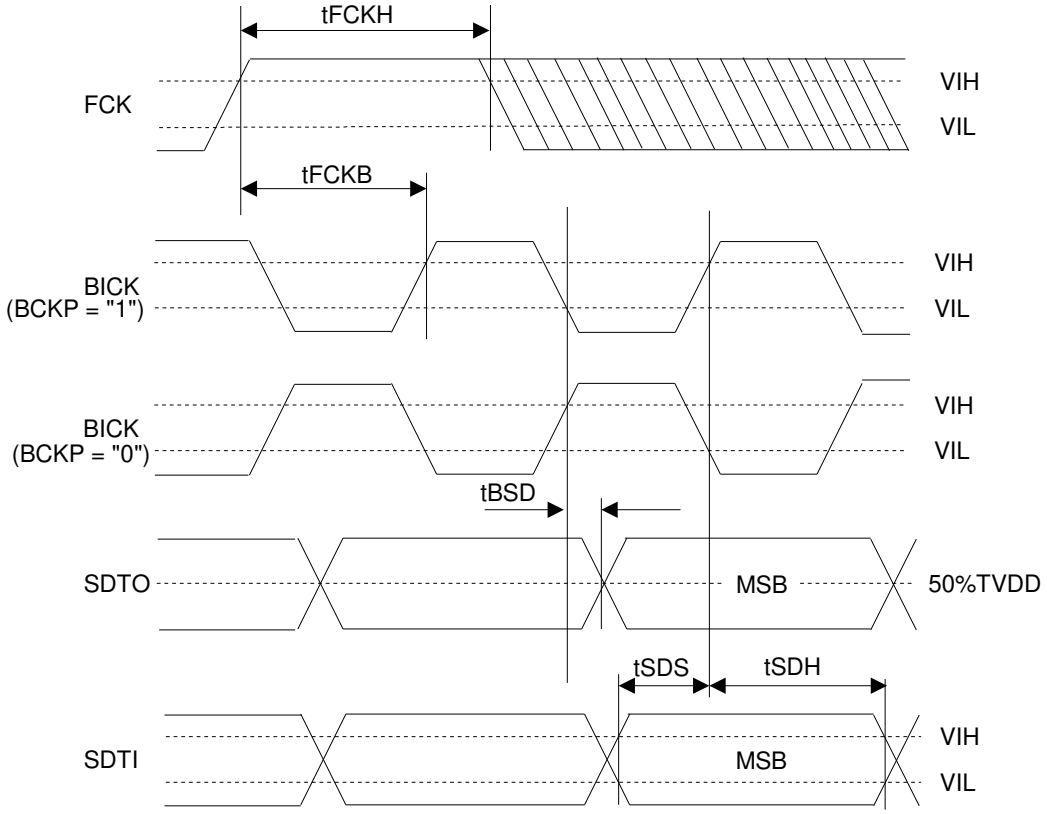


Figure 12. Audio Interface Timing (PLL/EXT Slave mode, DSP mode, MSBS bit= “1”)

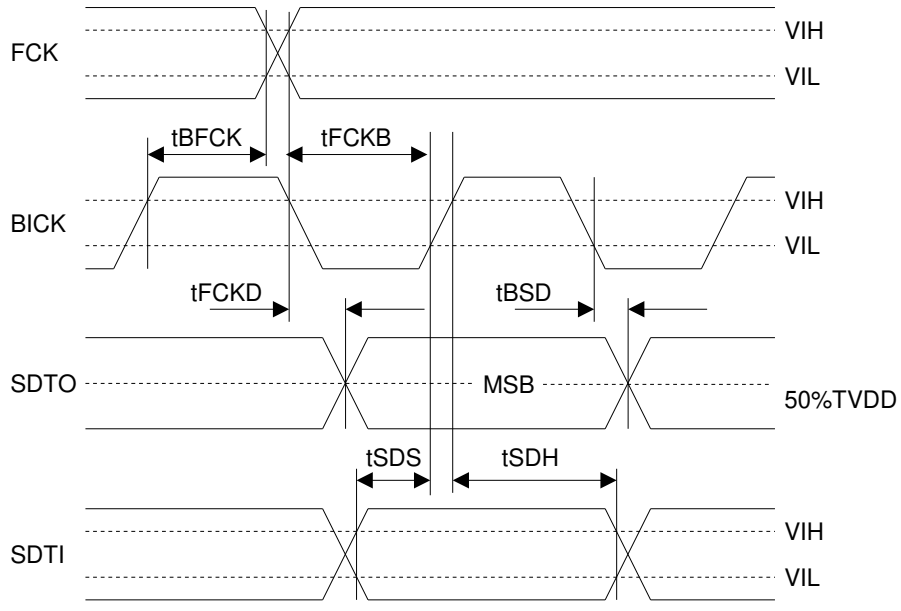
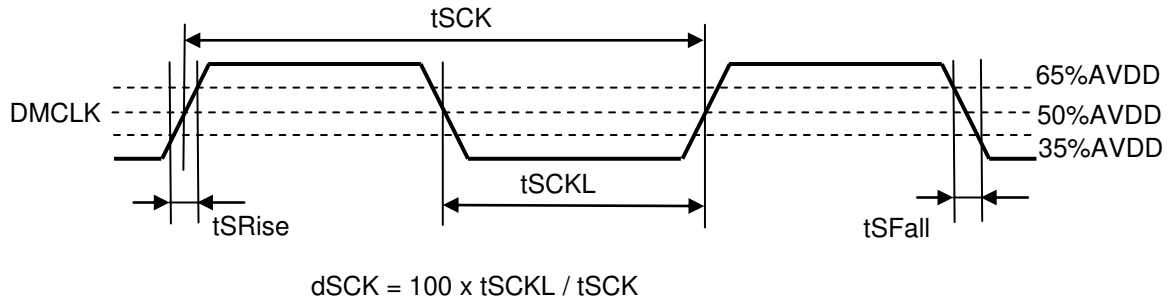


Figure 13. Audio Interface Timing (PLL/EXT Slave mode; Except DSP mode)



dSCK = 100 x tSCKL / tSCK

Figure 14. DMCLK Clock Timing

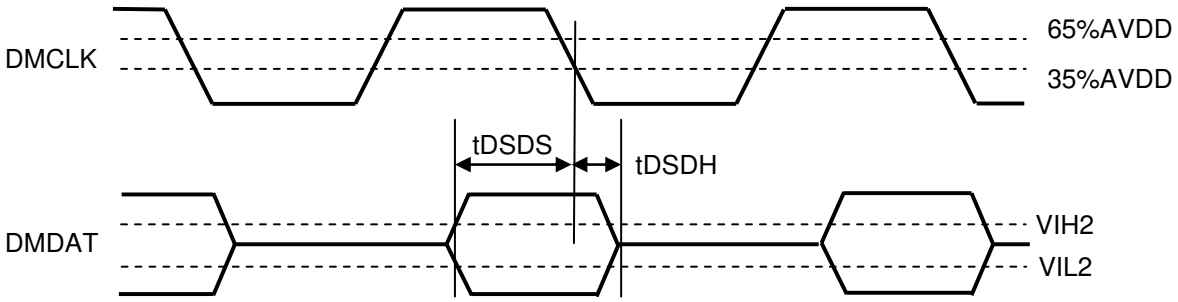


Figure 15. Audio Interface Timing (DCLKP bit = "1")

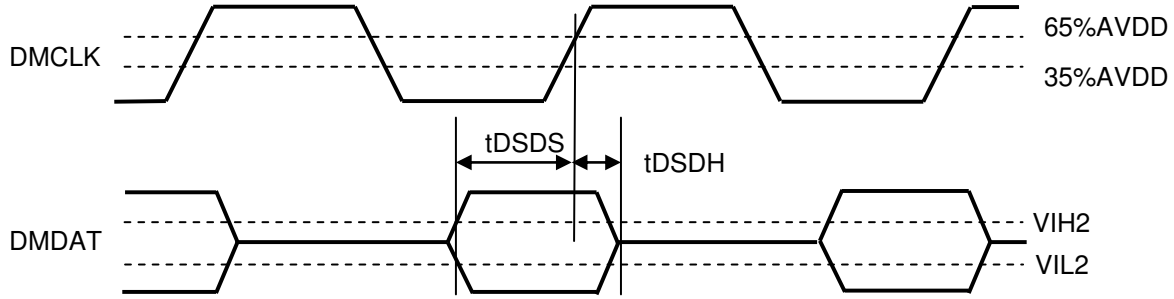


Figure 16. Audio Interface Timing (DCLKP bit = "0")

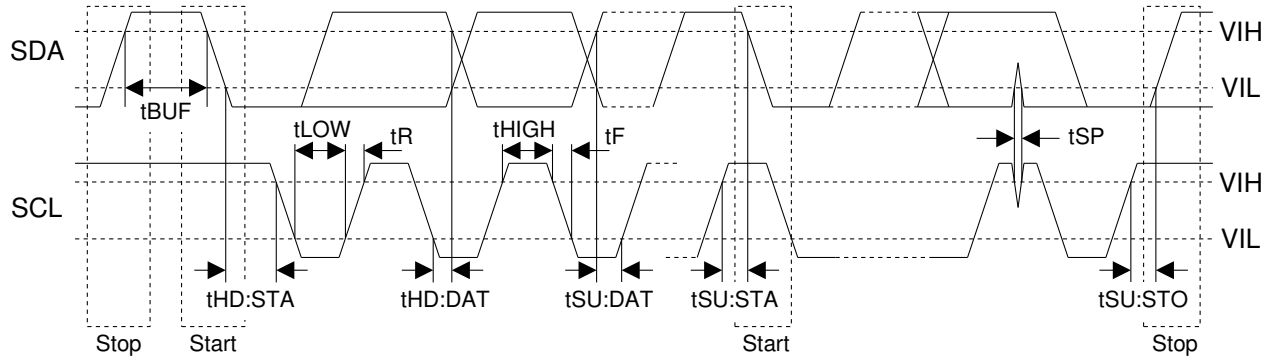


Figure 17. I^2C Bus Mode Timing