Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AK4649VN

24bit Stereo CODEC with MIC/SPK-AMP

GENERAL DESCRIPTION

The AK4649VN features a stereo CODEC with a built-in Microphone-Amplifier and Speaker-Amplifier. Input circuits include a Microphone-Amplifier and an ALC (Automatic Level Control) circuit, and Output circuits include a Speaker-Amplifier. These circuits are suitable for portable application with recording/playback function. The AK4649VN is available in 32pin QFN(5x5mm 0.5mm pitch) utilizing less board space than competitive offerings.

FEATURES

1. Recording Function
- **Stereo Single-ended input with two Selectors**
- **MIC Amplifier**
  (+29dB/+26dB/+23dB/+20dB/+16dB/+12dB/+9dB/+6dB/+3dB/0dB)
- **Digital ALC (Automatic Level Control)**
  - Setting Range: +36dB ~ –54dB, 0.375dB Step
  - Noise Suppression
- **ADC Performance: S/(N+D): 80dB, DR, S/N: 89dB (MIC-Amp=+20dB, AVDD=3.3V)**
  S/(N+D): 80dB, DR, S/N: 100dB (MIC-Amp=0dB, AVDD=3.3V)
- **Wind-noise Reduction Filter**
- **5 Band Notch Filter**
- **Stereo Separation Emphasis**
- **Digital MIC Interface**

2. Playback Function
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**
- **Digital ALC (Automatic Level Control)**
  - Setting Range: +36dB ~ –54dB, 0.375dB Step
  - Noise Suppression
- **Digital Volume Control:**
  - 0dB ~ –18dB, 6dB Step & 256 Linear Step (+0dB ~ - 48.13dB & Mute)
- **Stereo Separation Emphasis**
- **Stereo Line Output**
  - S/(N+D): 87dB, S/N: 97dB
- **Mono Speaker-Amp**
  - SPK-AMP Performance: S/(N+D): 60dB@150mW, S/N: 98dB
  - BTL Output
  - Output Power: 400mW@8Ω (SVDD=3.3V)
- **Analog Mixing: Mono Input**

3. Power Management

4. Master Clock:

(1) PLL Mode
- **Frequencies: 11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)**
  1fs (LRCK pin)
  32fs or 64fs (BICK pin)

(2) External Clock Mode
- **Frequencies: 256fs, 512fs or 1024fs (MCKI pin)**

5. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs
- **PLL Slave Mode (LRCK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (BICK pin): 7.35kHz ~ 48kHz**
- **PLL Slave Mode (MCKI pin):**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz

- **PLL Master Mode:**
  8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
- **EXT Master/Slave Mode:**
  7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)

6. **μP I/F: 3-wire Serial, I²C Bus (Ver 1.0, 400kHz Fast-Mode)**
7. **Master/Slave mode**
8. **Audio Interface Format: MSB First, 2's complement**
   - **ADC: 24bit MSB justified, 16/24bit I²S**
   - **DAC: 24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 16/24bit I²S**
9. **Ta = –40 ~ 85°C**
10. **Power Supply:**
    - **Analog Power Supply (AVDD): 3.0 ~ 3.6V**
    - **Digital Power Supply (DVDD): 3.0 ~ 3.6V**
    - **Speaker Power Supply (SVDD): 3.0 ~ 3.6V**
11. **Package : 32pin QFN, 5x5mm, 0.5mm pitch**
12. **Register Compatible with the AK4646**

■ Block Diagram

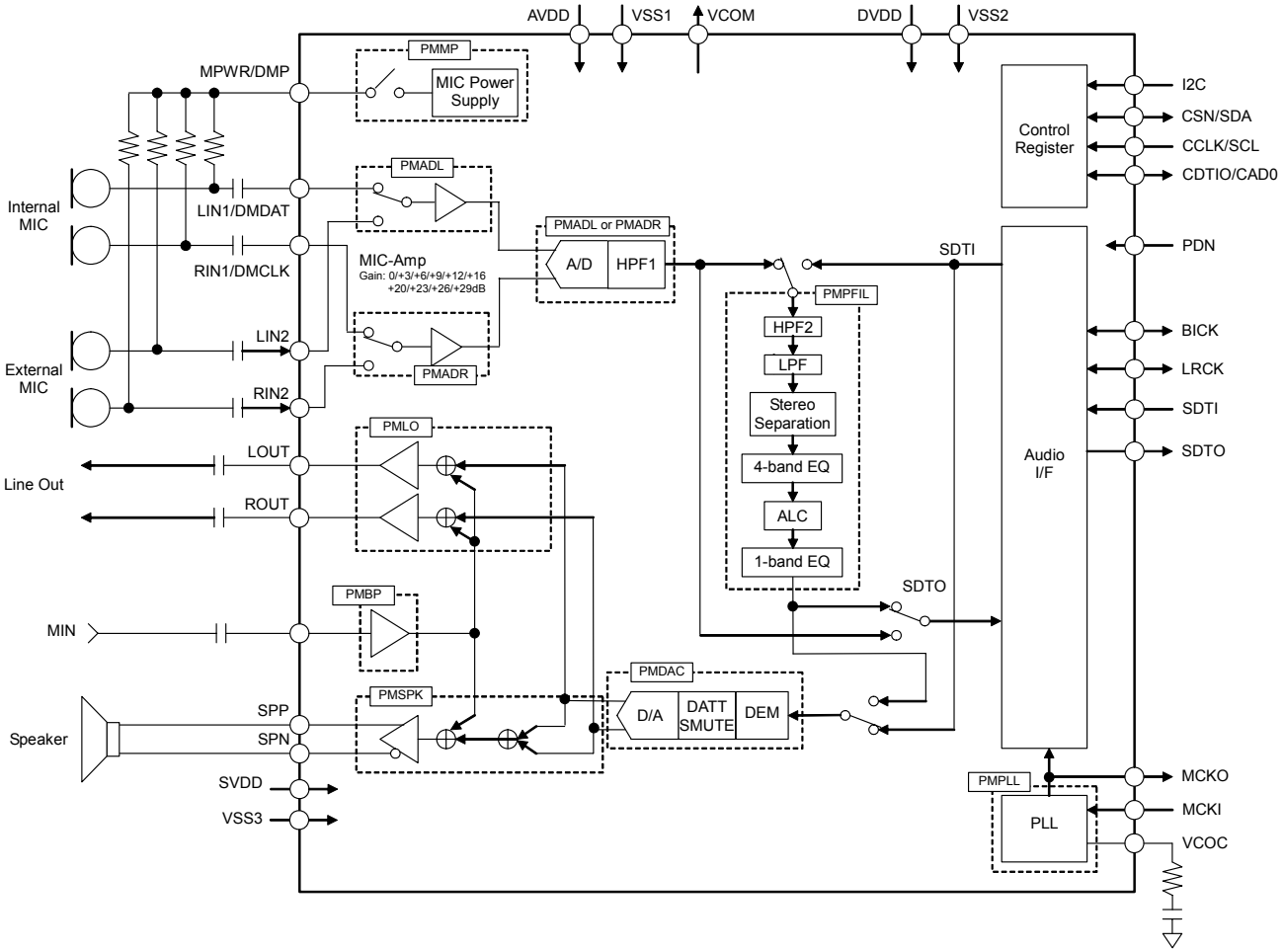
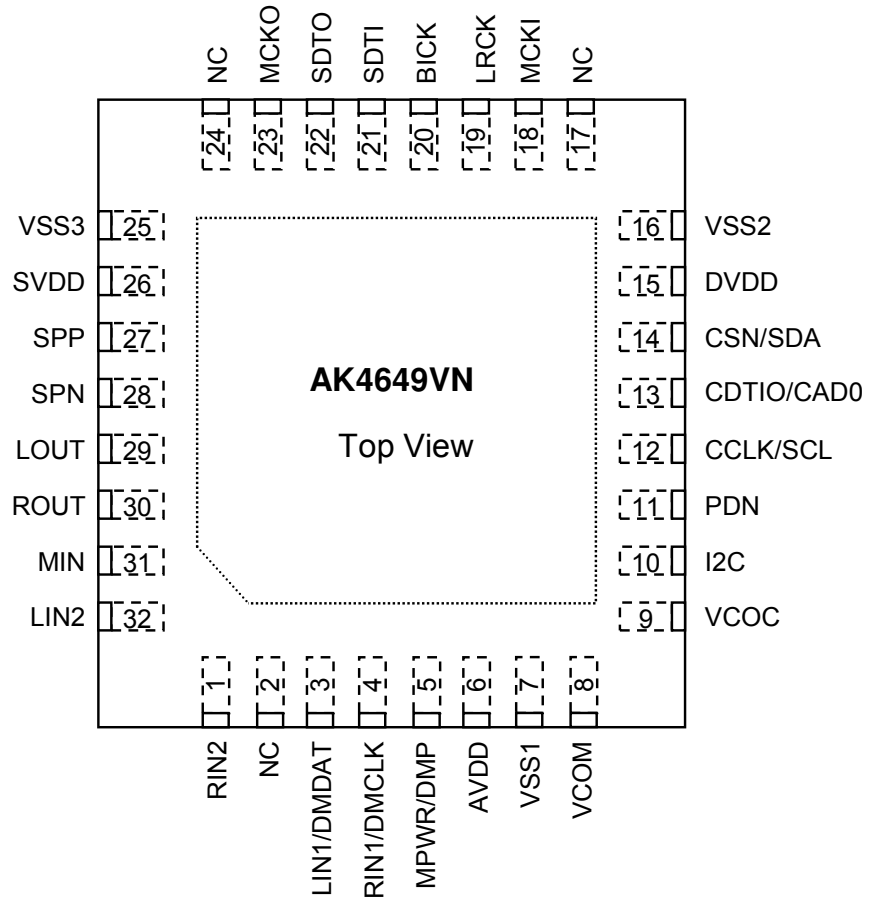


Figure 1. Block Diagram

■ Ordering Guide

AK4649VN	–40 ~ +85°C	32 pin QFN (0.5mm pitch)
AKD4649	Evaluation board for AK4649VN	

■ Pin Layout



Top View

PIN/FUNCTION

No	Pin Name	I/O	Function
1	RIN2	I	Rch Analog Input 2 Pin
2	NC	-	No Connection. No internal bonding. This pin must be connected to the ground.
3	LIN1	I	Lch Analog Input Line Input 1Pin (DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
4	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0")
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")
5	MPWR	O	MIC Power Supply Pin for Microphone (MPDMP bit = 0")
	DMP	O	MIC Power Supply pin for Digital Microphone (MPDMP bit = "1")
6	AVDD	-	Analog Power Supply Pin This pin must be connected to VSS1 with a 0.1μF ceramic capacitor in series.
7	VSS1	-	Ground 1 Pin
8	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs.
9	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin must be connected to VSS1 with one resistor and capacitor in series.
10	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire mode The input circuit of the I2C pin is operated by AVDD.
11	PDN	I	Power-down & Reset When "L", the AK4649VN is in power-down mode and is held in reset. The AK4649VN must be always reset upon power-up.
12	CCLK	I	Control Data Clock Pin (I2C pin = "L")
	SCL	I	Control Data Clock Pin (I2C pin = "H")
13	CDTIO	I/O	Control Data Input/Output Pin (I2C pin = "L")
	CAD0	I	Chip Address Select Pin (I2C pin = "H")
14	CSN	I	Chip Select Pin (I2C pin = "L")
	SDA	I/O	Control Data Input/Output Pin (I2C pin = "H")
15	DVDD	-	Digital Power Supply Pin
16	VSS2	-	Ground 2 Pin
17	NC		No Connection. No internal bonding. This pin must be connected to the ground.
18	MCKI	I	External Master Clock Input Pin
19	LRCK	I/O	Input/Output Channel Clock Pin
20	BICK	I/O	Audio Serial Data Clock Pin
21	SDTI	I	Audio Serial Data Input Pin
22	SDTO	O	Audio Serial Data Output Pin
23	MCKO	O	Master Clock Output Pin
24	NC		No Connection. No internal bonding. This pin must be connected to the ground.
25	VSS3	-	Ground 3 Pin
26	SVDD	-	Speaker Amp Power Supply Pin
27	SPP	O	Speaker Amp Positive Output Pin
28	SPN	O	Speaker Amp Negative Output Pin
29	LOUT	O	Lch Analog Output Pin
30	ROUT	O	Rch Analog Output Pin
31	MIN	I	Mono Analog Signal Input Pin
32	LIN2	I	Lch Analog Input 2 pin

Note 1. All input pins except analog input pins (MIN, LIN1, RIN1, LIN1, RIN2) must not allowed to float.

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR/DMP, VCOC, SPN, SPP, ROUT, LOUT, MIN, RIN2, LIN2, LIN1/DMDAT, RIN1/DMCLK	These pins must be open.
Digital	MCKO	These pins must be open.
	MCKI	This pin must be connected to VSS2.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=0V; Note 2)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	Speaker-Amp	SVDD	–0.3	4.6	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 4)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 5)		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 6)		Pd1	-	390	mW

Note 2. All voltages are with respect to ground.
Note 3. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.
Note 4. MIN, LIN1, RIN1, LIN2 and RIN2 pins
Note 5. PDN, CSN, CCLK, CDTIO, SDTI, LRCK, BICK and MCKI pins
Note 6. In case that PCB wiring density is 200% over and surface wiring density is 50% over. This power is the AK4649VN internal dissipation that does not include power dissipation of an externally connected speaker.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=0V; Note 2)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 7)	Analog	AVDD	3.0	3.3	3.6	V
	Digital	DVDD	3.0	3.3	3.6	V
	SPK-Amp	SVDD	3.0	3.3	3.6	V
	Difference	DVDD-AVDD	-	-	+0.6	V
		AVDD–SVDD	-	-	+0.6	V

Note 2. All voltages are with respect to ground.
Note 7. The power-up sequence between AVDD, DVDD and SVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

*** When DVDD is powered ON and the PDN pin is "L", AVDD or SVDD can be powered OFF. However, when AVDD is powered OFF, the power supply current of DVDD at power-down mode may be increased. When the AK4649VN is changed from power down state to power ON, the PDN pin must be "H" after all power supplies are ON.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=SVDD=3.3V; VSS1=VSS2=VSS3=0V; fs=44.1kHz, BICK=64fs;
Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Unit
MIC Amplifier: LIN1, RIN1, LIN2, RIN2 pins						
Input Resistance			20	30	40	kΩ
Gain	MGAIN3-0 bits = "0000"		-1	0	+1	dB
	MGAIN3-0 bits = "0001"		+19	+20	+21	dB
	MGAIN3-0 bits = "0010"		+25	+26	+27	dB
	MGAIN3-0 bits = "0100"		+8	+9	+10	dB
	MGAIN3-0 bits = "0101"		+15	+16	+17	dB
	MGAIN3-0 bits = "0110"		+22	+23	+24	dB
	MGAIN3-0 bits = "0111"		+28	+29	+30	dB
	MGAIN3-0 bits = "1000"		+2	+3	+4	dB
	MGAIN3-0 bits = "1001"		+5	+6	+7	dB
	MGAIN3-0 bits = "1010"		+11	+12	+13	dB
MIC Power Supply: MPWR pin						
Output Voltage (Note 8)			2.38	2.64	2.90	V
Load Resistance			0.5	-	-	kΩ
Load Capacitance			-	-	30	pF
ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2 pins → ADC → IVOL, IVOL=0dB, ALC=OFF						
Resolution			-	-	24	Bits
Input Voltage (Note 9)		(Note 10)	0.208	0.231	0.254	Vpp
		(Note 11)	2.08	2.31	2.54	Vpp
S/(N+D)	(–1dBFS)	(Note 10)	70	80	-	dBFS
		(Note 11)	-	80	-	dBFS
D-Range	(–60dBFS, A-weighted)	(Note 10)	79	89	-	dB
		(Note 11)	-	100	-	dB
S/N	(A-weighted)	(Note 10)	79	89	-	dB
		(Note 11)	-	100	-	dB
Interchannel Isolation		(Note 10)	75	90	-	dB
		(Note 11)	-	100	-	dB
Interchannel Gain Mismatch		(Note 10)	-	0	0.8	dB
		(Note 11)	-	0	0.8	dB

Note 8. Output voltage is proportional to AVDD voltage. Vout = 0.8 x AVDD (typ)
Note 9. Input voltage is proportional to AVDD voltage. Vin = 0.07 x AVDD (typ) @MGAIN3-0 bits = "0001" (+20dB),
Vin = 0.7 x AVDD (typ) @MGAIN3-0 bits = "0000" (0dB)
Note 10. MGAIN3-0 bits = "0001" (+20dB)
Note 11. MGAIN3-0 bits = "0000" (0dB)

Parameter		min	typ	max	Unit
DAC Characteristics:					
Resolution		-	-	24	Bits
Stereo Line Output Characteristics: DAC → LOUT, ROUT pins, ALC=OFF, DVOL=OVOL=DATT=0dB, LOVL1-0 bit = "00", R_L=10kΩ					
Output Voltage (Note 12)	LOVL1-0 bit = "00"	2.08	2.31	2.54	Vpp
	LOVL1-0 bit = "01"	2.62	2.91	3.20	Vpp
S/(N+D) (–3dBFS)		77	87	-	dBFS
S/N (A-weighted)		87	97	-	dB
Interchannel Isolation		85	100	-	dB
Interchannel Gain Mismatch		-	0	0.8	dB
Load Resistance		10	-	-	kΩ
Load Capacitance		-	-	30	pF
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, DVOL=OVOL=DATT=0dB, R_L=8Ω, BTL					
Output Voltage (Note 13)					
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)		3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)		-	1.79	-	Vrms
S/(N+D)					
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)		-	60	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)		20	50	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)		-	20	-	dB
S/N (A-weighted)		88	98	-	dB
Load Resistance		8	-	-	Ω
Load Capacitance		-	-	30	pF

Note 12. Output voltage is proportional to AVDD voltage. Vout = 0.7 x AVDD (typ) @LOVL1-0 bit = "00".

Note 13. Output voltage is proportional to AVDD voltage.
In case of Full-differential (DAC Input Level = 0dBFS), Vout = 1.02 x AVDD (typ) @SPKG1-0 bits = "00", 1.28 x AVDD (typ) @SPKG1-0 bits = "01", 1.62 x AVDD (typ) @ SPKG1-0 bits = "10".
The output level is calculated by assuming that output signal is no clipped. In the actual case, output signal may be clipped when DAC outputs 0dBFS signal. Therefore, DAC output level should be set to lower level by setting digital volume so that Speaker-Amp output level is not clipped.

Parameter			min	typ	max	Unit
Mono Input: MIN pin, External Resistance mode (BPM bit = "0"), External Input Resistance=33kΩ						
Maximum Input Voltage (Note 14)			-	2.31	-	Vpp
Gain (Note 15)						
	MIN → LOUT/ROUT	LOVL1-0 bit = "00"	-4.5	0	+4.5	dB
		LOVL1-0 bit = "01"	-	+2	-	dB
		LOVL1-0 bit = "10"	-	+4	-	dB
		LOVL1-0 bit = "11"	-	+6	-	dB
	MIN → SPP/SPN					
		ALC bit = "0", SPKG1-0 bits = "00"	-1.2	+3.3	+7.8	dB
		ALC bit = "0", SPKG1-0 bits = "01"	-	+5.3	-	dB
		ALC bit = "0", SPKG1-0 bits = "10"	-	+7.3	-	dB
		ALC bit = "0", SPKG1-0 bits = "11"	-	+9.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "00"	-	+5.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "01"	-	+7.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "10"	-	+9.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "11"	-	+11.3	-	dB
Mono Input: MIN pin, Internal Resistance Mode (BPM bit = "1")						
Input Resistance			23	33	43	kΩ
Maximum Input Voltage (Note 16)			-	2.31	-	Vpp
Gain						
	MIN → LOUT/ROUT	LOVL1-0 bit = "00"	-1	0	+1	dB
		LOVL1-0 bit = "01"	-	+2	-	dB
		LOVL1-0 bit = "10"	-	+4	-	dB
		LOVL1-0 bit = "11"	-	+6	-	dB
	MIN → SPP/SPN					
		ALC bit = "0", SPKG1-0 bits = "00"	+1.3	+3.3	+5.3	dB
		ALC bit = "0", SPKG1-0 bits = "01"	-	+5.3	-	dB
		ALC bit = "0", SPKG1-0 bits = "10"	-	+7.3	-	dB
		ALC bit = "0", SPKG1-0 bits = "11"	-	+9.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "00"	-	+5.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "01"	-	+7.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "10"	-	+9.3	-	dB
		ALC bit = "1", SPKG1-0 bits = "11"	-	+11.3	-	dB

Note 14. The Maximum input voltage is in proportion to both AVDD and external input resistance (Rin). Vin = 0.7 x AVDD x Rin / 33kΩ (typ).

Note 15. The gain is in inverse proportion to external input resistance.

Note 16. The Maximum input voltage is in proportion to AVDD. Vin = 0.7 x AVDD (typ) @ BPLVL = 0dB.

Parameter			min	typ	max	Unit
Power Supplies:						
Power Up (PDN pin = "H")						
	All Circuit Power-up (Note 17)					
		AVDD+DVDD	-	12.5	19	mA
		SVDD (No Load)	-	4.0	12	mA
Power Down (PDN pin = "L") (Note 18)						
	AVDD+DVDD+SVDD		-	1	5	μA

Note 17. When PLL Master Mode (MCKI=12MHz), and PMADL = PMADR = PMDAC =PMPFIL = PMLO = PMSPK = PMVCM = PMPLL = MCKO = PMBP = PMMP = M/S bits = "1". The MPWR pin outputs 0mA. AVDD = 6.8mA (typ), DVDD = 5.7mA (typ).

Note 18. All digital input pins are fixed to DVDD or VSS2.

FILTER CHARACTERISTICS

(Ta =25°C; AVDD=SVDD=3.0 ~ 3.6V, DVDD =3.0 ~ 3.6V; fs=44.1kHz; DEM=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 19)	±0.16dB	PB	0	-	17.3	kHz
	–0.66dB		-	19.4	-	kHz
	–1.1dB		-	19.9	-	kHz
	–6.9dB		-	22.1	-	kHz
Stopband		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 20)		GD	-	19	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	3.4	-	Hz
	–0.5dB		-	10	-	Hz
	–0.1dB		-	22	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 19)	±0.05dB	PB	0	-	20.0	kHz
	–6.0dB		-	22.05	-	kHz
Stopband		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.02	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 20)		GD	-	20	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 19. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=20.0kHz (@–1.0dB) is 0.454 x fs (ADC). Each response refers to that of 1kHz

Note 20. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 24-bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 24-bit data of both channels from the input register to the output of analog signal.
For the signal through the programmable filters (First HPF + First LPF + 4-band Equalizer + ALC + Equalizer), group delay is increased 5/fs at Recording Mode or 7/fs at Playback Mode from the value above if there is no phase change by the IIR filter.

DC CHARACTERISTICS

(Ta = 25°C; AVDD=SVDD=3.0 ~ 3.6V, DVDD =3.0 ~ 3.6V; fs=44.1kHz)

Parameter	Symbol	min	typ	max	Unit
Audio Interface & Serial µP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)					
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
Audio Interface & Serial µP Interface (CDTIO, SDA MCKO, BICK, LRCK, SDTO pins Output)					
High-Level Output Voltage (Iout = −80µA)	VOH	DVDD−0.2	-	-	V
Low-Level Output Voltage					
(Except SDA pin : Iout = 80µA)	VOL1	-	-	0.2	V
(SDA pin : Iout = 3mA)	VOL2	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	µA
Digital MIC Interface (DMDAT pin Input ; DMIC bit = "1")					
High-Level Input Voltage	VIH3	65%AVDD	-	-	V
Low-Level Input Voltage	VIL3	-	-	35%AVDD	V
Digital MIC Interface (DMCLK pin Output ; DMIC bit = "1")					
High-Level Output Voltage (Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 80µA)	VOL3	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD=SVDD=3.0 ~ 3.6V, DVDD =3.0 ~ 3.6V; C_L=20pF)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	12.288	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter			Symbol	min	typ	max	Unit
PLL Slave Mode (PLL Reference Clock = LRCK pin)							
LRCK Input Timing							
Frequency			fs	7.35	-	48	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period			tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low			tBCKL	240	-	-	ns
Pulse Width High			tBCKH	240	-	-	ns
PLL Slave Mode (PLL Reference Clock = BICK pin)							
LRCK Input Timing							
Frequency			fs	7.35	-	48	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period	PLL3-0 bits = “0010”		tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = “0011”		tBCK	-	1/(64fs)	-	ns
Pulse Width Low			tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High			tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	1.8816	-	12.288	MHz
	512fs		fCLK	3.7632	-	13.312	MHz
	1024fs		fCLK	7.5264	-	13.312	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing							
Frequency	256fs		fs	7.35	-	48	kHz
	512fs		fs	7.35	-	26	kHz
	1024fs		fs	7.35	-	13	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period			tBCK	312.5	-	-	ns
Pulse Width Low			tBCKL	130	-	-	ns
Pulse Width High			tBCKH	130	-	-	ns
External Master Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	1.8816	-	12.288	MHz
	512fs		fCLK	3.7632	-	13.312	MHz
	1024fs		fCLK	7.5264	-	13.312	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing							
Frequency			fs	7.35	-	48	kHz
Duty Cycle			Duty	-	50	-	%
BICK Output Timing							
Period		BCKO bit = “0”	tBCK	-	1/(32fs)	-	ns
		BCKO bit = “1”	tBCK	-	1/(64fs)	-	ns
Duty Cycle			dBCK	-	50	-	%

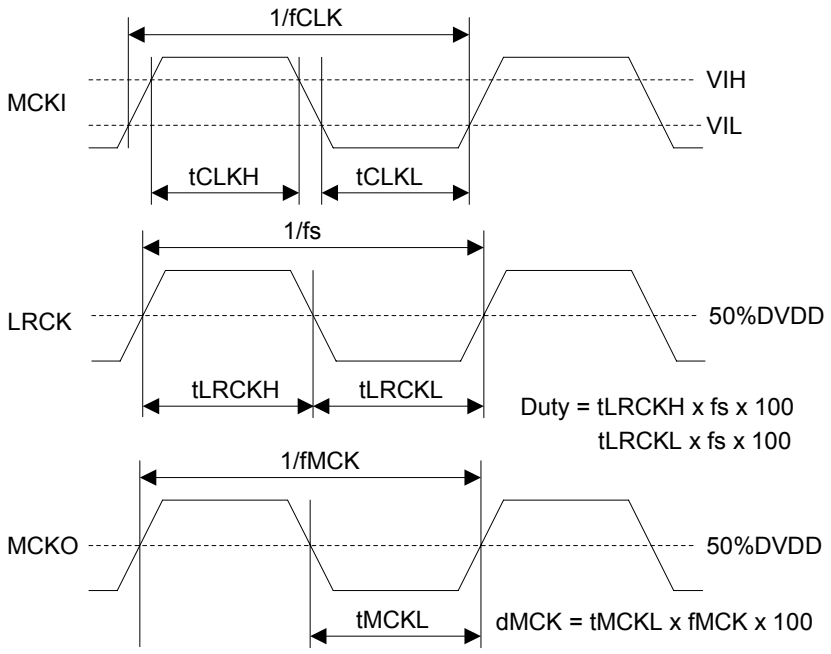
Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 21)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 21)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 21)	tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	80	ns
BICK "↓" to SDTO	tBSD	-	-	80	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Control Interface Timing (3-wire Mode):					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 22)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 22)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command)(Note 24)	tCCZ	-	-	70	ns
Control Interface Timing (I²C Bus Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 25)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 21. BICK rising edge must not occur at the same time as LRCK edge.
Note 22. CCLK rising edge must not occur at the same time as CSN edge.
Note 23. I²C-bus is a trademark of NXP B.V.
Note 24. R_L=1kΩ/10% change (pull-up or DVDD)
Note 25. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Parameter	Symbol	min	typ	max	Unit
Digital Audio Interface Timing; C_L=100pF					
DMCLK Output Timing					
Period	tSCK	-	1/(64fs)	-	ns
Rising Time	tSRise	-	-	10	ns
Falling Time	tSFall	-	-	10	ns
Duty Cycle	dSCK	40	50	60	%
Audio Interface Timing					
DMDAT Setup Time	tSDS	50	-	-	ns
DMDAT Hold Time	tSDH	0	-	-	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 26)	tPD	150	-	-	ns
PMADL or PMADR "↑" to SDTO valid (Note 27)					
ADRST bit = "0"	tPDV	-	1059	-	1/fs
ADRST bit = "1"	tPDV	-	267	-	1/fs

Note 26. The AK4649VN can be reset by the PDN pin = "L".
Note 27. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

■ Timing Diagram



Note 28. MCKO is not available at EXT Master mode.
Figure 2. Clock Timing (PLL/EXT Master mode)

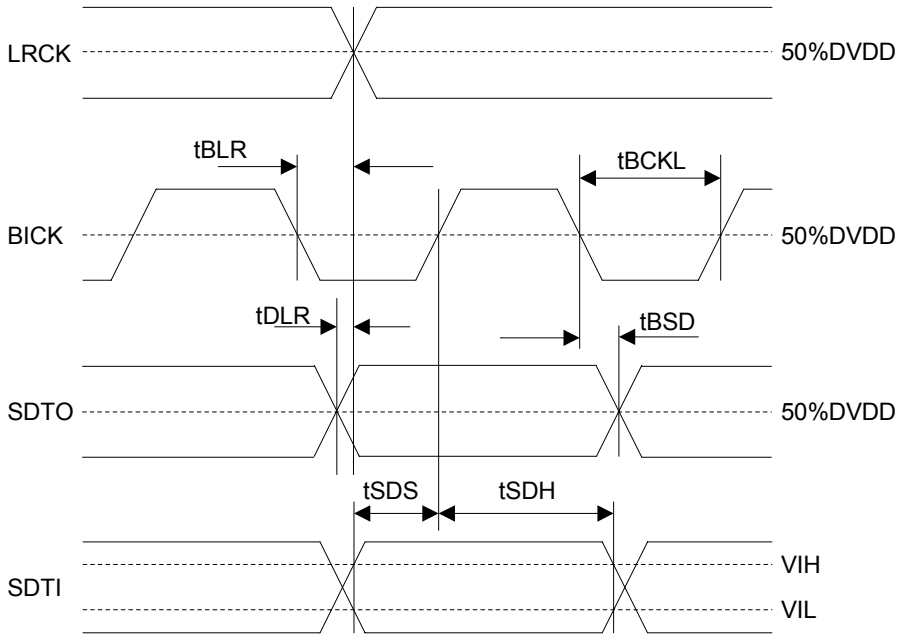


Figure 3. Audio Interface Timing (PLL/EXT Master mode)

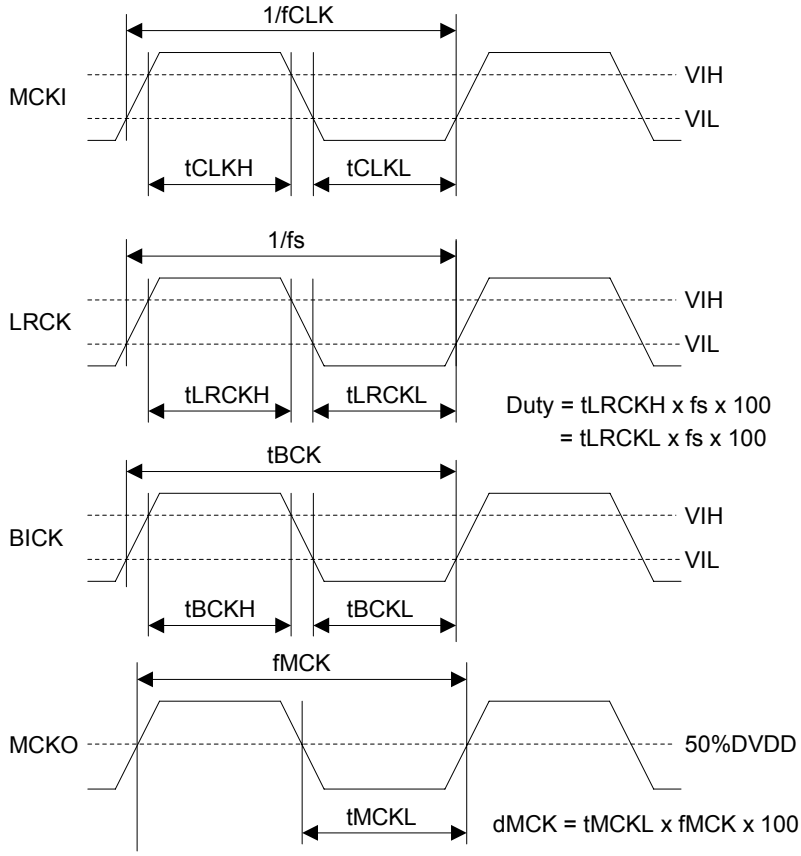


Figure 4. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin)

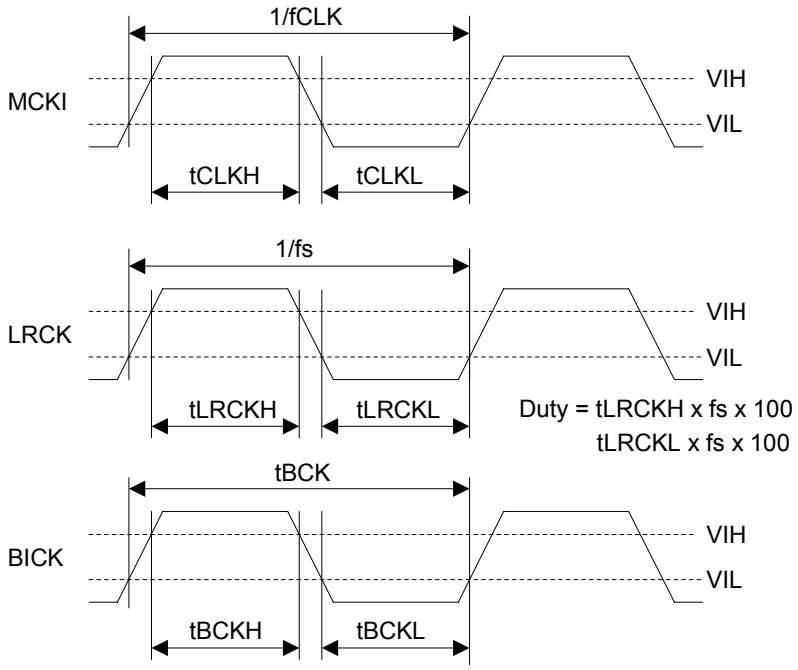


Figure 5. Clock Timing (EXT Slave mode)

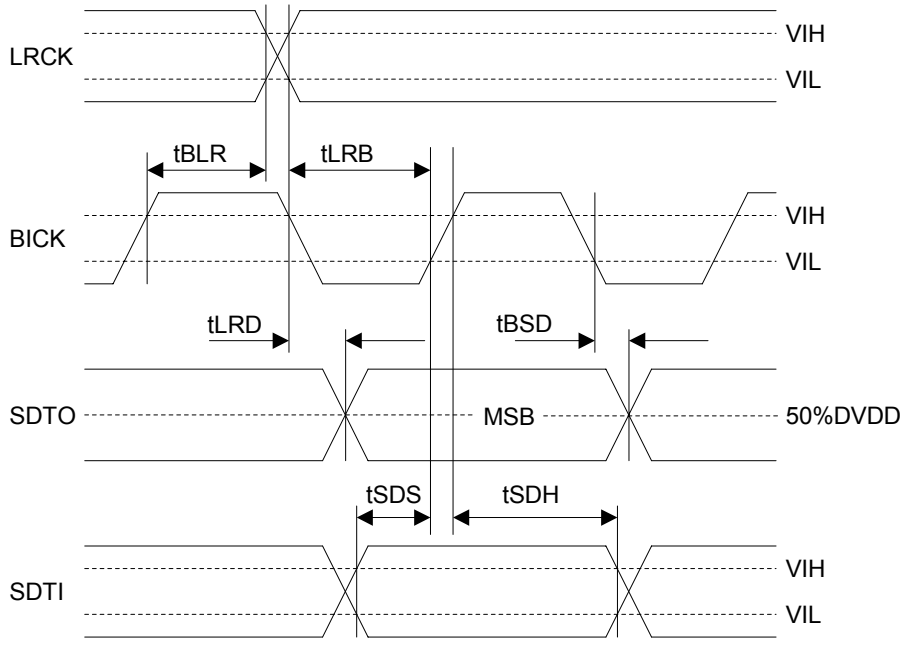


Figure 6. Audio Interface Timing (PLL/EXT Slave mode)

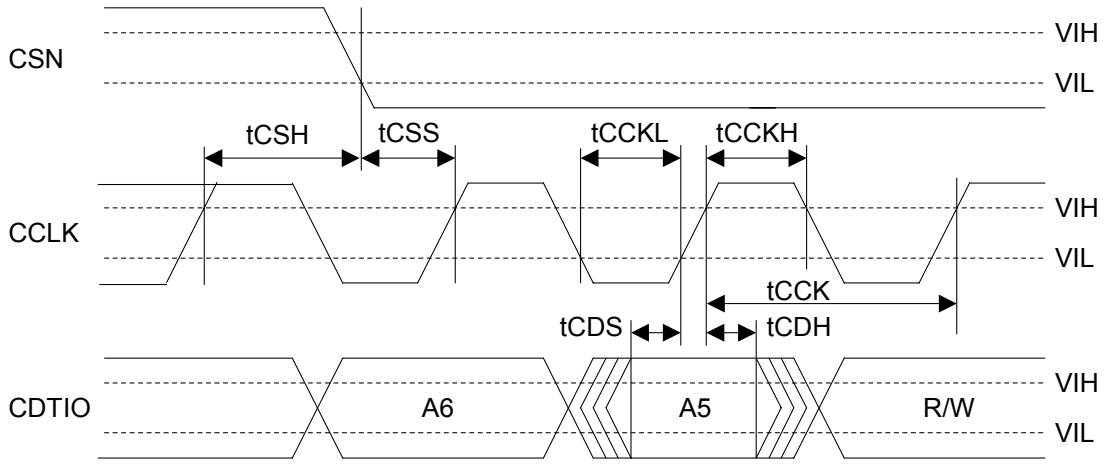


Figure 7. WRITE Command Input Timing

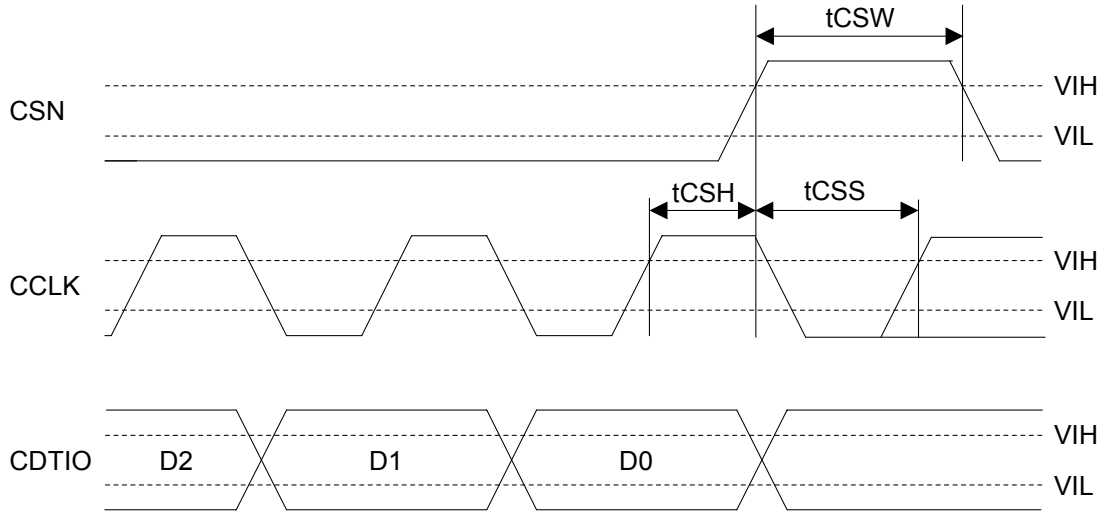


Figure 8. WRITE Data Input Timing

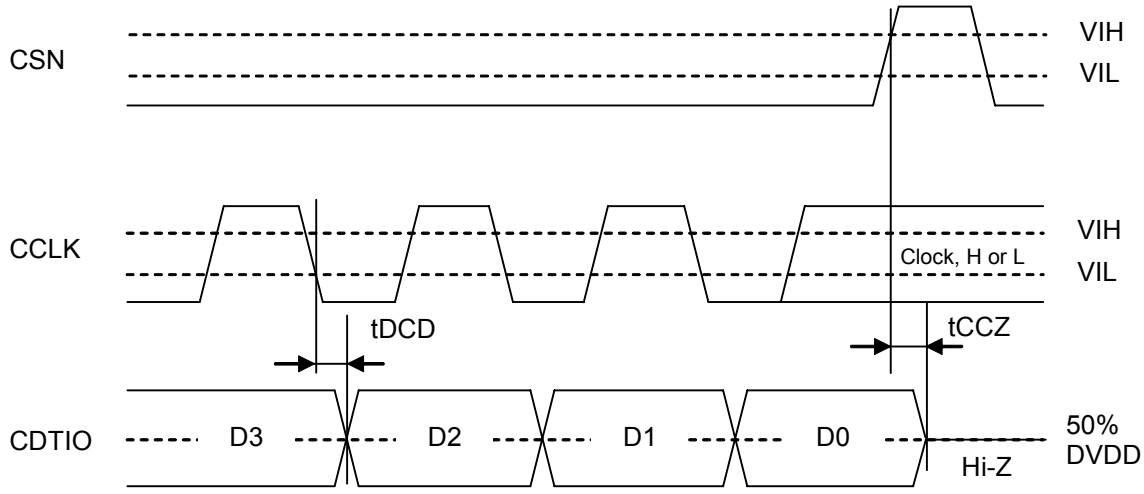


Figure 9. Read Data Output Timing

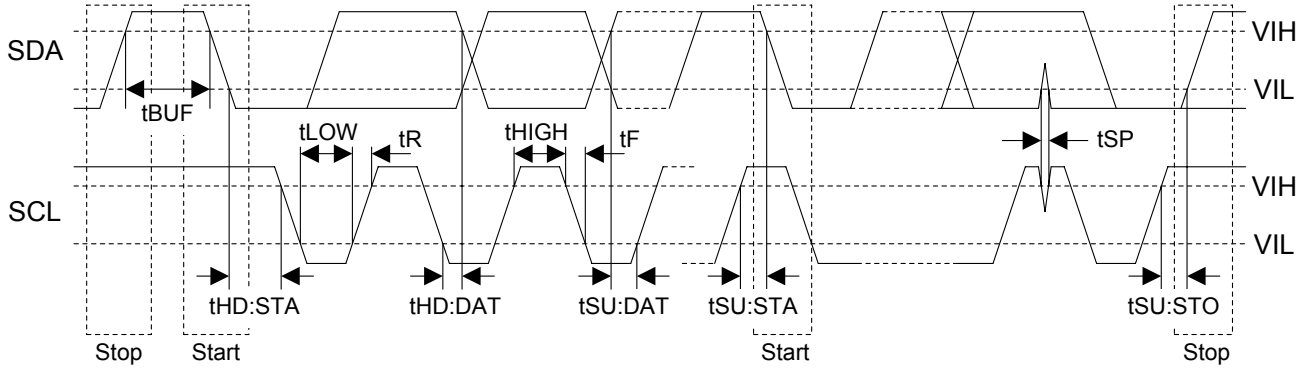


Figure 10. I^{2}C Bus Mode Timing

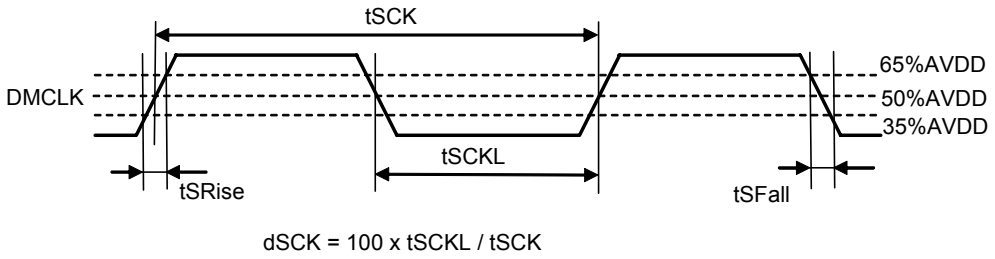


Figure 11. DMCLK Clock Timing

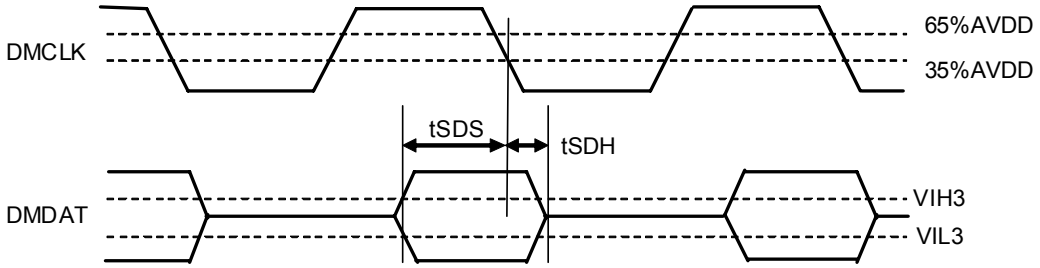


Figure 30. Audio Interface Timing (DCLKP bit = "1")

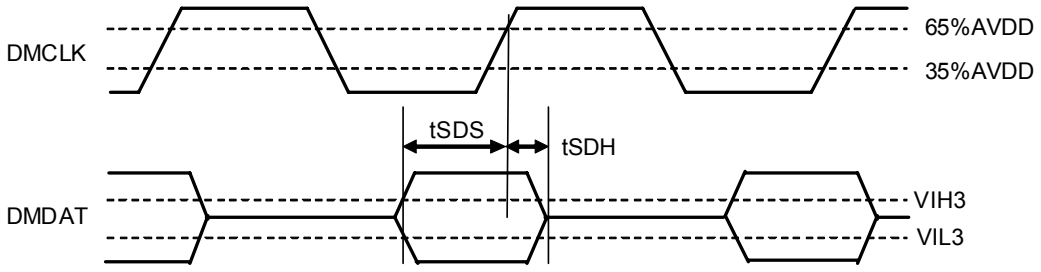


Figure 31. Audio Interface Timing (DCLKP bit = "0")

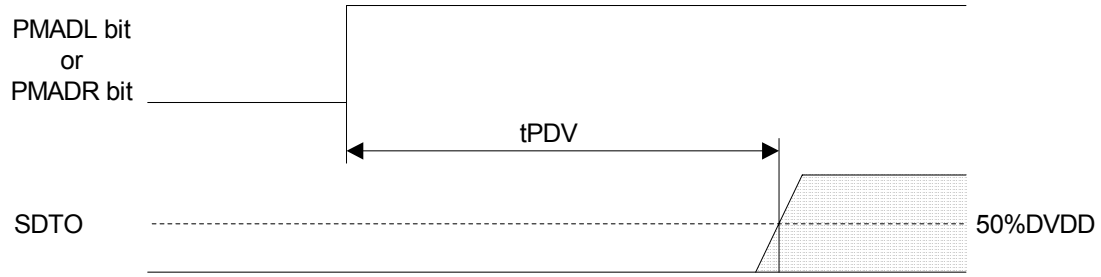


Figure 12. Power Down & Reset Timing 1

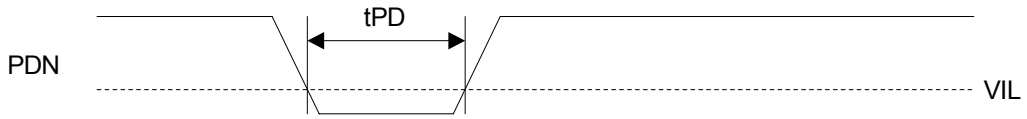


Figure 13. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 1, Table 2).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 29)	1	1	Table 4	Figure 14
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 4	Figure 15
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	Table 4	Figure 16 Figure 17
EXT Slave Mode	0	0	x	Figure 18
EXT Master Mode	0	1	x	Figure 19

Note 29. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from the MCKO pin.

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	Input (Selected by BCKO bit)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	0	L	GND	Input (Selected by BCKO bit)	Input (1fs)
EXT Slave Mode	0	L	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Note 30. When PMVCM bit = M/S bit = "1" and MCKI is input, LRCK and BICK are output, even if PMDAC bit = PMADL bit = PMADR bit = "0".

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4649VN is power-down mode (PDN pin = "L") and exits reset state, the AK4649VN is in slave mode. After exiting reset state, the AK4649VN goes to master mode by changing M/S bit = "1".

When the AK4649VN is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes "1". The LRCK and BICK pins of the AK4649VN must be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, when the AK4649VN is supplied stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or when the sampling frequency is changed.

1) PLL Mode Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	LRCK pin	1fs	6.8k	220n	160ms	(default)
1	0	0	0	1	N/A	-	-	-	-	
2	0	0	1	0	BICK pin	32fs	10k	4.7n	2ms	
3	0	0	1	1	BICK pin	64fs	10k	4.7n	2ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	10ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	10ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	10ms	
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	10ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	10ms	
Others	Others				N/A					

Note 31. R has a tolerance of ± 5%, and C has a tolerance of ± 30%.

Table 4. Setting of PLL Mode (*fs: Sampling Frequency, N/A: Not Available)

2) Setting of sampling frequency in PLL Mode

When PLL2 bit is "1" (PLL reference clock input is MCKI pin), the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	(default)
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz	
5	0	1	0	1	11.025kHz	
6	0	1	1	0	14.7kHz	
7	0	1	1	1	22.05kHz	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz	
15	1	1	1	1	44.1kHz	
Others	Others				N/A	

Table 5. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1" (Reference Clock = MCKI pin), (N/A: Not Available)

When PLL2 bit is "0" (PLL reference clock input is LRCK or BICK pin), the sampling frequency is selected by FS3 and FS2 bits. (Table 6).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	x	x	7.35kHz ≤ fs ≤ 12kHz	(default)
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	0	x	x	24kHz < fs ≤ 48kHz	
Others	Others				N/A	

Table 6. Setting of Sampling Frequency at PLL2 bit = "0" and PMPLL bit = "1" PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin), (x: Don't care, N/A: Not Available)

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, the LRCK and BICK pins go to "L" and irregular frequency clock is output from the MCKO pin at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin goes to "L" (Table 7).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, the BICK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except the case above)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	Table 9	Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". Then, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal can be muted by writing "0" to DACL and DACS bits.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock (except the case above)	"L" Output	Invalid
PLL Lock	"L" Output	Output

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "0", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 13.5MHz, 24MHz or 27MHz) is input to the MCKI pin, MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 10).

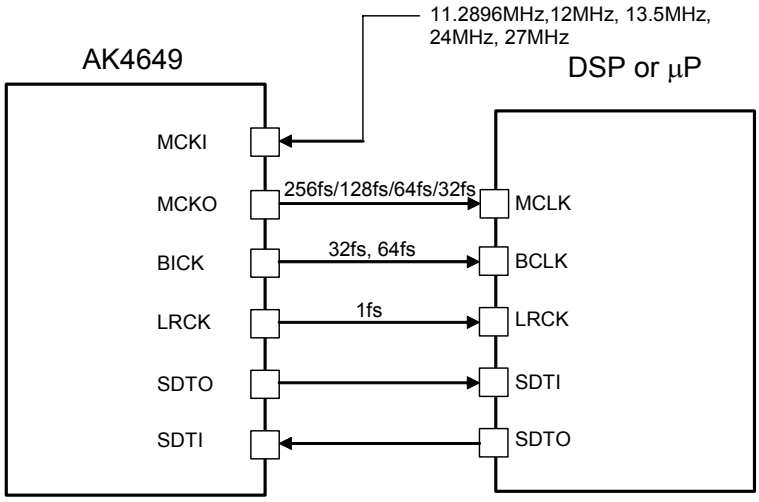


Figure 14. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO bit	BICK Output Frequency	
0	32fs	(default)
1	64fs	

Table 10. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to the MCKI, BICK or LRCK pin. The required clock for the AK4649VN is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL reference clock: MCKI pin

BICK and LRCK inputs must be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5)

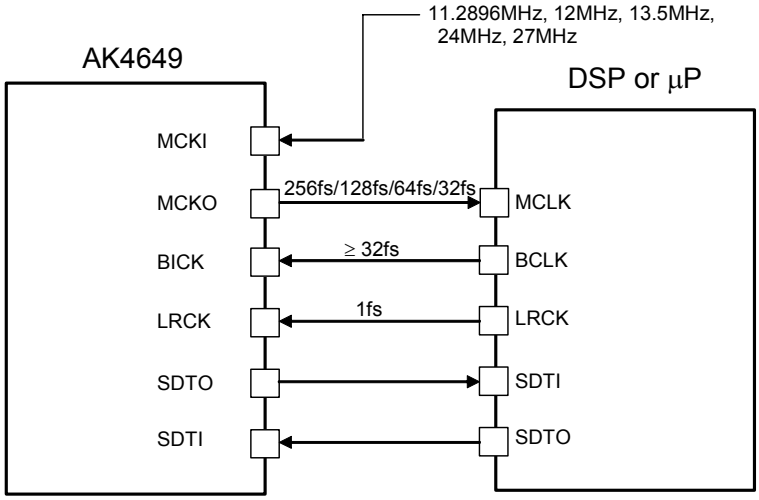


Figure 15. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)