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AK4683

Asynchronous Multi-Channel Audio CODEC with DIR/T

GENERAL DESCRIPTION

The AK4683 is a single chip CODEC that includes two channels of ADC and four channels of DAC. The ADC outputs 24bit data and the DAC accepts up to 24bit input data. The ADC has the Enhanced Dual Bit architecture with wide dynamic range. The DAC introduces the new developed Advanced Multi-Bit architecture, and achieves wider dynamic range and lower outband noise. The AK4683 also has digital audio receiver (DIR) and transmitter (DIT) compatible with 192kHz, 24bits. The DIR can automatically detect a Non-PCM bit stream such as Dolby Digital (AC-3)*. The AK4683 has a dynamic range of 100dB for ADC, 106dB for DAC and is well suited for digital TV and home theater system.

* Dolby Digital (AC-3) is a trademark of Dolby Laboratories.

FEATURES

- **ADC/DAC part**
  - **Asynchronous ADC/DAC Operation**
  - **6:1 Input Selector with Pre-amp**
  - **2ch 24bit ADC**
    - **64x Oversampling**
    - **Sampling Rate up to 96kHz**
    - **Linear Phase Digital Anti-Alias Filter**
    - **Single-Ended Input**
    - **S/(N+D): 90dB**
    - **Dynamic Range, S/N: 100dB**
    - **Digital HPF for Offset Cancellation**
    - **Channel Independent Digital Volume (+24/-103dB, 0.5dB/step)**
    - **Soft Mute**
    - **Overflow Flag**
  - **4ch 24bit DAC**
    - **128x Oversampling**
    - **Sampling Rate up to 192kHz**
    - **24bit 8 times Digital Filter**
    - **Single-Ended Outputs**
    - **S/(N+D): 90dB**
    - **Dynamic Range, S/N: 106dB**
    - **Channel Independent Digital Volume (+12/-115dB, 0.5dB/step)**
    - **Soft Mute**
    - **De-emphasis Filter (32kHz, 44.1kHz, 48kHz)**
    - **Zero Detect Function**
  - **Stereo Headphone Amp with Volume**
    - **50mW at 16ohm**
    - **Click-noise free at Power on/off**
  - **High Jitter Tolerance**

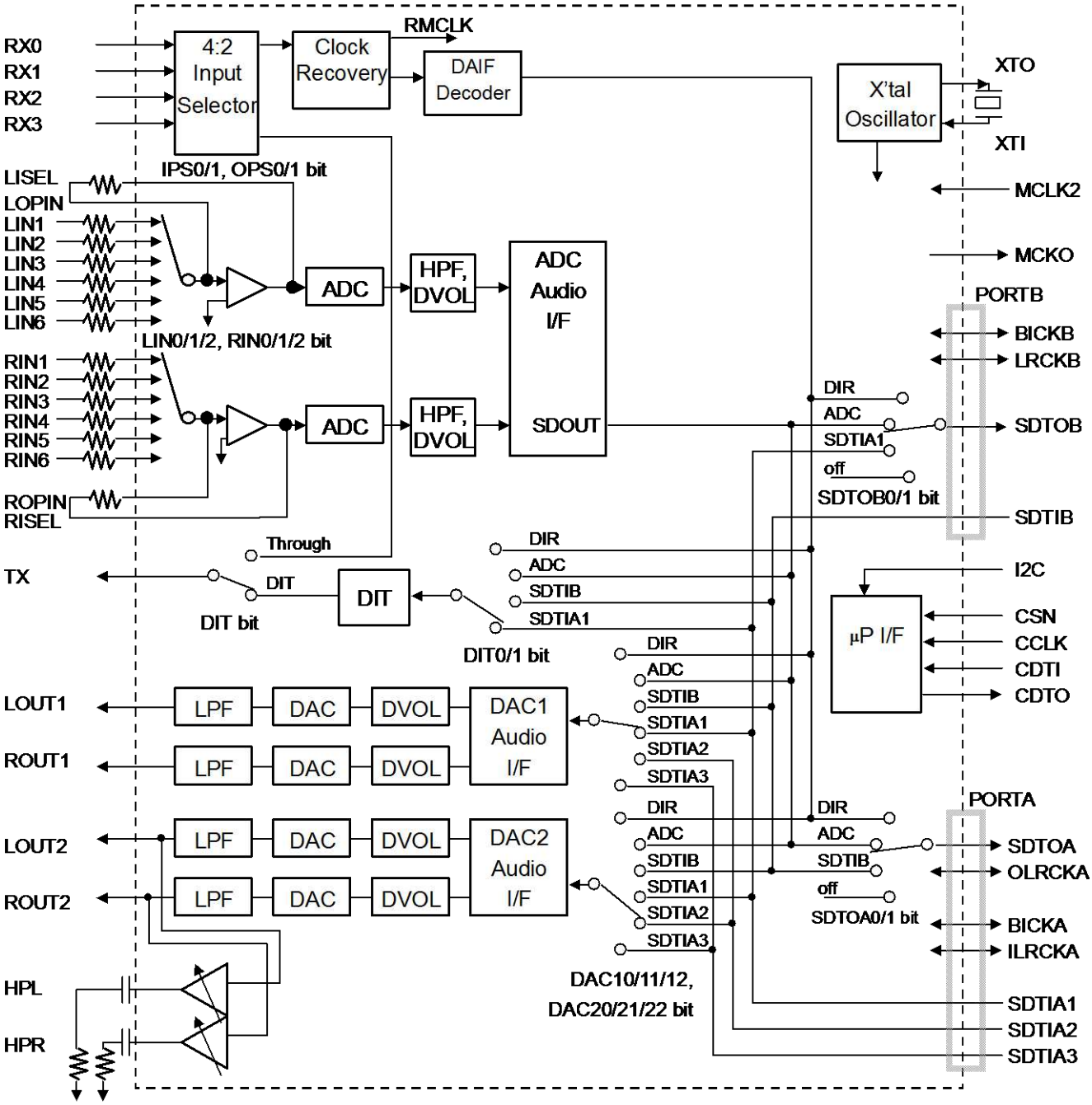
☐ DIR/DIT Part
- AES3, IEC60958, S/PDIF, EIAJ CP1201 Compatible
- Low jitter Analog PLL
- PLL Lock Range : 32kHz to 192kHz
- Clock Source: PLL or X'tal
- 4-channel Receiver input
- 1-channel Transmission output (Through output or DIT)
- Auxiliary digital input
- De-emphasis for 32kHz, 44.1kHz, 48kHz and 96kHz
- Detection Functions
  - Non-PCM Bit Stream Detection
  - DTS-CD Bit Stream Detection
  - Sampling Frequency Detection
    (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz, 192kHz)
  - Unlock & Parity Error Detection
  - Validity Flag Detection
- Up to 24bit Audio Data Format
- 40-bit Channel Status Buffer
- Burst Preamble bit Pc and Pd Buffer for Non-PCM bit stream
- Q-subcode Buffer for CD bit stream

☐ TTL Level Digital I/F
☐ External Master Clock Input:
- 256fs, 384fs, 512fs (fs=32kHz ~ 48kHz)
- 128fs, 192fs, 256fs (fs=64kHz ~ 96kHz)
- 128fs (fs=120kHz ~ 192kHz)

☐ Master Clock Output: 128fs/256fs/384fs/512fs
☐ 2 Audio Serial I/F (PORTA, PORTB)
- Master/Slave mode
- I/F format
  PORTA: Left/Right(20/24 bit) justified, I^2S, TDM
  PORTB: Left/Right(20/24 bit) justified, I^2S

☐ 4-wire Serial and I^2C Bus μP I/F for mode setting
☐ Operating Voltage: 4.5 to 5.5V
☐ Power Supply for output buffer: 2.7 to 5.5V
☐ 64pin LQFP Package (0.5mm pitch)

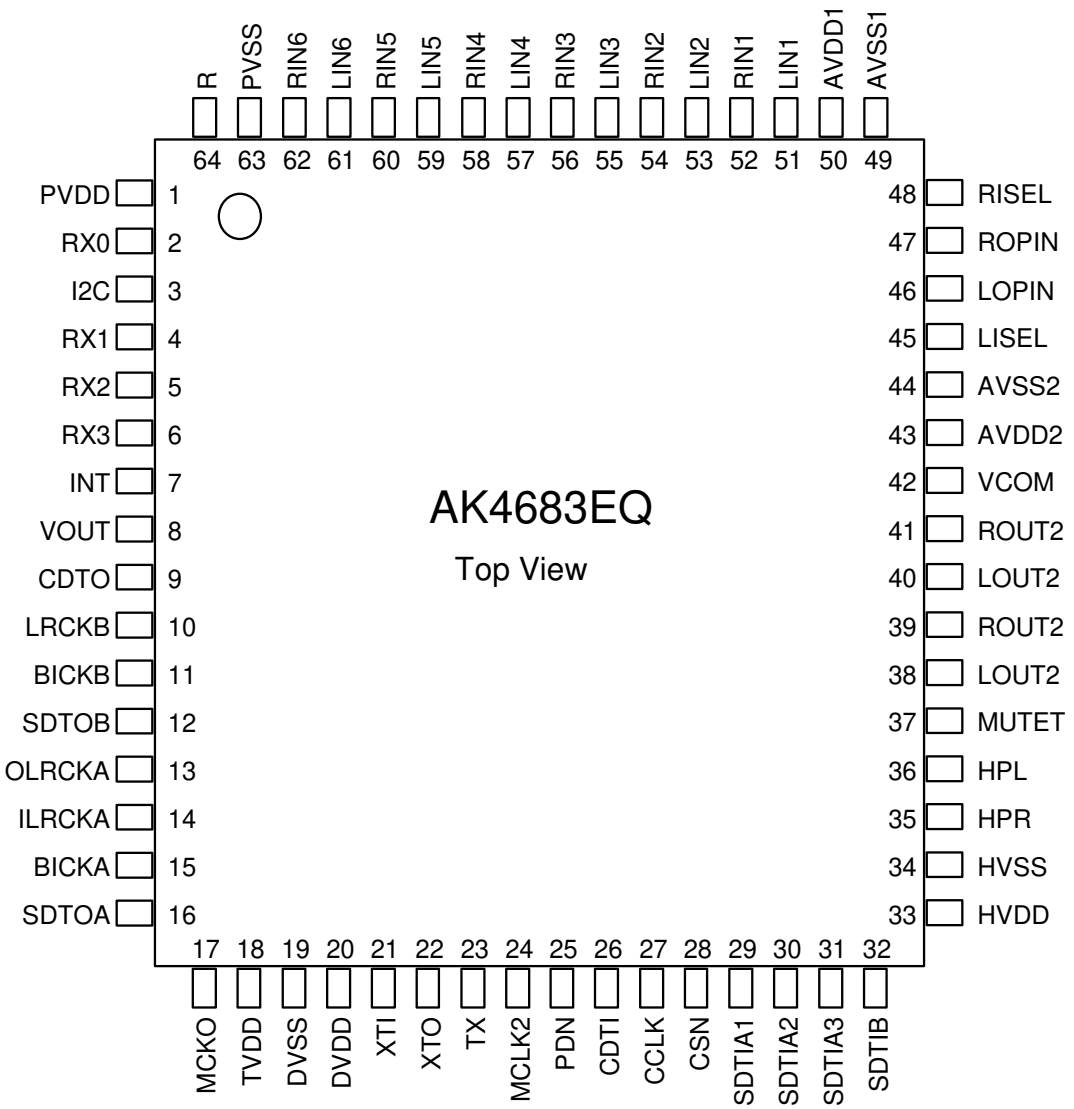
■ Block Diagram



■ Ordering Guide

AK4683EQ	-20 ~ +85°C	64pin LQFP (0.5mm pitch)
AKD4683	Evaluation Board for AK4683	

■ Pin Layout



■ Compatibility with AK4588

Functions	AK4588	AK4683
DAC, ADC Asynchronous operation	NOT Available	Available
DAC ch#	8ch	4ch
HP-Amp	-	2ch
ADC Input selector	-	6:1

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	PVDD	-	PLL Power supply Pin, 4.5V~5.5V
2	RX0	I	Receiver Channel 0 Pin (Internal biased pin. Internally biased at PVDD/2)
3	I2C	I	Control Mode Select Pin. "L": 4-wire Serial, "H": I^2C Bus
4	RX1	I	Receiver Channel 1 Pin
5	RX2	I	Receiver Channel 2 Pin
6	RX3	I	Receiver Channel 3 Pin
7	INT	O	Interrupt Pin
8	VOUT	O	V-bit Output Pin for Receiver Input
	DZF	O	Zero Input Detect Pin When the input data of DAC follow total 8192 LRCK cycles with "0" input data, this pin goes to "H". And when RSTN1 bit is "0", PWDA bit is "0", this pin goes to "H".
	OVF	O	Analog Input Overflow Detect Pin This pin goes to "H" if the analog input of Lch or Rch overflows.
9	CDTO	O	Control Data Output Pin in Serial Mode and I2C pin = "L".
10	LRCKB	I/O	Channel Clock B Pin
11	BICKB	I/O	Audio Serial Data Clock B Pin
12	SDTOB	O	Audio Serial Data Output B Pin
13	OLRCKA	I/O	Output Channel Clock A Pin
14	ILRCKA	I/O	Input Channel Clock A Pin
15	BICKA	I/O	Audio Serial Data Clock A Pin
16	SDTOA	O	Audio Serial Data Output A Pin
17	MCKO	O	Master Clock Output Pin
18	TVDD	-	Output Buffer Power Supply Pin, 2.7V~5.5V
19	DVSS	-	Digital Ground Pin, 0V
20	DVDD	-	Digital Power Supply Pin, 4.5V~5.5V
21	XTI	I	X'tal Input Pin
22	XTO	O	X'tal Output Pin
23	TX	O	Transmit Channel Output pin When DIT bit = "0", RX0~3 Through. When DIT bit = "1", Internal DIT Output.
24	MCLK2	I	Master Clock Input Pin
25	PDN	I	Power-Down Mode & Reset Pin When "L", the AK4683 is powered-down, all registers are reset. And then all digital output pins go "L". The AK4683 must be reset once upon power-up.
26	CDTI	I	Control Data Input Pin in Serial Mode and I2C pin = "L".
	SDA	I/O	Control Data Pin in Serial Mode and I2C pin = "H".
27	CCLK	I	Control Data Clock Pin in Serial Mode and I2C pin = "L"
	SCL	I	Control Data Clock Pin in Serial Mode and I2C pin = "H"
28	CSN	I	Chip Select Pin in Serial Mode and I2C pin = "L".
	TEST	I	This pin should be connected to DVSS in Serial Mode and I2C pin = "H".
29	SDTIA1	I	Audio Serial Data Input A1 Pin
30	SDTIA2	I	Audio Serial Data Input A2 Pin
31	SDTIA3	I	Audio Serial Data Input A3 Pin
32	SDTIB	I	Audio Serial Data Input B Pin
33	HVDD	-	HP Power Supply Pin, 4.5V~5.5V
34	HVSS	-	HP Ground Pin, 0V
35	HPR	O	HP Rch Output Pin
36	HPL	O	HP Lch Output Pin
37	MUTET	-	HP Common Voltage Output Pin 1μF capacitor should be connected to HVSS externally.

No.	Pin Name	I/O	Function
38	LOUT2	O	DAC2 Lch Positive Analog Output Pin
39	ROUT2	O	DAC2 Rch Positive Analog Output Pin
40	LOUT1	O	DAC1 Lch Positive Analog Output Pin
41	ROUT1	O	DAC1 Rch Positive Analog Output Pin
42	VCOM	-	DAC/ADC Common Voltage Output Pin 2.2μF capacitor should be connected to AVSS2 externally.
43	AVDD2	-	DAC Power Supply Pin, 4.5V~5.5V
44	AVSS2	-	DAC Ground Pin, 0V
45	LISEL	O	Lch Feedback Resistor Output Pin
46	LOPIN	O	Lch Feedback Resistor Input Pin. 0.5 x AVDD1.
47	ROPIN	O	Rch Feedback Resistor Input Pin. 0.5 x AVDD1.
48	RISEL	O	Rch Feedback Resistor Output Pin
49	AVSS1	-	ADC Ground Pin, 0V
50	AVDD1	-	ADC Power Supply Pin, 4.5V~5.5V
51	LIN1	I	Lch Input 1 Pin
52	RIN1	I	Rch Input 1 Pin
53	LIN2	I	Lch Input 2 Pin
54	RIN2	I	Rch Input 2 Pin
55	LIN3	I	Lch Input 3 Pin
56	RIN3	I	Rch Input 3 Pin
57	LIN4	I	Lch Input 4 Pin
58	RIN4	I	Rch Input 4 Pin
59	LIN5	I	Lch Input 5 Pin
60	RIN5	I	Rch Input 5 Pin
61	LIN6	I	Lch Input 6 Pin
62	RIN6	I	Rch Input 6 Pin
63	PVSS	-	PLL Ground pin
64	R	-	External Resistor Pin 12kΩ +/-1% resistor should be connected to PVSS externally.

Note: All input pins except internal biased pin (RX0) and analog input pins (LIN1-6, RIN1-6) should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	RX0, LOUT1-2, ROUT1-2, LIN1-6, RIN1-6	These pins should be open.
Digital	INT, XTO, MCKO, VOUT/DZF/OVF, SDTOA-B, CDTO, TX	These pins should be open.
	RX1-3, CSN, CCLK, CDTI, XTI, MCLK2, OLRCKA, ILRCKA, BICKA, SDTIA1-3, LRCKB, BICKB, SDTIB	These pins should be connected to DVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS1, AVSS2, DVSS, PVSS, HVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	ADC Analog	AVDD1	-0.3	6.0	V
	DAC Analog	AVDD2	-0.3	6.0	V
	Headphone Analog	HVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	PLL	PVDD	-0.3	6.0	V
	Output buffer	TVDD	-0.3	6.0	V
	|AVSS2-AVSS1| (Note 2)	ΔGND1	-	0.3	V
	|AVSS2-DVSS| (Note 2)	ΔGND2	-	0.3	V
	|AVSS2-PVSS| (Note 2)	ΔGND3	-	0.3	V
	|AVSS2-HVSS| (Note 2)	ΔGND4	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (LIN, RIN pins)		VINA	-0.3	AVDD1+0.3	V
Digital Input Voltage					
	Except for ILRCKA, OLRCKA, LRCKB, BICKA-B, RX0, I2C pins	VIND1	-0.3	DVDD+0.3	V
	ILRCKA, OLRCKA, LRCKB, BICKA-B pins	VIND2	-0.3	TVDD+0.3	V
	RX0, I2Cpins	VIND3	-0.3	PVDD+0.3	V
Ambient Temperature (power applied)		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS, DVSS and PVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS, PVSS=0V; Note 3)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 4)	ADC Analog	AVDD1	4.5	5.0	5.5	V
	DAC Analog	AVDD2	4.5	5.0	5.5	V
	Headphone Analog	HVDD	AVDD2	5.0	5.5	V
	Digital	DVDD	4.5	5.0	5.5	V
	PLL	PVDD	4.5	5.0	5.5	V
	Output buffer	TVDD	2.7	5.0	DVDD	V
	|DVDD - AVDD1|	ΔVDD1	-0.3	0	+0.3	V
	|DVDD - AVDD2|	ΔVDD2	-0.3	0	+0.3	V
	|DVDD - HVDD|	ΔVDD3	-0.3	0	+0.3	V
	|DVDD - PVDD|	ΔVDD4	-0.3	0	+0.3	V
	|AVDD1 – AVDD2|	ΔVDD5	-0.1	0	+0.1	V

Note 3. All voltages with respect to ground.
Note 4. The power up sequences among AVDD1, AVDD2, DVDD, PVDD, HVDD and TVDD are not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD1, AVDD2, HVDD, DVDD, PVDD, TVDD=5V; AVSS1, AVSS2, HVSS, DVSS, PVSS=0V; fs=48kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at fs=48kHz, 20Hz~40kHz at fs=96kHz; 20Hz~40kHz at fs=192kHz, all blocks are synchronized, unless otherwise specified)

Parameter		min	typ	max	Units
Pre-Amp Characteristics:					
Feedback Resistance		10		50	kΩ
S/(N+D)	(Note 5)	-	100		dB
S/N	(A-weighted) (Note 5)	-	108		dB
Load Capacitance				20	pF
ADC Analog Input Characteristics (Note 6)					
Resolution				24	Bits
S/(N+D) (-0.5dBFS)	fs=48kHz	84	92		dB
	fs=96kHz	-	86		dB
DR (-60dBFS)	fs=48kHz, A-weighted	92	100		dB
	fs=96kHz	-	96		dB
	fs=96kHz, A-weighted	-	100		dB
S/N (Note 7)	fs=48kHz, A-weighted	92	100		dB
	fs=96kHz	-	96		dB
	fs=96kHz, A-weighted	-	100		dB
Interchannel Isolation	(Note 8)	90	105		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			50	-	ppm/°C
Input Voltage (Note 6)	AIN=1.22xAVDD1	5.7	6.1	6.5	Vpp
Power Supply Rejection	(Note 9)		50		dB
DAC Analog Output Characteristics					
Resolution				24	Bits
S/(N+D)	fs=48kHz	80	90		dB
	fs=96kHz	-	88		dB
	fs=192kHz	-	88		dB
DR (-60dBFS)	fs=48kHz, A-weighted	95	106		dB
	fs=96kHz	-	100		dB
	fs=96kHz, A-weighted	-	106		dB
	fs=192kHz	-	100		dB
	fs=192kHz, A-weighted	-	106		dB
S/N (Note 10)	fs=48kHz, A-weighted	95	106		dB
	fs=96kHz	-	100		dB
	fs=96kHz, A-weighted	-	106		dB
	fs=192kHz	-	100		dB
	fs=192kHz, A-weighted	-	106		dB
Interchannel Isolation		90	110		dB
Interchannel Gain Mismatch			0.2	0.5	dB
Gain Drift			50	-	ppm/°C
Output Voltage	AOUT=0.6xAVDD2	2.75	3.0	3.25	Vpp
Load Resistance	(AC Load)	5			kΩ
Load Capacitance				30	pF
Power Supply Rejection	(Note 9)		50		dB

Analog Volume Characteristics (OPGA):					
Step Size:	+0dB ~ -16dB	0.1	1	-	dB
	-16dB ~ -38dB	0.1	2	-	dB
	-38dB ~ -50dB	-	4	-	dB
Headphone-Amp Characteristics: DAC → HPL/HPR pins, RL=16Ω					
Output Voltage	(0.506xHVDD)	1.94	2.43	2.92	Vpp
S/(N+D)	(–3dBFS)	-	70	-	dBFS
S/N	(A-weighted)	-	90	-	dB
Interchannel Isolation		-	80	-	dB
Interchannel Gain Mismatch		-	0.1	0.5	dB
Load Resistance		16	-	-	Ω
Load Capacitance	C1 in Figure 1	-	-	30	pF
	C2 in Figure 1	-	-	300	pF
Power Supplies					
Power Supply Current					
Normal Operation (PDN pin = "H")	(Note 11)				
AVDD1+ AVDD2	fs=48kHz, fs=96kHz		37	52	mA
	fs=192kHz		19	27	mA
HVDD			7	10	mA
PVDD			8	11	mA
DVDD+TVDD	fs=48kHz (Note 12)		35	49	mA
	fs=96kHz		45	63	mA
	fs=192kHz		55	77	mA
Power-down mode (PDN pin = "L")	(Note 13)		80	200	μA

Note 5. Measured at LISEL/RISEL pins when the input resistor=47kohm, the feedback resistor=24kohm and input level =2Vrms.
Note 6. Measured through Pre-Amp -> ADC. Input resistor=47kohm, feedback resistor=24kohm.
Note 7. S/N measured by CCIR-ARM is 96dB(@fs=48kHz).
Note 8. This value is the interchannel isolation between all the channels of the LIN1-6 and RIN1-6.
Note 9. PSR is applied to AVDD, DVDD, PVDD and TVDD with 1kHz, 50mVpp.
Note 10. S/N measured by CCIR-ARM is 102dB(@fs=48kHz).
Note 11. C_L=20pF, X'tal=24.576MHz, CM1-0="10", CM1-0="10", OCKS1-0="10"@48kHz,"00"@96kHz, "11"@192kHz. Headphone = No output. The resister network is attached to TX pin.
Note 12. TVDD=6mA(typ@fs=48kHz), 7mA(typ@fs=96kHz), 10mA(typ@fs=192kHz).
Note 13. In the power-down mode. RX0 input is open and all digital input pins including clock pins (MCLK2, BICKA, BICKB, ILRCKA, OLRCKA, BICKB pins) and RX1-3 pins are held DVSS

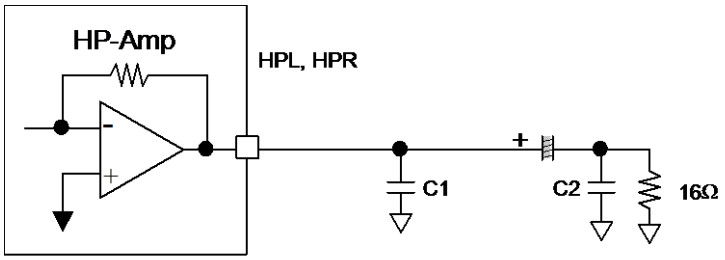


Figure 1. Headphone Amplifier output circuit

FILTER CHARACTERISTICS

(Ta=25°C; AVDD1, AVDD2, DVDD, PVDD, HVDD=4.5~5.5V; TVDD=2.7~5.5V; fs=48kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 14)	±0.1dB	PB	0		18.9	kHz
	-0.2dB		-	20.0	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband		SB	28.0			kHz
Passband Ripple		PR			±0.04	dB
Stopband Attenuation		SA	68			dB
Group Delay (Note 15)		GD		19		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 14)	-3dB	FR		1.0		Hz
	-0.1dB			6.5		Hz
DAC Digital Filter:						
Passband (Note 14)	-0.1dB	PB	0		21.8	kHz
	-6.0dB		-	24.0	-	kHz
Stopband		SB	26.2			kHz
Passband Ripple		PR			±0.02	dB
Stopband Attenuation		SA	54			dB
Group Delay (Note 15)		GD		21		1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response: 0 ~ 20.0kHz		FR		±0.2		dB
40.0kHz (Note 16)		FR		±0.3		dB
80.0kHz (Note 16)		FR		±1.0		dB

Note 14. The passband and stopband frequencies are proportional to fs.
For example, 21.8kHz at –0.1dB is 0.454 x fs (DAC). The reference frequency of these responses is 1kHz.

Note 15. The calculating delay time which occurred by digital filtering. This time is from setting the input of analog signal to setting the 24bit data of both channels to the output register of PORTA or PORTB.
For DAC, this time is from setting the 20/24bit data of both channels on input register of PORTA or PORTB to the output of analog signal.

Note 16. 40kHz@fs=96kHz, 80kHz@fs=192kHz

DC CHARACTERISTICS

(Ta=25°C; AVDD1, AVDD2, DVDD, PVDD, HVDD=4.5~5.5V; TVDD=2.7~5.5V)

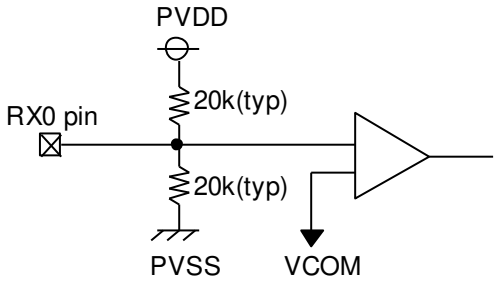
Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage (Except XTI pin)	VIH	2.2	-	-	V
(XTI pin)	VIH	70%DVDD	-	-	V
Low-Level Input Voltage (Except XTI pin)	VIL	-	-	0.8	V
(XTI pin)	VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling (XTI pin) (Note 17)	VAC	40%DVDD	-	-	Vpp
High-Level Output Voltage					
(Except TX pins: Iout=-400μA)	VOH	TVDD-0.4	-	-	V
(TX pin: Iout=-400μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage (Iout=400μA)	VOL	-		0.4	V
Input Leakage Current (Except RX0 pin)	Iin	-	-	±10	μA

Note 17. In case of connecting capacitance to XTI pin.

S/PDIF RECEIVER CHARACTERISTICS (RX0)

(Ta=25°C; AVDD1, AVDD2, DVDD, PVDD, HVDD=4.5~5.5V; TVDD=2.7~5.5V)

Parameter	Symbol	min	typ	max	Units
Input Resistance	Zin		10		kΩ
Input Voltage (internally biased at PVDD/2)	VTH	200			mVpp
Input Hysteresis	VHY	-	50		mV
Input Sample Frequency	fs	32	-	192	kHz



Internal biased pin Circuit

S/PDIF RECEIVER CHARACTERISTICS (RX1-3)

(Ta=25°C; AVDD1, AVDD2, DVDD, PVDD, HVDD=4.5~5.5V;TVDD=2.7~5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-		V
Low-Level Input Voltage	VIL	-	-	0.8	V
Input Sample Frequency	fs	32	-	192	kHz
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD1, AVDD2, DVDD, PVDD, HVDD=4.5~5.5V; TVDD=2.7~5.5V; C_L=20pF; Note 18)

Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Crystal Resonator	Frequency	fXTAL	11.2896		24.576	MHz
External Clock	Frequency	fECLK	4.096		24.576	MHz
	Duty	dECLK	40	50	60	%
MCKO Output	Frequency	fMCK	4.096		24.576	MHz
	Duty (Note 19)	dMCLK	40	50	60	%
	(Note 20)	dMCK		33		%
PLL Clock Recover Frequency (RX0-3)		fpll	32	-	192	kHz
Master Clock						
256fsn, 128fsd:		fCLK	8.192		12.288	MHz
Pulse Width Low		tCLKL	27			ns
Pulse Width High		tCLKH	27			ns
384fsn, 192fsd:		fCLK	12.288		18.432	MHz
Pulse Width Low		tCLKL	20			ns
Pulse Width High		tCLKH	20			ns
512fsn, 256fsd, 128fsq:		fCLK	16.384		24.576	MHz
Pulse Width Low		tCLKL	15			ns
Pulse Width High		tCLKH	15			ns
LRCKA (LRCKB) Timing (Slave Mode)						
Normal mode						
Normal Speed Mode		fsn	32		48	kHz
Double Speed Mode		fsd	64		96	kHz
Quad Speed Mode		fsq	120		192	kHz
Duty Cycle		Duty	45		55	%
TDM 256 mode						
LRCKA frequency		fsd	32		48	kHz
"H" time		tLRH	1/256fs			ns
"L" time		tLRL	1/256fs			ns
TDM 128 mode						
LRCKA frequency		fsd	64		96	kHz
"H" time		tLRH	1/128fs			ns
"L" time		tLRL	1/128fs			ns
LRCKA (LRCKB) Timing (Master Mode)						
Normal mode						
Normal Speed Mode		fsn	32		48	kHz
Double Speed Mode		fsd	64		96	kHz
Quad Speed Mode		fsq	120		192	kHz
Duty Cycle		Duty		50		%
TDM 256 mode						
LRCKA frequency		fsn	32		48	kHz
"H" time	(Note 21)	tLRH		1/8fs		ns
TDM 128 mode						
LRCKA frequency		fsd	64		96	kHz
"H" time	(Note 21)	tLRH		1/4fs		ns
Power-down & Reset Timing						
PDN Pulse Width	(Note 22)	tPD	150			ns
PDN "↑" to SDTO valid	(Note 23)	tPDV		522		1/fs

Note 18. SDTOA is specified against OLRCKA, SDTIA1-3 are measured against ILRCKA.
Note 19. When MCKO1-0 bits = "01", "10" or MCKO1-0 bits = "00" and CKSDT bit = "0".
Note 20. When MCKO1-0 bits = "00" and CKSDT bit = "1" and the EXTCLK is selected by CM1-0 bits.
Duty = ("H" width) / (clock cycle) x 100
Note 21. "L" time at I^2S format
Note 22. The AK4683 can be reset by bringing PDN "L" to "H" upon power-up.
Note 23. These cycles are the number of LRCKA (LRCKB) rising from PDN rising.

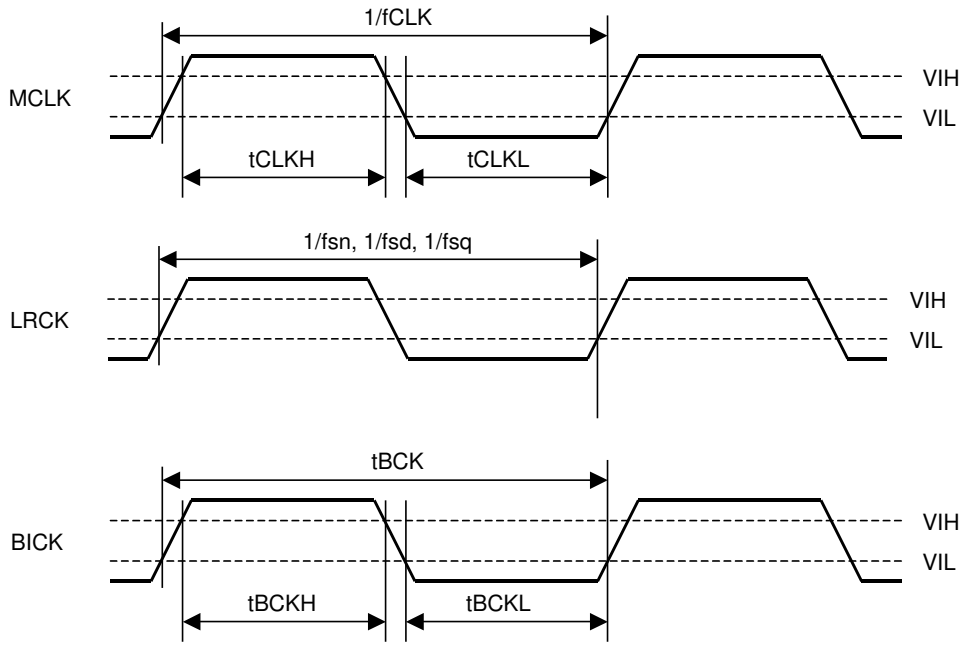
Parameter	Symbol	min	typ	max	Units
Audio Interface Timing (Slave Mode)					
Normal mode					
BICKA (BICKB) Period	tBCK	81			ns
BICKA (BICKB) Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCKA (LRCKB) Edge to BICKA (BICKB) "↑" (Note 24)	tLRB	20			ns
BICKA (BICKB) "↑" to LRCKA (LRCKB) Edge (Note 24)	tBLR	20			ns
LRCKA (LRCKB) to SDTOA, SDTOB (MSB)	tLRS			20	ns
BICKA (BICKB) "↓" to SDTOA, SDTOB	tBSD			20	ns
SDTIA1-3, SDTIB Hold Time	tSDH	20			ns
SDTIA1-3, SDTIB Setup Time	tSDS	20			ns
TDM 256 mode					
BICKA Period	tBCK	81			ns
BICKA Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCKA Edge to BICKA "↑" (Note 24)	tLRB	20			ns
BICKA "↑" to LRCKA Edge (Note 24)	tBLR	20			ns
BICKA "↓" to SDTOA	tBSD			20	ns
SDTIA1 Hold Time	tSDH	10			ns
SDTIA1 Setup Time	tSDS	10			ns
TDM 128 mode					
BICKA Period	tBCK	81			ns
BICKA Pulse Width Low	tBCKL	32			ns
Pulse Width High	tBCKH	32			ns
LRCKA Edge to BICKA "↑" (Note 24)	tLRB	20			ns
BICKA "↑" to LRCKA Edge (Note 24)	tBLR	20			ns
BICKA "↓" to SDTOA	tBSD			20	ns
SDTIA1-2 Hold Time	tSDH	10			ns
SDTIA1-2 Setup Time	tSDS	10			ns
Audio Interface Timing (Master Mode)					
Normal mode					
BICKA (BICKB) Frequency	fBCK		64fs		Hz
BICKA (BICKB) Duty	dBCK		50		%
BICKA (BICKB) "↓" to LRCKA (LRCKB) Edge	tMBLR	-20		20	ns
BICKA (BICKB)"↓" to SDTO	tBSD			20	ns
SDTIA1-3, B Hold Time	tSDH	20			ns
SDTIA1-3, B Setup Time	tSDS	20			ns
TDM 256 mode					
BICKA Frequency	fBCK		256fs		Hz
BICKA Duty (Note 25)	dBCK		50		%
BICKA "↓" to LRCKA Edge	tMBLR	-12		12	ns
BICKA "↓" to SDTOA	tBSD			20	ns
SDTIA1 Hold Time	tSDH	10			ns
SDTIA1 Setup Time	tSDS	10			ns
TDM 128 mode					
BICKA Frequency	fBCK		128fs		Hz
BICKA Duty (Note 26)	dBCK		50		%
BICKA "↓" to LRCKA Edge	tMBLR	-12		12	ns
BICKA "↓" to SDTOA	tBSD			20	ns
SDTIA1-2 Hold Time	tSDH	10			ns
SDTIA1-2 Setup Time	tSDS	10			ns

Note 24. BICK rising edge must not occur at the same time as LRCK edge.
Note 25. When MCLK2/XTI is 512fs, dBCK is guaranteed. When 384fs and 256fs, dBCK can not be guaranteed.
Note 26. When MCLK2/XTI is 256fs, dBCK is guaranteed. When 128fs, dBCK can not be guaranteed.

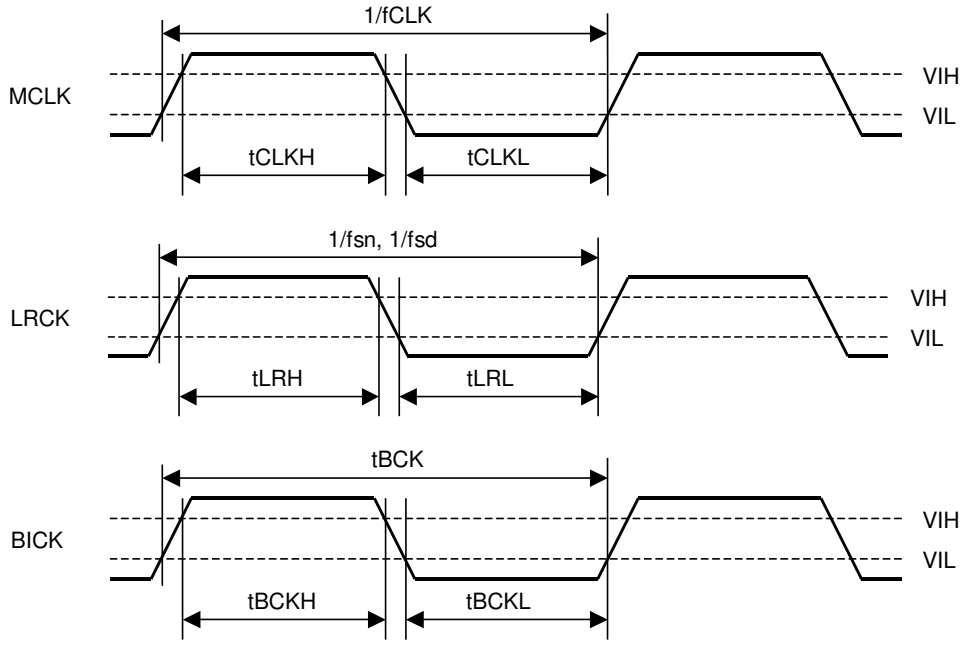
Parameter	Symbol	min	typ	max	Units
Control Interface Timing (4-wire serial mode)					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTI Setup Time	tCDS	50			ns
CDTI Hold Time	tCDH	50			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
CDTO Delay	tDCD			45	ns
CSN "↑" to CDTO Hi-Z	tCCZ			70	ns
Control Interface Timing (I^2C Bus mode)					
SCL Clock Frequency	fSCL	-		100	kHz
Bus Free Time Between Transmissions	tBUF	4.7		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	4.0		-	µs
Clock Low Time	tLOW	4.7		-	µs
Clock High Time	tHIGH	4.0		-	µs
Setup Time for Repeated Start Condition	tSU:STA	4.7		-	µs
SDA Hold Time from SCL Falling (Note 27)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.25		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	4.0		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF

Note 27. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 28. I^2C-bus is a trademark of NXP B.V.

■ Timing Diagram

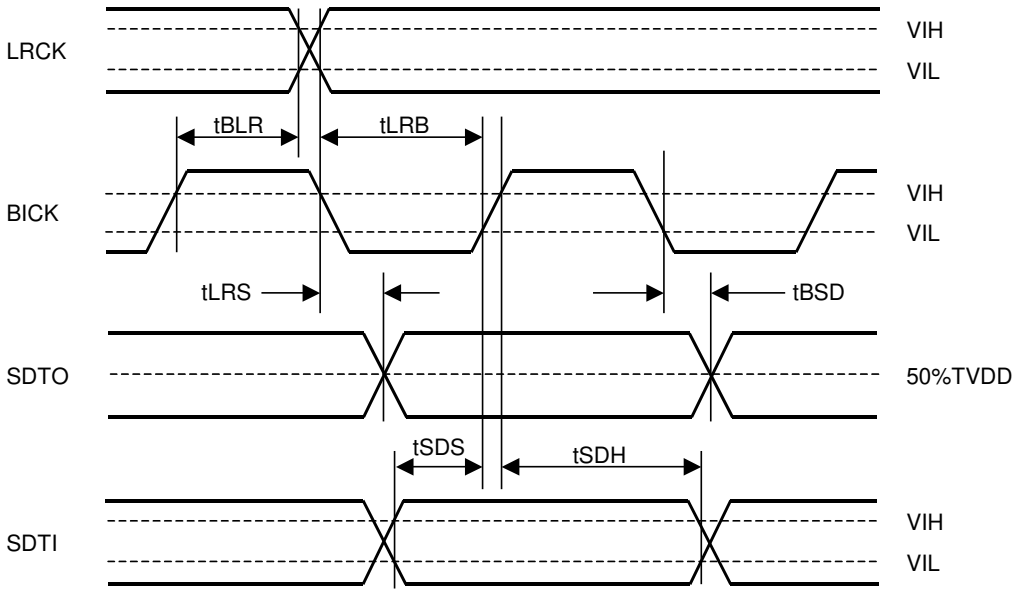


Clock Timing (Normal mode)

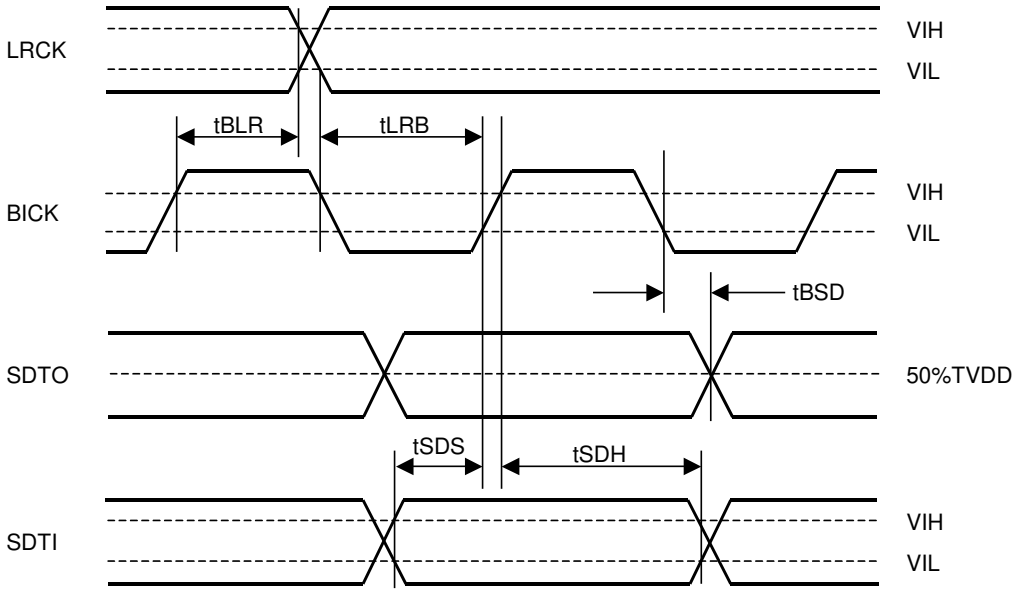


Clock Timing (TDM 256 mode, TDM 128 mode)

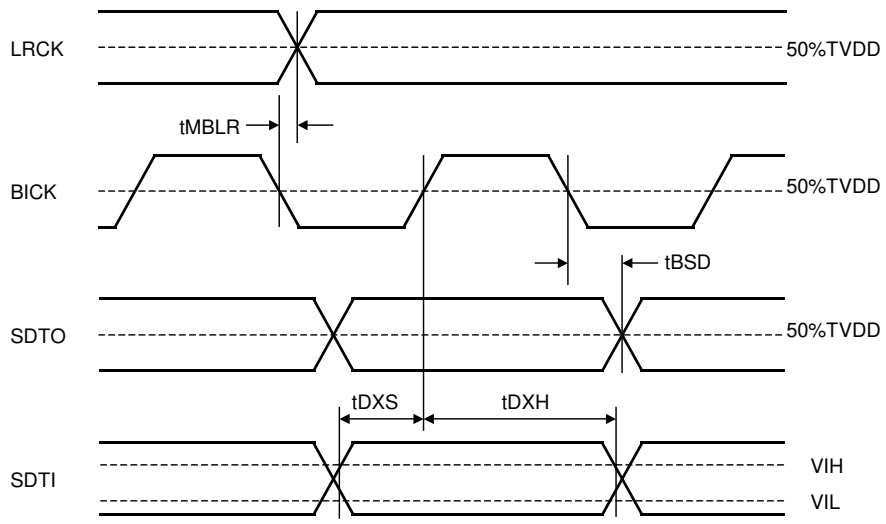
LRCK= LRCKB, ILRCKA, OLRCKA,
BICK= BICKA, BICKB,
SDTI= SDTIA, SDTIB,
SDTO= SDTOA, SDTOB.



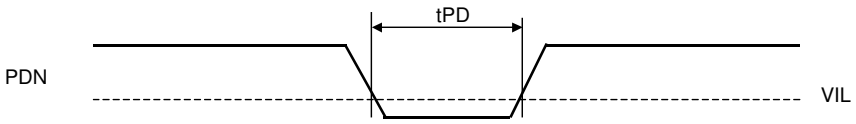
Audio Interface Timing (Normal mode)



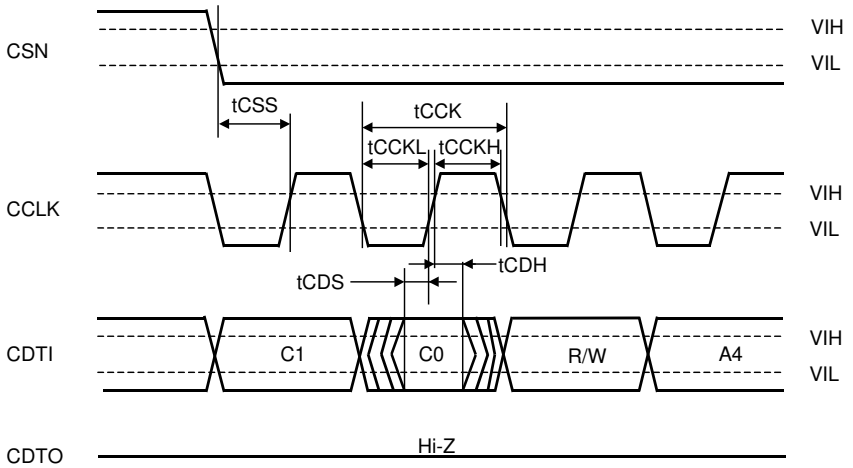
Audio Interface Timing (TDM 256 mode, TDM 128 mode)



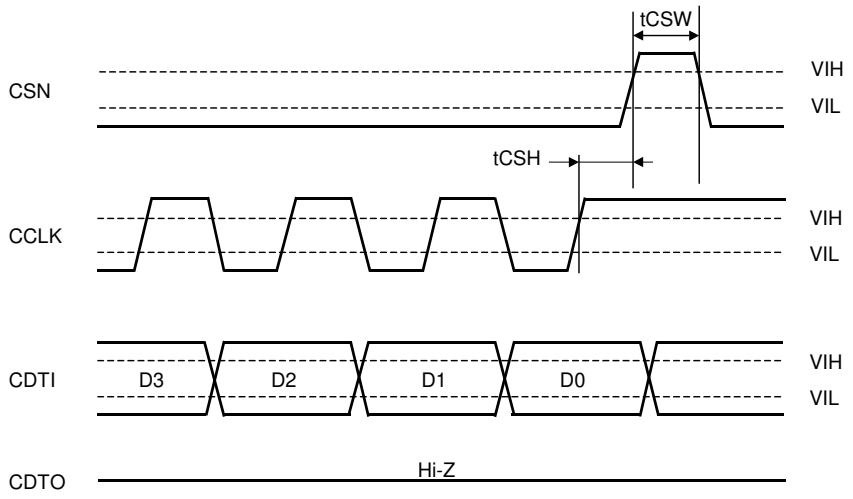
Audio Interface timing (Master Mode)



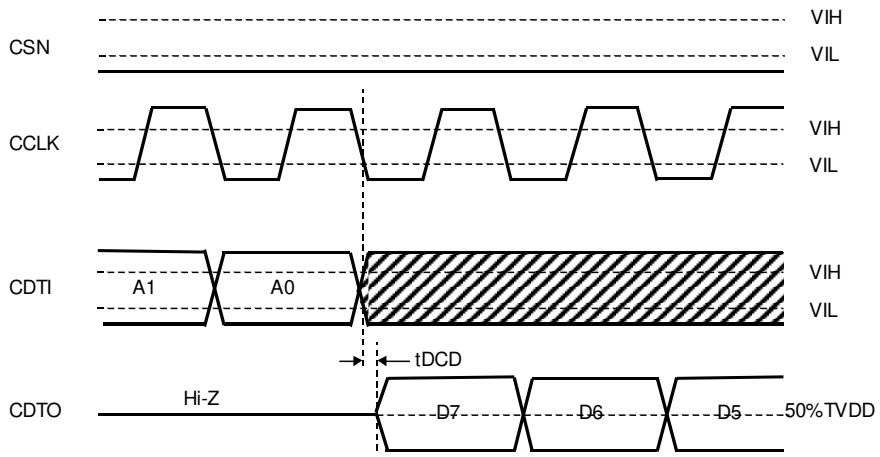
Power Down & Reset Timing



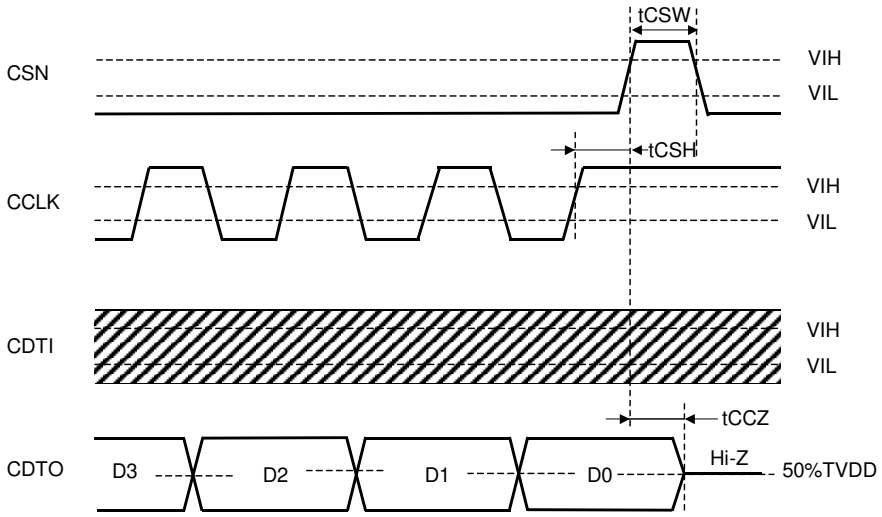
WRITE/READ Command Input Timing in 4-wire serial mode
The ADC/DAC part doesn't support READ command.



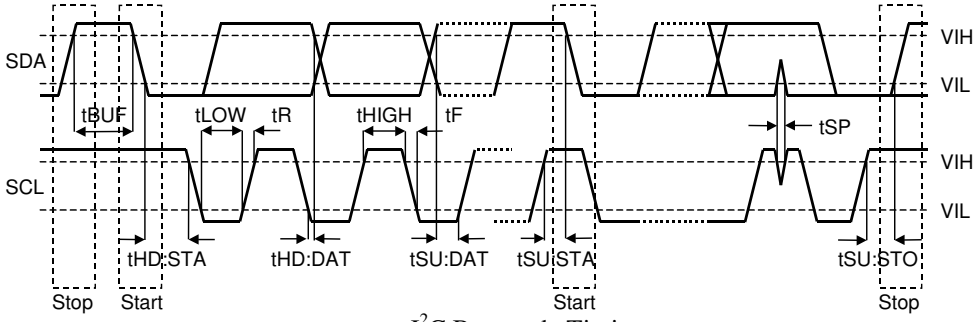
WRITE Data Input Timing in 4-wire serial mode



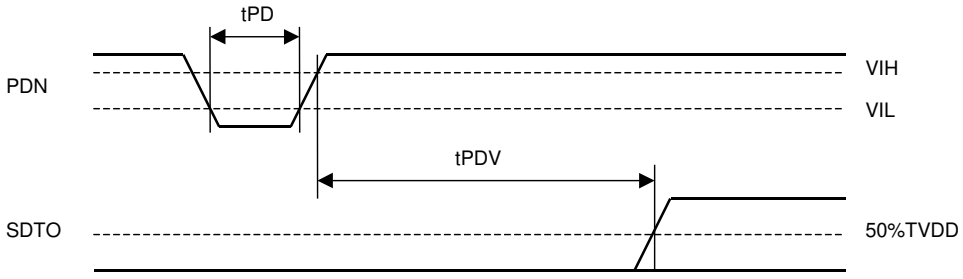
READ Data Output Timing 1 in 4-wire serial mode
The ADC/DAC part doesn't support READ command..



READ Data Input Timing 2 in 4-wire serial mode
The ADC/DAC part doesn't support READ command.



I^2C Bus mode Timing
The ADC/DAC part doesn't support READ command.



Power-down & Reset Timing

OPERATION OVERVIEW (General)

■ Device Configuration and System Clocks

The AK4683 integrates the stereo ADC with input selector, 4ch DAC with stereo HP amp, DIR and DIT. The AK4683 has two serial audio interfaces (PORTA, B) for two input/output dataset (Figure 2). Each block can independently select the operation clock from the three clock sources (recovered clock from DIR (RMCLK), X'tal clock (XTI) and external clock (MCLK2)) and also input data source/output data destination. By using the Clock Gen C, the loop-back such as AD-DA can operate even if the PORTA/B are powered down.

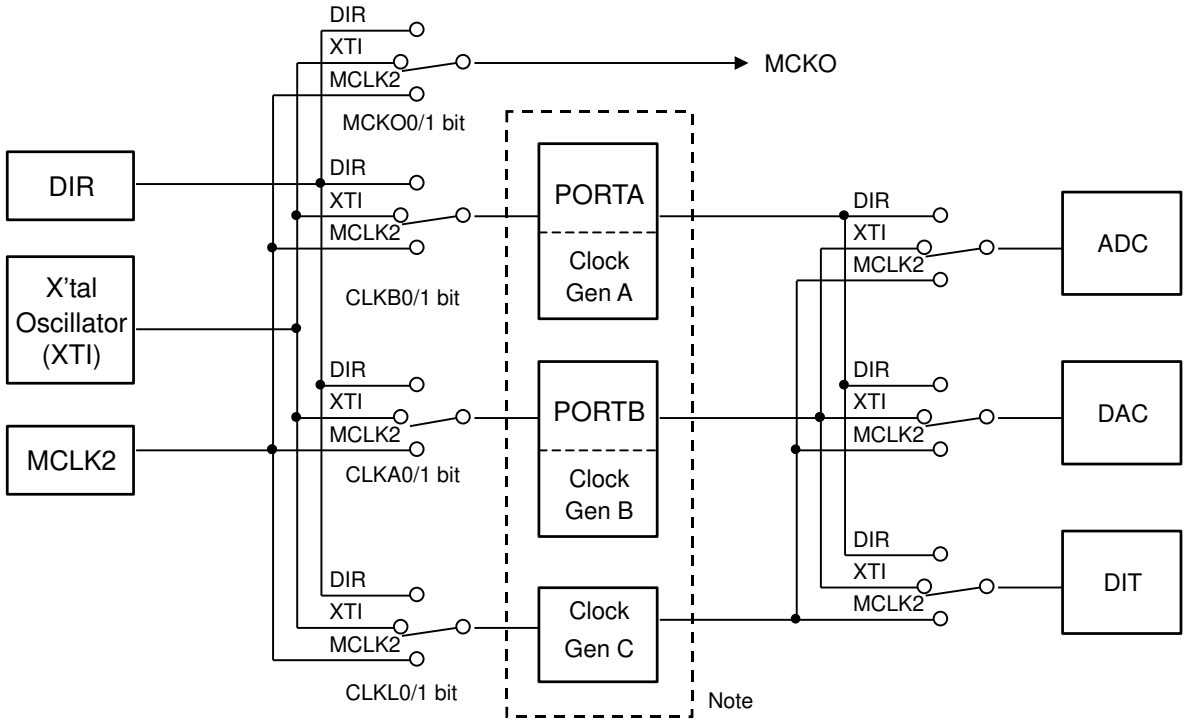


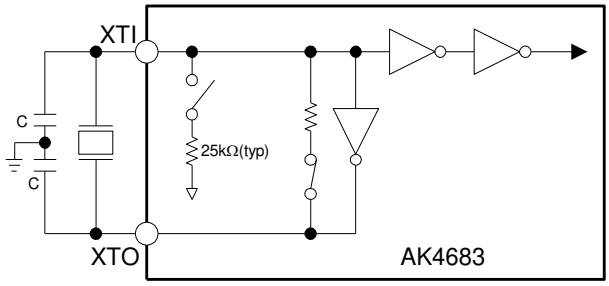
Figure 2. System Clock

Note: Each block must select the same clock source each other when connected. The operation will not be normal when the clock sources are not same among a connection. The ADC and DAC are synchronized to the clock source that the connected block uses. Even if the RMCLK is selected, the X'tal/MCLK2 may be chosen by the setting of CM1-0bits. DIR and DIT must be synchronized when these two blocks operates.

■ X'tal Oscillator

The following circuits are available to feed the clock to XTI pin of the AK4683.

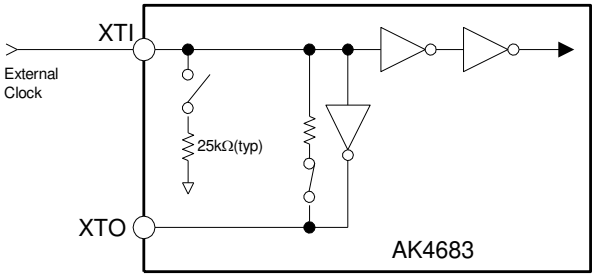
1) X'tal



Note: External capacitance depends on the crystal oscillator (Typ. 10-40pF)

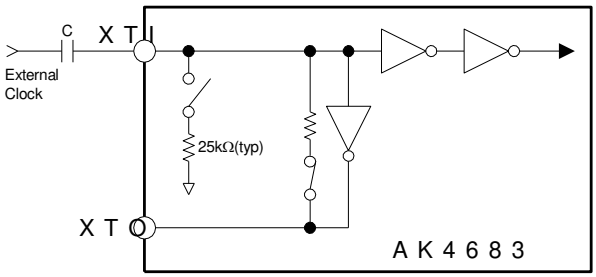
Figure 3. X'tal mode

2) External clock
- Note: Input clock must not exceed DVDD.



(Input: CMOS Level)

Figure 4. DC-coupled Input



(Input: ≥40%DVDD, C=0.1μF)

Figure 5. AC-coupled Input

3) XTI/XTO are not used

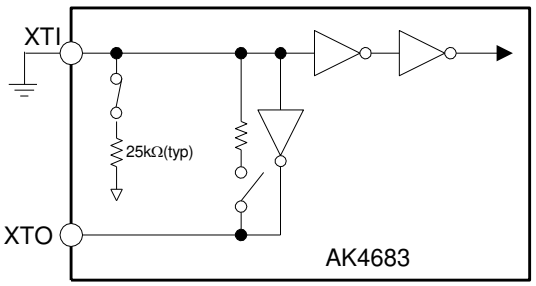


Figure 6. OFF mode

■ Master Clock Output

The AK4683 has one master clock output pin. The clock source can be selected from the three clocks (recovered clock from DIR (RMCLK), X'tal clock (XTI) and external clock (MCLK2)). When the DIR is powered-down or unlocked state at CM1/0 bit = "10", the CLKDT bit selects the clock source. The OCKS1/0 bits select the clock speed. The 512fs at fs=96kHz, 256fs/512fs at fs=192kHz are not available.

CM1 bit	CM0 bit	UNLOCK	Clock Source
0	0	-	RMCLK
0	1	-	EXTCLK
1	0	0	RMCLK
		1	EXTCLK
1	1	-	EXTCLK

Table 1. Clock Mode Control

CLKDT bit	Clock Source	
0	XTI	(default)
1	MCLK2	

Table 2. EXTCLK Control

OCKS1 bit	OCKS0 bit	MCLKO(RMCLK)	fs (max)
0	0	256fs	96 kHz
0	1	256fs	96 kHz
1	0	512fs	48 kHz
1	1	128fs	192 kHz

Table 3. MCLKO Speed

MCKO1 bit	MCKO0 bit	MCKO Clock Source	
0	0	DIR	
0	1	X'tal(XTI)	default
1	0	MCLK2	
1	1	Reserved	

Table 4. MCKO Clock Source Control

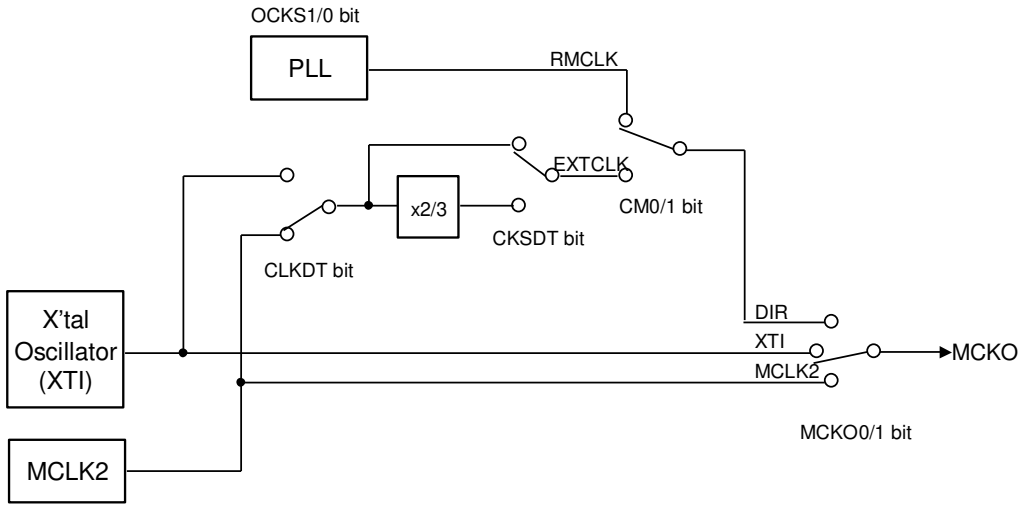


Figure 7. MCKO Clock

■ Master/Slave Mode Change

MSA and MSB bits control the master/slave mode of PORTA and PORTB respectively. The "1" is for master mode, "0" is for slave mode. The AK4683 is slave mode at power-down (PDN pin = "L"). To change to the master mode, write "1" to MSA/MSB bit. The ACKSAI, ACKSAO and ACKSB bits are ignored in master mode. Until when writing "1" to MSA/MSB bit, the ILRCKA, OLRCKA, BICKA, LRCKB and BICKB pin are input pins. Pull-up (or down) resistor with around 100kohm is required to prevent the floating of these input pins.

MSA, MSB bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 5. Select Master/Salve Mode

Note: When PORTA and PORTB operate synchronously, PORTB must not be the Master Mode. In that case the PORTA must be the Master Mode, or both PORTA and PORTB must be the Slave Mode with supplying the same BICK and LRCK.

■ Other Detection Function

The FUNC1-0 bit selects the function of VOUT / DZF / OVF pin.

Mode	FUNC1	FUNC0	Mode	
0	0	0	OFF ("L")	Default
1	0	1	ADC Overflow Detection	
2	1	0	DAC Zero Detection	
3	1	1	V bit output	

Table 6. Detection Function Control

1. Overflow Detection

The AK4683 has overflow detect function for analog input. OVF pin goes to "H" if analog input of Lch or Rch overflows (more than -0.3dBFS). OVF output for overflowed analog input has the same group delay as ADC (GD = 16/fs = 333μs @fs=48kHz). OVF pin is "L" for 522/fs (=10.9ms @fs=48kHz) after PDN = "↑", and then overflow detection is enabled. The overflow detection is applied to the data between the digital HPF and the DATT.

2. Zero Detection

The AK4683 has one pin for zero detect flag output. The DZFM1-0 bits select the channel grouping (Table 7). The DZF pin goes "H" when all of the enabled channels are continuously zeros for 8192 LRCK cycles. DZF pin immediately goes to "L" if input data of any enabled channel is not zero after going DZF "H".

Mode	DZFM1 bit	DZFM0 bit	AOUT				
			L1	R1	L2	R2	
0	0	0	Enable	Enable	Enable	Enable	(default)
1	0	1	Enable	Enable	-	-	
2	1	0	-	-	Enable	Enable	
3	1	1	-	-	-	-	

Table 7. Zero Detection Control

3. Validity Detection

The AK4683 has Validity Detection function. DIR decodes the V bit and output "H" via pin. When unlocked, "L" is output.

OPERATION OVERVIEW (ADC/DAC/PORTA, B part)

■ System Clock

The AK4683 has two audio serial interface (PORTA, B), can operate these PORTs with asynchronous. At each PORT, the external clocks, which are required to operate the AK4683, are MCLK, LRCK and BICK. The MCLK should be synchronized with LRCK but the phase is not critical.

The CLKA1-0, CLKB1-0bits select the clock sources for each PORT (Table 8, Table 9). The MSA and MSB bits select the master/slave mode (Table 16, Table 17).

The block that is connected to PORTA/B and the block that is connected to the PORT indirectly operate at the same clock as the PORTA/B selects. e. g. When the DAC selects the ADC data while the PORTB selects the ADC data also, the DAC operates same clock as the PORTB selects. The block that isn't connected to PORTA/B is automatically connected to the Clock Gen C and operates the same clock as the Clock Gen C selects with the CLKL1-0 bits (Table 10).

In master mode, the CKSIA2-0, OLRA1-0, BICKAF, CKSB2-0 bits select the clock frequency (Table 11, Table 12 , Table 13, Table 14). In master mode, external clock (MCLK) should always be supplied except in the power-down mode. The AK4683 is in power-down mode until MCLK will be supplied, when reset was canceled by Power-ON and so on. At PORTA, the input/output data has independent LRCK (ILRCKA/OLRCKA) and common BICK (BICKA). The ILRCK and OLRCK can operate at different sample rate but synchronized each other (Table 12).

In slave mode, external clocks (MCLK, BICK, LRCK) should always be present whenever the AK4683 is in normal operation mode (PDN pin = "H"). The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. If these clocks are not provided, the AK4683 may draw excess current because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4683 should be in the power-down mode (PDN pin = "L") or in the reset mode (RSTN1 bit = "0"). After exiting reset at power-up etc., the AK4683 is in the power-down mode until MCLK and LRCK are input.

When the block selects RMCLK as clock source, the sample rate of the PORT in the master mode or ADC/DAC connecting to the Clock Gen C is forced to the same rate as DIR. The DFSAD, DFSDA1-0 bits should be controlled properly.

Note: When PORTA and PORTB operate synchronously, PORTB must not be the in Master Mode. In that case the PORTA must be in the Master Mode, or both PORTA and PORTB must be in the Slave Mode with supplying the same BICK and LRCK.