Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AK4753

2-in, 4-out CODEC with DSP Functions

GENERAL DESCRIPTION

The AK4753 is a two input, four output audio CODEC with integrated digital signal processing. The outputs can be configured either as single-ended or differential. An internal PLL allows the chip to run in master clock free mode. The digital signal processing block includes an ALC/limiter, 5 configurable biquads for EQ, volume control, and 4th-order filters for each output channel to enable a variety of configurations. Wide dynamic range is achieved with 96dB S/N for the ADC, and 103dB S/N for the DAC's. A two-input 8-bit SAR ADC is integrated for processing of external potentiometers, supporting volume and bass control functions. A small external EEP-ROM is used to store the coefficient values for the DSP blocks. The AK4753 is controlled by an I^{2}C control interface.

FEATURES

- **Digital audio input interface**
  - **Data format: MSB-first, two's complement**
  - **16, 20, or 24-bits, I2S, MSB justified, LSB justified, or DSP mode**
  - **Audio sampling rates: 8kHz to 48kHz**
- **Analog audio input**
  - **Single-ended input stereo 24-bit audio ADC**
  - **S/N: 96dB S/(N+D): 85dB**
  - **Digital high-pass filter for DC-offset correction**
- **Analog audio output**
  - **Four-channel 24-bit audio DAC**
  - **Single-ended or differential output**
  - **S/N: 103dB S/(N+D): 88dB**
- **8-bit SAR ADC with two input selector**
- **Digital mixer for balancing inputs**
- **Digital signal processing block: DSP1, DSP2 independently**
  - **Configurable ALC / limiter function**
  - **Volume control: 0dB to -127dB, 0.5dB steps, mute**
  - **Pre-gain setting: 0dB, +6dB, +12dB, +18dB**
  - **Post-gain setting: 0dB, +3.5dB, +6dB, +8dB**
  - **Five programmable biquads for EQ**
  - **4th-order high-pass filter or low-pass filter**
- **Integrated PLL for master clock-free operation**
- **PLL**
  - **Input frequency: 24.576MHz, 24MHz, 22.5792MHz, 12.288MHz, 12MHz, and 11.2896MHz (XTI/MCKI pin)**
    1fs (LRCK pin), 32fs or 64fs (BICK pin)
  - **Input level: CMOS or AC-coupled (XTI/MCKI pin)**
- **Master clock input: 256fs, 512fs, 1024fs**
- **µP I/F: I^{2}C bus-slave (400kHz Fast-mode)**
- **EEP-ROM control I/F: I^{2}C bus-master (400kHz Fast-mode)**
- **Ta = -30 ~ +85°C**
- **Power supply:**
  Analog (AVDD): 3.0 ~ 3.6V (typ 3.3V)
  Digital (DVDD: 3.0 ~ 3.6V (typ 3.3V)
- **Package: 32 pin QFN (4 x 4 mm, 0.4mm pitch)**

■ Block Diagram

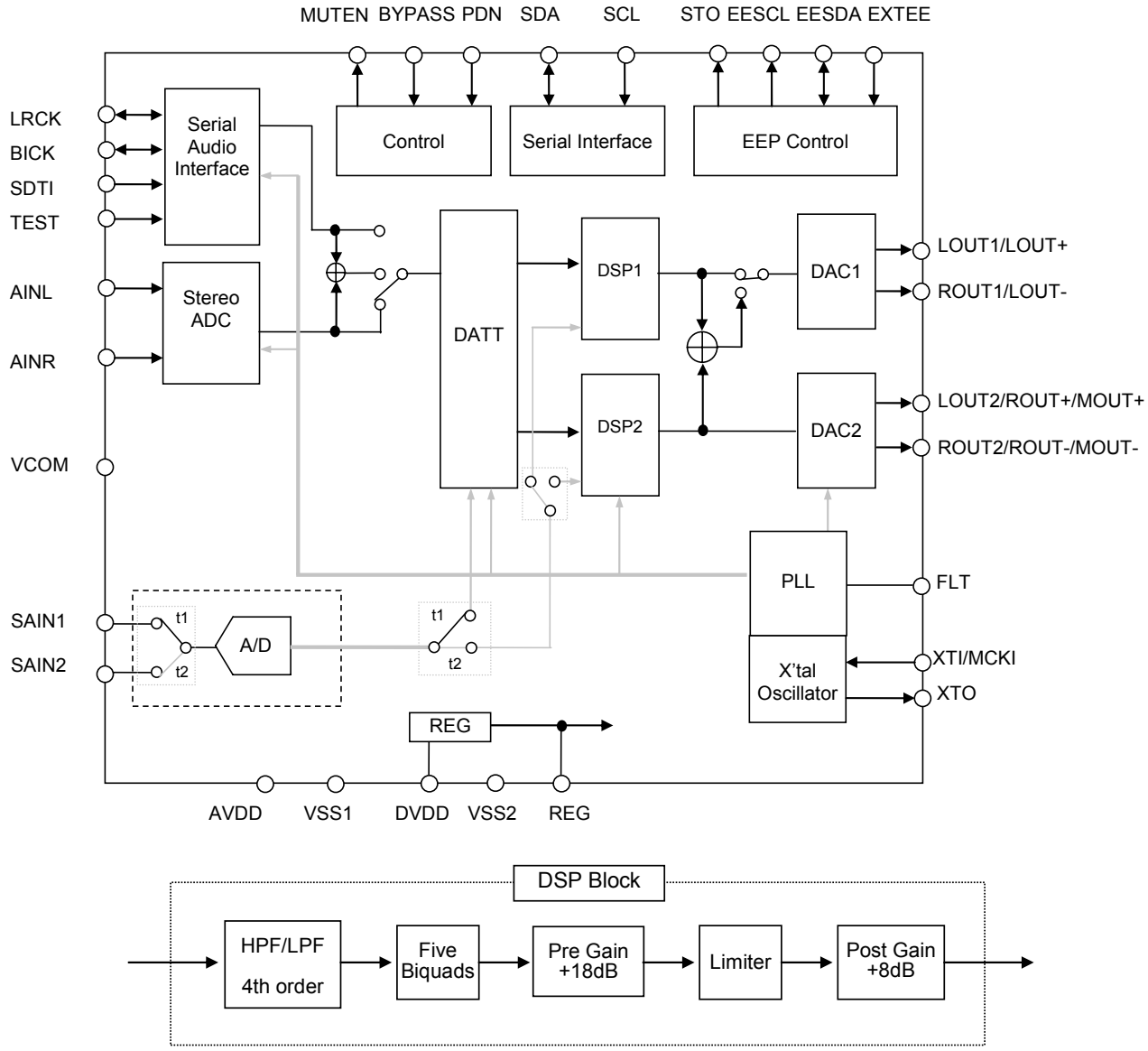
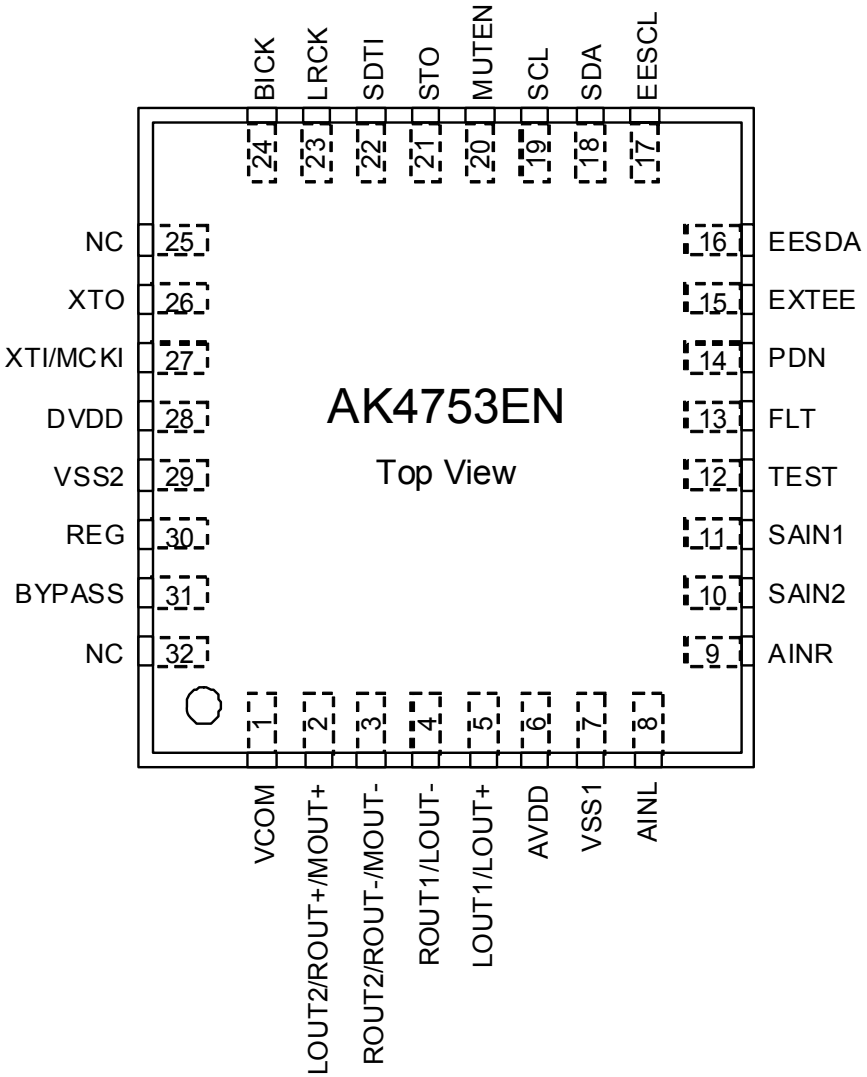


Figure 1. Block Diagram

■ Ordering Guide

AK4753EN	–30 ~ +85°C	32 pin QFN (4 x 4 mm, 0.4mm pitch)
AKD4753	Evaluation Board for AK4753	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCOM	O	Common voltage output pin This pin must be connected to VSS1 with the capacitors of 2.2μF capacitor in series.
2	LOUT2	O	Lch Line-Amp Output 2 Pin Single-ended mode (SPC1-0 bits = "11")
	ROUT+	O	Rch Line-Amp Positive Output Pin Differential mode (SPC1-0 bits = "00", "01")
	MOUT+	O	Mono Line-Amp Positive Output Pin Differential mode (SPC1-0 bits = "10")
3	ROUT2	O	Rch Line-Amp Output 2 Pin Single-ended mode (SPC1-0 bits = "11")
	ROUT–	O	Rch Line-Amp Negative Output Pin Differential mode (SPC1-0 bits = "00", "01")
	MOUT–	O	Mono Line-Amp Negative Output Pin Differential mode (SPC1-0 bits = "10")
4	ROUT1	O	Rch Line-Amp Output 1 Pin Single-ended mode (SPC1-0 bits = "10", "11")
	LOUT–	O	Lch Line-Amp Negative Output Pin Differential mode (SPC1-0 bits = "00", "01")
5	LOUT1	O	Lch Line-Amp Output 1 Pin Single-ended mode (SPC1-0 bits = "10", "11")
	LOUT+	O	Lch Line-Amp Positive Output Pin Differential mode (SPC1-0 bits = "00", "01")
6	AVDD	-	Analog Power Supply Pin, 3.0V ~ 3.6V
7	VSS1	-	Ground 1 Pin
8	AINL	I	L channel Analog Input Pin
9	AINR	I	R channel Analog Input Pin
10	SAIN2	I	8-bit SAR ADC Analog Input 2 Pin
11	SAIN1	I	8-bit SAR ADC Analog Input 1 Pin
12	TEST	I	TEST Input pin This pin must be connected to VSS2.
13	FLT	O	PLL Loop Filter Pin This pin must be connected to VSS1 with one resistor and one capacitor in series.
14	PDN	I	Power Down Pin When "L", the AK4753 is in power-down mode and is held in reset. The AK4753 must be always reset upon power-up.
15	EXTEE	I	EEP-ROM Enable Pin "H": EEP-ROM download mode "L": Serial control mode
16	EESDA	I/O	EEP-ROM Control Data Input/Output Pin
17	EESCL	O	EEP-ROM Control Data Clock Output Pin
18	SDA	I/O	Control Data Input/Output Pin
19	SCL	I	Control Data Clock Input Pin
20	MUTEN	O	Mute Control Output Pin. "H": Normal Operation "L": Mute
21	STO	O	EEP-ROM Status Output Pin "H": Read error "L": No error
22	SDTI	I	Audio Serial Data Input Pin
23	LRCK	I/O	Input/Output Channel Clock Pin
24	BICK	I/O	Audio Serial Data Clock Pin
25	NC	-	No Connect Pin No internal bonding. This pin must be connected to VSS2.

No.	Pin Name	I/O	Function
26	XTO	O	X'tal Clock Output Pin
27	XTI	I	X'tal / External Clock Input Pin
	MCKI	I	External Master Clock Input Pin
28	DVDD	-	Digital Power Supply Pin, 3.0V ~ 3.6V
29	VSS2	-	Ground 2 Pin
30	REG	O	Regulator Ripple Filter Pin This pin must be connected to VSS2 with 2.2μF capacitor in series.
31	BYPASS	I	Bypass Control Input Pin "H": DSP Bypass mode "L": Normal Operation
32	NC	-	No Connect Pin No internal bonding. This pin must be connected to VSS2.

Note 1. All input pins except analog input pins (AINL, AINR, SAIN1, SAIN2) must not be left floating.

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	AINL, AINR, SAIN1, SAIN2, FLT, LOUT1/LOUT+, ROUT1/LOUT-, LOUT2/ROUT+/MOUT+, ROUT2/ROUT-/MOUT-	Open
Digital	XTO, SDA, EESDA, EESCL, MUTEN, STO	Open
	LRCK, BICK, SDTI, XTI/MCKI, EXTEE, TEST, SCL	These pins must be connected to VSS2.

ABSOLUTE MAXIMUM RATINGS

(All VSS pins =0V; Note 2)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	-0.3	4.2	V
	Digital	DVDD	-0.3	4.2	V
Analog Input Voltage (Note 3)		VINA1	-0.3	AVDD+0.3	V
Digital Input Voltage (Note 4)		VIND	-0.3	DVDD+0.3	V
Input Current, Any Pin Except Supplies		IIN	-10	+10	mA
Ambient Operating Temperature		Ta	-30	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltage with respect to ground. All VSS pins must be connected to the common analog ground.
Note 3. AINL pin, AINR pin, SAIN1 pin, SAIN2 pin.
Note 4. BYPASS, PDN, EESDA, XTI/MCKI, BICK, LRCK, SDTI, SCL, SDA, TEST pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(All VSS pins =0V; Note 2)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 5)	Analog	AVDD	3.0	3.3	3.6	V
	Digital	DVDD	3.0	3.3	3.6	V
	Difference	|DVDD-AVDD|	-	0	0.3	V

Note 5. The power up sequence between AVDD and DVDD is not critical. Each power supplies should be powered up during the PDN pin = “L”. AVDD and DVDD must be the same voltage at the PDN pin = “H”. The PDN pin should be “H” after all power supplies are powered up. All power supplies should be powered on, only a part of these power supplies cannot be powered off. (Power off means power supplies equal to ground or power supplies are floating.) Do not turn off only the AK4753 under the condition that a surrounding device is powered on and the I2C bus is in use.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS (CODEC)

(Ta=25°C; AVDD=DVDD=3.3V; VSS1=VSS2=0V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24-bit Data; Measurement Band Width =20Hz~20kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
DAC Analog Output Characteristics: DAC → LOUT1/ROUT1, LOUT2/ROUT2 pins, Single-ended mode (SPC1-0 bits = "11"), HPF=LPF=EQ(5-BiQuads)=Limiter=OFF, DATT= 0dB, R_L=5kΩ					
Resolution		-	-	24	Bits
S/(N+D)	(0dBFS)	75	85	-	dB
DR	(-60dBFS with A-weighted)	87	97	-	dB
S/N	(A-weighted)	87	97	-	dB
Interchannel Isolation		80	95	-	dB
Interchannel Gain Mismatch		-	0	0.5	dB
Output Voltage	AOUT=0.68 x AVDD	1.98	2.24	2.51	Vpp
Load Resistance	(AC load)	5	-	-	kΩ
Load Capacitance		-	-	150	pF
Power Supply Rejection Ratio	(Note 6)	-	50	-	dB
DAC Analog Output Characteristics: DAC → LOUT+/-, ROUT+/- pins, Differential mode (SPC1-0 bits = "00"), HPF=LPF=EQ(5-BiQuads)=Limiter=OFF, DATT= 0dB, R_L=5kΩ					
S/(N+D)	(0dBFS)	78	88	-	dB
DR	(-60dBFS with A-weighted)	93	103	-	dB
S/N	(A-weighted)	93	103	-	dB
Interchannel Isolation		95	110	-	dB
Interchannel Gain Mismatch		-	0	0.5	dB
Output Voltage	AOUT=0.70 x AVDD	±2.08	±2.31	±2.54	Vpp
Load Resistance	(AC load)	5	-	-	kΩ
Load Capacitance		-	-	150	pF
Power Supply Rejection	(Note 6)	-	50	-	dB
ADC to DAC Characteristics: AINL/AINR pins → DAC → LOUT1/ROUT1, LOUT2/ROUT2 pins, Single-ended mode (SPC1-0 bits = "11"), HPF=LPF=EQ(5-BiQuads)=Limiter=OFF, DATT= 0dB, R_L=5kΩ					
Input Voltage	AIN=0.8xAVDD	2.38	2.64	2.90	Vpp
Input Resistance		24	35	-	kΩ
S/(N+D)	(-1dBFS)	73	84	-	dB
DR	(-60dBFS with A-weighted)	83	94	-	dB
S/N	(A-weighted)	83	94	-	dB
ADC to DAC Characteristics: AINL/AINR pins → DAC → LOUT+/-, ROUT+/- pins, Differential mode (SPC1-0 bits = "00", "01"), HPF=LPF=EQ(5-BiQuads)=Limiter=OFF, DATT= 0dB, R_L=5kΩ					
Input Voltage	AIN=0.8xAVDD	2.38	2.64	2.90	Vpp
Input Resistance		24	35	-	kΩ
S/(N+D)	(-1dBFS)	74	85	-	dB
DR	(-60dBFS with A-weighted)	85	96	-	dB
S/N	(A-weighted)	85	96	-	dB

Note 6. PSRR is applied to AVDD and DVDD with 1kHz, 50mVpp.

Parameter	min	typ	max	Unit
Power Supplies				
All Circuit Power-up (PDN pin = "H") (Note 7)				
Differential Mode (SPC1-0 bits = "00")				
AVDD	-	5.8	8.7	mA
DVDD	-	4.2	6.3	mA
Single-ended Mode (SPC1-0 bits = "11")				
AVDD	-	9.0	13.5	mA
DVDD	-	4.6	6.9	mA
Power-down (PDN pin = "L") (Note 7)				
AVDD + DVDD	-	1	10	μA

Note 7. PLL Master Mode (MCKI=12MHz), PMAD=PMDIG=PMLO1=PMLO2=PMSAR=PMPLL bits = "1".
Note 8. All digital input pins are fixed to DVDD or VSS2.

ANALOG CHARACTERISTICS (8-bit SAR ADC)

(Ta=25°C; AVDD=DVDD =3.3V; VSS1=VSS2=0V; unless otherwise specified)

Parameter		min	typ	max	Units
8-bit SAR ADC Characteristics					
Resolution		-	8	-	Bits
No Missing Codes		7	8	-	Bits
Integral Nonlinearity Error		-	-	±1	LSB
Differential Nonlinearity Error		-	-	±1	LSB
Analog Input Voltage Range		0	-	AVDD	V
Offset Error		-	-	±1	LSB
Gain Error		-	-	±1	LSB
Accuracy (Note 9)		-	-	±1.2	%
Potentiometer Resistance (Figure 2)	VR	-	-	100	kΩ

Note 9. Accuracy is the difference between the output code when 1.1V is input to SAIN1 or SAIN2 pin and the "ideal" code at 1.1V.

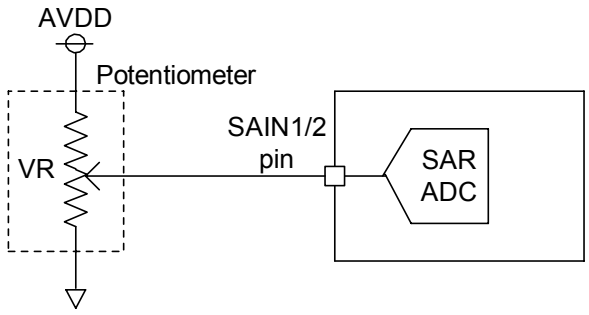


Figure 2. Potentiometer Resistance

FILTER CHARACTERISTICS

(Ta =-30 ~ 85°C; AVDD=DVDD=3.0V ~ 3.6V; fs=44.1kHz; HPF=LPF=EQ(5-BiQuads)=Limiter=OFF)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 10)	±0.16dB	PB	0	-	17.3	kHz
	−0.66dB		-	19.4	-	kHz
	−1.1dB		-	19.9	-	kHz
	−6.9dB		-	22.1	-	kHz
Stopband		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 11)		GD	-	15	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response	−3.0dB	FR	-	0.9	-	Hz
	−0.1dB		-	6.0	-	Hz
DAC Digital Filter:						
Passband (Note 12)	±0.05dB	PB	0	-	20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	53	-	-	dB
Group Delay (Note 13)		GD	-	25	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±0.4	-	dB

Note 10. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 11. A calculating delay time which induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register.

Note 12. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 13. A calculating delay time which induced by digital filtering. This time is from setting the 24-bit data of both channels to input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=-30 ~ 85°C; AVDD=DVDD= 3.0V ~ 3.6V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
Input Voltage at AC Coupling (XTI/MCKI pin) (Note 14)	VAC	40%DVDD	-	-	Vpp
High-Level Output Voltage (Note 15) (Iout = −100μA)	VOH	DVDD−0.4	-	-	V
Low-Level Output Voltage (Note 15) (Except SDA, EESDA, EESCL pins: Iout = 100μA)	VOL	-	-	0.4	V
(SDA, EESDA, EESCL pins: Iout = 3mA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA

Note 14. It is a case when AC coupling capacitor is connected to the XTI/MCKI pin.

Note 15. Except XTO pin.

SWITCHING CHARACTERISTICS

(Ta=-30 ~ 85°C, AVDD= DVDD= 3.0V ~ 3.6V, C_L=20pF; unless otherwise specified)

Parameter		Symbol	min	typ	max	Unit
Crystal Resonator						
Frequency		fXTAL	11.2896	-	12.288	MHz
PLL Master Mode (PLL Reference Clock = XTI/MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	24.576	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
AC Pulse Width		tACW	18.5	-	-	ns
LRCK Output Timing						
Frequency		fs	-	Table 6	-	kHz
DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = LRCK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period	PLL3-0 bits = "0010"	tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = "0011"	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter		Symbol	min	typ	max	Unit
External Slave Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	13.312	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing						
Frequency	256fs	fs	7.35	-	48	kHz
	512fs	fs	7.35	-	26	kHz
	1024fs	fs	7.35	-	13	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK−60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
BICK Input Timing						
Period (Note 16)		tBCK	312.5 or 1/(126fs)	-	-	ns s
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	13.312	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = “0”	tBCK	-	1/(32fs)	-	ns
	BCKO bit = “1”	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%

Note 16. The minimum value is longer time between 312.5ns and 1/(126fs)s.

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (DSP Mode)					
Master Mode					
LRCK "↑" to BICK "↑" (Note 17)	tDBF	0.5 x tBCK –40	0.5 x tBCK	0.5 x tBCK +40	ns
LRCK "↑" to BICK "↓" (Note 18)	tDBF	0.5 x tBCK –40	0.5 x tBCK	0.5 x tBCK +40	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK "↑" to BICK "↑" (Note 17)	tLRB	0.4 x tBCK	-	-	ns
LRCK "↑" to BICK "↓" (Note 18)	tLRB	0.4 x tBCK	-	-	ns
BICK "↑" to LRCK "↑" (Note 17)	tBLR	0.4 x tBCK	-	-	ns
BICK "↓" to LRCK "↑" (Note 18)	tBLR	0.4 x tBCK	-	-	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Audio Interface Timing (Right/Left justified & I^2S)					
Master Mode					
BICK "↓" to LRCK Edge (Note 19)	tMBLR	–40	-	40	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 19)	tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 19)	tBLR	50	-	-	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns

Note 17. MSBS, BCKP bits = "00" or "11".
Note 18. MSBS, BCKP bits = "01" or "10".
Note 19. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (I^2C bus-slave): SCL, SDA pins (Note 20)					
SCL Clock Frequency	fSCL1	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF1	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD1:STA	0.6	-	-	µs
Clock Low Time	tLOW1	1.3	-	-	µs
Clock High Time	tHIGH1	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU1:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 21)	tHD1:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU1:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR1	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF1	-	-	0.3	µs
Capacitive Load on Bus	Cb1	-	-	400	pF
Setup Time for Stop Condition	tSU1:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP1	0	-	50	ns
EEP-ROM Control Interface Timing (I^2C bus-master): EESCL, EESDA pins (Note 20)					
EESCL Clock Frequency	fSCL2	200	280	400	kHz
Bus Free Time Between Transmissions	tBUF2	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA2	0.6	-	-	µs
Clock Low Time	tLOW2	1.3	-	-	µs
Clock High Time	tHIGH2	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU2:STA	0.6	-	-	µs
EESDA Hold Time from EESCL Falling (Note 21)	tHD2:DAT	0	-	0.9	µs
EESDA Setup Time from EESCL Rising	tSU2:DAT	0.1	-	-	µs
Rise Time of Both EESDA and EESCL Lines	tR2	-	-	0.3	µs
Fall Time of Both EESDA and EESCL Lines	tF2	-	-	0.3	µs
Capacitive Load on Bus	Cb2	-	-	400	pF
Setup Time for Stop Condition	tSU2:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP2	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 22)	tPD	10	-	-	ms

Note 20. I^2C-bus is a trademark of NXP B.V.
Note 21. Data must be held long enough to bridge the 300ns-transition time of SCL and EESCL.
Note 22. The AK4753 can be reset by the PDN pin = “L”.

■ Timing Diagram

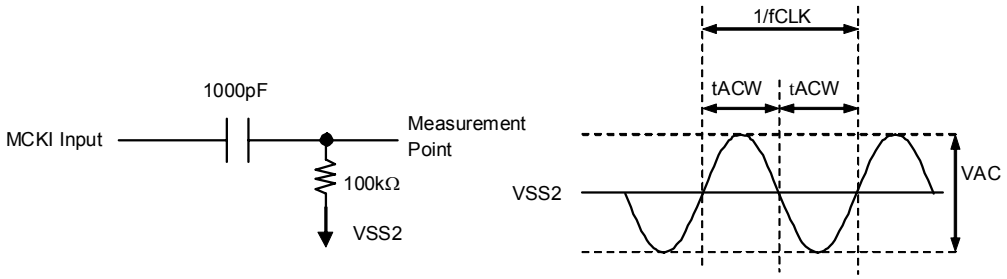


Figure 3. MCKI AC Coupling Timing

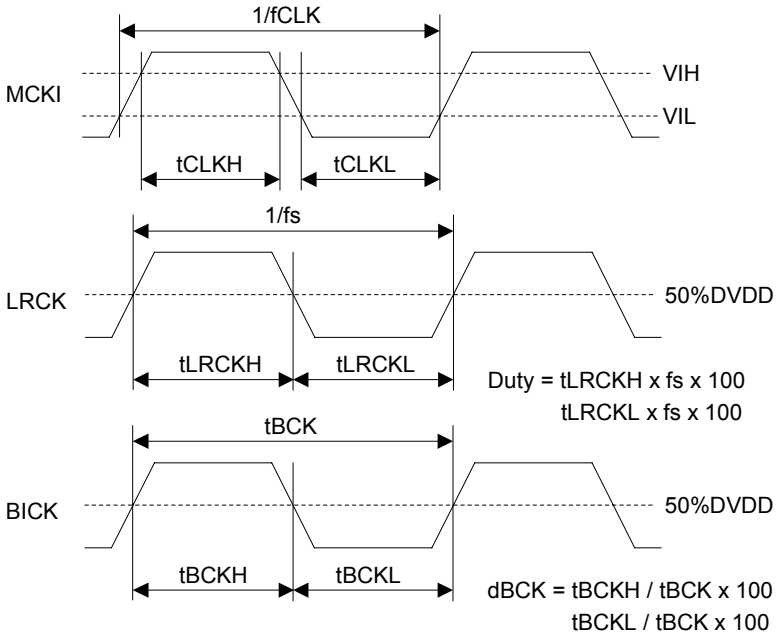


Figure 4. Clock Timing (PLL/EXT Master mode)

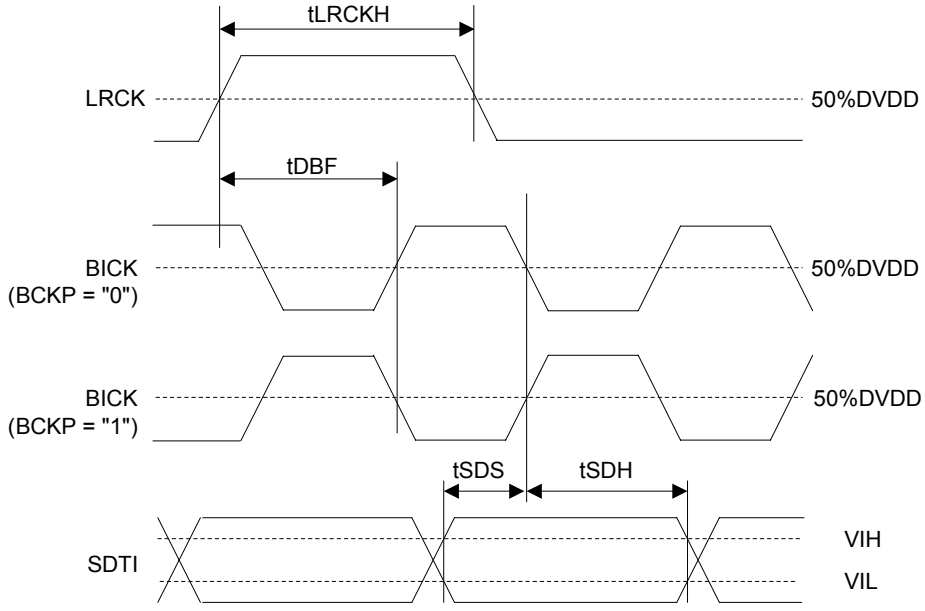


Figure 5. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = “0”)

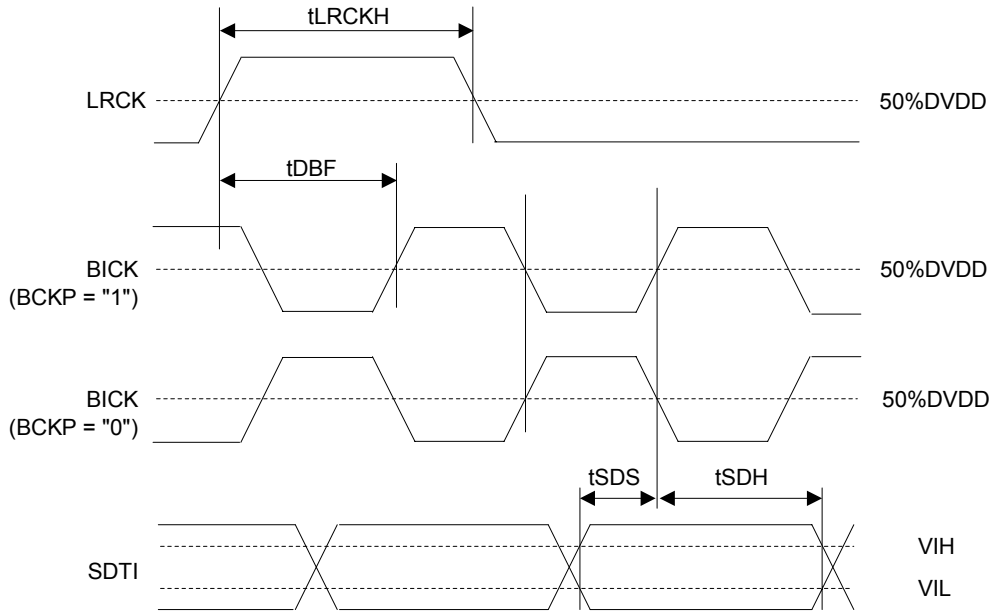


Figure 6. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = "1")

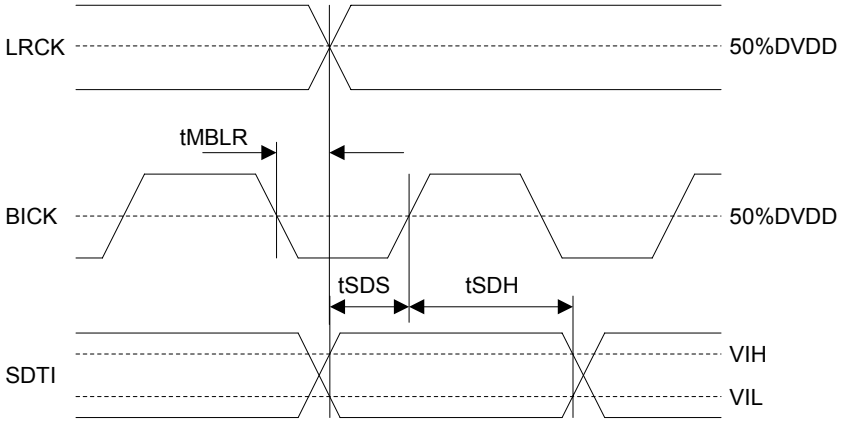


Figure 7. Audio Interface Timing (PLL/EXT Master mode, Except DSP mode)

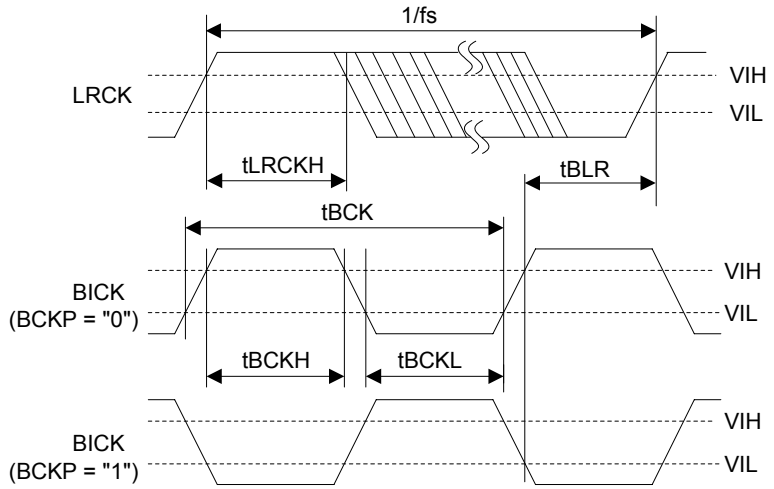


Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = "0")

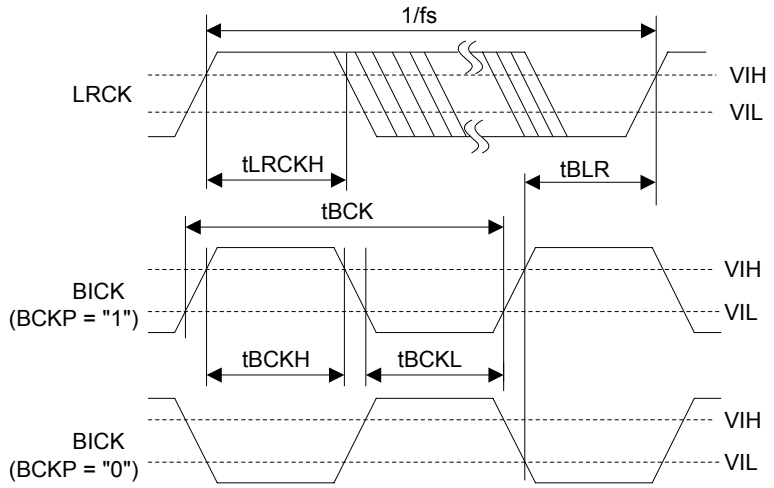


Figure 9. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = "1")

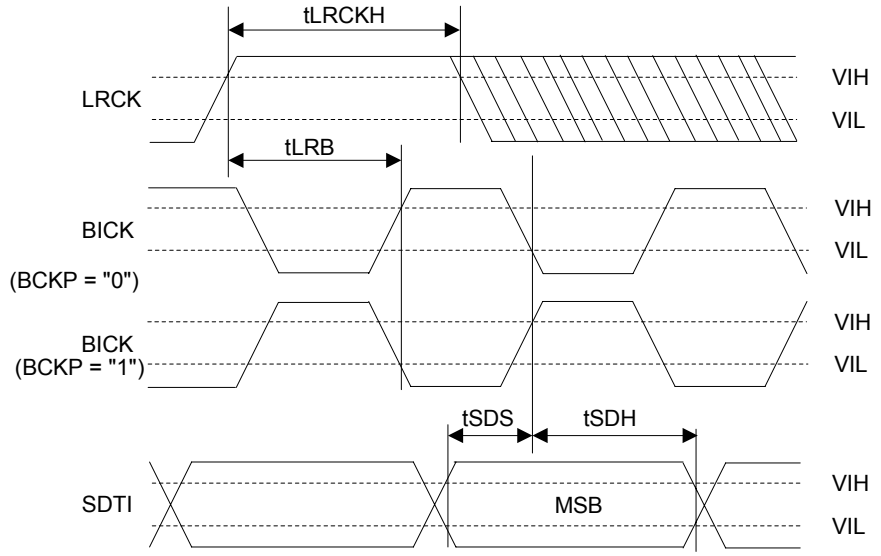


Figure 10. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = "0")

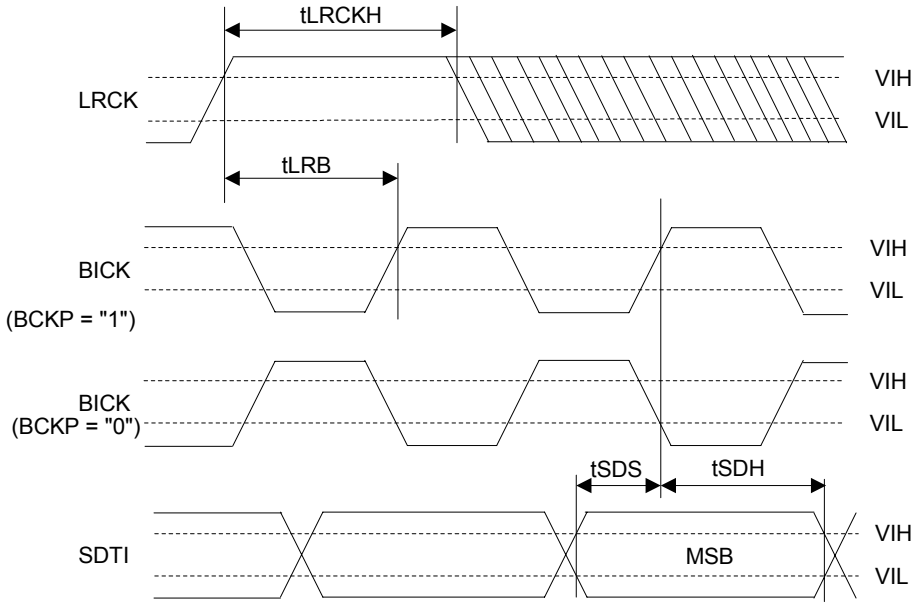


Figure 11. Audio Interface Timing (PLL Slave mode, DSP mode, MSBS = "1")

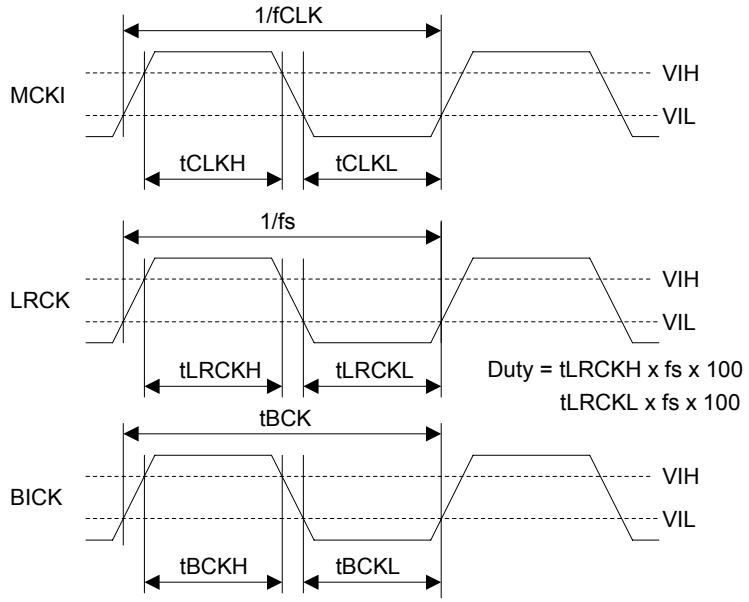


Figure 12. Clock Timing (EXT Slave mode)

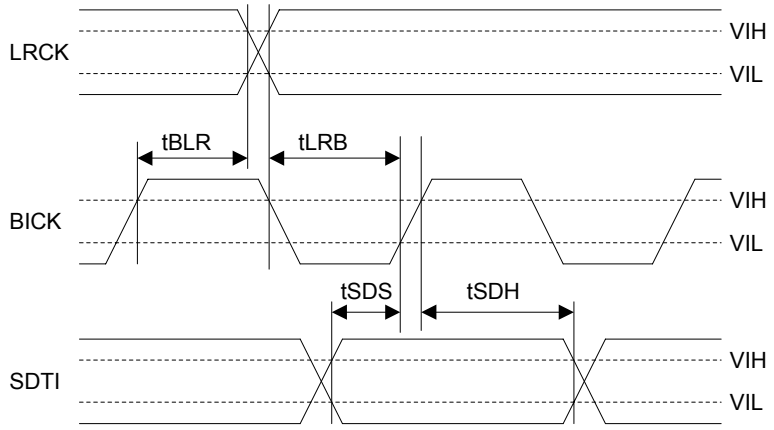


Figure 13. Audio Interface Timing (PLL/EXT Slave mode, Except DSP mode)

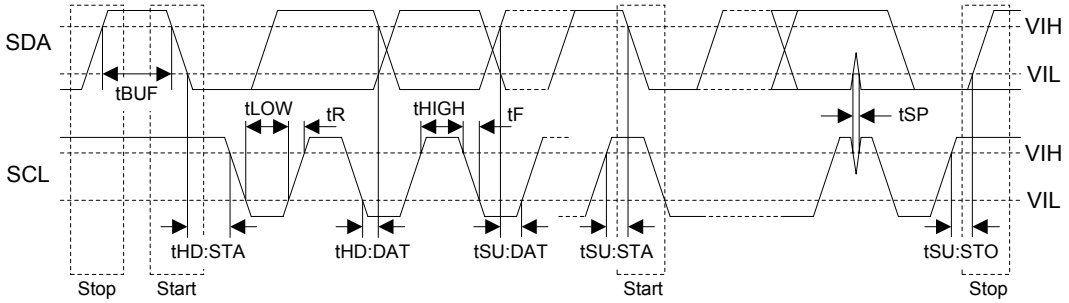


Figure 14. I^2C Bus Mode Timing

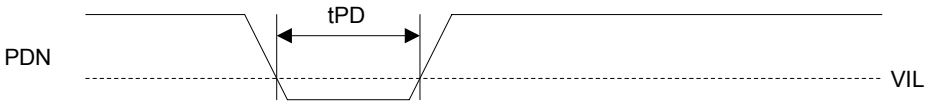


Figure 15. Power Down & Reset Timing

OPERATION OVERVIEW

■ Overview of AK4753

The AK4753 is an audio CODEC with integrated digital signal processors.

It is easy to use since the two inputs 8-bit SAR ADC and EEP-ROM I/F are integrated.

The SAR ADC has 2-channel input selector and the AD conversion is executed sequentially.
The SAIN1 value is used to control the internal DATT. The SAIN2 value is used to control the gain of the EQ. When the analog input of the SAIN1/2 changes, the register value of the DATT/EQ is changed automatically.

This external EEP-ROM is used to store the coefficient values for the DSP blocks, and the setting data. When the AK4753 is powered up, it reads the data in EEP-ROM at first, and maps these values into the internal registers.

The following contents are stored in EEP-ROM.
a. Fundamental function
- -Output Configuration Setting (Stereo mode, 2.1-channel mode or 4-channel mode)
- -PLL mode setting: master or slave, PLL Reference Clock, Sampling Frequency
- -Audio Interface Format
- -DATT
- -Post-Gain and Pre-Gain setting for DSP1/2
- -Limiter setting for DSP1/2

b. Coefficient data for DSP1/2
- -Coefficient data of LPF/HPF
- -Coefficient data of Five Biquads

■ System Clock

There are the following four methods to interface with external devices. (Table 1, Table 2)

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode	1	1	Table 4	Figure 20 Figure 21
PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	1	0	Table 4	Figure 22 Figure 23
EXT Slave Mode	0	0	x	Figure 24
EXT Master Mode	0	1	x	Figure 25 Figure 26

Table 1. Clock Mode Setting (x: Don't care)

Mode	XTI/MCKI pin	BICK pin	LRCK pin
PLL Master Mode	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin)	GND	Input (Selected by PLL3-0 bits)	Input (1fs)
EXT Slave Mode	Selected by FS1-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	Selected by FS1-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4753 is in power-down mode (PDN pin = "L") and when exits reset state, the AK4753 is in slave mode. After exiting reset state, the AK4753 goes to master mode by changing M/S bit = "1".

When the AK4753 is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes "1". The LRCK and BICK pins of the AK4753 must be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ Crystal Oscillator Circuit

A clock for the XTI/MCKI pin can be generated by the following three methods.

1. X'tal Mode (PWXTAL bit= "1")

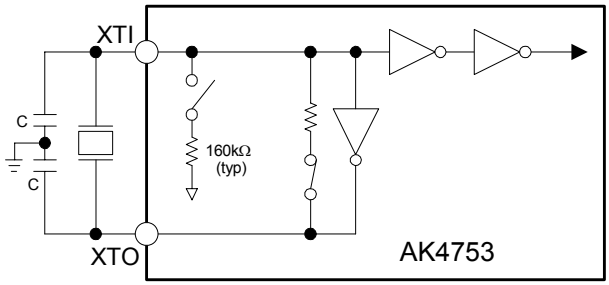


Figure 16. X'tal Mode
Note: The value of the capacitor depends on a crystal (Typ.10-40pF).

2. External Clock Mode (PWXTAL bit= "1")
Note: Do not input a clock beyond the voltage of DVDD.

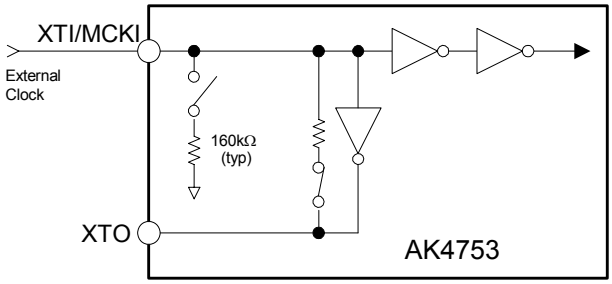


Figure 17. Direct Connection
(Input: CMOS Level)

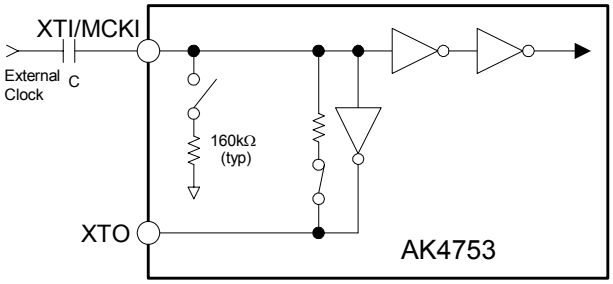


Figure 18. AC Coupling Connection
(Input: ≥ 40%DVDD, C=1000pF)

3. OFF Mode of XTI/MCKI, XTO pins (PWXTAL bit= "0")

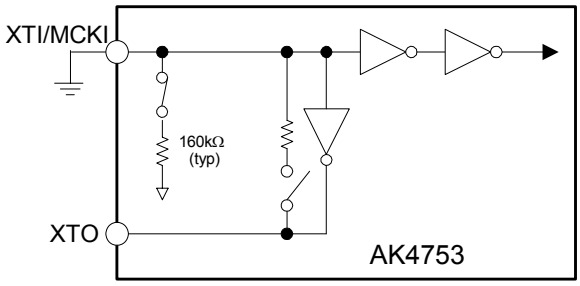


Figure 19. OFF Mode

■ PLL Mode (PMPLL bit = "1")

When PMPLL bit = "1", the built-in high precision PLL works according to the clock which is set by FS3-0 bits and PLL3-0 bits. The PLL lock time is shown in Table 4, whenever the AK4753 is supplied to a stable clock after PLL is powered-up (PMPLL bit = "0" →"1") or sampling frequency changes.

1. PLL Mode setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	FLT pin Rp, Cp		PLL Lock Time (max)	
							Rp[Ω]	Cp[F]		
0	0	0	0	0	LRCK pin	1fs	10k	100n	40 ms	(default)
1	0	0	1	0	BICK pin	32fs	10k	4.7n	4 ms	
2	0	0	1	1	BICK pin	64fs	10k	4.7n	4 ms	
3	0	1	0	0	XTI/MCKI pin	11.2896MHz	10k	4.7n	4 ms	
4	0	1	0	1	XTI/MCKI pin	12.288MHz	10k	4.7n	4 ms	
5	0	1	1	0	XTI/MCKI pin	12MHz	10k	4.7n	4 ms	
6	0	1	1	1	XTI/MCKI pin	24MHz	10k	4.7n	4 ms	
7	1	1	0	0	XTI/MCKI pin	22.5792MHz	10k	4.7n	4 ms	
8	1	1	0	1	XTI/MCKI pin	24.576MHz	10k	4.7n	4 ms	
Others	Others				N/A					

(*fs: Sampling Frequency, N/A: Not Available)

Table 4. PLL Mode Setting

2. Sampling Frequency setting in PLL Mode (PLL reference clock pin: XTI/MCKI pin)

In the case of PLL2 bit = "1", and the reference clock is input to the XTI/MCKI pin or the crystal oscillator circuit is used, the sampling frequency can be set according to Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (Note 23)	
0	0	0	0	0	8kHz mode	(default)
1	0	0	0	1	12kHz mode	
2	0	0	1	0	16kHz mode	
3	0	0	1	1	24kHz mode	
4	0	1	0	0	7.35kHz mode	
5	0	1	0	1	11.025kHz mode	
6	0	1	1	0	14.7kHz mode	
7	0	1	1	1	22.05kHz mode	
10	1	0	1	0	32kHz mode	
11	1	0	1	1	48kHz mode	
14	1	1	1	0	29.4kHz mode	
15	1	1	1	1	44.1kHz mode	
Others	Others				N/A	

(Reference Clock = XTI/MCKI pin) (N/A: Not Available)

Table 5. Sampling Frequency Setting (PMPLL bit = "1")

Note 23. When the XTI/MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL3-0 bits) and sampling frequency (FS3-0 bits). Refer to Table 6 for the details of sampling frequency. In master mode, LRCK and BICK output frequency correspond to sampling frequencies shown in Table 6. When the LRCK or BICK pin is the PLL reference clock input, the sampling frequency generated by PLL is the same sampling frequency of mode name.

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz] (Note 24)
11.2896	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
	7.35kHz mode	7.350000
	14.7kHz mode	14.700000
	29.4kHz mode	29.400000
12.288	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
	7.35kHz mode	7.350000
	14.7kHz mode	14.700000
	29.4kHz mode	29.400000
12	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
	7.35kHz mode	7.349918
	14.7kHz mode	14.699836
	29.4kHz mode	29.399671
	Sampling frequency that differs from sampling frequency of mode name	

Note 24. These are rounded off to six decimal places.

Table 6. Sampling Frequency at PLL mode (Reference clock is MCKI)

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz] (Note 24)
24	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
	7.35kHz mode	7.349918
	14.7kHz mode	14.699836
	29.4kHz mode	29.399671
22.5792	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
	7.35kHz mode	7.350000
	14.7kHz mode	14.700000
	29.4kHz mode	29.400000
24.576	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
	7.35kHz mode	7.350000
	14.7kHz mode	14.700000
	29.4kHz mode	29.400000
	Sampling frequency that differs from sampling frequency of mode name	

Note 24 These are rounded off to six decimal places.

Table 6. Sampling Frequency at PLL mode (Reference clock is MCKI)

3. Sampling Frequency setting in PLL Mode (PLL reference clock pin: LRCK or BICK pin)

In the case of PLL2 bit = "0" and the reference clock is input to the LRCK or BICK pins, the sampling frequency is set by FS3 and FS2 bits according to Table 7.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	x	x	7.35kHz ≤ fs ≤ 12kHz	(default)
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	0	x	x	24kHz < fs ≤ 48kHz	
Others	Others				N/A	

(PLL Reference: Clock: LRCK or BICK pin) (x: Don't care, N/A: Not Available)

Table 7. Sampling Frequency Setting (PLL2 bit = "0" and PMPLL bit = "1")

■ PLL Un-Lock

1. PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, the BICK and LRCK pins go to "L" before the PLL goes to lock state after PMPLL bit = "0" →"1" (Table 8). After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs. When sampling frequency is changed, the BICK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	BICK pin	LRCK pin
PMPLL bit "0" → "1"	"L" Output	"L" Output
PLL Unlock (Except for the above)	Not fixed	Not fixed
PLL Lock	Table 9	1fs Output

Table 8. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 22.5792MHz, 24MHz or 24.576MHz) is input to the XTI/MCKI pin or the crystal oscillator circuit is used, the BICK and LRCK clocks are generated by an internal PLL circuit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 9).

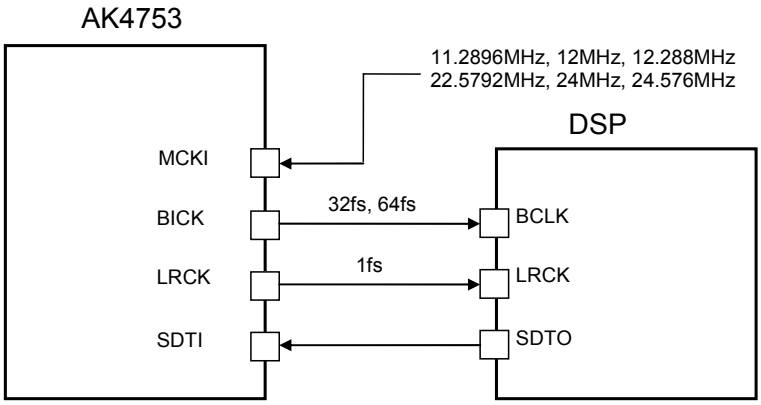


Figure 20. PLL Master Mode (External Clock Mode)

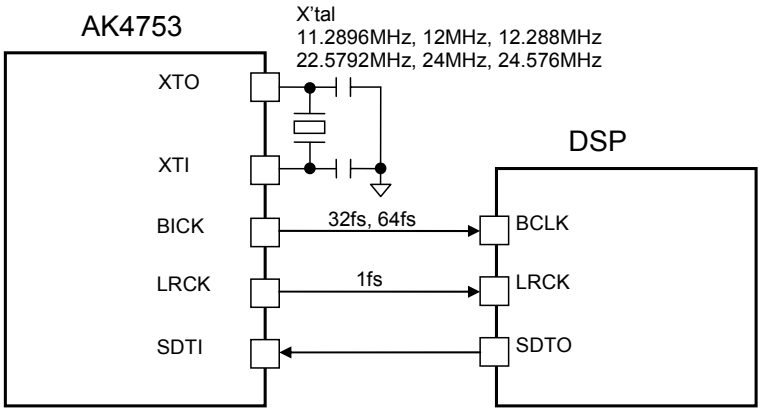


Figure 21. PLL Master Mode (X'tal Mode)

BCKO bit	BICK Output Frequency	
0	32fs	
1	64fs	(default)

Table 9. BICK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to the BICK or LRCK pin. Required clock for the AK4753 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

Sampling frequency corresponds to a range from 7.35kHz to 48kHz by changing FS3-0 bits (Table 7).

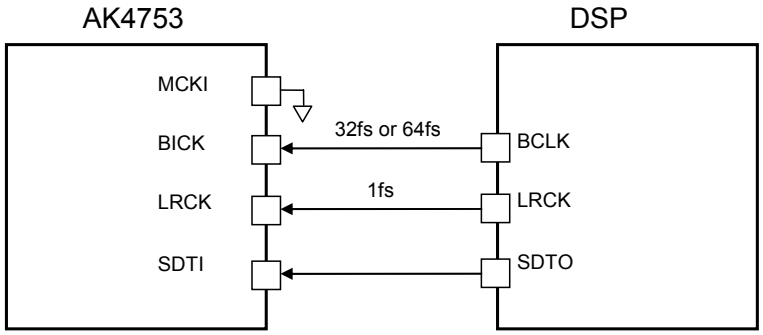


Figure 22. PLL Slave Mode (PLL Reference Clock: BICK pin)

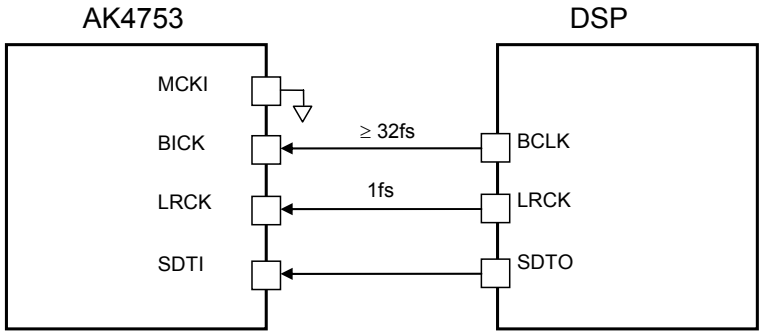


Figure 23. PLL Slave Mode (PLL Reference Clock: LRCK pin)

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK4753 changes to EXT mode. Master clock is input from the XTI/MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of a normal audio CODEC. The clocks required to operate the AK4753 are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks is not important. The input frequency of MCKI is selected by FS1-0 bits (Table 10).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	x	0	0	256fs	7.35kHz ~ 48kHz	(default)
1	x	0	1	1024fs	7.35kHz ~ 13kHz	
2	x	1	0	512fs	7.35kHz ~ 26kHz	
3	x	1	1	512fs	7.35kHz ~ 26kHz	

Table 10. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0") (x: Don't care)