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AK4951A

24bit Stereo CODEC with MIC/HP/SPK-AMP

1. General Description

The AK4951A is a low power 24-bit stereo CODEC with a microphone, headphone and speaker amplifiers.

The AK4951A supports sampling frequency from 8kHz to 48kHz. It is suitable for a wide range of application from speech signal processing for narrowband, wideband and super wideband to sound signal processing for audio band.

The input circuits include a microphone amplifier, an automatic wind noise reduction filter of the proprietary algorithms and a high performance digital ALC (automatic level control) circuit, therefore the AK4951A can record with high-quality sound regardless of whether indoors or outdoors. In addition, the output circuits include a cap-less headphone amplifier with a negative voltage generated by charge pump circuit and a speaker amplifier with 1W output power. It is suitable for various products as well as portable applications with recording/playback function.

The AK4951A are available in a small 32-pin QFN (4mm x 4mm, 0.4mm pitch) package saving mounting area on the board.

Application:

- IP Camera
- Digital Camera
- IC Recorder
- Tablet
- Wireless Headphone
- Headset

2. Features

1. Recording Functions

- **Analog Input: 3 Stereo Single-ended inputs with Selectors**
- **Microphone Amplifier: +30dB ~ 0dB, 3dB Step**
- **Microphone Power Supply: 2.0V or 2.4V, Noise Level= -108dBV**
- **Digital ALC (Automatic Level Control)**
 - **Setting Range: +36dB ~ -52.5dB, 0.375dB Step & Mute**
- **ADC Performance: S/(N+D): 83dB, DR, S/N: 88dB (MIC-Amp=+18dB)**
S/(N+D): 85dB, DR, S/N: 96dB (MIC-Amp=0dB)
- **Microphone Sensitivity Correction**
- **Automatic Wind Noise Reduction Filter**
 - Selectable voice peak detection mode**
- **5-Band Notch Filter: Include Dynamic Gain Control**
- **Stereo Separation Emphasis Circuit**
- **Digital Microphone Interface**

2. **Playback Functions**
 - **Digital ALC (Automatic Level Control)**
 - Setting Range: +36dB ~ -52.5dB, 0.375dB Step & Mute
 - **Sidetone Mixer & Volume Control (0dB ~ -18dB, 6dB Step)**
 - **Digital Volume Control**
 - +12dB ~ -89.5dB, 0.5dB Step & Mute
 - **Capacitor-less Stereo Headphone Amplifier**
 - HP-Amplifier Performance: S/(N+D): 75dB@20mW, S/N: 97dB
 - Output Power: 20mW@16Ω
 - Pop Noise Free at Power-ON/OFF
 - **Mono Speaker Amplifier (with Stereo Line Output Switch)**
 - Speaker Amplifier Performance: S/(N+D): 75dB@250mW, S/N: 99dB
 - BTL Output
 - Output Power: 400mW@8Ω (SVDD=3.3V), 1W@8Ω (SVDD=5V)
 - **Analog Mixing: BEEP Input**
3. **Power Management**
4. **Master Clock:**
 - (1) **PLL Mode**
 - Frequencies: 11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 16MHz, 24MHz, 27MHz (MCKI pin), 32fs or 64fs (BICK pin)
 - (2) **External Clock Mode**
 - Frequencies: 256fs, 384fs, 512fs or 1024fs (MCKI pin)
5. **Sampling Frequencies**
 - **PLL Master Mode:**
 - 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
 - **PLL Slave Mode (BICK pin):** 8kHz ~ 48kHz
 - **EXT Master/Slave Mode:**
 - 8kHz ~ 48kHz (256fs, 384fs, 512fs), 8kHz ~ 24kHz (1024fs)
6. **Master/Slave Mode**
7. **Audio Interface Format: MSB First, 2's complement**
 - **ADC:** 16/24bit MSB justified, 16/24bit I²S
 - **DAC:** 16/24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 16/24bit I²S
8. **μP I/F: I²C Bus (Ver 1.0, 400kHz Fast-Mode)**
9. **Ambient Operating Temperature: Ta = -40 ~ 85°C**
10. **Power Supply**
 - **Analog Power Supply (AVDD):** 2.8 ~ 3.5V
 - **Speaker Power Supply (SVDD):** 1.8 ~ 5.5V
 - **Digital & Headphone Power Supply (DVDD):** 1.6 ~ 1.98V
 - **Digital I/O Power Supply (TVDD):** 1.6 or (DVDD - 0.2) ~ 3.5V
11. **Package: 32-pin QFN (4 x 4 mm, 0.4mm pitch)**

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4. Block Diagram and Functions

■ Block Diagram

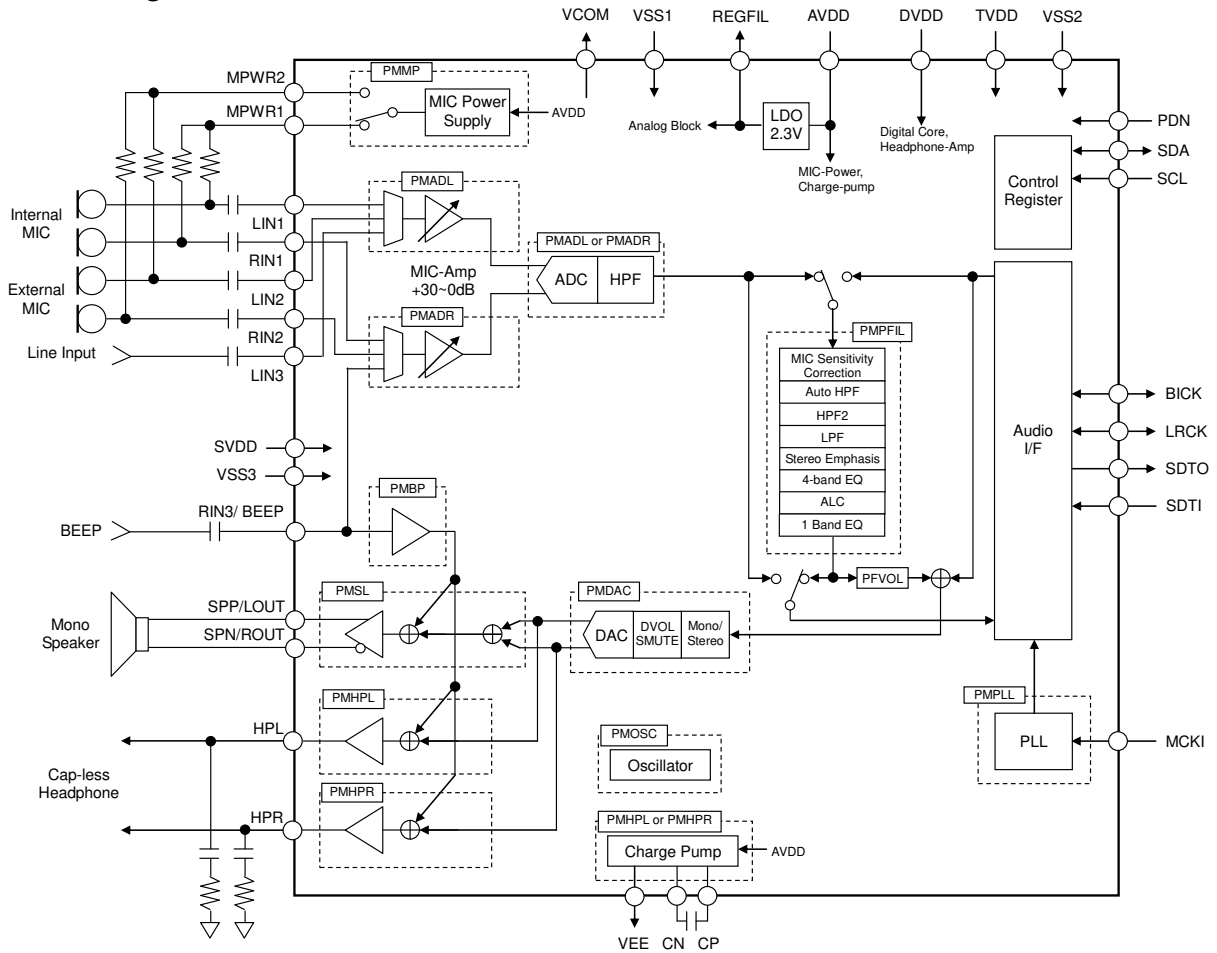


Figure 1. Block Diagram

■ Comparison Table to AK4951

1. Function

Function	AK4951	AK4951A
PLL Mode (MCKI Frequency)	11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz	11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 16MHz , 24MHz, 27MHz
Automatic Wind Noise Reduction Filter	Voice peak detection mode: Auto	Voice peak detection mode: Selectable

2. Register Setting

1) PLL Reference Clock Setting

Mode 0 of the PLL mode setting was added from AK4951.

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)
0	0	0	0	0	MCKI pin	16MHz	5ms
2	0	0	1	0	BICK pin	32fs	2ms
3	0	0	1	1	BICK pin	64fs	2ms
4	0	1	0	0	MCKI pin	11.2896MHz	5ms
5	0	1	0	1	MCKI pin	12.288MHz	5ms
6	0	1	1	0	MCKI pin	12MHz	5ms
7	0	1	1	1	MCKI pin	24MHz	5ms
12	1	1	0	0	MCKI pin	13.5MHz	5ms
13	1	1	0	1	MCKI pin	27MHz	5ms
Others	Others				N/A		

2) Automatic Wind Noise Reduction Filter

VODETN bit was added from AK4951.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Signal Select 2	SPKG1	SPKG0	VODETN	MICL	INL1	INL0	INR1	INR0

VODETN: Voice Peak Detection Disable

0: Enable (default)

1: Disable

When AHPF and VODETN bits = "1", voice peak detection is disable. VODETN bit must be set when PMPFIL bit = "0".

3) Device Information

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
31H	Device Information	REV3	REV2	REV1	REV0	DVN3	DVN2	DVN1	DVN0

REV3-0: Device Revision ID (Read operation only.)

1100: AK4951

1101: AK4951A

5. Pin Configurations and Functions

■ Pin Layout

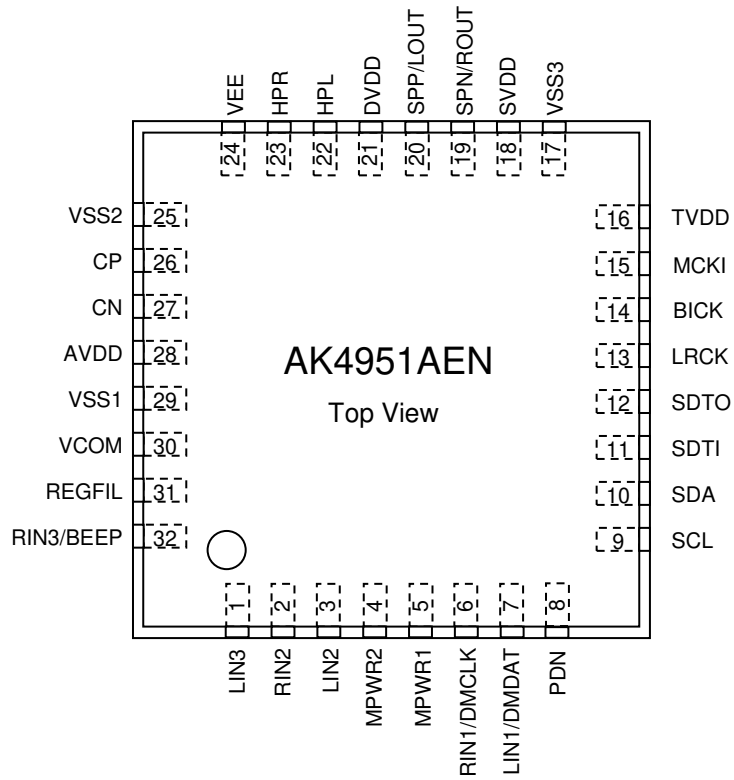


Figure 2. Pin Layout

■ PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LIN3	I	Lch Analog Input 3 pin
2	RIN2	I	Rch Analog Input 2 Pin
3	LIN2	I	Lch Analog Input 2 pin
4	MPWR2	O	MIC Power Supply 2 Pin
5	MPWR1	O	MIC Power Supply 1 Pin
6	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0": default)
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")
7	LIN1	I	Lch Analog Input 1 Pin (DMIC bit = "0": default)
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
8	PDN	I	Reset & Power-down Pin "L": Reset & Power-down, "H": Normal Operation
9	SCL	I	Control Data Clock Pin
10	SDA	I/O	Control Data Input/Output Pin
11	SDTI	I	Audio Serial Data Input Pin
12	SDTO	O	Audio Serial Data Output Pin
13	LRCK	I/O	Input/Output Channel Clock Pin
14	BICK	I/O	Audio Serial Data Clock Pin
15	MCKI	I	External Master Clock Input Pin
16	TVDD	-	Digital I/O Power Supply Pin, 1.6 or (DVDD-0.2) ~ 3.5V
17	VSS3	-	Ground 3 Pin
18	SVDD	-	Speaker-Amp Power Supply Pin, 1.8 ~ 5.5V
19	SPN	O	Speaker-Amp Negative Output Pin (LOSEL bit = "0": default)
	ROUT	O	Rch Stereo Line Output Pin (LOSEL bit = "1")
20	SPP	O	Speaker-Amp Positive Output Pin (LOSEL bit = "0": default)
	LOUT	O	Lch Stereo Line Output Pin (LOSEL bit = "1")
21	DVDD	-	Digital Power Supply Pin, 1.6 ~ 1.98V
22	HPL	O	Lch Headphone-Amp Output Pin
23	HPR	O	Rch Headphone-Amp Output Pin
24	VEE	O	Charge-Pump Circuit Negative Voltage Output Pin This pin must be connected to VSS2 with 2.2 μ F \pm 20% capacitor in series.
25	VSS2	-	Ground 2 Pin
26	CP	O	Positive Charge-Pump Capacitor Terminal Pin This pin must be connected to CN pin with 2.2 μ F \pm 20% capacitor in series.
27	CN	I	Negative Charge-Pump Capacitor Terminal Pin This pin must be connected to CP pin with 2.2 μ F \pm 20% capacitor in series.
28	AVDD	-	Analog Power Supply Pin, 2.8 ~ 3.5V
29	VSS1	-	Ground 1 Pin
30	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 with 2.2F \pm 20% capacitor in series.
31	REGFIL	O	LDO Voltage Output pin for Analog Block (typ 2.3V) This pin must be connected to VSS1 with 2.2 μ F \pm 20% capacitor in series.
32	RIN3	I	Rch Analog Input 3 Pin (PMBP bit = "0": default)
	BEEP	I	Beep Signal Input Pin (PMBP bit = "1")

Note 1. All input pins except analog input pins (LIN1, RIN1, LIN2, RIN2, LIN3, RIN3/BEEP) must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, SPN, SPP, HPL, HPR, CP, CN, VEE, LIN1/DMDAT, RIN1/DMCLK, LIN2, RIN2, LIN3, RIN3/BEEP	Open
Digital	MCKI, SDTI	Connect to VSS2
	SDTO	Open

6. Absolute Maximum Ratings

(VSS1=VSS2=VSS3=0V; [Note 2](#))

Parameter	Symbol	Min.	Max.	Unit	
Power Supplies	Analog	AVDDam	-0.3	6.0	V
	Digital	DVDDam	-0.3	2.5	V
	Digital I/O	TVDDam	-0.3	6.0	V
	Speaker-Amp	SVDDam	-0.3	6.0	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA	
Analog Input Voltage (Note 3)	VINA	-0.3	AVDD+0.3	V	
Digital Input Voltage (Note 4)	VIND	-0.3	TVDD+0.3	V	
Ambient Operating Temperature (powered applied)	Ta	-40	85	°C	
Storage Temperature	Tstg	-65	150	°C	
Maximum Power Dissipation (Note 5)	Pd	-	840	mW	

Note 2. All voltages are with respect to ground. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.

Note 3. LIN1, RIN1, LIN2, RIN2, LIN3 and RIN3/BEEP pins

Note 4. PDN, CCLK/SCL, CSN/SDA, CDTIO/CAD0, SDTI, LRCK, BICK and MCKI pins

Pull-up resistors at the SDA and SCL pins must be connected to a voltage in the range from TVDD or more to 6V or less.

Note 5. This power is the AK4951A internal dissipation that does not include power dissipation of externally connected speakers. The maximum junction temperature is 125°C and θ_{ja} (Junction to Ambient) is 42°C/W at JESD51-9 (2p2s). When $P_d = 840\text{mW}$ and the θ_{ja} is 42°C/W, the junction temperature does not exceed 125°C. In this case, the AK4951A will not be damaged by its internal power dissipation. Therefore, the AK4951A should be used in the condition of $\theta_{ja} \leq 42^\circ\text{C/W}$.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions
--

(VSS1=VSS2=VSS3 =0V; [Note 2](#))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 6)	Analog	AVDD	2.8	3.3	3.5	V
	Digital	DVDD	1.6	1.8	1.98	V
	Digital I/O (Note 7)	TVDD	1.6 or (DVDD-0.2)	1.8	3.5	V
	Speaker-Amp	SVDD	1.8	3.3	5.5	V

Note 2. All voltages are with respect to ground.

Note 6. The power-up sequence between AVDD, DVDD, TVDD and SVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

Note 7. The minimum value is higher voltage between DVDD-0.2 and 1.6V.

*** When SVDD is powered ON and the PDN pin is "L", AVDD, DVDD and TVDD can be powered ON/OFF. When TVDD is powered ON and the PDN pin is "L", AVDD, DVDD and SVDD can be powered ON/OFF. The PDN pin must be set to "H" after all power supplies are ON, when the AK4951A is powered-up from power-down state.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

■ Analog Characteristics

(Ta=25°C; AVDD=SVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3=0V; fs=48kHz, BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Bandwidth=20Hz ~ 20kHz; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
MIC Amplifier: LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins					
Input Resistance		20	30	40	kΩ
Gain	Gain Setting	0	-	+30	dB
	Step Width	-	3	-	dB
MIC Power Supply: MPWR1, MPWR2 pins					
Output Voltage	MICL bit = "0"	2.2	2.4	2.6	V
	MICL bit = "1"	1.8	2.0	2.2	V
Output Noise Level (A-weighted)		-	-108	-	dBV
Load Resistance		1.0	-	-	kΩ
Load Capacitance		-	-	30	pF
PSRR (f = 1kHz) (Note 8)		-	100	-	dB
ADC Analog Input Characteristics: LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins → ADC(Programmable Filter = OFF) → SDTO					
Resolution		-	-	24	Bits
Input Voltage (Note 9)	(Note 10)	-	0.261	-	Vpp
	(Note 11)	1.86	2.07	2.28	Vpp
S/(N+D) (-1dBFS)	(Note 10)	73	83	-	dBFS
	(Note 11)	-	85	-	dBFS
D-Range (-60dBFS, A-weighted)	(Note 10)	78	88	-	dB
	(Note 11)	-	96	-	dB
S/N (A-weighted)	(Note 10)	78	88	-	dB
	(Note 11)	-	96	-	dB
Interchannel Isolation	(Note 10)	75	100	-	dB
	(Note 11)	-	110	-	dB
Interchannel Gain Mismatch	(Note 10)	-	0	0.5	dB
	(Note 11)	-	0	0.5	dB
PSRR (f = 1kHz) (Note 8)		-	80	-	dB

Note 8. PSRR applied to AVDD with 500mVpp sine wave.

Note 9. Vin = 0.9 x 2.3Vpp (typ) @MGAIN3-0 bits = "0000" (0dB)

Note 10. MGAIN3-0 bits = "0110" (+18dB)

Note 11. MGAIN3-0 bits = "0000" (0dB)

Parameter	Min.	Typ.	Max.	Unit		
DAC Characteristics:						
Resolution	-	-	24	Bits		
Headphone-Amp Characteristics: DAC → HPL, HPR pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=16Ω						
Output Voltage (0dBFS)	1.44	1.60	1.76	V _{pp}		
S/(N+D)	R _L =16Ω	50	75	-	dB	
	R _L =10kΩ	-	80	-	dB	
S/N (A-weighted)	87	97	-	dB		
Interchannel Isolation	65	80	-	dB		
Interchannel Gain Mismatch	-	0	0.8	dB		
Output Offset Voltage	-1	0	+1	mV		
Load Resistance	16	-	-	Ω		
Load Capacitance	-	-	300	pF		
PSRR (f = 1kHz) (Note 12)	AVDD	-	74	-	dB	
	DVDD	-	90	-	dB	
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=8Ω, BTL						
Output Voltage						
SPKG1-0 bits = "00", -0.5dBFS (Po=150mW)		-	3.18	-	V _{pp}	
SPKG1-0 bits = "01", -0.5dBFS (Po=250mW)		3.20	4.00	4.80	V _{pp}	
SPKG1-0 bits = "10", -0.5dBFS (Po=400mW)		-	1.79	-	V _{rms}	
SPKG1-0 bits = "11", -0.5dBFS (Po=1000mW) (SVDD=5V)		-	2.83	-	V _{rms}	
S/(N+D)						
SPKG1-0 bits = "00", -0.5dBFS (Po=150mW)		-	80	-	dB	
SPKG1-0 bits = "01", -0.5dBFS (Po=250mW)		40	75	-	dB	
SPKG1-0 bits = "10", -0.5dBFS (Po=400mW)		-	20	-	dB	
SPKG1-0 bits = "11", -0.5dBFS (Po=1000mW) (SVDD=5V)		-	20	-	dB	
S/N (A-weighted)	SPKG1-0 bits = "01"	80	99	-	dB	
Output Offset Voltage	SPKG1-0 bits = "01"	-30	0	+30	mV	
Load Resistance		8	-	-	Ω	
Load Capacitance		-	-	100	pF	
PSRR (f = 1kHz) (Note 13)	AVDD	-	80	-	dB	
	SVDD	-	60	-	dB	
Stereo Line Output Characteristics: DAC → LOU_T, ROU_T pins, ALC=OFF, IVOL=DVOL = 0dB, R_L=10kΩ, LVCM1-0 bits = "01"						
Output Voltage	(0dBFS)	LVCM0 bit = "0", SVDD=2.8V	-	2.26	-	V _{pp}
		LVCM0 bit = "1"	-	1.0	-	V _{rms}
	(-3dBFS)	LVCM0 bit = "0", SVDD=2.8V	1.44	1.6	1.76	V _{pp}
		LVCM0 bit = "1"	1.82	2.0	2.22	V _{pp}
S/(N+D)	(0dBFS)	LVCM0 bit = "0", SVDD=2.8V	-	80	-	dB
		LVCM0 bit = "1"	-	80	-	dB
	(-3dBFS)		75	85	-	dB
S/N (A-weighted)		82	94	-	dB	
Interchannel Isolation		-	100	-	dB	
Interchannel Gain Mismatch		-	0	0.8	dB	
Load Resistance		10	-	-	kΩ	
Load Capacitance		-	-	30	pF	

Note 12. PSRR applied with 500mV_{pp} sine wave.

Note 13. PSRR applied to AVDD or SVDD with 500mV_{pp} sine wave.

Parameter	Min.	Typ.	Max.	Unit
Mono Input: BEEP pin (PMBP bit = "1", BPVCM bit = "0", BPLVL3-0 bits = "0000")				
Input Resistance	46	66	86	kΩ
Maximum Input Voltage (Note 14)	-	-	1.54	Vpp
Gain				
BEEP pin → HPL, HPR pins	-1	0	+1	dB
BEEP pin → SPP/SPN pins (Note 15)				
SPKG1-0 bits = "00"	+4.4	+6.4	+8.4	dB
SPKG1-0 bits = "01"	-	+8.4	-	dB
SPKG1-0 bits = "10"	-	+11.1	-	dB
SPKG1-0 bits = "11"	-	+14.9	-	dB
BEEP pin → LOU, ROUT pins				
LVCM1-0 bits = "00"	-1	0	+1	dB
LVCM 1-0 bits = "01"	-	+2	-	dB
LVCM 1-0 bits = "10"	-	+2	-	dB
LVCM 1-0 bits = "11"	-	+4	-	dB
Power Supplies:				
Power Up (PDN pin = "H")				
MIC + ADC + DAC + Headphone out				
AVDD+DVDD+TVDD (Note 16)	-	6.5	9.8	mA
AVDD+DVDD+TVDD (Note 17)	-	5.7	-	mA
SVDD (No Load)	-	36	54	μA
MIC + ADC + DAC + Speaker out				
AVDD+DVDD+TVDD (Note 18)	-	5.6	8.4	mA
AVDD+DVDD+TVDD (Note 19)	-	4.7	-	mA
SVDD (No Load)	-	1.8	2.7	mA
Power Down (PDN pin = "L") (Note 20)				
AVDD+DVDD+TVDD+SVDD	-	0	10	μA
SVDD (Note 21)	-	0	10	μA

Note 14. The maximum value is AVDD Vpp when BPVCM bit = "1". However, a click noise may occur when the amplitude after BEEP-Amp is 0.5Vpp or more. (set by BPLVL3-0 bits)

Note 15. The gain is in inverse proportion to external input resistance.

Note 16. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMHPL=PMHPR=PMVCM=PMPLL =PMBP=PMMP=M/S bits = "1". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 4.4mA (typ), DVDD= 2.0mA (typ), TVDD= 0.08mA (typ).

Note 17. When EXT Slave Mode (PMPLL=M/S bits = "0"), PMADL=PMADR=PMDAC=PMHPL=PMHPR=PMVCM=PMBP=PMMP bits = "1", and PMPFIL bit = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 4.2mA (typ), DVDD= 1.5mA (typ), TVDD= 0.02mA (typ).

Note 18. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMSL=PMVCM= PMPLL =PMBP=PMMP=SLPSN=DACS=M/S bits = "1". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 3.8mA, DVDD= 1.7mA (typ), TVDD= 0.08mA (typ).

Note 19. When EXT Slave Mode (PMPLL=M/S bits = "0"), PMADL=PMADR=PMDAC=PMSL=PMVCM= PMBP=PMMP=SLPSN=DACS bits = "1", and PMPFIL bit = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 3.5mA, DVDD= 1.2mA (typ), TVDD= 0.02mA (typ).

Note 20. All digital input pins are fixed to TVDD or VSS2.

Note 21. When AVDD, DVDD and TVDD are powered OFF.

■ Power Consumption on Each Operation Mode

Conditions: Ta=25°C; AVDD=SVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3=0V; fs=48kHz, Programmable Filter=OFF, External Slave Mode, BICK=64fs; LIN1/RIN1 input = No signal; SDTI input = No data; Headphone & Speaker outputs = No load.

Table 1. Power Consumption on Each Operation Mode (typ)

Mode	Power Management Bit									AVDD [mA]	DVDD [mA]	TVDD [mA]	SVDD [mA]	Total Power [mW]
	PMVCM	PMSL	PMDAC	PMADL	PMADR	PMHPL	PMHPR	PMFFIL	LOSEL					
All Power-down	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LIN1/RIN1 → ADC	1	0	0	1	1	0	0	0	0	2.40	0.75	0.02	0	9.3
LIN1 (Mono) → ADC	1	0	0	1	0	0	0	0	0	1.62	0.75	0.02	0	6.7
DAC → HP	1	0	1	0	0	1	1	0	0	2.15	0.80	0.02	0	8.6
DAC → SPK	1	1	1	0	0	0	0	0	0	1.50	0.50	0.02	1.80	11.8
DAC → Line out	1	1	1	0	0	0	0	0	1	1.68	0.50	0.02	0.34	7.6
LIN1/RIN1 → ADC & DAC → HP	1	0	1	1	1	1	1	0	0	3.75	1.55	0.02	0	15.2
LIN1/RIN1 → ADC & DAC → SPK	1	1	1	1	1	0	0	0	0	3.10	1.25	0.02	1.80	18.5
LIN1/RIN1 → ADC & DAC → Line out	1	1	1	1	1	0	0	0	1	3.30	1.25	0.02	0.34	14.3

■ Filter Characteristics

(Ta =25°C; fs=48kHz; AVDD=2.8 ~ 3.5V, SVDD=1.8 ~ 5.5V, DVDD = 1.6 ~ 1.98V, TVDD = 1.6 or (DVDD-0.2)~ 3.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 22)	±0.16dB	PB	0	-	18.8	kHz
	-0.66dB		-	21.1	-	kHz
	-1.1dB		-	21.7	-	kHz
	-6.9dB		-	24.1	-	kHz
Stopband (Note 22)		SB	28.4	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 23)		GD	-	17	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response (Note 22)	-3.0dB	FR	-	3.7	-	Hz
	-0.5dB		-	10.9	-	Hz
	-0.1dB		-	23.9	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 22)	±0.05dB	PB	0	-	21.8	kHz
	-6.0dB		-	24	-	kHz
Stopband (Note 22)		SB	27.0	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 23)		GD	-	29	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 22. The passband and stopband frequencies scale with fs (sampling frequency).

Note 23. A calculating delay time which is induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the DAC, this time is from setting the 24-bit data of a channel from the input register to the output of analog signal. For the signal through the programmable filters (Microphone Sensitivity Correction + Automatic Wind Noise Reduction Filter + 1st order HPF + 1st order LPF + Stereo Separation Emphasis + 4-band Equalizer + ALC + 1-band Equalizer), the group delay is increased by 4/fs from the value above in both recording and playback modes if there is no phase change by the IIR filter.

■ DC Characteristics

(Ta =25°C; fs=48kHz; AVDD=2.8 ~ 3.5V, SVDD= 1.8 ~ 5.5V, DVDD = 1.6 ~ 1.98V, TVDD = 1.6 or (DVDD-0.2) ~ 3.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Audio Interface & Serial μP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)						
High-Level Input Voltage	(TVDD \geq 2.2V)	VIH	70%TVDD	-	-	V
	(TVDD < 2.2V)	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	(TVDD \geq 2.2V)	VIL	-	-	30%TVDD	V
	(TVDD < 2.2V)	VIL	-	-	20%TVDD	V
Input Leakage Current		lin1	-	-	\pm 10	μ A
Audio Interface & Serial μP Interface (CDTIO, SDA, BICK, LRCK, SDTO pins Output)						
High-Level Output Voltage	(Iout = -80 μ A)	VOH	TVDD-0.2	-	-	V
Low-Level Output Voltage (Except SDA pin : Iout = 80 μ A)		VOL1	-	-	0.2	V
	(SDA pin, 2.0V \leq TVDD \leq 3.5V: Iout = 3mA)	VOL2	-	-	0.4	V
	(SDA pin, 1.6V \leq TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Digital Microphone Interface (DMDAT pin Input; DMIC bit = "1")						
High-Level Input Voltage		VIH2	65%AVDD	-	-	V
Low-Level Input Voltage		VIL2	-	-	35%AVDD	V
Input Leakage Current		lin2	-	-	\pm 10	μ A
Digital Microphone Interface (DMCLK pin Output; DMIC bit = "1")						
High-Level Output Voltage	(Iout=-80 μ A)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage	(Iout= 80 μ A)	VOL3	-	-	0.4	V

■ Switching Characteristics

(Ta=25°C; fs=48kHz; CL=20pF; AVDD=2.8~3.5V, SVDD=1.8~5.5V, DVDD=1.6~1.98V, TVDD=1.6 or (DVDD-0.2)~3.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency	PLL3-0 bits = "0100"	fCLK	-	11.2896	-	MHz
	PLL3-0 bits = "0101"	fCLK	-	12.288	-	MHz
	PLL3-0 bits = "0110"	fCLK	-	12	-	MHz
	PLL3-0 bits = "0111"	fCLK	-	24	-	MHz
	PLL3-0 bits = "1100"	fCLK	-	13.5	-	MHz
	PLL3-0 bits = "1101"	fCLK	-	27	-	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	s	
Pulse Width High	tCLKH	0.4/fCLK	-	-	s	
LRCK Output Timing						
Frequency	fs	-	Table 7	-	Hz	
Duty Cycle	Duty	-	50	-	%	
BICK Output Timing						
Frequency	BCKO bit = "0"	fBCK	-	32fs	-	Hz
	BCKO bit = "1"	fBCK	-	64fs	-	Hz
Duty Cycle	dBCK	-	50	-	%	
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency	PLL3-0 bits = "0010"	fs	-	fBCK/32	-	Hz
	PLL3-0 bits = "0011"	fs	-	fBCK/64	-	Hz
Duty	Duty	45	-	55	%	
BICK Input Timing						
Frequency	PLL3-0 bits = "0010"	fBCK	0.256	-	1.536	MHz
	PLL3-0 bits = "0011"	fBCK	0.512	-	3.072	MHz
Pulse Width Low	tBCKL	0.4/fBCK	-	-	s	
Pulse Width High	tBCKH	0.4/fBCK	-	-	s	
External Slave Mode						
MCKI Input Timing						
Frequency	CM1-0 bits = "00"	fCLK	-	256fs	-	Hz
	CM1-0 bits = "01"	fCLK	-	384fs	-	Hz
	CM1-0 bits = "10"	fCLK	-	512fs	-	Hz
	CM1-0 bits = "11"	fCLK	-	1024fs	-	Hz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	s	
Pulse Width High	tCLKH	0.4/fCLK	-	-	s	
LRCK Input Timing						
Frequency	CM1-0 bits = "00"	fs	8	-	48	kHz
	CM1-0 bits = "01"	fs	8	-	48	kHz
	CM1-0 bits = "10"	fs	8	-	48	kHz
	CM1-0 bits = "11"	fs	8	-	24	kHz
Duty	Duty	45	-	55	%	
BICK Input Timing						
Frequency	fBCK	32fs	-	64fs	Hz	
Pulse Width Low	tBCKL	130	-	-	ns	
Pulse Width High	tBCKH	130	-	-	ns	

Parameter	Symbol	Min.	Typ.	Max.	Unit	
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	2.048	-	12.288	MHz
	384fs	fCLK	3.072	-	18.432	MHz
	512fs	fCLK	4.096	-	24.576	MHz
	1024fs	fCLK	8.192	-	24.576	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing						
Frequency	CM1-0 bits = "00"	fs	-	fCLK/256	-	Hz
	CM1-0 bits = "01"	fs	-	fCLK/384	-	Hz
	CM1-0 bits = "10"	fs	-	fCLK/512	-	Hz
	CM1-0 bits = "11"	fs	-	fCLK/1024	-	Hz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Frequency	BCKO bit = "0"	fBCK	-	32fs	-	Hz
	BCKO bit = "1"	fBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%
Audio Interface Timing						
Master Mode						
BICK "↓" to LRCK Edge (Note 24)		tBLR	-40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I ² S mode)		tLRD	-70	-	70	ns
BICK "↓" to SDTO		tBSD	-70	-	70	ns
SDTI Hold Time		tSDH	50	-	-	ns
SDTI Setup Time		tSDS	50	-	-	ns
Slave Mode						
LRCK Edge to BICK "↑" (Note 24)		tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 24)		tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I ² S mode)		tLRD	-	-	80	ns
BICK "↓" to SDTO		tBSD	-	-	80	ns
SDTI Hold Time		tSDH	50	-	-	ns
SDTI Setup Time		tSDS	50	-	-	ns
Digital Audio Interface Timing; C_L=100pF						
DMCLK Output Timing						
Period		tSCK	-	1/(64fs)	-	s
Rising Time		tSRise	-	-	10	ns
Falling Time		tSFall	-	-	10	ns
Duty Cycle		dSCK	40	50	60	%
Audio Interface Timing						
DMDAT Setup Time		tDSDS	50	-	-	ns
DMDAT Hold Time		tDSDH	0	-	-	ns

Note 24. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I²C Bus)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 26)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 29)	tAPD	200	-	-	ns
PDN Reject Pulse Width (Note 29)	tRPD	-	-	50	ns
PMADL or PMADR “↑” to SDTO valid (Note 30)					
ADRST1-0 bits =“00”	tPDV	-	1059	-	1/fs
ADRST1-0 bits =“01”	tPDV	-	267	-	1/fs
ADRST1-0 bits =“10”	tPDV	-	531	-	1/fs
ADRST1-0 bits =“11”	tPDV	-	135	-	1/fs
VCOM Voltage					
Rising Time (Note 31)	tRVCM	-	0.6	2.0	ms

Note 25. I²C Bus is a trademark of NXP B.V.

Note 26. Data must be held for sufficient time to bridge the 300ns transition time of SCL.

Note 27. CCLK rising edge must not occur at the same time as CSN edge.

Note 28. It is the time of 10% potential change of the CDTIO pin when R_L = 1kΩ (pull-up or TVDD).

Note 29. The AK4951A can be reset by the PDN pin = “L”. The PDN pin must be held “L” for more than 200ns for a certain reset. The AK4951A is not reset by the “L” pulse less than 50ns.

Note 30. This is the count of LRCK “↑” from the PMADL or PMADR bit = “1”.

Note 31. All analog blocks including PLL block are powered up after the VCOM voltage (VCOM pin) rises up. An external capacitor of the VCOM pin is 2.2μF and the REGFIL pin is 2.2μF. The capacitance variation should be ±50%.

■ Timing Diagram

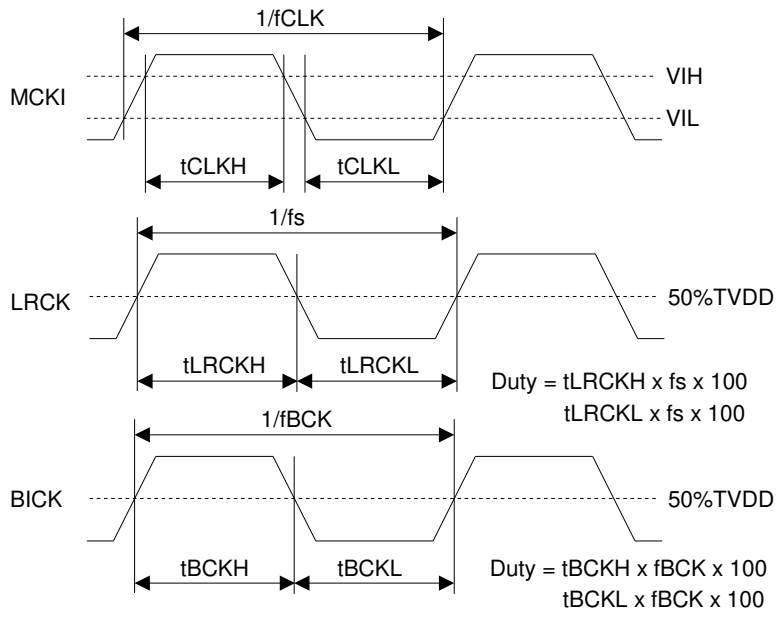


Figure 3. Clock Timing (PLL/EXT Master mode)

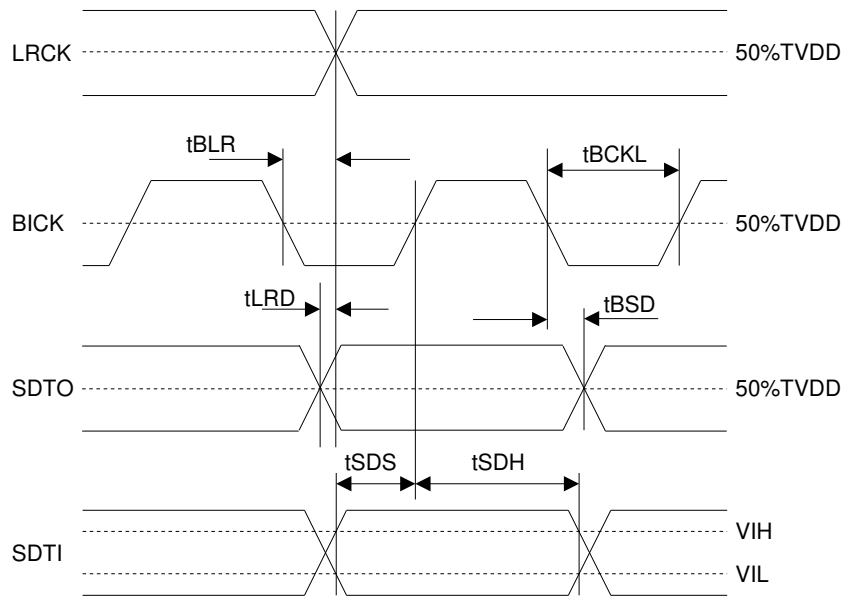


Figure 4. Audio Interface Timing (PLL/EXT Master mode)

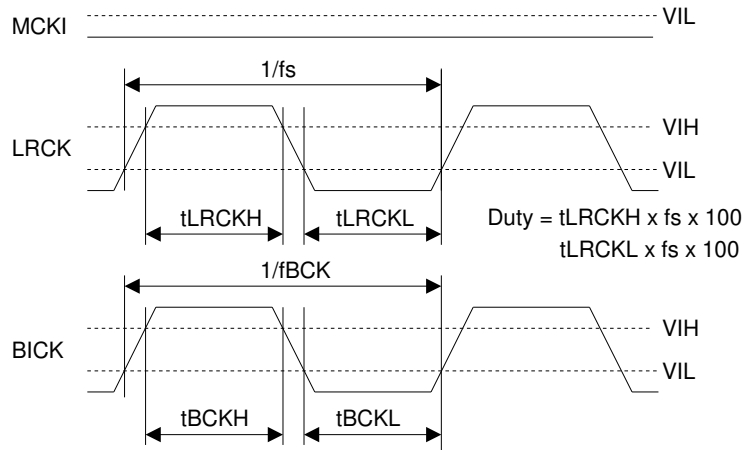


Figure 5. Clock Timing (PLL Slave mode)

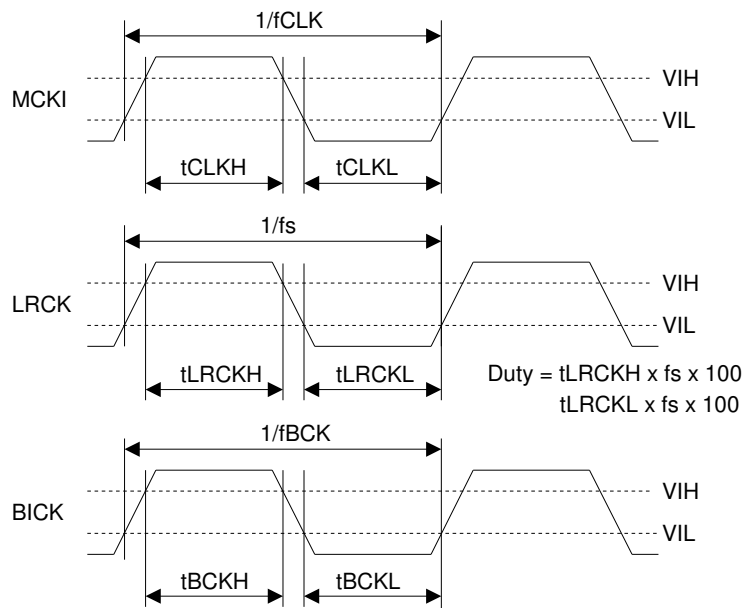


Figure 6. Clock Timing (EXT Slave mode)

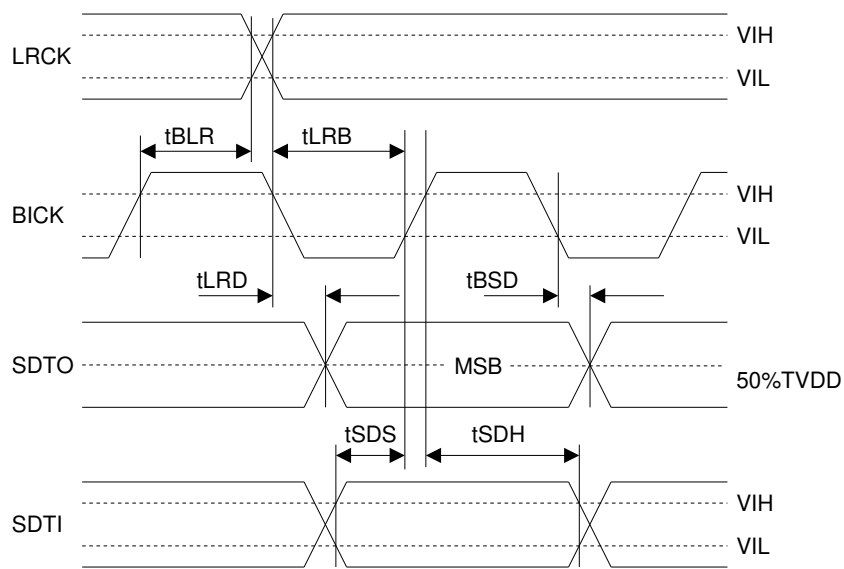


Figure 7. Audio Interface Timing (PLL/EXT Slave mode)

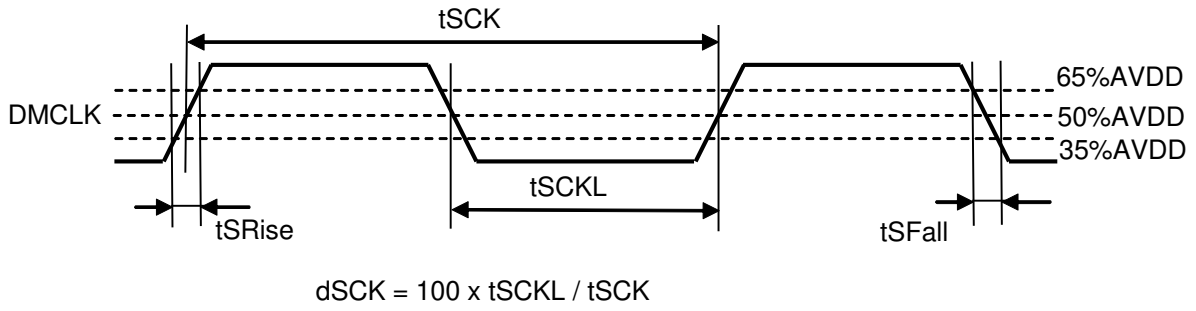


Figure 8. DMCLK Clock Timing

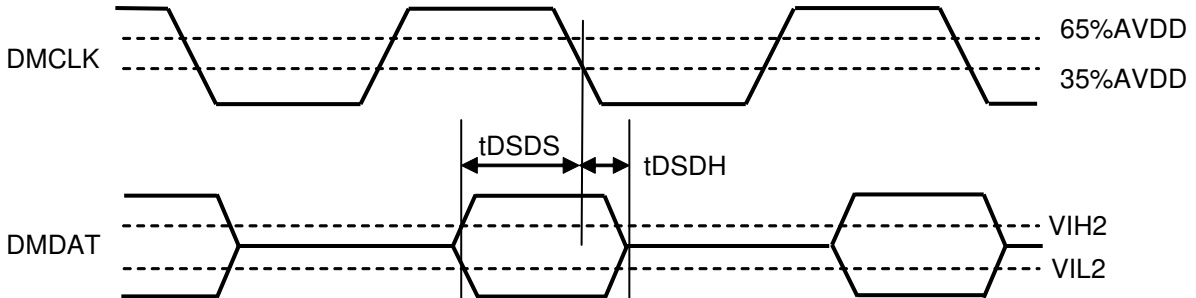


Figure 9. Audio Interface Timing (DCLKP bit = "1")

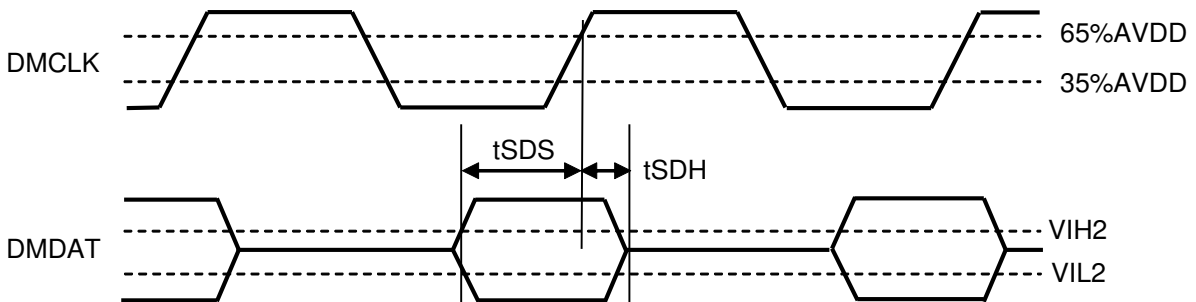


Figure 10. Audio Interface Timing (DCLKP bit = "0")

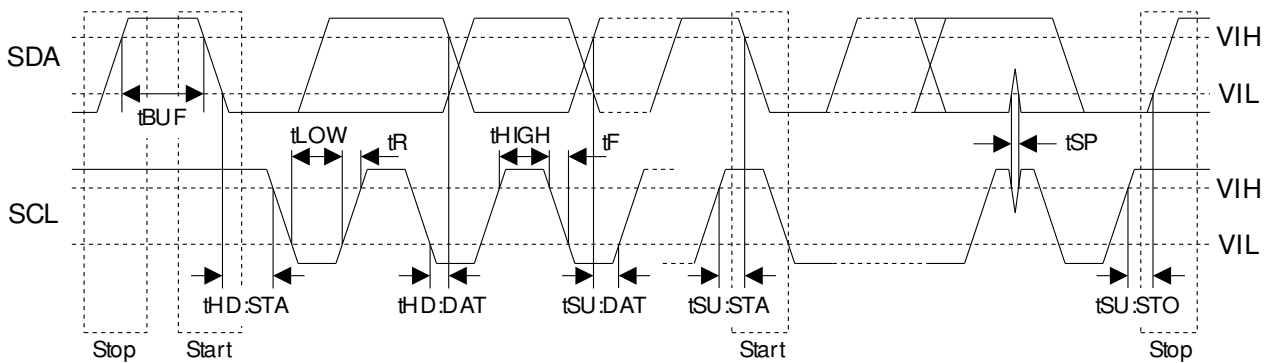


Figure 11. I²C Bus Mode Timing

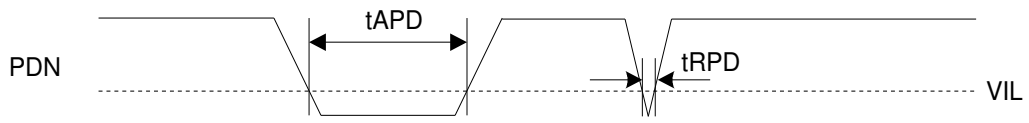


Figure 12. Power Down & Reset Timing 1

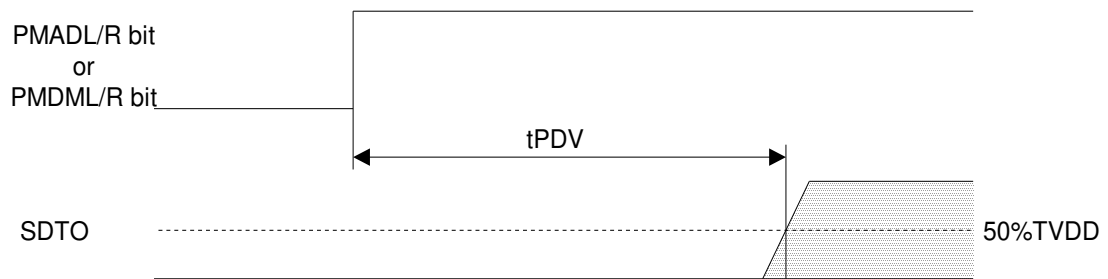


Figure 13. Power Down & Reset Timing 2

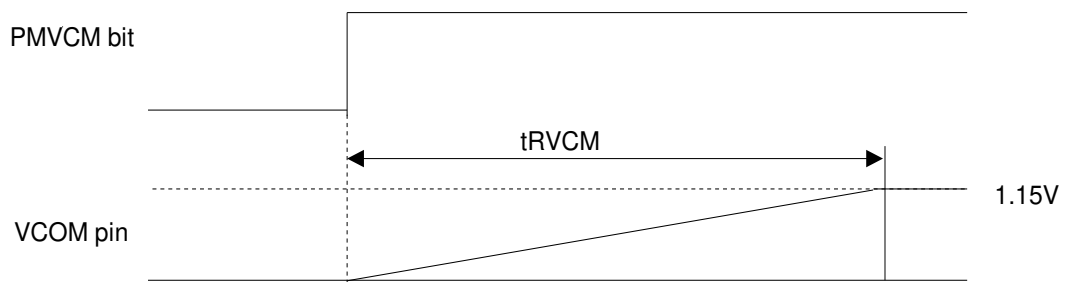


Figure 14. VCOM Rising Timing

9. Functional Descriptions

■ System Clock

There are the following four clock modes to interface with external devices (Table 2, Table 3).

Table 2. Clock Mode Setting

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode	1	1	Table 5	Figure 15
PLL Slave Mode (PLL Reference Clock: BICK pin)	1	0	Table 5	Figure 16
EXT Slave Mode	0	0	x	Figure 17
EXT Master Mode	0	1	x	Figure 18

(x: Do not care)

Table 3. Clock pins state in Clock Mode

Mode	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	Input Frequency of Table 5 (Selected by PLL3-0 bits)	Output (Selected by BCKO bit)	Output (1fs)
PLL Slave Mode (PLL Reference Clock: BICK pin)	GND	Input (Selected by PLL3-0 bits)	Input (1fs)
EXT Slave Mode	Input Frequency of Table 11 (Selected by CM1-0 bits)	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	Input Frequency of Table 14 (Selected by CM1-0 bits)	Output (Selected by BCKO bit)	Output (1fs)

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = “1” selects master mode and “0” selects slave mode. When the AK4951A is in power-down mode (PDN pin = “L”) and when exits reset state, the AK4951A is in slave mode. After exiting reset state, the AK4951A goes to master mode by changing M/S bit to “1”.

When the AK4951A is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes “1”. The LRCK and BICK pins of the AK4951A must be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

Table 4. Select Master/Slave Mode

M/S bit	Mode
0	Slave Mode
1	Master Mode

(default)

■ PLL Mode

When PMPLL bit is “1”, a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by PLL3-0 and FS3-0 bits. The PLL lock times, when the AK4951A is supplied stable clocks after PLL is powered-up (PMPLL bit = “0” → “1”) or the sampling frequency is changed, are shown in [Table 5](#).

1) PLL Mode Reference Clock Setting

Table 5. PLL Mode Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)
0	0	0	0	0	MCKI pin	16MHz	5ms
2	0	0	1	0	BICK pin	32fs	2ms
3	0	0	1	1	BICK pin	64fs	2ms
4	0	1	0	0	MCKI pin	11.2896MHz	5ms
5	0	1	0	1	MCKI pin	12.288MHz	5ms
6	0	1	1	0	MCKI pin	12MHz	5ms
7	0	1	1	1	MCKI pin	24MHz	5ms
12	1	1	0	0	MCKI pin	13.5MHz	5ms
13	1	1	0	1	MCKI pin	27MHz	5ms
Others	Others			N/A			

(default)

(*fs: Sampling Frequency, N/A: Not Available)

2) Setting of sampling frequency in PLL Mode (PLL reference clock input pin = MCKI pin)

When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in [Table 6](#).

Table 6. Setting of Sampling Frequency (Reference Clock = MCKI pin)

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (Note 32)
0	0	0	0	0	8kHz mode
1	0	0	0	1	12kHz mode
2	0	0	1	0	16kHz mode
5	0	1	0	1	11.025kHz mode
7	0	1	1	1	22.05kHz mode
9	1	0	0	1	24kHz mode
10	1	0	1	0	32kHz mode
11	1	0	1	1	48kHz mode
15	1	1	1	1	44.1kHz mode
Others	Others				N/A

(default)

(N/A: Not Available)

Note 32. When the MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL3-0 bits) and sampling frequency (FS3-0 bits). Refer to [Table 7](#) for the details of sampling frequency. In master mode, LRCK and BICK output frequency correspond to sampling frequencies shown in [Table 7](#).