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AK4951

24bit Stereo CODEC with MIC/HP/SPK-AMP

1. General Description

The AK4951 is a low power 24-bit stereo CODEC with a microphone, headphone and speaker amplifiers.

The AK4951 supports sampling frequency from 8kHz to 48kHz. It is suitable for a wide range of application from speech signal processing for narrowband, wideband and super wideband to sound signal processing for audio band.

The input circuits include a microphone amplifier, an automatic wind noise reduction filter of the proprietary algorithms and a high performance digital ALC (automatic level control) circuit, therefore the AK4951 can record with high-quality sound regardless of whether indoors or outdoors. In addition, the output circuits include a cap-less headphone amplifier with a negative voltage generated by charge pump circuit and a speaker amplifier with 1W output power. It is suitable for various products as well as portable applications with recording/playback function.

The AK4951 are available in a small 32-pin QFN (4mm x 4mm, 0.4mm pitch: AK4951EN) and a 32-pin BGA (3.5mm x 3.5mm, 0.5mm pitch: AK4951EG) packages saving mounting area on the board.

Application:

- **IP Camera**
- **Digital Camera**
- **IC Recorder**
- **Tablet**
- **Wireless Headphone**
- **Headset**

2. Features

1. Recording Functions

- **Analog Input**
  (AK4951EN) 3 Stereo Single-ended inputs with Selectors
  (AK4951EG) 2 Stereo and 1 Monaural Single-ended inputs with Selectors
- **Microphone Amplifier: +30dB ~ 0dB, 3dB Step**
- **Microphone Power Supply: 2.0V or 2.4V, Noise Level= –108dBV**
- **Digital ALC (Automatic Level Control)**
  - Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute
- **ADC Performance: S/(N+D): 83dB, DR, S/N: 88dB (MIC-Amp=+18dB)**
  S/(N+D): 85dB, DR, S/N: 96dB (MIC-Amp=0dB)
- **Microphone Sensitivity Correction**
- **Automatic Wind Noise Reduction Filter**
- **5-Band Notch Filter: Include Dynamic Gain Control**
- **Stereo Separation Emphasis Circuit**
- **Digital Microphone Interface**

2. **Playback Functions**
   - **Digital ALC (Automatic Level Control)**
     - **Setting Range: +36dB ~ –52.5dB, 0.375dB Step & Mute**
   - **Sidetone Mixer & Volume Control (0dB ~ –18dB, 6dB Step)**
   - **Digital Volume Control**
     - **+12dB ~ –89.5dB, 0.5dB Step & Mute**
   - **Capacitor-less Stereo Headphone Amplifier**
     - **HP-Amplifier Performance: S/(N+D): 75dB@20mW, S/N: 97dB**
     - **Output Power: 20mW@16Ω**
     - **Pop Noise Free at Power-ON/OFF**
   - **Mono Speaker Amplifier (with Stereo Line Output Switch)**
     - **Speaker Amplifier Performance: S/(N+D): 75dB@250mW, S/N: 90dB**
     - **BTL Output**
     - **Output Power:**
       (AK4951EN) 400mW@8Ω (SVDD=3.3V), 1W@8Ω (SVDD=5V)
       (AK4951EG) 400mW@8Ω (AVDD=3.3V)
   - **Analog Mixing: BEEP Input**
3. **Power Management**
4. **Master Clock:**
   (1) PLL Mode
   Frequencies: 11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin), 32fs or 64fs (BICK pin)
   (2) External Clock Mode
   Frequencies: 256fs, 384fs, 512fs or 1024fs (MCKI pin)
5. **Sampling Frequencies**
   - **PLL Master Mode:**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **PLL Slave Mode (BICK pin): 8kHz ~ 48kHz**
   - **EXT Master/Slave Mode:**
     8kHz ~ 48kHz (256fs, 384fs, 512fs), 8kHz ~ 24kHz (1024fs)
6. **Master/Slave Mode**
7. **Audio Interface Format: MSB First, 2's complement**
   - **ADC: 16/24bit MSB justified, 16/24bit I^2S**
   - **DAC: 16/24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 16/24bit I^2S**
8. **μP I/F:**
   (AK4951EN) I^2C Bus (Ver 1.0, 400kHz Fast-Mode)
   (AK4951EG) 3-wire Serial, I^2C Bus (Ver 1.0, 400kHz Fast-Mode)
9. **Operating Temperature: Ta = –40 ~ 85°C**
10. **Power Supply**
    (AK4951EN)
    - **Analog Power Supply (AVDD): 2.8 ~ 3.5V**
    - **Speaker Power Supply (SVDD): 1.8 ~ 5.5V**
    - **Digital & Headphone Power Supply (DVDD): 1.6 ~ 1.98V**
    - **Digital I/O Power Supply (TVDD): 1.6 or (DVDD – 0.2) ~ 3.5V**

    (AK4951EG)
    - **Analog & Speaker Power Supply (AVDD): 2.8 ~ 3.5V**
    - **Digital & Headphone Power Supply (DVDD): 1.6 ~ 1.98V**
    - **Digital I/O Power Supply (TVDD): 1.6 or (DVDD – 0.2) ~ 3.5V**
11. **Package:**
    (AK4951EN)
    - **32-pin QFN (4 x 4 mm, 0.4mm pitch)**

    (AK4951EG)
    - **32-pin BGA (3.5 x 3.5 mm, 0.5mm pitch)**

3. Table of Contents

4. Block Diagram

[AK4951EN]

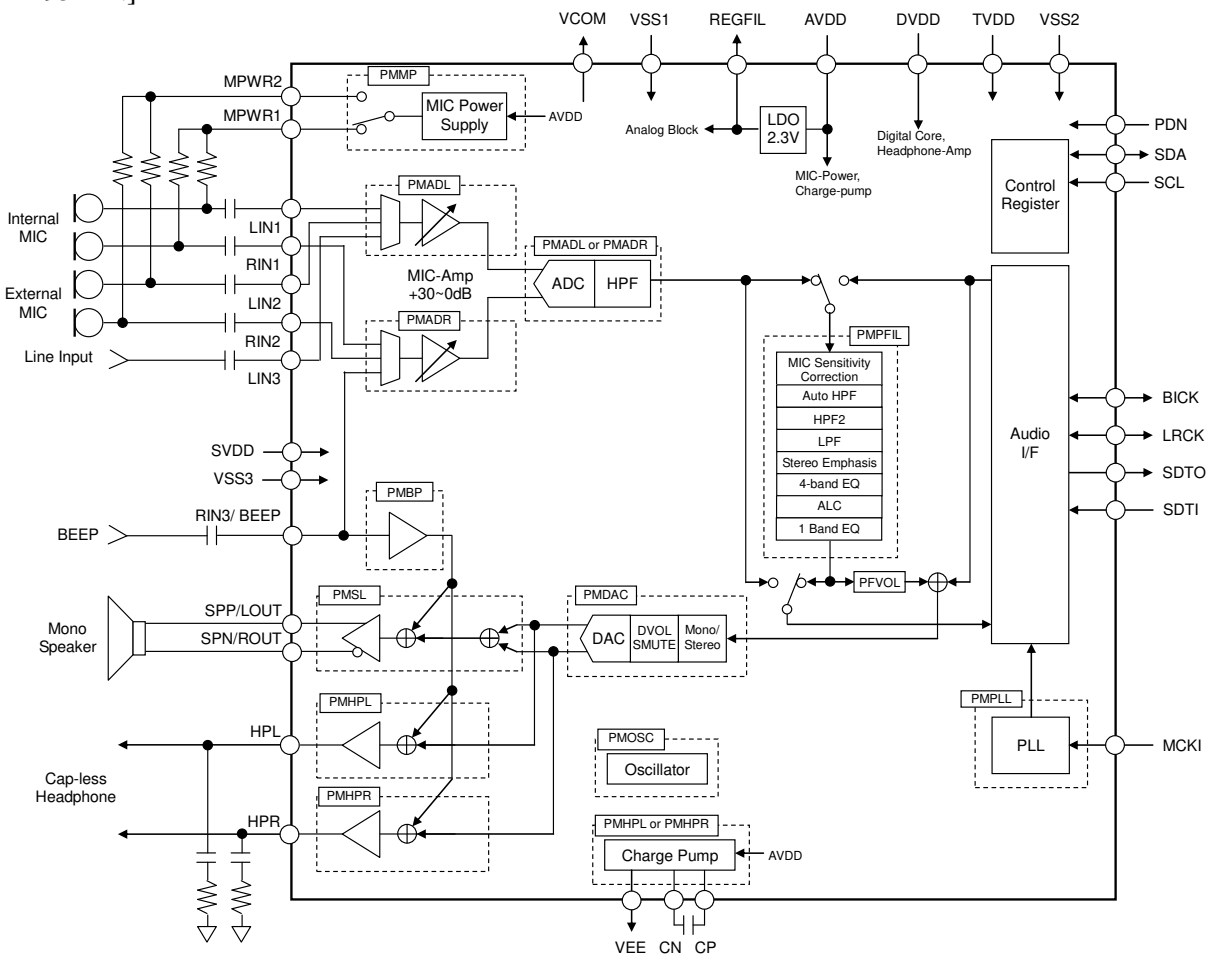


Figure 1. Block Diagram (AK4951EN)

[AK4951EG]

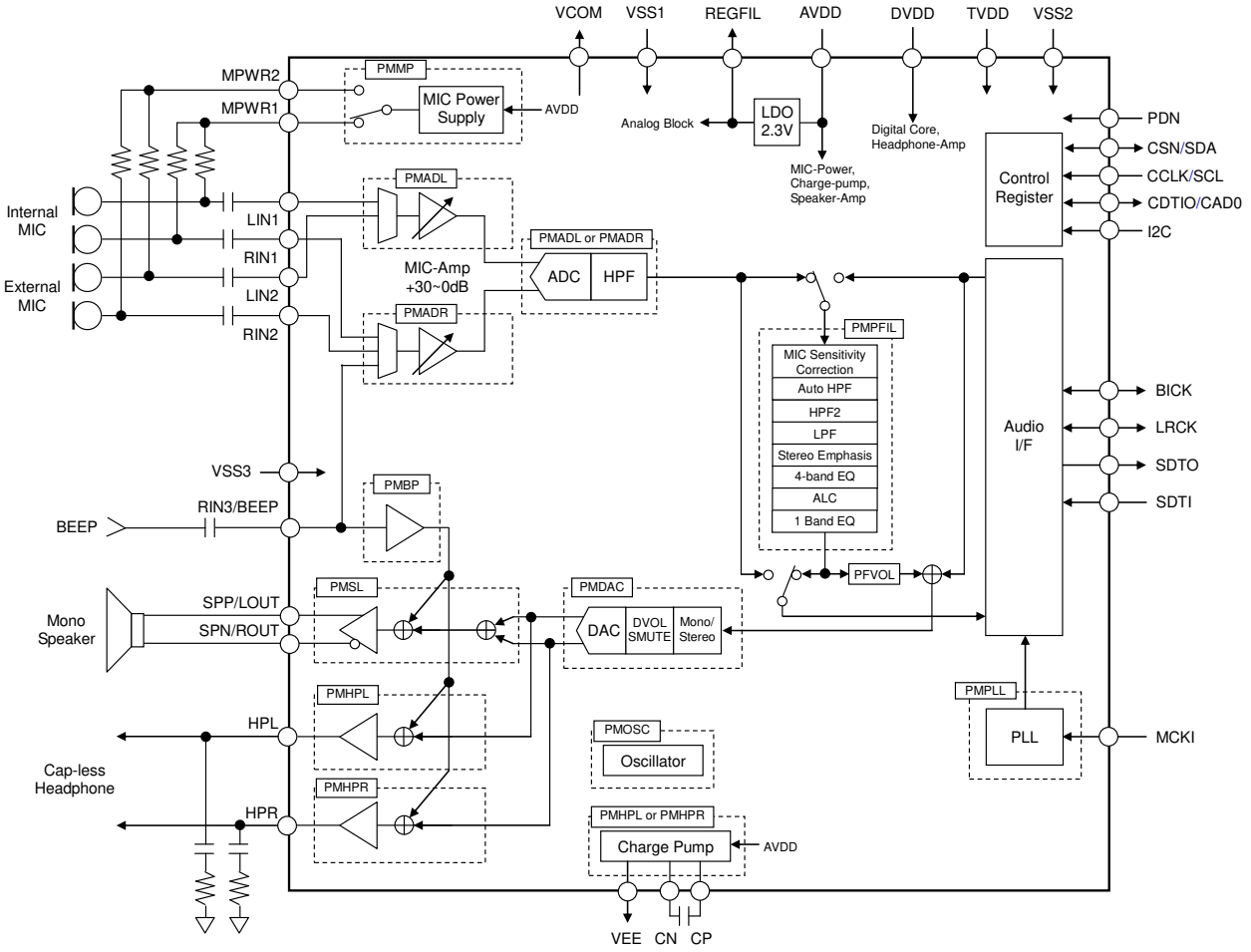


Figure 2. Block Diagram (AK4951EG)

5. Pin Configurations and Functions

■ Ordering Guide

AK4951EN	–40 ~ +85°C	32-pin QFN (0.4mm pitch)
AKD4951EN	Evaluation board for AK4951EN	
AK4951EG	–40 ~ +85°C	32-pin BGA (0.5mm pitch)
AKD4951EG	Evaluation board for AK4951EG	

■ Pin Layout

[AK4951EN]

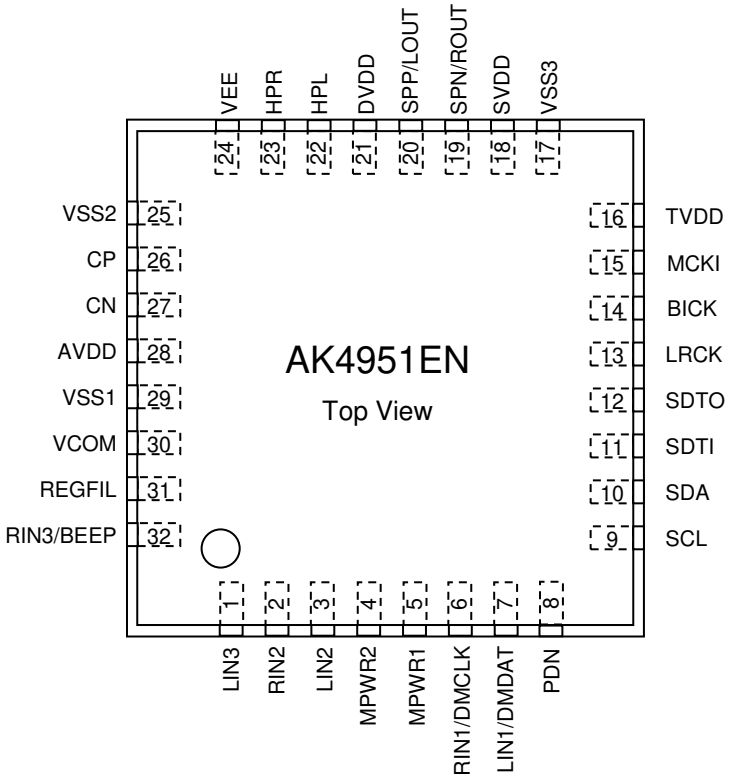
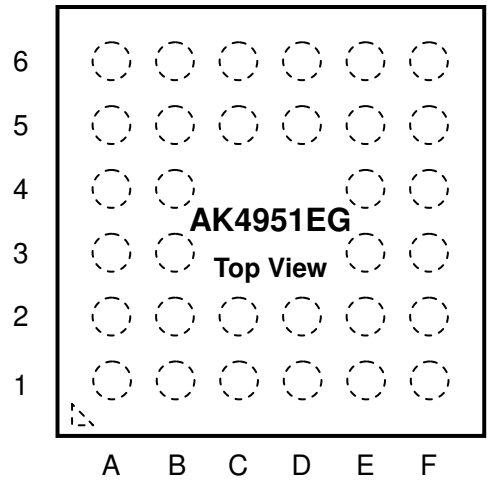


Figure 3. Pin Layout (AK4951EN)

[AK4951EG]



6	LIN2	RIN2	REGFIL	VSS1	AVDD	VSS2
5	MPWR2	MPWR1	RIN3 /BEEP	VCOM	CN	VEE
4	RIN1 /DMCLK	LIN1 /DMDAT			CP	HPR
3	PDN	CCLK /SCL			DVDD	HPL
2	CSN /SDA	SDTO	BICK	TVDD	SPP	SPN
1	SDTI	LRCK	MCKI	I2C	CDTIO /CAD0	VSS3
	A	B	C	D	E	F

Top View

Figure 4. Pin Layout (AK4951EG)

■ Comparison Table of the AK4954A

1. Function

Function	AK4954A	AK4951
Resolution	32bit	24bit
AVDD	2.5V ~ 3.5V	2.8V ~ 3.5V
SVDD	0.9V ~ 5.5V	1.8V ~ 5.5V
DVDD	1.6V ~ 1.98V	←
TVDD	1.6V or (DVDD-0.2)V ~ 3.5V	←
ADC DR, S/N	97dB @MGAIN = +20dB 100dB @MGAIN = 0dB	88dB @MGAIN = +18dB 96dB @MGAIN = 0dB
DAC(Headphone) S/N	100dB	97dB
Input Level	typ. 0.8 x AVDD @MGAIN=0dB	typ. 2.07Vpp @MGAIN=0dB
Output Level (Headphone)	typ. 0.485 x AVDD @DVOL=0dB	typ. 1.62Vpp @DVOL=0dB
MIC Power Output Voltage	typ. 2.3V (2 Line Outputs)	typ. 2.0V or 2.4V (2 Line Outputs)
MIC Power Output Noise	-120dBV (A-weighted)	-108dBV (A-weighted)
MIC-Amp Gain	+26dB/+20dB/+13dB/+6dB/0dB	+30dB ~ 0dB, 3dB Step
MIC Sensitivity Correction	No	Yes
Automatic Wind Noise Reduction	No	Yes
Output Volume	+36dB ~ -52.5dB, 0.375dB Step (Note 1) & +6dB ~ -65.5dB, 0.5dB Step	+36dB ~ -52.5dB, 0.375dB Step (Note 1) & +12dB ~ -89.5dB, 0.5dB Step
3-band DRC	Yes	No
Serial µP I/F	I^2C Bus	AK4951EN: I^2C Bus AK4951EG: 3-wire Serial, I^2C Bus
Power Consumption **(Stereo Recording)** **(Headphone Playback)**	 typ. 10.4mW (Low Power Mode) typ. 6.2mW (Low Power Mode)	 typ. 9.3mW typ. 8.6mW
Package	32-pin QFN (4 x 4mm, 0.4mm pitch)	AK4951EN: 32-pin QFN (4 x 4mm, 0.4mm pitch) AK4951EG: 32-pin BGA (3.5 x 3.5mm, 0.5mm pitch)

Note 1. ALC and Volume circuits are shared by input and output. Therefore, it is impossible to use ALC and Volume control function at the same time for both recording and playback mode.

2. Pin

Pin#	AK4954A	AK4951
15	MCKI/OVF	MCKI
31	MRF	REGFIL
32	RIN3	RIN3/BEEP

3. Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 1	PMPFIL	PMVCM	PMBP	0	~~LSV~~	PMDAC	PMADR	PMADL
01H	Power Management 2	PMOSC	0	PMHPR	PMHPL	M/S	PMPLL	PMSL	LOSEL
02H	Signal Select 1	SLPSN	MGAIN3	DACS	MPSEL	PMMP	MGAIN2	MGAIN1	MGAIN0
03H	Signal Select 2	SPKG1	SPKG0	0	MICL	INL1	INL0	INR1	INR0
04H	Signal Select 3	LVCM1	LVCM0	DACL	~~1~~	PTS1	PTS0	MONO1	MONO0
05H	Mode Control 1	PLL3	PLL2	PLL1	PLL0	BCKO	CKOFF	DIF1	DIF0
07H	Mode Control 3	TSDSEL	THDET	SMUTE	DVOLC	0	IVOLC	~~LPMIC~~	~~LPDA~~
09H	Timer Select	ADRST1	ADRST0	FRATT	FRN	~~OVTM1~~	~~OVTM0~~	MOFF	DVTM
0AH	ALC Timer Select	~~IVTM1~~	IVTM	EQFC1	EQFC0	WTM1	WTM0	RFST1	RFST0
0BH	ALC Mode Control 1	ALCEQN	LMTH2	ALC	RGAIN2	RGAIN1	RGAIN0	LMTH1	LMTH0
0FH	ALC Volume	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
11H	Rch MIC Gain Setting	MGR7	MGR6	MGR5	MGR4	MGR3	MGR2	MGR1	MGR0
12H	BEEP Control	HPZ	BPVCM	BEEPS	BEEPH	BPLVL3	BPLVL2	BPLVL1	BPLVL0
15H	EQ Common Gain Select	~~BPCNT~~	0	0	EQC5	EQC4	EQC3	EQC2	~~BPLVL0~~
16H	EQ2 Common Gain Setting	EQ2G5	EQ2G4	EQ2G3	EQ2G2	EQ2G1	EQ2G0	EQ2T1	EQ2T0
17H	EQ3 Common Gain Setting	EQ3G5	EQ3G4	EQ3G3	EQ3G2	EQ3G1	EQ3G0	EQ3T1	EQ3T0
18H	EQ4 Common Gain Setting	EQ4G5	EQ4G4	EQ4G3	EQ4G2	EQ4G1	EQ4G0	EQ4T1	EQ4T0
19H	EQ5 Common Gain Setting	EQ5G5	EQ5G4	EQ5G3	EQ5G2	EQ5G1	EQ5G0	EQ5T1	EQ5T0
1AH	Auto HPF Control	0	0	AHPF	SENC2	SENC1	SENC0	STG1	STG0
1BH	Digital Filter Select 1	0	0	0	0	~~SDAD~~	HPFC1	HPFC0	HPFAD
1DH	Digital Filter Mode	~~PMDRC~~	0	PFVOL1	PFVOL0	PFDAC1	PFDAC0	ADCPF	PFSDO
31H	Device Information	REV3	REV2	REV1	REV0	DVN3	DVN2	DVN1	DVN0
50H ~7FH	DRC Function								

These bits are added to the AK4951.
These bits are removed from the AK4951.
These bits are changed from the AK4951.

■ PIN/FUNCTION

[AK4951EN]

No.	Pin Name	I/O	Function
1	LIN3	I	Lch Analog Input 3 pin
2	RIN2	I	Rch Analog Input 2 Pin
3	LIN2	I	Lch Analog Input 2 pin
4	MPWR2	O	MIC Power Supply 2 Pin
5	MPWR1	O	MIC Power Supply 1 Pin
6	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0": default)
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")
7	LIN1	I	Lch Analog Input 1 Pin (DMIC bit = "0": default)
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
8	PDN	I	Reset & Power-down Pin "L": Reset & Power-down, "H": Normal Operation
9	SCL	I	Control Data Clock Pin
10	SDA	I/O	Control Data Input/Output Pin
11	SDTI	I	Audio Serial Data Input Pin
12	SDTO	O	Audio Serial Data Output Pin
13	LRCK	I/O	Input/Output Channel Clock Pin
14	BICK	I/O	Audio Serial Data Clock Pin
15	MCKI	I	External Master Clock Input Pin
16	TVDD	-	Digital I/O Power Supply Pin, 1.6 or (DVDD-0.2) ~ 3.5V
17	VSS3	-	Ground 3 Pin
18	SVDD	-	Speaker-Amp Power Supply Pin, 1.8 ~ 5.5V
19	SPN	O	Speaker-Amp Negative Output Pin (LOSEL bit = "0": default)
	ROUT	O	Rch Stereo Line Output Pin (LOSEL bit = "1")
20	SPP	O	Speaker-Amp Positive Output Pin (LOSEL bit = "0": default)
	LOUT	O	Lch Stereo Line Output Pin (LOSEL bit = "1")
21	DVDD	-	Digital Power Supply Pin, 1.6 ~ 1.98V
22	HPL	O	Lch Headphone-Amp Output Pin
23	HPR	O	Rch Headphone-Amp Output Pin
24	VEE	O	Charge-Pump Circuit Negative Voltage Output Pin This pin must be connected to VSS2 with 2.2μF±20% capacitor in series.
25	VSS2	-	Ground 2 Pin
26	CP	O	Positive Charge-Pump Capacitor Terminal Pin This pin must be connected to CN pin with 2.2μF±20% capacitor in series.
27	CN	I	Negative Charge-Pump Capacitor Terminal Pin This pin must be connected to CP pin with 2.2μF±20% capacitor in series.
28	AVDD	-	Analog Power Supply Pin, 2.8 ~ 3.5V
29	VSS1	-	Ground 1 Pin
30	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 with 2.2F±20% capacitor in series.
31	REGFIL	O	LDO Voltage Output pin for Analog Block (typ 2.3V) This pin must be connected to VSS1 with 2.2μF±20% capacitor in series.
32	RIN3	I	Rch Analog Input 3 Pin (PMBP bit = "0": default)
	BEEP	I	Beep Signal Input Pin (PMBP bit = "1")

Note 2. All input pins except analog input pins (LIN1, RIN1, LIN2, RIN2, LIN3, RIN3/BEEP) must not be allowed to float.

[AK4951EG]

No.	Pin Name	I/O	Function
B6	RIN2	I	Rch Analog Input 2 Pin
A6	LIN2	I	Lch Analog Input 2 pin
B5	MPWR1	O	MIC Power Supply 1 Pin
A5	MPWR2	O	MIC Power Supply 2 Pin
A4	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0": default)
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")
B4	LIN1	I	Lch Analog Input 1 Pin (DMIC bit = "0": default)
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
A3	PDN	I	Reset & Power-down Pin "L": Reset & Power-down, "H": Normal Operation
D1	I2C	I	Control Mode Select Pin "L": 3-wire Serial, "H": I^2C Bus
B3	CCLK	I	Control Data Clock Pin (I2C pin = "L")
	SCL	I	Control Data Clock Pin (I2C pin = "H")
E1	CDTIO	I/O	Control Data Input/Output Pin (I2C pin = "L")
	CAD0	I	Chip Address Select Pin (I2C pin = "H")
A2	CSN	I	Chip Select Pin (I2C pin = "L")
	SDA	I/O	Control Data Input/Output Pin (I2C pin = "H")
A1	SDTI	I	Audio Serial Data Input Pin
B2	SDTO	O	Audio Serial Data Output Pin
B1	LRCK	I/O	Input/Output Channel Clock Pin
C2	BICK	I/O	Audio Serial Data Clock Pin
C1	MCKI	I	External Master Clock Input Pin
D2	TVDD	-	Digital I/O Power Supply Pin, 1.6 or (DVDD-0.2) ~ 3.5V
F1	VSS3	-	Ground 3 Pin
F2	SPN	O	Speaker-Amp Negative Output Pin (LOSEL bit = "0": default)
	ROUT	O	Rch Stereo Line Output Pin (LOSEL bit = "1")
E2	SPP	O	Speaker-Amp Positive Output Pin (LOSEL bit = "0": default)
	LOUT	O	Lch Stereo Line Output Pin (LOSEL bit = "1")
E3	DVDD	-	Digital Power Supply Pin, 1.6 ~ 1.98V
F3	HPL	O	Lch Headphone-Amp Output Pin
F4	HPR	O	Rch Headphone-Amp Output Pin
F5	VEE	O	Charge-Pump Circuit Negative Voltage Output Pin This pin must be connected to VSS2 with 2.2μF±20% capacitor in series.
F6	VSS2	-	Ground 2 Pin
E4	CP	O	Positive Charge-Pump Capacitor Terminal Pin This pin must be connected to CN pin with 2.2μF±20% capacitor in series.
E5	CN	I	Negative Charge-Pump Capacitor Terminal Pin This pin must be connected to CP pin with 2.2μF±20% capacitor in series.
E6	AVDD	-	Analog & Speaker-Amp Power Supply Pin, 2.8 ~ 3.5V
D6	VSS1	-	Ground 1 Pin
D5	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 with 2.2μF±20% capacitor in series.
C6	REGFIL	O	LDO Voltage Output pin for Analog Block (typ 2.3V) This pin must be connected to VSS1 with 2.2μF±20% capacitor in series.
C5	RIN3	I	Rch Analog Input 3 Pin (PMBP bit = "0": default)
	BEEP	I	Beep Signal Input Pin (PMBP bit = "1")

Note 3. All input pins except analog input pins (LIN1, RIN1, LIN2, RIN2, LIN3, RIN3/BEEP) must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, SPN, SPP, HPL, HPR, CP, CN, VEE, LIN1/DMDAT, RIN1/DMCLK, LIN2, RIN2, LIN3, RIN3/BEEP	Open
Digital	MCKI, SDTI	Connect to VSS2
	SDTO	Open

6. Absolute Maximum Ratings

(VSS1=VSS2=VSS3=0V; Note 4)

Parameter		Symbol	min	max	Unit
Power Supplies	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	2.5	V
	Digital I/O	TVDD	–0.3	6.0	V
	Speaker-Amp	SVDD	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 5)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 6)		VIND	–0.3	TVDD+0.3	V
Operating Temperature (powered applied)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 7)	AK4951EN	Pd	-	840	mW
	AK4951EG	Pd	-	340	mW

Note 4. All voltages are with respect to ground. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.

Note 5. LIN1, RIN1, LIN2, RIN2, LIN3 and RIN3/BEEP pins

Note 6. PDN, CCLK/SCL, CSN/SDA, CDTIO/CAD0, SDTI, LRCK, BICK and MCKI pins
Pull-up resistors at the SDA and SCL pins must be connected to a voltage in the range from TVDD or more to 6V or less.

Note 7. This power is the AK4951 internal dissipation that does not include power dissipation of externally connected speakers. The maximum junction temperature is 125°C and θja (Junction to Ambient) is 42°C/W at JESD51-9 (2p2s) for the AK4951EN and 80°C/W at JESD51-9 (2p2s) for the AK4951EG. When Pd =840mW and the θja is 42°C/W for the AK4951EN, the junction temperature does not exceed 125°C. When Pd =340mW and the θja is 80°C/W for the AK4951EG, the junction temperature does not exceed 125°C. In this case, the AK4951 will not be damaged by its internal power dissipation. Therefore, the AK4951EN should be used in the condition of θja ≤ 42°C/W, and the AK4951EG should be used in the condition of θja ≤ 80°C/W.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

[AK4951EN]
(VSS1=VSS2=VSS3 =0V; Note 4)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 8)	Analog	AVDD	2.8	3.3	3.5	V
	Digital	DVDD	1.6	1.8	1.98	V
	Digital I/O (Note 9)	TVDD	1.6 or (DVDD-0.2)	1.8	3.5	V
	Speaker-Amp	SVDD	1.8	3.3	5.5	V

Note 4. All voltages are with respect to ground.
Note 8. The power-up sequence between AVDD, DVDD, TVDD and SVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.
Note 9. The minimum value is higher voltage between DVDD-0.2 and 1.6V.

*** When SVDD is powered ON and the PDN pin is "L", AVDD, DVDD and TVDD can be powered ON/OFF. When TVDD is powered ON and the PDN pin is "L", AVDD, DVDD and SVDD can be powered ON/OFF. The PDN pin must be set to "H" after all power supplies are ON, when the AK4951EN is powered-up from power-down state.**

[AK4951EG]
(VSS1=VSS2=VSS3 =0V; Note 4)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 10)	Analog & Speaker	AVDD	2.8	3.3	3.5	V
	Digital	DVDD	1.6	1.8	1.98	V
	Digital I/O (Note 11)	TVDD	1.6 or (DVDD-0.2)	1.8	3.5	V

Note 4. All voltages are with respect to ground.
Note 10. The power-up sequence between AVDD, DVDD and TVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.
Note 11. The minimum value is higher voltage between DVDD-0.2 and 1.6V.

*** When TVDD is powered ON and the PDN pin is "L", AVDD and DVDD can be powered ON/OFF. The PDN pin must be set to "H" after all power supplies are ON, when the AK4951EG is powered-up from power-down state.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

■ Analog Characteristics

(Ta=25°C; AVDD=SVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3=0V; fs=48kHz, BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement Bandwidth=20Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Unit
MIC Amplifier: LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins						
Input Resistance			20	30	40	kΩ
Gain	Gain Setting		0	-	+30	dB
	Step Width		-	3	-	dB
MIC Power Supply: MPWR1, MPWR2 pins						
Output Voltage		MICL bit = "0"	2.2	2.4	2.6	V
		MICL bit = "1"	1.8	2.0	2.2	V
Output Noise Level (A-weighted)			-	-108	-	dBV
Load Resistance			1.0	-	-	kΩ
Load Capacitance			-	-	30	pF
PSRR (f = 1kHz) (Note 12)			-	100	-	dB
ADC Analog Input Characteristics: LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins → ADC (Programmable Filter = OFF) → SDTO						
Resolution			-	-	24	Bits
Input Voltage (Note 13)		(Note 14)	-	0.261	-	Vpp
		(Note 15)	1.86	2.07	2.28	Vpp
S/(N+D) (-1dBFS)	(Note 14)		73	83	-	dBFS
	(Note 15: AK4951EN)		-	85	-	dBFS
	(Note 15: AK4951EG)		-	84	-	dBFS
D-Range (–60dBFS, A-weighted)		(Note 14)	78	88	-	dB
		(Note 15)	-	96	-	dB
S/N (A-weighted)		(Note 14)	78	88	-	dB
		(Note 15)	-	96	-	dB
Interchannel Isolation		(Note 14)	75	100	-	dB
		(Note 15)	-	110	-	dB
Interchannel Gain Mismatch		(Note 14)	-	0	0.5	dB
		(Note 15)	-	0	0.5	dB
PSRR (f = 1kHz) (Note 12)			-	80	-	dB

Note 12. PSRR applied to AVDD with 500mVpp sine wave.
Note 13. Vin = 0.9 x 2.3Vpp (typ) @MGAIN3-0 bits = "0000" (0dB)
Note 14. MGAIN3-0 bits = "0110" (+18dB)
Note 15. MGAIN3-0 bits = "0000" (0dB)

Parameter			min	typ	max	Unit
DAC Characteristics:						
Resolution			-	-	24	Bits
Headphone-Amp Characteristics: DAC → HPL, HPR pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=16Ω						
Output Voltage (0dBFS)			1.44	1.60	1.76	Vpp
S/(N+D)	R_L=16Ω		50	75	-	dB
	R_L=10kΩ		-	80	-	dB
S/N (A-weighted)			87	97	-	dB
Interchannel Isolation			65	80	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Output Offset Voltage			-1	0	+1	mV
Load Resistance			16	-	-	Ω
Load Capacitance			-	-	300	pF
PSRR (f = 1kHz) (Note 16)	AVDD		-	74	-	dB
	DVDD		-	90	-	dB
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=8Ω, BTL						
Output Voltage						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	1.79	-	Vrms
SPKG1-0 bits = "11", –0.5dBFS (Po=1000mW) (SVDD=5V)			-	2.83	-	Vrms
S/(N+D)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	80	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			40	75	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	20	-	dB
SPKG1-0 bits = "11", –0.5dBFS (Po=1000mW) (AK4951EN: SVDD=5V)			-	20	-	dB
S/N (A-weighted)	SPKG1-0 bits = "01"		80	99	-	dB
Output Offset Voltage	SPKG1-0 bits = "01"		-30	0	+30	mV
Load Resistance			8	-	-	Ω
Load Capacitance			-	-	100	pF
PSRR (f = 1kHz) (Note 17)		AVDD	-	80	-	dB
		SVDD	-	60	-	dB
Stereo Line Output Characteristics: DAC → LOUT, ROUT pins, ALC=OFF, IVOL=DVOL = 0dB, R_L=10kΩ, LVCM1-0 bits = "01"						
Output Voltage	(0dBFS)	LVCM0 bit = "0", SVDD=2.8V	-	2.26	-	Vpp
		LVCM0 bit = "1"	-	1.0	-	Vrms
	(-3dBFS)	LVCM0 bit = "0", SVDD=2.8V	1.44	1.6	1.76	Vpp
		LVCM0 bit = "1"	1.82	2.0	2.22	Vpp
S/(N+D)	(0dBFS)	LVCM0 bit = "0", SVDD=2.8V	-	80	-	dB
		LVCM0 bit = "1"	-	80	-	dB
	(-3dBFS)		75	85	-	dB
S/N (A-weighted)			82	94	-	dB
Interchannel Isolation			-	100	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Load Resistance			10	-	-	kΩ
Load Capacitance			-	-	30	pF

Note 16. PSRR applied with 500mVpp sine wave.
Note 17. PSRR applied to AVDD or SVDD with 500mVpp sine wave.

Parameter			min	typ	max	Unit
Mono Input: BEEP pin (PMBP bit =“1”, BPVCM bit = “0”, BPLVL3-0 bits = “0000”)						
Input Resistance			46	66	86	kΩ
Maximum Input Voltage (Note 18)			-	-	1.54	Vpp
Gain						
BEEP pin → HPL, HPR pins			–1	0	+1	dB
BEEP pin → SPP/SPN pins (Note 19)						
	SPKG1-0 bits = “00”		+4.4	+6.4	+8.4	dB
	SPKG1-0 bits = “01”		-	+8.4	-	dB
	SPKG1-0 bits = “10”		-	+11.1	-	dB
	SPKG1-0 bits = “11”		-	+14.9	-	dB
BEEP pin → LOUT, ROUT pins						
	LVCM1-0 bits = “00”		-1	0	+1	dB
	LVCM 1-0 bits = “01”		-	+2	-	dB
	LVCM 1-0 bits = “10”		-	+2	-	dB
	LVCM 1-0 bits = “11”		-	+4	-	dB
Power Supplies:						
Power Up (PDN pin = “H”)						
MIC + ADC + DAC + Headphone out						
AVDD+DVDD+TVDD (Note 20)			-	6.5	9.8	mA
AVDD+DVDD+TVDD (Note 21)			-	5.7	-	mA
SVDD (No Load)			-	36	54	μA
MIC + ADC + DAC + Speaker out						
AVDD+DVDD+TVDD (Note 22)		AK4951EN	-	5.6	8.4	mA
		AK4951EG	-	7.4	11.3	mA
AVDD+DVDD+TVDD (Note 23)		AK4951EN	-	4.7	-	mA
		AK4951EG	-	6.5	-	mA
SVDD (No Load)		AK4951EN	-	1.8	2.7	mA
Power Down (PDN pin = “L”) (Note 24)						
AVDD+DVDD+TVDD+SVDD			-	0	10	μA
SVDD (Note 25)			-	0	10	μA

Note 18. The maximum value is AVDD Vpp when BPVCM bit = “1”. However, a click noise may occur when the amplitude after BEEP-Amp is 0.5Vpp or more. (set by BPLVL3-0 bits)

Note 19. The gain is in inverse proportion to external input resistance.

Note 20. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMHPL= PMHPR= PMVCM=PMPLL =PMBP=PMMP=M/S bits = “1”. In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 4.4mA (typ), DVDD= 2.0mA (typ), TVDD= 0.08mA (typ).

Note 21. When EXT Slave Mode (PMPLL=M/S bits =“0”), PMADL=PMADR=PMDAC=PMHPL=PMHPR= PMVCM=PMBP=PMMP bits = “1”, and PMPFIL bit = “0”. In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 4.2mA (typ), DVDD= 1.5mA (typ), TVDD= 0.02mA (typ).

Note 22. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMSL= PMVCM= PMPLL =PMBP=PMMP=SLPSN=DACS=M/S bits = “1”. In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 3.8mA (AK4951EN: typ), 5.6mA (AK4951EG: typ), DVDD= 1.7mA (typ), TVDD= 0.08mA (typ).

Note 23. When EXT Slave Mode (PMPLL=M/S bits =“0”), PMADL=PMADR=PMDAC=PMSL=PMVCM= PMBP=PMMP=SLPSN=DACS bits = “1”, and PMPFIL bit = “0”. In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 3.5mA (AK4951EN: typ), 5.3mA (AK4951EG: typ), DVDD= 1.2mA (typ), TVDD= 0.02mA (typ).

Note 24. All digital input pins are fixed to TVDD or VSS2.

Note 25. When AVDD, DVDD and TVDD are powered OFF.

■ Power Consumption on Each Operation Mode

[AK4951EN]

Conditions: Ta=25°C; AVDD=SVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3=0V; fs=48kHz, Programmable Filter=OFF, External Slave Mode, BICK=64fs; LIN1/RIN1 input = No signal; SDTI input = No data; Headphone & Speaker outputs = No load.

Mode	Power Management Bit									AVDD [mA]	DVDD [mA]	TVDD [mA]	SVDD [mA]	Total Power [mW]
	PMVCM	PMSL	PMDAC	PMADL	PMADR	PMHPL	PMHPR	PMPFIL	LOSEL					
All Power-down	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LIN1/RIN1 → ADC	1	0	0	1	1	0	0	0	0	2.40	0.75	0.02	0	9.3
LIN1 (Mono) → ADC	1	0	0	1	0	0	0	0	0	1.62	0.75	0.02	0	6.7
DAC → HP	1	0	1	0	0	1	1	0	0	2.15	0.80	0.02	0	8.6
DAC → SPK	1	1	1	0	0	0	0	0	0	1.50	0.50	0.02	1.80	11.8
DAC → Line out	1	1	1	0	0	0	0	0	1	1.68	0.50	0.02	0.34	7.6
LIN1/RIN1 → ADC & DAC → HP	1	0	1	1	1	1	1	0	0	3.75	1.55	0.02	0	15.2
LIN1/RIN1 → ADC & DAC → SPK	1	1	1	1	1	0	0	0	0	3.10	1.25	0.02	1.80	18.5
LIN1/RIN1 → ADC & DAC → Line out	1	1	1	1	1	0	0	0	1	3.30	1.25	0.02	0.34	14.3

Table 1. Power Consumption on Each Operation Mode (AK4951EN: typ)

[AK4951EG]

Conditions: Ta=25°C; AVDD==3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3=0V; fs=48kHz, Programmable Filter=OFF, External Slave Mode, BICK=64fs; LIN1/RIN1 input = No signal; SDTI input = No data; Headphone & Speaker outputs = No load.

Mode	Power Management Bit									AVDD [mA]	DVDD [mA]	TVDD [mA]	Total Power [mW]
	PMVCM	PMSL	PMDAC	PMADL	PMADR	PMHPL	PMHPR	PMPFIL	LOSEL				
All Power-down	0	0	0	0	0	0	0	0	0	0	0	0	0
LIN1/RIN1 → ADC	1	0	0	1	1	0	0	0	0	2.40	0.75	0.02	9.3
LIN1 (Mono) → ADC	1	0	0	1	0	0	0	0	0	1.62	0.75	0.02	6.7
DAC → HP	1	0	1	0	0	1	1	0	0	2.15	0.80	0.02	8.6
DAC → SPK	1	1	1	0	0	0	0	0	0	3.30	0.50	0.02	11.8
DAC → Line out	1	1	1	0	0	0	0	0	1	2.02	0.50	0.02	7.6
LIN1/RIN1 → ADC & DAC → HP	1	0	1	1	1	1	1	0	0	3.75	1.55	0.02	15.2
LIN1/RIN1 → ADC & DAC → SPK	1	1	1	1	1	0	0	0	0	4.90	1.25	0.02	18.5
LIN1/RIN1 → ADC & DAC → Line out	1	1	1	1	1	0	0	0	1	3.64	1.25	0.02	14.3

Table 2. Power Consumption on Each Operation Mode (AK4951EG: typ)

■ Filter Characteristics

(Ta =25°C; fs=48kHz; AVDD=2.8 ~ 3.5V, SVDD=1.8 ~ 5.5V, DVDD = 1.6 ~ 1.98V, TVDD = 1.6 or (DVDD-0.2)~ 3.5V)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 26)	±0.16dB	PB	0	-	18.8	kHz
	–0.66dB		-	21.1	-	kHz
	–1.1dB		-	21.7	-	kHz
	–6.9dB		-	24.1	-	kHz
Stopband (Note 26)		SB	28.4	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 27)		GD	-	17	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	3.7	-	Hz
(Note 26)	–0.5dB		-	10.9	-	Hz
	–0.1dB		-	23.9	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 26)	±0.05dB	PB	0	-	21.8	kHz
	–6.0dB		-	24	-	kHz
Stopband (Note 26)		SB	27.0	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	70	-	-	dB
Group Delay (Note 27)		GD	-	29	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

Note 26. The passband and stopband frequencies scale with fs (sampling frequency).

Note 27. A calculating delay time which is induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the DAC, this time is from setting the 24-bit data of a channel from the input register to the output of analog signal. For the signal through the programmable filters (Microphone Sensitivity Correction + Automatic Wind Noise Reduction Filter + 1st order HPF + 1st order LPF + Stereo Separation Emphasis + 4-band Equalizer + ALC + 1-band Equalizer), the group delay is increased by 4/fs from the value above in both recording and playback modes if there is no phase change by the IIR filter.

■ DC Characteristics

(Ta =25°C; fs=48kHz; AVDD=2.8 ~ 3.5V, SVDD= 1.8 ~ 5.5V, DVDD = 1.6 ~ 1.98V, TVDD = 1.6 or (DVDD-0.2)~ 3.5V)

Parameter	Symbol	min	typ	max	Unit
Audio Interface & Serial µP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)					
High-Level Input Voltage (TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
(TVDD < 2.2V)	VIH	80%TVDD	-	-	V
Low-Level Input Voltage (TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
(TVDD < 2.2V)	VIL	-	-	20%TVDD	V
Input Leakage Current	Iin1	-	-	±10	µA
Audio Interface & Serial µP Interface (CDTIO, SDA, BICK, LRCK, SDTO pins Output)					
High-Level Output Voltage (Iout = −80µA)	VOH	TVDD−0.2	-	-	V
Low-Level Output Voltage					
(Except SDA pin : Iout = 80µA)	VOL1	-	-	0.2	V
(SDA pin, 2.0V ≤ TVDD ≤ 3.5V: Iout = 3mA)	VOL2	-	-	0.4	V
(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Digital Microphone Interface (DMDAT pin Input; DMIC bit = "1")					
High-Level Input Voltage	VIH2	65%AVDD	-	-	V
Low-Level Input Voltage	VIL2	-	-	35%AVDD	V
Input Leakage Current	Iin2	-	-	±10	µA
Digital Microphone Interface (DMCLK pin Output; DMIC bit = "1")					
High-Level Output Voltage (Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 80µA)	VOL3	-	-	0.4	V

■ Switching Characteristics

(Ta=25°C; fs=48kHz; C_L=20pF; AVDD=2.8~3.5V, SVDD=1.8~5.5V, DVDD=1.6~1.98V, TVDD=1.6 or (DVDD-0.2)~3.5V)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency	PLL3-0 bits = "0100"	fCLK	-	11.2896	-	MHz
	PLL3-0 bits = "0101"	fCLK	-	12.288	-	MHz
	PLL3-0 bits = "0110"	fCLK	-	12	-	MHz
	PLL3-0 bits = "0111"	fCLK	-	24	-	MHz
	PLL3-0 bits = "1100"	fCLK	-	13.5	-	MHz
	PLL3-0 bits = "1101"	fCLK	-	27	-	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing						
Frequency		fs	-	Table 8	-	Hz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Frequency	BCKO bit = "0"	fBCK	-	32fs	-	Hz
	BCKO bit = "1"	fBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency	PLL3-0 bits = "0010"	fs	-	fBCK/32	-	Hz
	PLL3-0 bits = "0011"	fs	-	fBCK/64	-	Hz
Duty		Duty	45	-	55	%
BICK Input Timing						
Frequency	PLL3-0 bits = "0010"	fBCK	0.256	-	1.536	MHz
	PLL3-0 bits = "0011"	fBCK	0.512	-	3.072	MHz
Pulse Width Low		tBCKL	0.4/fBCK	-	-	s
Pulse Width High		tBCKH	0.4/fBCK	-	-	s
External Slave Mode						
MCKI Input Timing						
Frequency	CM1-0 bits = "00"	fCLK	-	256fs	-	Hz
	CM1-0 bits = "01"	fCLK	-	384fs	-	Hz
	CM1-0 bits = "10"	fCLK	-	512fs	-	Hz
	CM1-0 bits = "11"	fCLK	-	1024fs	-	Hz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Input Timing						
Frequency	CM1-0 bits = "00"	fs	8	-	48	kHz
	CM1-0 bits = "01"	fs	8	-	48	kHz
	CM1-0 bits = "10"	fs	8	-	48	kHz
	CM1-0 bits = "11"	fs	8	-	24	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Frequency		fBCK	32fs	-	64fs	Hz
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns

Parameter		Symbol	min	typ	max	Unit
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	2.048	-	12.288	MHz
	384fs	fCLK	3.072	-	18.432	MHz
	512fs	fCLK	4.096	-	24.576	MHz
	1024fs	fCLK	8.192	-	24.576	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing						
Frequency	CM1-0 bits = "00"	fs	-	fCLK/256	-	Hz
	CM1-0 bits = "01"	fs	-	fCLK/384	-	Hz
	CM1-0 bits = "10"	fs	-	fCLK/512	-	Hz
	CM1-0 bits = "11"	fs	-	fCLK/1024	-	Hz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Frequency	BCKO bit = "0"	fBCK	-	32fs	-	Hz
	BCKO bit = "1"	fBCK	-	64fs	-	Hz
Duty Cycle		dBCK	-	50	-	%
Audio Interface Timing						
Master Mode						
BICK "↓" to LRCK Edge (Note 28)		tBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)		tLRD	–70	-	70	ns
BICK "↓" to SDTO		tBSD	–70	-	70	ns
SDTI Hold Time		tSDH	50	-	-	ns
SDTI Setup Time		tSDS	50	-	-	ns
Slave Mode						
LRCK Edge to BICK "↑" (Note 28)		tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 28)		tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)		tLRD	-	-	80	ns
BICK "↓" to SDTO		tBSD	-	-	80	ns
SDTI Hold Time		tSDH	50	-	-	ns
SDTI Setup Time		tSDS	50	-	-	ns
Digital Audio Interface Timing; C_L=100pF						
DMCLK Output Timing						
Period		tSCK	-	1/(64fs)	-	s
Rising Time		tSRise	-	-	10	ns
Falling Time		tSFall	-	-	10	ns
Duty Cycle		dSCK	40	50	60	%
Audio Interface Timing						
DMDAT Setup Time		tDSDS	50	-	-	ns
DMDAT Hold Time		tDSDH	0	-	-	ns

Note 28. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (I^2C Bus)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 30)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Control Interface Timing (3-wire Serial: AK4951EG)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 31)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 31)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command) (Note 32)	tCCZ	-	-	70	ns
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 33)	tAPD	200	-	-	ns
PDN Reject Pulse Width (Note 33)	tRPD	-	-	50	ns
PMADL or PMADR "↑" to SDTO valid (Note 34)					
ADRST1-0 bits ="00"	tPDV	-	1059	-	1/fs
ADRST1-0 bits ="01"	tPDV	-	267	-	1/fs
ADRST1-0 bits ="10"	tPDV	-	531	-	1/fs
ADRST1-0 bits ="11"	tPDV	-	135	-	1/fs
VCOM Voltage					
Rising Time (Note 35)	tRVCM	-	0.6	2.0	ms

Note 29. I^2C Bus is a trademark of NXP B.V.

Note 30. Data must be held for sufficient time to bridge the 300ns transition time of SCL.

Note 31. CCLK rising edge must not occur at the same time as CSN edge.

Note 32. It is the time of 10% potential change of the CDTIO pin when R_L = 1kΩ (pull-up or TVDD).

Note 33. The AK4951 can be reset by the PDN pin = "L". The PDN pin must be held "L" for more than 200ns for a certain reset. The AK4951 is not reset by the "L" pulse less than 50ns.

Note 34. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

Note 35. All analog blocks including PLL block are powered up after the VCOM voltage (VCOM pin) rises up. An external capacitor of the VCOM pin is 2.2µF and the REGFIL pin is 2.2µF. The capacitance variation should be ±50%.

■ Timing Diagram

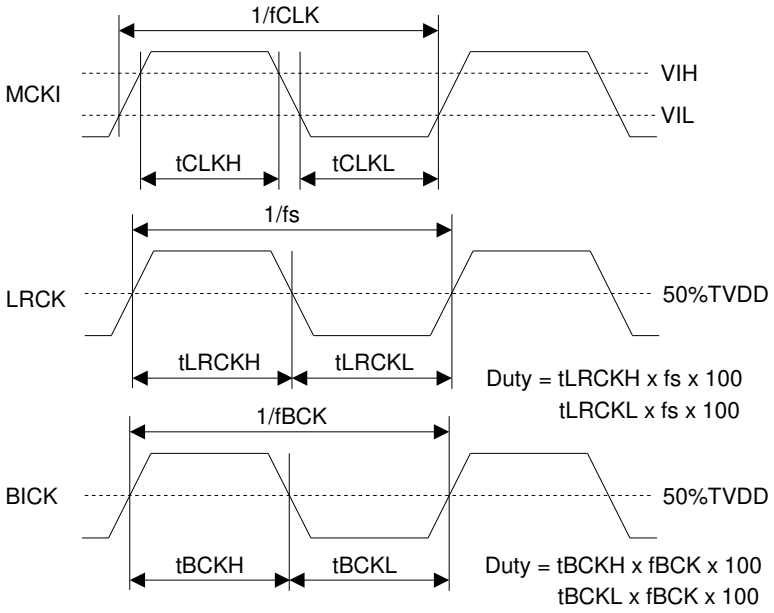


Figure 5. Clock Timing (PLL/EXT Master mode)

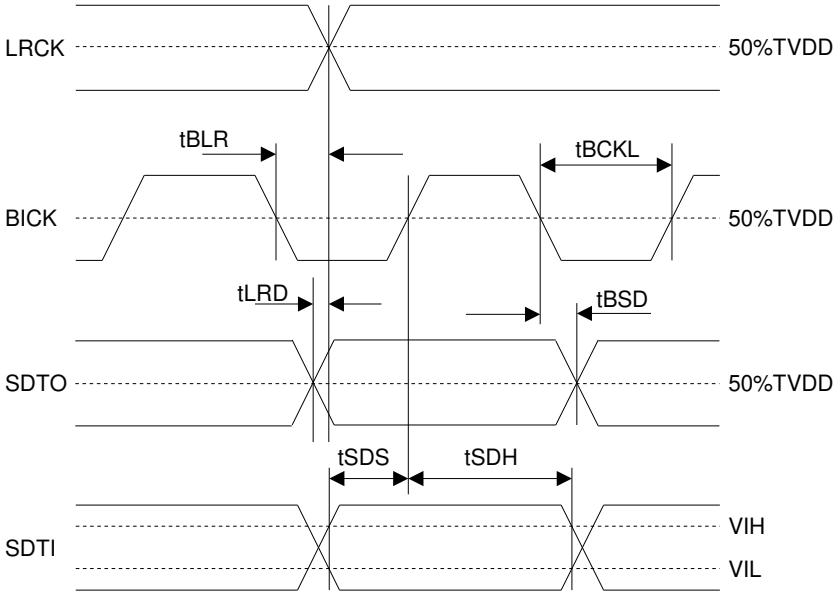


Figure 6. Audio Interface Timing (PLL/EXT Master mode)

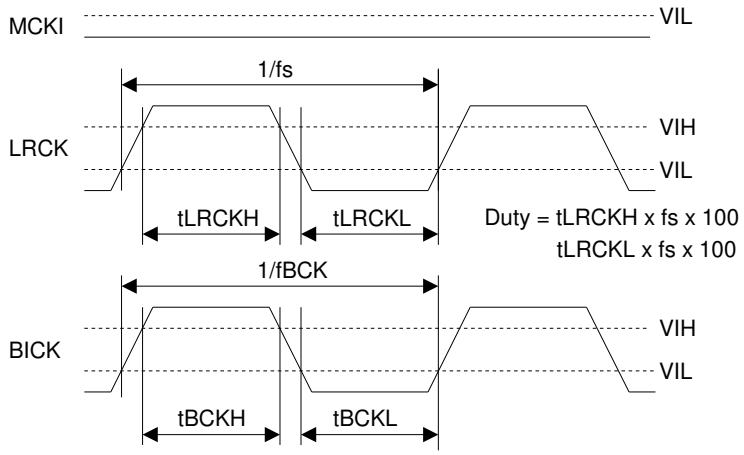


Figure 7. Clock Timing (PLL Slave mode)

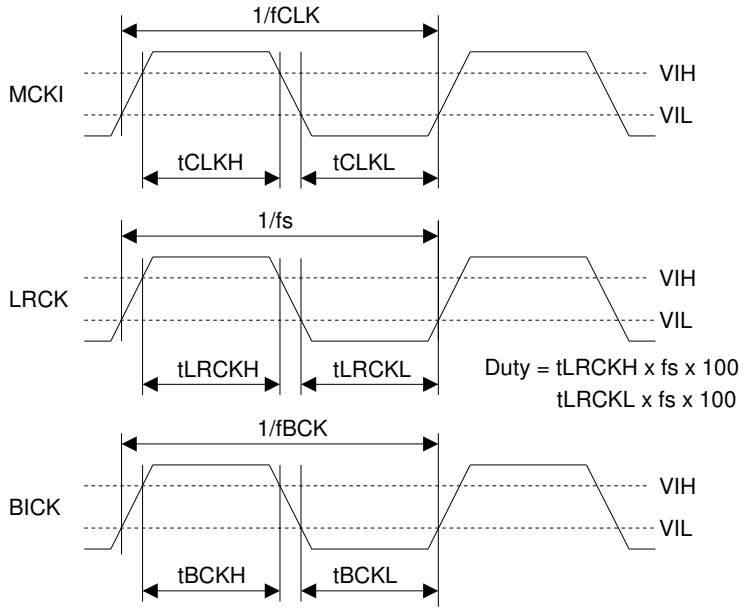


Figure 8. Clock Timing (EXT Slave mode)

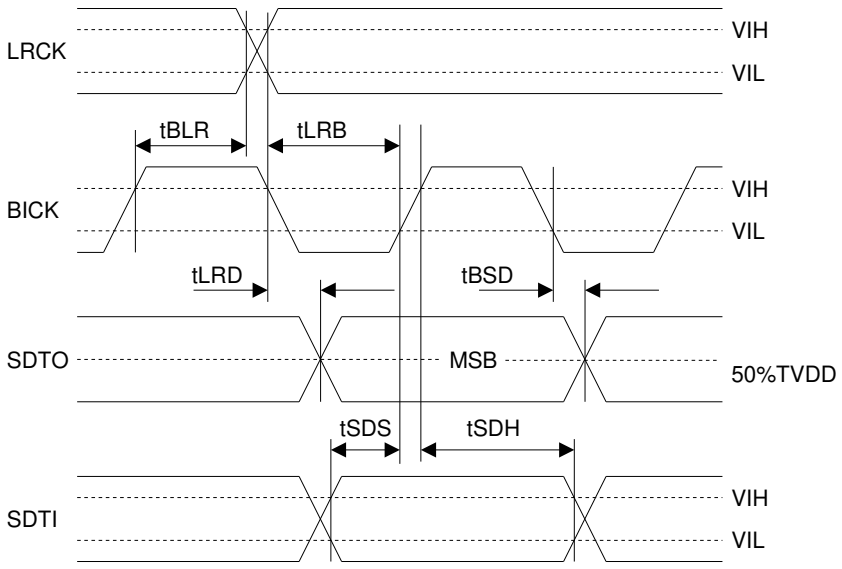


Figure 9. Audio Interface Timing (PLL/EXT Slave mode)