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AK4953A

24bit Stereo CODEC with MIC/HP/SPK-AMP

GENERAL DESCRIPTION

The AK4953A is a low power consumption 24bit stereo CODEC with a microphone, headphone and speaker amplifiers. The input circuits include a microphone amplifier and an ALC (Automatic Level Control) circuit, and the output circuits include a cap-less headphone amplifier and a speaker amplifier. It is suitable for portable application with recording/playback function. The integrated charge pump circuit generates a negative voltage and removes the output AC coupling capacitors. The speaker amplifier has a wide operating voltage range, which is from 0.9V to 5.5V, enabling a direct drive to batteries. The AK4953A is available in a small 36-pin QFN (5x5mm 0.4mm pitch), utilizing less board space than competitive offerings.

FEATURES

1. Recording Function
- **Stereo Single-ended input with three Selectors**
- **MIC Amplifier (+29dB/+26dB/+23dB/+20dB/+16dB/+12dB/0dB)**
- **Digital ALC (Automatic Level Control)**
  (Setting Range: +36dB ~ –54dB, 0.375dB Step)
- **ADC Performance: S/(N+D): 82dB, DR, S/N: 88dB (MIC-Amp=+20dB)**
  S/(N+D): 85dB, DR, S/N: 96dB (MIC-Amp=0dB)
- **Wind-noise Reduction Filter**
- **5 Band Notch Filter**
- **Digital MIC Interface**

2. Playback Function
- **Digital De-emphasis Filter (tc=50/15μs, fs=32kHz, 44.1kHz, 48kHz)**
- **Digital ALC (Automatic Level Control)**
  (Setting Range: +36dB ~ –54dB, 0.375dB Step)
- **Digital Volume Control (+12dB ~ –115dB, 0.5dB Step, Mute)**
- **Capacitor-less Stereo Headphone Amplifier**
  - **HP-Amp Performance: S/(N+D): 80dB@24mW, S/N: 96dB**
  - **Output Power: 24mW@16Ω**
  - **Pop Noise Free at Power-ON/OFF**
- **Mono Speaker-Amplifier**
  - **SPK-Amp Performance: S/(N+D): 70dB@250mW, S/N: 95dB**
  - **BTL Output**
  - **Output Power: 400mW@8Ω (SVDD=3.3V)**
    100mW@8Ω (SVDD=1.5V)
- **Beep Generator**

3. Power Management

4. Master Clock:

(1) PLL Mode
- **Frequencies: 11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)**
  32fs or 64fs (BICK pin)

(2) External Clock Mode
- **Frequencies: 256fs, 384fs, 512fs or 1024fs (MCKI pin)**

5. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs
- **PLL Slave Mode (BICK pin): 7.35kHz ~ 96kHz**
- **PLL Slave Mode (MCKI pin): 7.35kHz, 8kHz, 11.025kHz, 12kHz, 14.7kHz, 16kHz, 22.05kHz, 24kHz, 29.4kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz**
- **PLL Master Mode: 7.35kHz, 8kHz, 11.025kHz, 12kHz, 14.7kHz, 16kHz, 22.05kHz, 24kHz, 29.4kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz**
- **EXT Master/Slave Mode: 7.35kHz ~ 96kHz (256fs), 7.35kHz ~ 48kHz (384fs), 7.35kHz ~ 48kHz (512fs), 7.35kHz ~ 12kHz (1024fs)**

6. μP I/F: 3-wire Serial, I^2C Bus (Ver 1.0, 400kHz Fast-Mode)
7. Master/Slave mode
8. Audio Interface Format: MSB First, 2's complement
- **ADC: 24bit MSB justified, 16/24bit I^2S**
- **DAC: 24bit MSB justified, 16bit LSB justified, 24bit LSB justified, 16/24bit I^2S**

9. Ta = –30 ~ 85°C (SPK-Amp = OFF)
Ta = –30 ~ 70°C (SPK-Amp = ON)
10. Power Supply:
- **Analog Power Supply (AVDD): 2.85 ~ 3.5V**
- **Digital Power Supply (DVDD): 1.6 ~ 2.0V**
- **Digital I/O Power Supply (TVDD): DVDD ~ 3.5V**
- **Speaker Power Supply (SVDD): 0.9 ~ 5.5V**

11. Package: 36-pin QFN (5 x 5mm, 0.4mm pitch)

■ Block Diagram

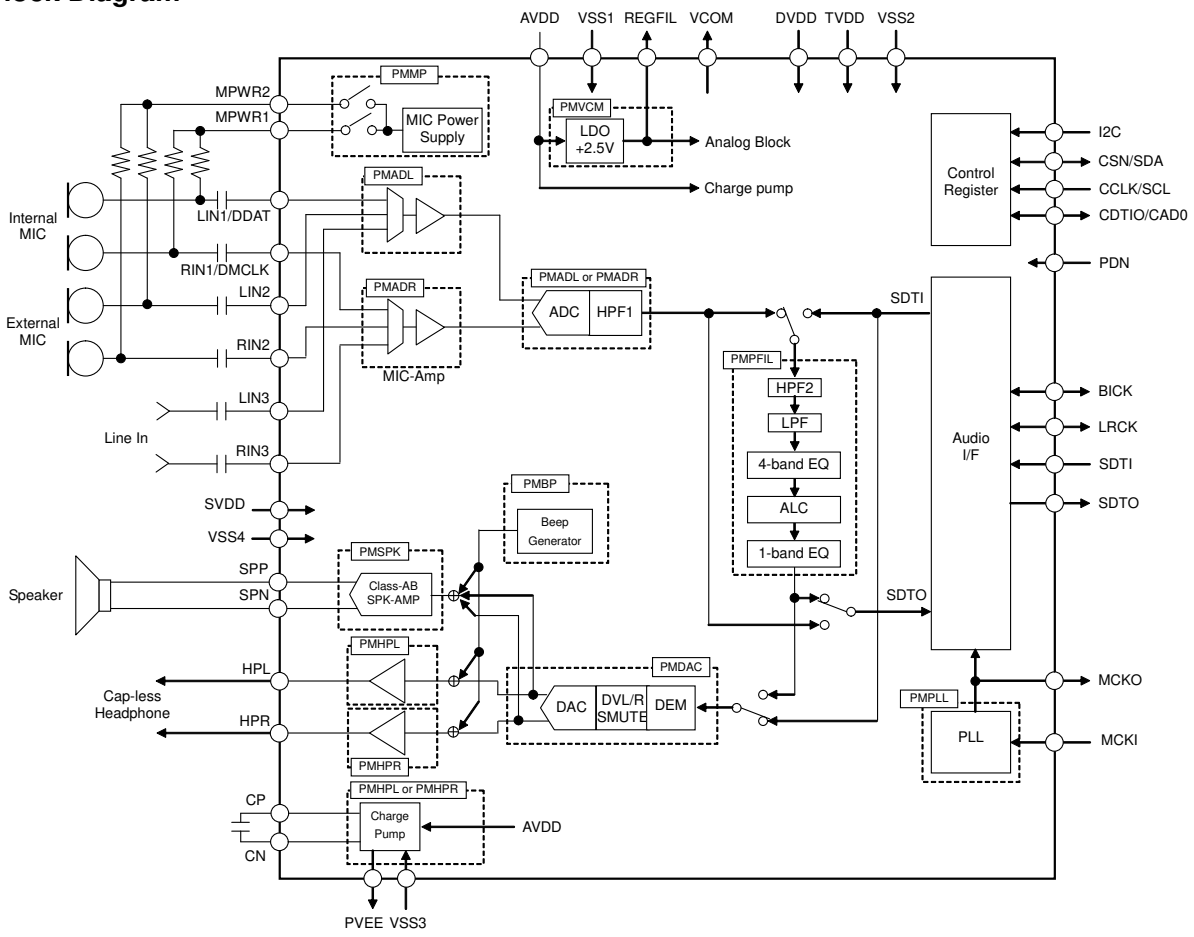
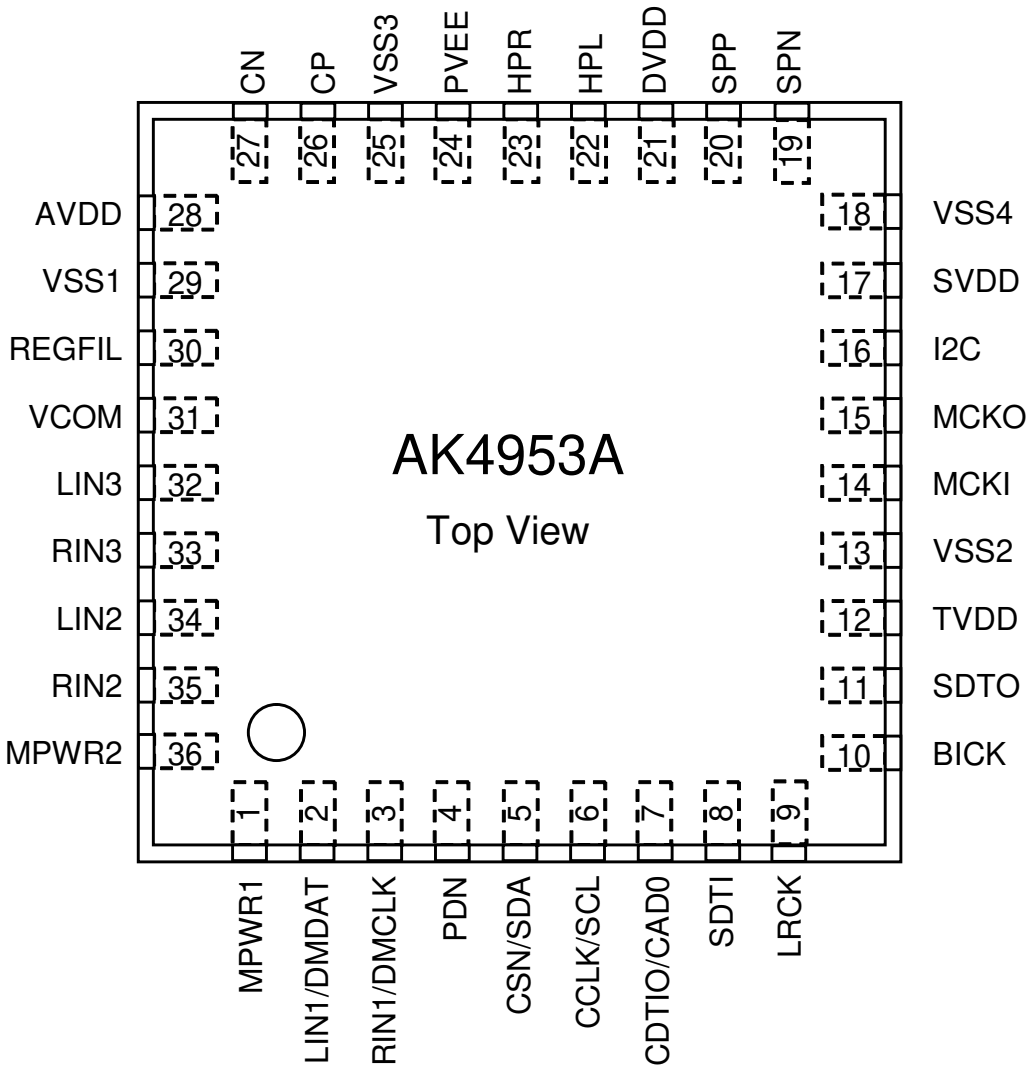


Figure 1. Block Diagram

■ Ordering Guide

AK4953AEN	–30 ~ +85°C	36-pin QFN (0.4mm pitch)
AKD4953A	Evaluation board for AK4953A	

■ Pin Layout



■ Comparison with AK4645

Function	AK4645	AK4953A
Resolution	16bit	24bit
AVDD	2.6V ~ 3.6V	2.85V ~ 3.5V
DVDD	2.6V ~ 3.6V	1.6V ~ 2.0V
HVDD	2.6V ~ 5.25V	-
SVDD	-	0.9V ~ 5.5V
TVDD	1.6V ~ 3.6V	DVDD ~ 3.5V
ADC DR, S/N	86dB @ MGAIN = +20dB 95dB @ MGAIN = 0dB	88dB @ MGAIN = +20dB 96dB @ MGAIN = 0dB
DAC S/N	92dB	96dB
Input level	typ. 0.6 x AVDD @ MIC Gain=0dB	typ. 2.4Vpp @ MIC Gain=0dB
Output level (Headphone)	typ. 0.6 x AVDD @LOVL=0dB	typ. 1.75Vpp @ DVOL=0dB
ADC Input Selector	4 Stereo	3 Stereo
MIC Power Output Voltage	0.8 x AVDD	typ 2.3V (2 Line Outputs)
MIC-Amp	0dB/+20dB/+26dB/+32dB	0dB/+12dB/+16dB/+20dB/+23dB/ +26dB/+29dB
Digital MIC I/F	No	Yes
HPF(HPF1) after ADC	Fixed (fc = 0.9Hz)	4 frequencies (fc = 3.4Hz/13.6Hz/108.8Hz/217.6Hz @ fs=44.1kHz)
Notch Filter	No	5 Step (4 Step + 1 Step)
Stereo Emphasis	Yes	No
Output Volume	+36dB ~ -54dB, 0.375dB Step (Note 1) & +12dB ~ -115dB, 0.5dB Step	+36dB ~ -54dB, 0.375dB Step (Note 1) & +12dB ~ -115dB, 0.5dB Step
Speaker-Amp	No	Yes
Master Clock Reference for PLL Mode	11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz	11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz
External Clock Mode Master Clock	256fs, 512fs, 1024fs	256fs, 384fs, 512fs, 1024fs
Power Supply Current **(Stereo Recording)** **(Headphone Playback)**	 typ. 7.3mA typ. 10.6mA	 typ. 3.3mA typ. 3.6mA
Package	32QFN (4 x 4mm, 0.4mm pitch)	36QFN (5 x 5mm, 0.4mm pitch)

Note 1. ALC and Volume circuits are shared by input and output. Therefore, it is impossible to use ALC and Volume control function at the same time for both recording and playback mode.

■ Compatibility with AK4953

1. Function

Function	AK4953	AK4953A
Headphone Hi-Z Mode	No	Yes

2. Register

Addr	Bit	AK4953	AK4953A
05H	D2	0 (Pull-down by 10Ω)	0: Pull-down by 10Ω (Default) 1: Hi-Z

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MPWR1	O	MIC Power Supply Pin for Microphone 1
2	LIN1	I	Lch Analog Input 1 Pin (DMIC bit = "0")
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
3	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0")
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")
4	PDN	I	Power-down & Reset When "L", the AK4953A is in power-down mode and is held in reset. The AK4953A must be always reset upon power-up.
5	CSN	I	Chip Select Pin (I2C pin = "L")
	SDA	I/O	Control Data Input/Output Pin (I2C pin = "H")
6	CCLK	I	Control Data Clock Pin (I2C pin = "L")
	SCL	I	Control Data Clock Pin (I2C pin = "H")
7	CDTIO	I/O	Control Data Input/Output Pin (I2C pin = "L")
	CAD0	I	Chip Address Select Pin (I2C pin = "H")
8	SDTI	I	Audio Serial Data Input Pin
9	LRCK	I/O	Input/Output Channel Clock Pin
10	BICK	I/O	Audio Serial Data Clock Pin
11	SDTO	O	Audio Serial Data Output Pin
12	TVDD	-	Digital I/O Power Supply Pin, 1.6 ~ 3.5V
13	VSS2	-	Ground 2 Pin
14	MCKI	I	External Master Clock Input Pin
15	MCKO	O	Master Clock Output Pin
16	I2C	I	Control Mode Select Pin "H": I^2C Bus, "L": 3-wire Serial
17	SVDD	-	Speaker-Amp Power Supply Pin, 0.9 ~ 5.5V
18	VSS4	-	Ground 4 Pin
19	SPN	O	Speaker-Amp Negative Output Pin
20	SPP	O	Speaker-Amp Positive Output Pin
21	DVDD	-	Digital Power Supply Pin, 1.6 ~ 2.0V
22	HPL	O	Lch Headphone-Amp Output Pin
23	HPR	O	Rch Headphone-Amp Output Pin
24	PVEE	O	Charge-Pump Circuit Negative Voltage Output Pin This pin must be connected to VSS3 with 2.2µF±50% capacitor in series.
25	VSS3	-	Ground 3 Pin
26	CP	O	Positive Charge-Pump Capacitor Terminal Pin This pin must be connected to CN pin with 2.2µF±50% capacitor in series.
27	CN	I	Negative Charge-Pump Capacitor Terminal Pin This pin must be connected to CP pin with 2.2µF±50% capacitor in series.
28	AVDD	-	Analog Power Supply Pin, 2.85 ~ 3.5V
29	VSS1	-	Ground 1 Pin
30	REGFIL	O	Regulator Ripple Filter Pin This pin must be connected to VSS1 with 2.2µF±50% capacitor in series.
31	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 with 2.2µF±50% capacitor in series.
32	LIN3	I	Lch Analog Input 3 Pin
33	RIN3	I	Rch Analog Input 3 Pin
34	LIN2	I	Lch Analog Input 2 pin
35	RIN2	I	Rch Analog Input 2 Pin
36	MPWR2	O	MIC Power Supply Pin for Microphone 2

Note 2. All input pins except analog input pins (LIN1, RIN1, LIN2, RIN2, LIN3, RIN3) must not be left floating.

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR1, MPWR2, SPN, SPP, HPL, HPR, CP, CN, PVEE, LIN1/DMDAT, RIN1/DMCLK, LIN2, RIN2, LIN3, RIN3	These pins must be open.
Digital	MCKO	This pin must be open.
	MCKI	This pin must be connected to VSS2.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=VSS4=0V; Note 3)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	2.5	V
	Digital I/O	TVDD	–0.3	6.0	V
	Speaker-Amp	SVDD	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 5)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 6)		VIND	–0.3	TVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 7)	Ta = 85°C (Note 8)	Pd1	-	660	mW
	Ta = 70°C (Note 9)	Pd2	-	900	mW

Note 3. All voltages are with respect to ground.
Note 4. VSS1, VSS2, VSS3 and VSS4 must be connected to the same analog ground plane.
Note 5. LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins
Note 6. PDN, CSN, CCLK, CDTIO, SDTI, LRCK, BICK and MCKI pins
Pull-up resistors at SDA and SCL pins should be connected to (TVDD+0.3)V or less voltage.
Note 7. In case that PCB wiring density is 100% over. This power is the AK4953A internal dissipation that does not include power dissipation of externally connected speakers.
Note 8. The Speaker Amplifier is not available.
Note 9. The Speaker Amplifier is available.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4=0V; Note 3)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 10)	Analog	AVDD	2.85	3.3	3.5	V
	Digital	DVDD	1.6	1.8	2.0	V
	Digital I/O	TVDD	DVDD	3.3	3.5	V
	SPK-Amp	SVDD	0.9	3.3	5.5	V

Note 3. All voltages are with respect to ground.

Note 10. The power-up sequence between AVDD, DVDD, TVDD and SVDD is not critical. The PDN pin must be "L" upon power up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

*** When SVDD is powered ON and the PDN pin is "L", AVDD, DVDD or TVDD can be powered ON/OFF. When TVDD is powered ON and the PDN pin is "L", AVDD, DVDD or SVDD can be powered ON/OFF. When the AK4953A is changed from power down state to power ON, the PDN pin must be "H" after all power supplies are ON.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=TVDD=SVDD=3.3V, DVDD=1.8V; VSS1=VSS2=VSS3=VSS4=0V; fs=44.1kHz, BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter			Min.	Typ.	Max.	Unit
MIC Amplifier: LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins						
Input Resistance			20	30	40	kΩ
Gain	MGAIN2-0 bits = "000"		-1	0	+1	dB
	MGAIN2-0 bits = "001"		+11	+12	+13	dB
	MGAIN2-0 bits = "010"		+15	+16	+17	dB
	MGAIN2-0 bits = "011"		+19	+20	+21	dB
	MGAIN2-0 bits = "100"		+22	+23	+24	dB
	MGAIN2-0 bits = "101"		+25	+26	+27	dB
	MGAIN2-0 bits = "110"		+28	+29	+30	dB
MIC Power Supply: MPWR1, MPWR2 pins						
Output Voltage			2.1	2.3	2.5	V
Output Noise Level (A-weighted)			-	-108	-	dBV
PSRR (f = 1kHz) (Note 11)			-	100	-	dB
Load Resistance			1.0	-	-	kΩ
Load Capacitance			-	-	30	pF
ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3 pins → ADC → Programmable Filter (IVOL=0dB, EQ=ALC=OFF) → SDTO						
Resolution			-	-	24	Bits
Input Voltage		(Note 12)	0.21	0.24	0.27	Vpp
		(Note 13)	2.16	2.4	2.64	Vpp
S/(N+D) (-1dBFS)	fs=44.1kHz BW=20kHz	(Note 12)	72	82	-	dBFS
		(Note 13)	-	85	-	dBFS
	fs=96kHz BW=40kHz	(Note 12)	-	79	-	dBFS
		(Note 13)	-	80	-	dBFS
D-Range (−60dBFS, A-weighted)		(Note 12)	78	88	-	dB
		(Note 13)	-	96	-	dB
S/N (A-weighted)		(Note 12)	78	88	-	dB
		(Note 13)	-	96	-	dB
Interchannel Isolation		(Note 12)	75	90	-	dB
		(Note 13)	-	100	-	dB
Interchannel Gain Mismatch		(Note 12)	-	0	0.8	dB
		(Note 13)	-	0	0.8	dB

Note 11. PSR is applied to AVDD with 500mpVpp sine wave.
Note 12. MGAIN2-0 bits = "011" (+20dB)
Note 13. MGAIN2-0 bits = "000" (0dB)

Parameter			Min.	Typ.	Max.	Unit
DAC Characteristics:						
Resolution			-	-	24	Bits
Headphone-Amp Characteristics: DAC → HPL, HPR pins, ALC=OFF, OVOL=DVOL= 0dB, R_L=16Ω						
Output Voltage (0dBFS)		(0dBFS)	-	1.75	-	Vpp
		(-3dBFS)	1.11	1.24	1.37	Vpp
S/(N+D)	(0dBFS)	fs=44.1kHz, BW=20kHz (Note 14)	-	80	-	dB
	(-3dBFS)	fs=44.1kHz, BW=20kHz	70	80	-	dB
		fs=96kHz, BW=40kHz	-	77	-	dB
S/N (A-weighted)			86	96	-	dB
Interchannel Isolation			75	90	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Output Offset Voltage			- 1	0	+ 1	mV
PSRR (f = 1kHz) (Note 15)			-	80	-	dB
Load Resistance			16	-	-	Ω
Load Capacitance			-	-	300	pF
Speaker-Amp Characteristics: DAC → SPP/SPN pins, ALC=OFF, OVOL=DVOL= 0dB, R_L=8Ω, BTL						
Output Voltage (Note 16)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	3.18	-	Vpp
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	1.79	-	Vrms
SPKG1-0 bits = "00", –1.5dBFS (Po=100mW) (Note 17)			-	0.9	-	Vrms
S/(N+D)						
SPKG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	70	-	dB
SPKG1-0 bits = "01", –0.5dBFS (Po=250mW)			40	70	-	dB
SPKG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	20	-	dB
SPKG1-0 bits = "00", –1.5dBFS (Po=100mW) (Note 17)			-	20	-	dB
S/N (A-weighted)			85	95	-	dB
Output Offset Voltage			-30	0	+30	mV
PSRR (f = 1kHz) (Note 18)			-	50	-	dB
Load Resistance			6.8	8	-	Ω
Load Capacitance			-	-	30	pF

Note 14. When CPCK bit = "1".

Note 15. PSR is applied to AVDD or DVDD with 500mpVpp sine wave.

Note 16. The output level is calculated by assuming that output signals are not clipped. In the actual case, the output signal is clipped when DAC outputs 0dBFS signal. Therefore, DAC output level should be set to lower level by setting digital volume so that Speaker-Amp output level is not clipped.

Note 17. When SVDD = 1.5V.

Note 18. PSR is applied to AVDD or SVDD with 500mpVpp sine wave.

Parameter			Min.	Typ.	Max.	Unit
Power Supplies:						
Power Up (PDN pin = "H")						
	MIC + ADC + DAC + Headphone out					
		AVDD+DVDD+TVDD (Note 19)	-	8.9	13.4	mA
		AVDD+DVDD+TVDD (Note 20)	-	6.1	-	mA
		SVDD (No Load)	-	11	17	μA
	MIC + ADC + DAC + Speaker out					
		AVDD+DVDD+TVDD (Note 21)	-	7.8	11.7	mA
		AVDD+DVDD+TVDD (Note 22)	-	5.1	-	mA
		SVDD (No Load)	-	1.3	2.0	mA
	MIC + ADC (Note 23)					
		AVDD+DVDD+TVDD	-	3.3	-	mA
	DAC + Headphone out (Note 24)					
		AVDD+DVDD+TVDD	-	3.6	-	mA
Power Down (PDN pin = "L") (Note 25)						
	AVDD+DVDD+TVDD+SVDD		-	1	10	μA
	SVDD (Note 26)		-	0	10	μA

Note 19. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMHPL=PMHPR= PMVCM=PMPLL=MCKO=PMBP=PMMP=M/S bits = "1". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 4.6 mA (typ), DVDD= 2.2 mA (typ), TVDD= 2.1 mA (typ).

Note 20. When EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"), PMADL=PMADR=PMDAC=PMHPL=PMHPR= PMVCM=PMBP=PMMP bits = "1", and PMPFIL bit = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 4.2 mA (typ), DVDD= 1.8 mA(typ), TVDD= 0.1 mA (typ).

Note 21. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMSPK=PMVCM= PMPLL=MCKO=PMBP=PMMP=M/S bits = "1". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 3.9 mA (typ), DVDD= 1.8 mA (typ), TVDD= 2.1 mA (typ).

Note 22. When EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"), PMADL=PMADR=PMDAC=PMSPK=PMVCM= PMBP=PMMP bits = "1", and PMPFIL bit = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 3.6 mA (typ), DVDD= 1.4 mA(typ), TVDD= 0.1 mA (typ).

Note 23. When EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"), PMADL=PMADR=PMVCM bits = "1", and PMPFIL bit = "0". AVDD= 2.2 mA (typ), DVDD= 1.0 mA(typ), TVDD= 0.1 mA (typ).

Note 24. When EXT Slave Mode (PMPLL=M/S=MCKO bits ="0"), PMDAC=PMHPL=PMHPR=PMVCM bits = "1", and PMPFIL bit = "0". AVDD= 2.5 mA (typ), DVDD= 1.1 mA(typ), TVDD= 0 mA (typ).

Note 25. All digital input pins are fixed to TVDD or VSS2.

Note 26. When AVDD, DVDD, and TVDD are powered OFF.

■ Power Consumption on Each Operation Mode

Conditions: Ta=25°C; AVDD=TVDD=SVDD=3.3V, DVDD=1.8V; VSS1=VSS2=VSS3=VSS4=0V; fs=44.1kHz,
External Slave Mode, BICK=64fs; 1kHz, 0dBFS input; Headphone & Speaker = No output.

Mode	Power Management Bit							AVDD [mA]	DVDD [mA]	TVDD [mA]	SVDD [mA]	Total Power [mW]
	00H					01H						
	PMVCM	PMSPK	PMDAC	PMADL	PMADR	PMHPL	PMHPR					
All Power-down	0	0	0	0	0	0	0	0	0	0	0	0
LIN1/RIN1 → ADC	1	0	0	1	1	0	0	2.2	1.0	0.1	0	9.4
LIN1 (Mono) → ADC	1	0	0	1	0	0	0	1.5	1.0	0.1	0	7.1
DAC → HP	1	0	1	0	0	1	1	2.5	1.1	0	0	10.2
DAC → SPK	1	1	1	0	0	0	0	1.8	0.7	0	1.3	11.5
LIN1/RIN1 → ADC & DAC → HP	1	0	1	1	1	1	1	3.9	1.8	0.1	0	16.4
LIN1/RIN1 → ADC & DAC → SPK	1	1	1	1	1	0	0	3.1	1.4	0.1	1.3	17.4

Table 1. Power Consumption on Each Operation Mode (typ)

ADC FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta =25°C; AVDD=2.85~3.5V, DVDD=1.6~2.0V, TVDD=DVDD~3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 27)	±0.16dB	PB	0	-	17.3	kHz
	−0.66dB		-	19.4	-	kHz
	−1.1dB		-	19.9	-	kHz
	−6.9dB		-	22.1	-	kHz
Stopband		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 28)		GD	-	16	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	−3.0dB	FR	-	3.4	-	Hz
	−0.5dB		-	10	-	Hz
	−0.1dB		-	22	-	Hz

ADC FILTER CHARACTERISTICS (fs=96kHz)

(Ta =25°C; AVDD=2.85~3.5V, DVDD=1.6~2.0V, TVDD=DVDD ~ 3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 27)	±0.16dB	PB	0	-	37.7	kHz
	−0.66dB		-	42.2	-	kHz
	−1.1dB		-	43.3	-	kHz
	−6.9dB		-	48.0	-	kHz
Stopband		SB	56.8	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 28)		GD	-	16	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	−3.0dB	FR	-	7.4	-	Hz
	−0.5dB		-	21.8	-	Hz
	−0.1dB		-	47.9	-	Hz

Note 27. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 28. A calculating delay time which induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register. For the signal through the programmable filters (First HPF + First LPF + 4-band Equalizer + ALC + Equalizer), the group delay is increased 4/fs from the value above if there is no phase change by the IIR filter.

DAC FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta =25°C; AVDD=2.85 ~ 3.5V, DVDD =1.6 ~ 2.0V, TVDD=DVDD ~ 3.5V, SVDD=0.9 ~ 5.5V; DEM=OFF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 29)	±0.05dB −6.0dB	PB	0 -	- 22.05	20.0 -	kHz kHz
Stopband		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 30)		GD	-	22	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz		FR	-	±1.0	-	dB

DAC FILTER CHARACTERISTICS (fs=96kHz)

(Ta =25°C; AVDD=2.85 ~ 3.5V, DVDD =1.6 ~ 2.0V, TVDD=DVDD ~ 3.5V, SVDD=0.9 ~ 5.5V; DEM=OFF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
DAC Digital Filter (LPF):						
Passband (Note 29)	±0.05dB −6.0dB	PB	0 -	- 48.0	43.5 -	kHz kHz
Stopband		SB	52.5	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 30)		GD	-	22	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 40.0kHz		FR	-	±1.0	-	dB

Note 29. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 30. A calculating delay time which induced by digital filtering. This time is from setting the 24bit data of both channels to input register to the output of analog signal. For the signal through the programmable filters (First HPF + First LPF + 4-band Equalizer + ALC + Equalizer), the group delay is increased 7/fs from the value above if there is no phase change by the IIR filter.

DC CHARACTERISTICS

(Ta =25°C; AVDD=2.85 ~ 3.5V, DVDD =1.6 ~ 2.0V, TVDD=DVDD ~ 3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Audio Interface & Serial µP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, SDTI, MCKI pins)						
High-Level Input Voltage	(TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
	(TVDD < 2.2V)		80%TVDD	-	-	V
Low-Level Input Voltage	(TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
	(TVDD < 2.2V)		-	-	20%TVDD	V
Audio Interface & Serial µP Interface (CDTIO, SDA, MCKO, BICK, LRCK, SDTO pins Output)						
High-Level Output Voltage	(Iout = −80µA)	VOH	TVDD−0.2	-	-	V
Low-Level Output Voltage						
	(Except SDA pin : Iout = 80µA)	VOL1	-	-	0.2	V
	(SDA pin, 2.0V ≤ TVDD ≤ 3.5V: Iout = 3mA)	VOL2	-	-	0.4	V
	(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Input Leakage Current		Iin	-	-	±10	µA
Digital MIC Interface (DMDAT pin Input ; DMIC bit = "1")						
High-Level Input Voltage		VIH3	65%AVDD	-	-	V
Low-Level Input Voltage		VIL3	-	-	35%AVDD	V
Digital MIC Interface (DMCLK pin Output ; DMIC bit = "1")						
High-Level Output Voltage	(Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage	(Iout= 80µA)	VOL3	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta =25°C; AVDD=2.85 ~ 3.5V, DVDD =1.6 ~ 2.0V, TVDD=DVDD ~ 3.5V, SVDD=0.9 ~ 5.5V; C_L=20pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	24.576	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Output Timing						
Frequency		fs	7.35	Table 7	96	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing						
Frequency		fMCK	0.2352	-	24.576	MHz
Duty Cycle						
Except 256fs at fs=32kHz, 29.4kHz		dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz		dMCK	-	33	-	%
LRCK Input Timing						
Frequency		fs	7.35	Table 7	96	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period		tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter		Symbol	Min.	Typ.	Max.	Unit
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency		fs	7.35	-	96	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period	PLL3-0 bits = "0010"	tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = "0011"	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	24.576	MHz
	384fs	fCLK	2.8224	-	18.432	MHz
	512fs	fCLK	3.7632	-	24.576	MHz
	1024fs	fCLK	7.5264	-	12.288	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing						
Frequency	256fs	fs	7.35	-	96	kHz
	384fs	fs	7.35	-	48	kHz
	512fs	fs	7.35	-	48	kHz
	1024fs	fs	7.35	-	12	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period (Note 31)		tBCK	156.25 or 1/(254fs)	-	-	ns s
Pulse Width Low		tBCKL	65	-	-	ns
Pulse Width High		tBCKH	65	-	-	ns
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	24.576	MHz
	384fs	fCLK	2.8224	-	18.432	MHz
	512fs	fCLK	3.7632	-	24.576	MHz
	1024fs	fCLK	7.5264	-	12.288	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing						
Frequency		fs	7.35	-	96	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%

Note 31. The minimum value is longer time between 156.25ns and 1/(254fs)s.

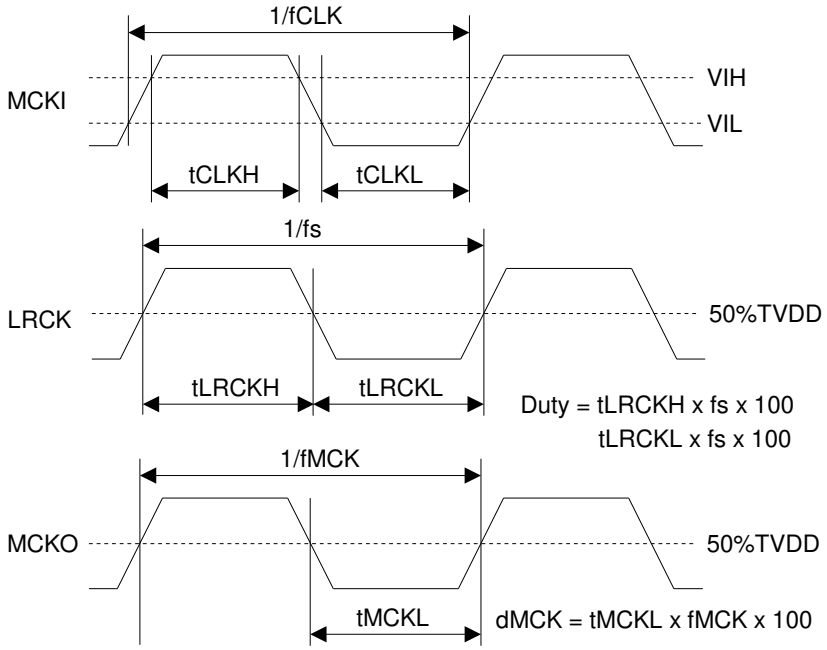
Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 32)	tMBLR	–20	-	20	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–35	-	35	ns
BICK "↓" to SDTO	tBSD	–35	-	35	ns
SDTI Hold Time	tSDH	25	-	-	ns
SDTI Setup Time	tSDS	20	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 32)	tLRB	25	-	-	ns
BICK "↑" to LRCK Edge (Note 32)	tBLR	25	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	45	ns
BICK "↓" to SDTO	tBSD	-	-	45	ns
SDTI Hold Time	tSDH	25	-	-	ns
SDTI Setup Time	tSDS	20	-	-	ns
Control Interface Timing (3-wire Mode):					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 33)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 33)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command)(Note 35)	tCCZ	-	-	70	ns
Control Interface Timing (I²C Bus Mode):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 36)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 32. BICK rising edge must not occur at the same time as LRCK edge.
Note 33. CCLK rising edge must not occur at the same time as CSN edge.
Note 34. I²C-bus is a trademark of NXP B.V.
Note 35. R_L=1kΩ/10% change (pull-up or TVDD)
Note 36. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Audio Interface Timing; fs = 7.35kHz ~ 48kHz, C_L=100pF						
DMCLK Output Timing						
Period		tSCK	-	1/(64fs)	-	ns
Rising Time		tSRise	-	-	10	ns
Falling Time		tSFall	-	-	10	ns
Duty Cycle		dSCK	40	50	60	%
Audio Interface Timing						
DMDAT Setup Time		tSDS	50	-	-	ns
DMDAT Hold Time		tSDH	0	-	-	ns
Power-down & Reset Timing						
PDN Pulse Width	(Note 37)	tPD	150	-	-	ns
PMADL or PMADR "↑" to SDTO valid	(Note 38)					
ADRST1-0 bits = "00"		tPDV	-	1059	-	1/fs
ADRST1-0 bits = "01"		tPDV	-	267	-	1/fs
ADRST1-0 bits = "10", "11"		tPDV	-	2115	-	1/fs

Note 37. The AK4953A can be reset by the PDN pin = "L".
Note 38. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

■ Timing Diagram



Note 39. MCKO is not available at EXT Master mode.

Figure 2. Clock Timing (PLL/EXT Master mode)

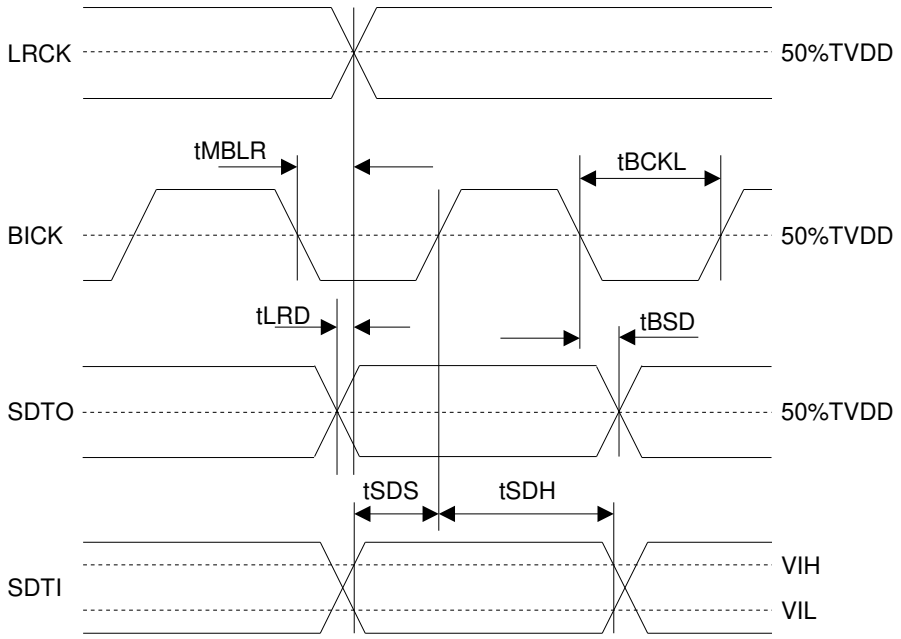


Figure 3. Audio Interface Timing (PLL/EXT Master mode)

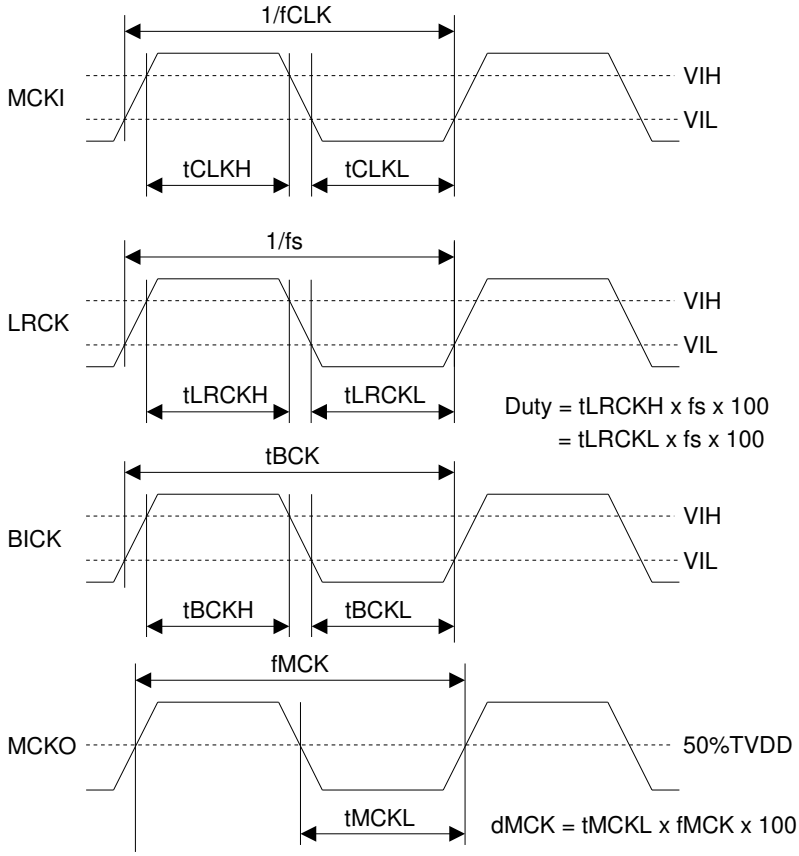


Figure 4. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin)

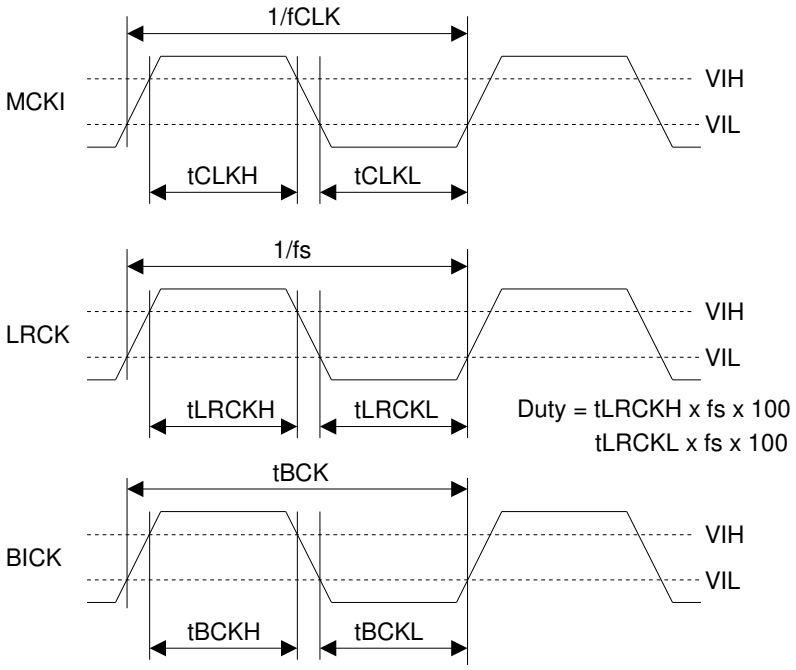


Figure 5. Clock Timing (EXT Slave mode)

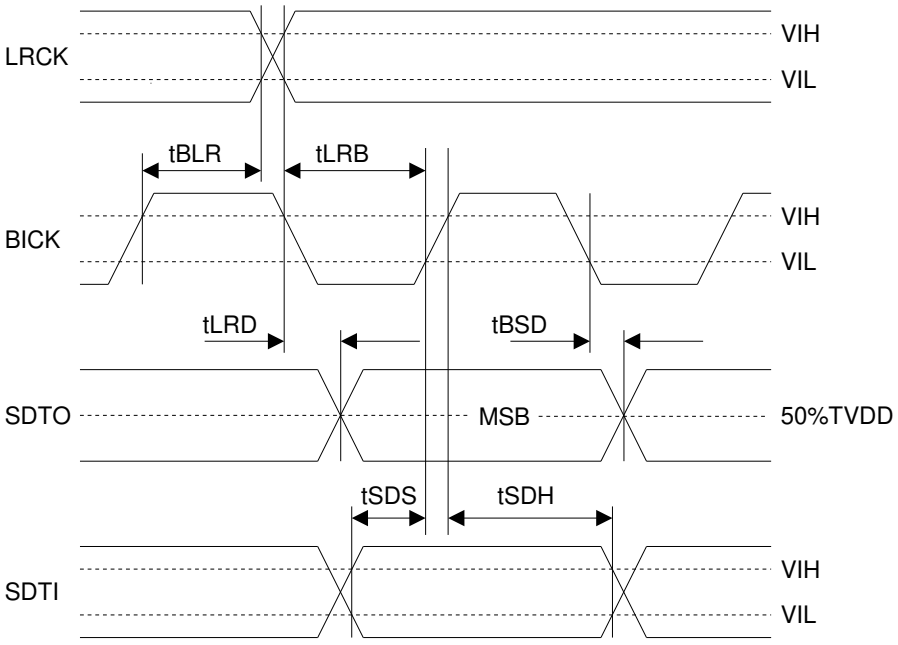


Figure 6. Audio Interface Timing (PLL/EXT Slave mode)

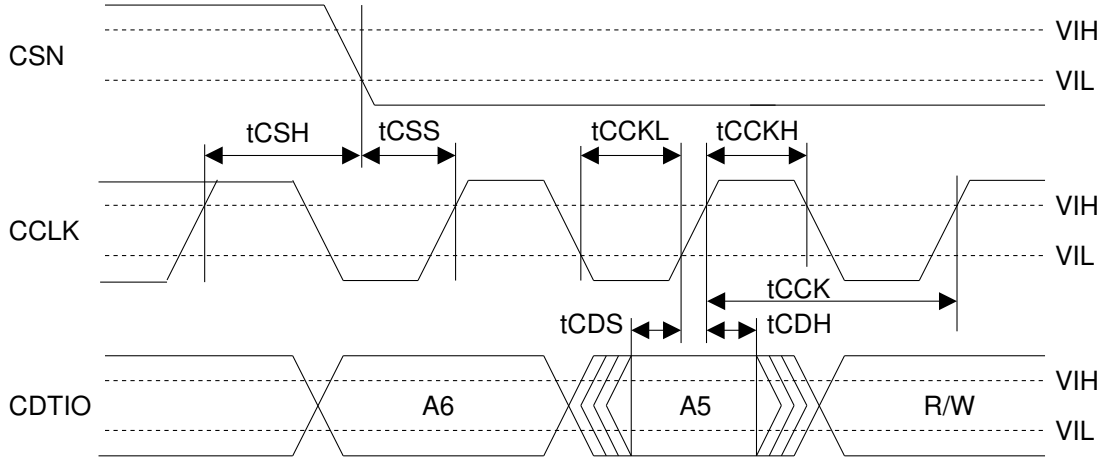


Figure 7. WRITE Command Input Timing

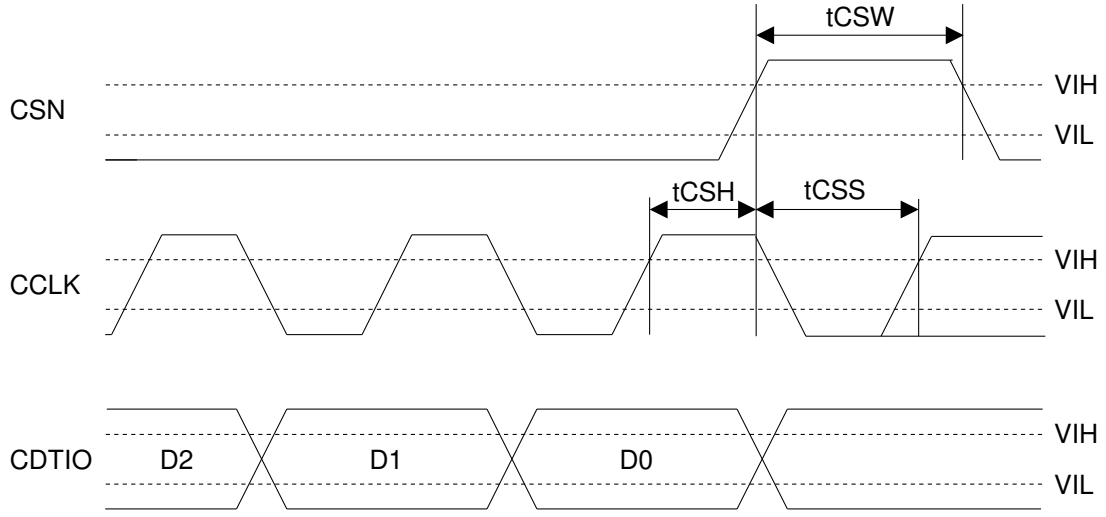


Figure 8. WRITE Data Input Timing

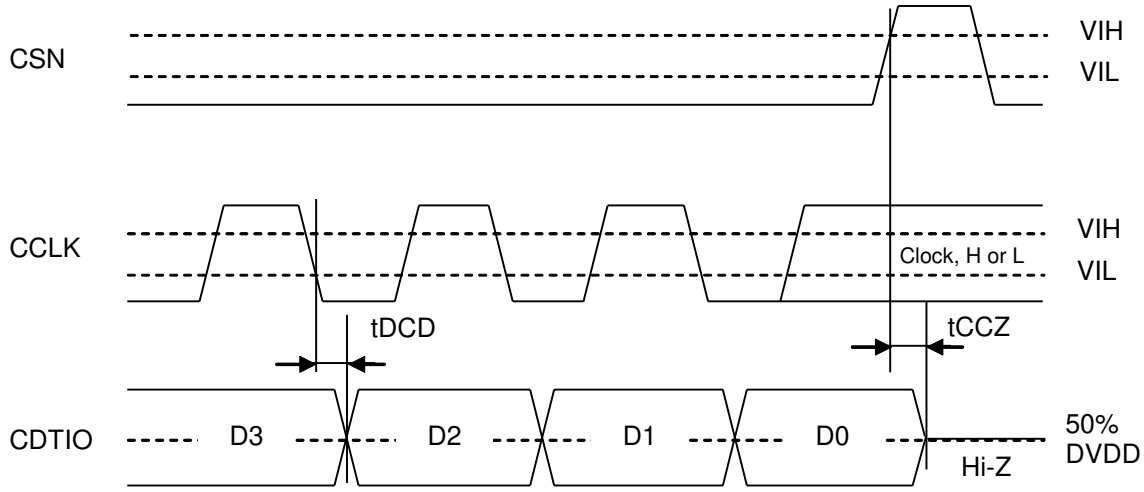


Figure 9. Read Data Output Timing

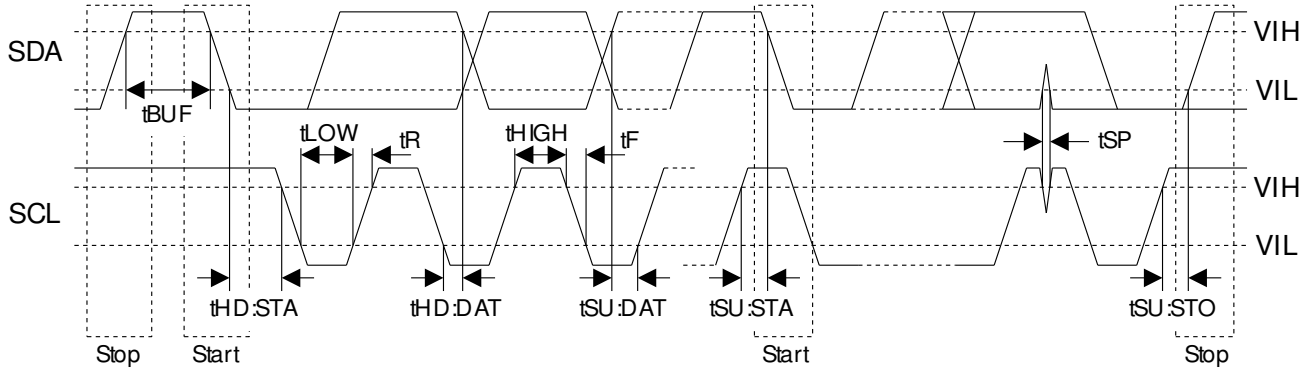
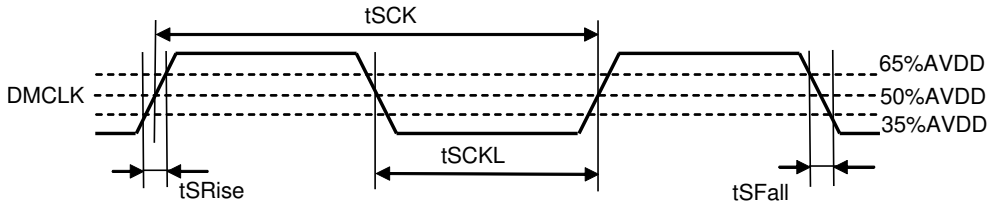


Figure 10. I²C Bus Mode Timing



dSCK = 100 x tSCKL / tSCK

Figure 11. DMCLK Clock Timing

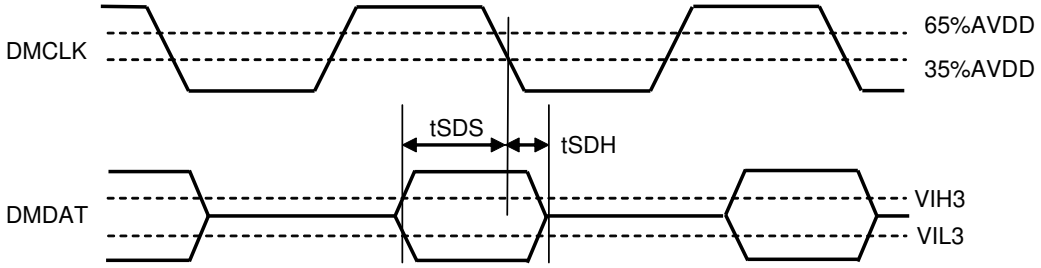


Figure 30. Audio Interface Timing (DCLKP bit = "1")

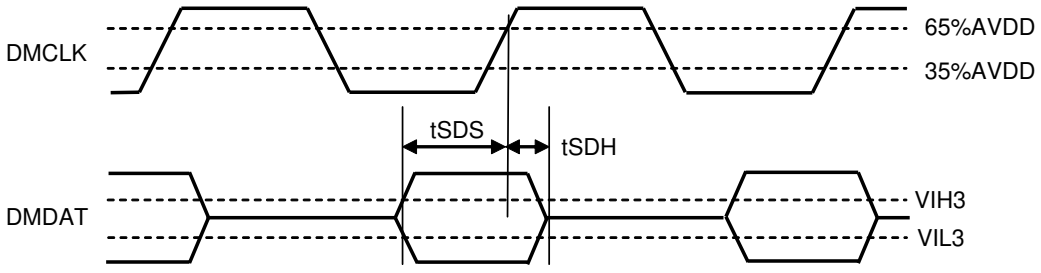


Figure 31. Audio Interface Timing (DCLKP bit = "0")

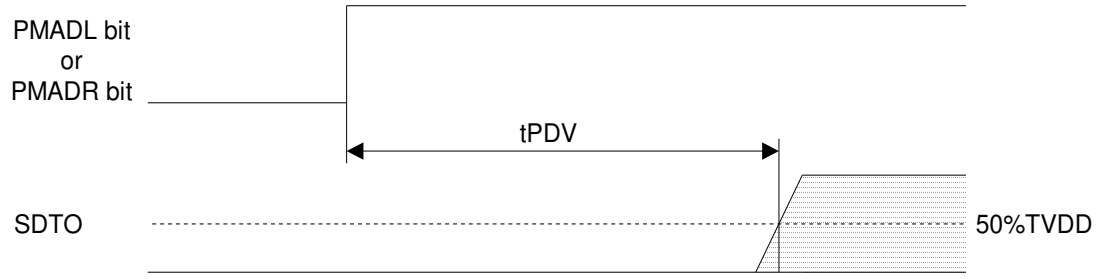


Figure 12. Power Down & Reset Timing 1

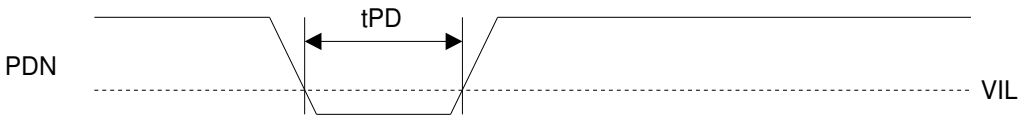


Figure 13. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 2, Table 3).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 40)	1	1	Table 5	Figure 14
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 5	Figure 15
PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin)	1	0	Table 5	Figure 16
EXT Slave Mode	0	0	x	Figure 17
EXT Master Mode	0	1	x	Figure 18

Note 40. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from the MCKO pin.

Table 2. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	Output (Selected by BCKO bit)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: BICK pin)	0	L	GND	Input (Selected by PLL3-0 bits)	Input (1fs)
EXT Slave Mode	0	L	Selected by FS3-0 bits	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	0	L	Selected by FS3-0 bits	Output (Selected by BCKO bit)	Output (1fs)

Note 41. When PMVCM bit = M/S bit = "1" and MCKI is input, LRCK and BICK are output, even if PMDAC bit = PMADL bit = PMADR bit = "0".

Table 3. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4953A is in power-down mode (PDN pin = "L") and when exits reset state, the AK44953 is in slave mode. After exiting reset state, the AK4953A goes to master mode by changing M/S bit = "1".

When the AK4953A is in master mode, the LRCK and BICK pins are a floating state until M/S bit becomes "1". The LRCK and BICK pins of the AK4953A must be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 4. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock times, when the AK4953A is supplied stable clocks or the sampling frequency is changed after PLL is powered-up (PMPLL bit = "0" → "1"), are shown in Table 5.

1) PLL Mode Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)
2	0	0	1	0	BICK pin	32fs	2 ms
3	0	0	1	1	BICK pin	64fs	2 ms
4	0	1	0	0	MCKI pin	11.2896MHz	10 ms
6	0	1	1	0	MCKI pin	12MHz	10 ms
7	0	1	1	1	MCKI pin	24MHz	10 ms
12	1	1	0	0	MCKI pin	13.5MHz	10 ms
13	1	1	0	1	MCKI pin	27MHz	10 ms
Others	Others				N/A		

Note 42. PLL3-0 bits = "0000"(Default: N/A). When PLL mode is used, PLL3-0 bits must be set before PMPLL bit = "0" → "1".

Table 5. PLL Mode Setting (*fs: Sampling Frequency, N/A: Not Available)

2) Setting of sampling frequency in PLL Mode (PLL reference clock pin: MCKI pin)
When PLL2 bit is "1" (PLL reference clock input is MCKI pin), the sampling frequency is selected by FS3-0 bits as defined in Table 6.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	DS bit	Sampling Frequency (Note 43)	
0	0	0	0	0	0	8kHz mode	(default)
1	0	0	0	1		12kHz mode	
2	0	0	1	0		16kHz mode	
3	0	0	1	1		24kHz mode	
4	0	1	0	0		7.35kHz mode	
5	0	1	0	1		11.025kHz mode	
6	0	1	1	0		14.7kHz mode	
7	0	1	1	1		22.05kHz mode	
8	1	0	0	0		32kHz mode	
9	1	0	0	1		48kHz mode	
10	1	0	1	0	1	64kHz mode	
11	1	0	1	1		96kHz mode	
12	1	1	0	0	0	29.4kHz mode	
13	1	1	0	1		44.1kHz mode	
15	1	1	1	1	1	88.2kHz mode	
Others	Others					N/A	

Table 6. Setting of Sampling Frequency at PLL2 bit = "1" and PMPLL bit = "1" (Reference Clock = MCKI pin), (N/A: Not Available)

Note 43. When the MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL3-0 bits) and sampling frequency (FS3-0 bits). Refer to Table 7 for the details of sampling frequency. In master mode, LRCK and BICK output frequency correspond to sampling frequencies shown in Table 7. When the BICK pin is the PLL reference clock input, the sampling frequency generated by PLL is the same sampling frequency of mode name.