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AK4954A

32-bit Stereo CODEC with MIC/HP/SPK-AMP

GENERAL DESCRIPTION

The AK4954A is a low power consumption 32-bit stereo CODEC with a microphone, a headphone and a speaker amplifiers. The input circuits include a microphone amplifier and an ALC (Automatic Level Control) circuit, and the output circuits include a cap-less headphone amplifier and a speaker amplifier. It is suitable for portable application with recording/playback function. The integrated charge pump circuit generates a negative voltage and removes the output AC coupling capacitors. The speaker amplifier has a wide operating voltage range, which is from 0.9V to 5.5V, enabling a direct drive to batteries. The AK4954A is available in a small 32-pin QFN (4x4mm 0.4mm pitch), utilizing less board space than competitive offerings.

FEATURES

1. Recording Function
- **Two Low Noise Microphone Power Supplies**
- **Stereo Single-ended input with three Selectors**
- **Low Noise Microphone Amplifier (+26dB/+20dB/+13dB/+6dB/0dB)**
- **Digital ALC (Automatic Level Control)**
  (Setting Range: +36dB ~ –52.5dB, 0.375dB Step)
- **ADC Performance: S/(N+D): 88dB, DR, S/N: 97dB (Microphone Amplifier =+20dB)**
  S/(N+D): 88dB, DR, S/N: 100dB (Microphone Amplifier =0dB)
- **Two Types of Decimation Filters**
- **Overflow Detection**
- **Wind-noise Reduction Filter**
- **Stereo Separation Emphasis Circuit**
- **5-band Notch Filter**
- **Digital Microphone Interface**

2. Playback Function
- **Digital ALC (Automatic Level Control)**
  (Setting Range: +36dB ~ –52.5dB, 0.375dB Step)
- **3-band Dynamic Range Control Circuit**
- **Digital Volume Control (+6dB ~ –65.5dB, 0.5dB Step, Mute)**
- **Capacitor-less Stereo Headphone Amplifier**
  - **HP-Amplifier Performance: S/(N+D): 65dB@20mW, S/N: 100dB**
  - **Output Power: 20mW@16Ω**
  - **Pop Noise Free at Power-ON/OFF**
- **Mono Speaker-Amplifier (with Stereo Line Output Switch)**
  - **SPK-Amplifier Performance: S/(N+D): 70dB@250mW**
    Output Noise Level: -97dBV
  - **BTL Output**
  - **Output Power: 400mW@8Ω (SVDD=3.3V)**
    100mW@8Ω (SVDD=1.5V)
- **Beep Generator**

3. Power Management

4. Master Clock:
- **(1) PLL Mode**
  - **Frequencies: 11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz (MCKI pin)**
    32fs or 64fs (BICK pin)
- **(2) External Clock Mode**
  - **Frequencies: 256fs, 384fs, 512fs or 1024fs (MCKI pin)**

5. Sampling Frequencies
- **PLL Slave Mode (BICK pin): 8kHz ~ 96kHz**
- **PLL Master Mode: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, 96kHz**
- **EXT Master/Slave Mode: 8kHz ~ 96kHz (256fs), 8kHz ~ 48kHz (384fs), 8kHz ~ 48kHz (512fs), 8kHz ~ 12kHz (1024fs)**

6. Master/Slave mode

7. Audio Interface Format: MSB First, 2's complement
- **ADC: 16/24/32-bit MSB justified, 16/24/32-bit I^{2}S**
- **DAC: 16/24/32-bit MSB justified, 16/24-bit LSB justified, 16/24/32-bit I^{2}S**

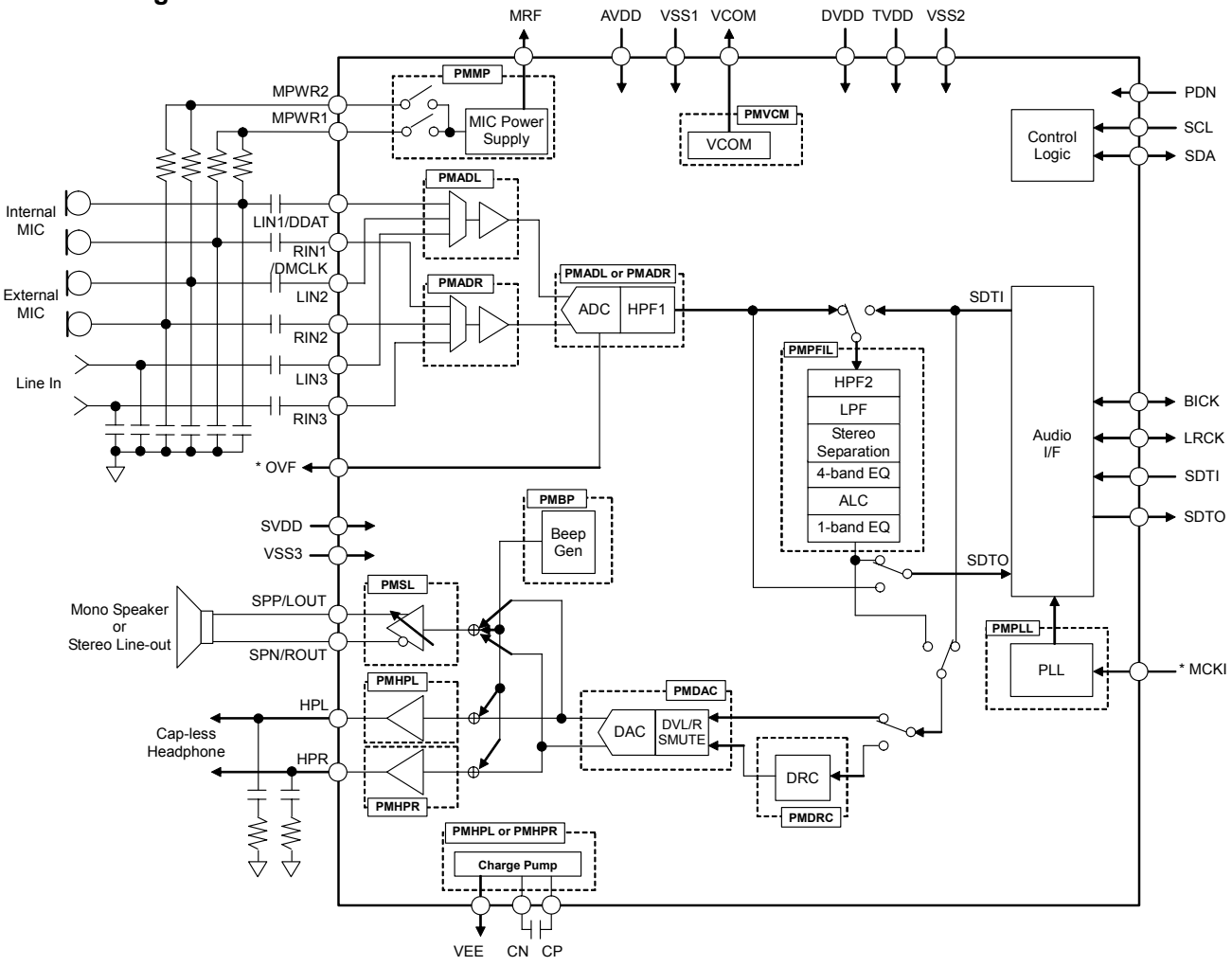
8. Serial μP I/F: I^{2}C Bus (Ver 1.0, 400kHz Fast-Mode)

9. Ta = –30 ~ 85°C

10. Power Supply:
- **Analog Power Supply (AVDD): 2.5 ~ 3.5V**
- **Digital Power Supply (DVDD): 1.6 ~ 1.98V**
- **Digital I/O Power Supply (TVDD): 1.6 or (DVDD-0.2) ~ 3.5V**
- **Speaker Power Supply (SVDD): 0.9 ~ 5.5V**

11. Package: 32-pin QFN (4 x 4mm, 0.4mm pitch)

■ Block Diagram

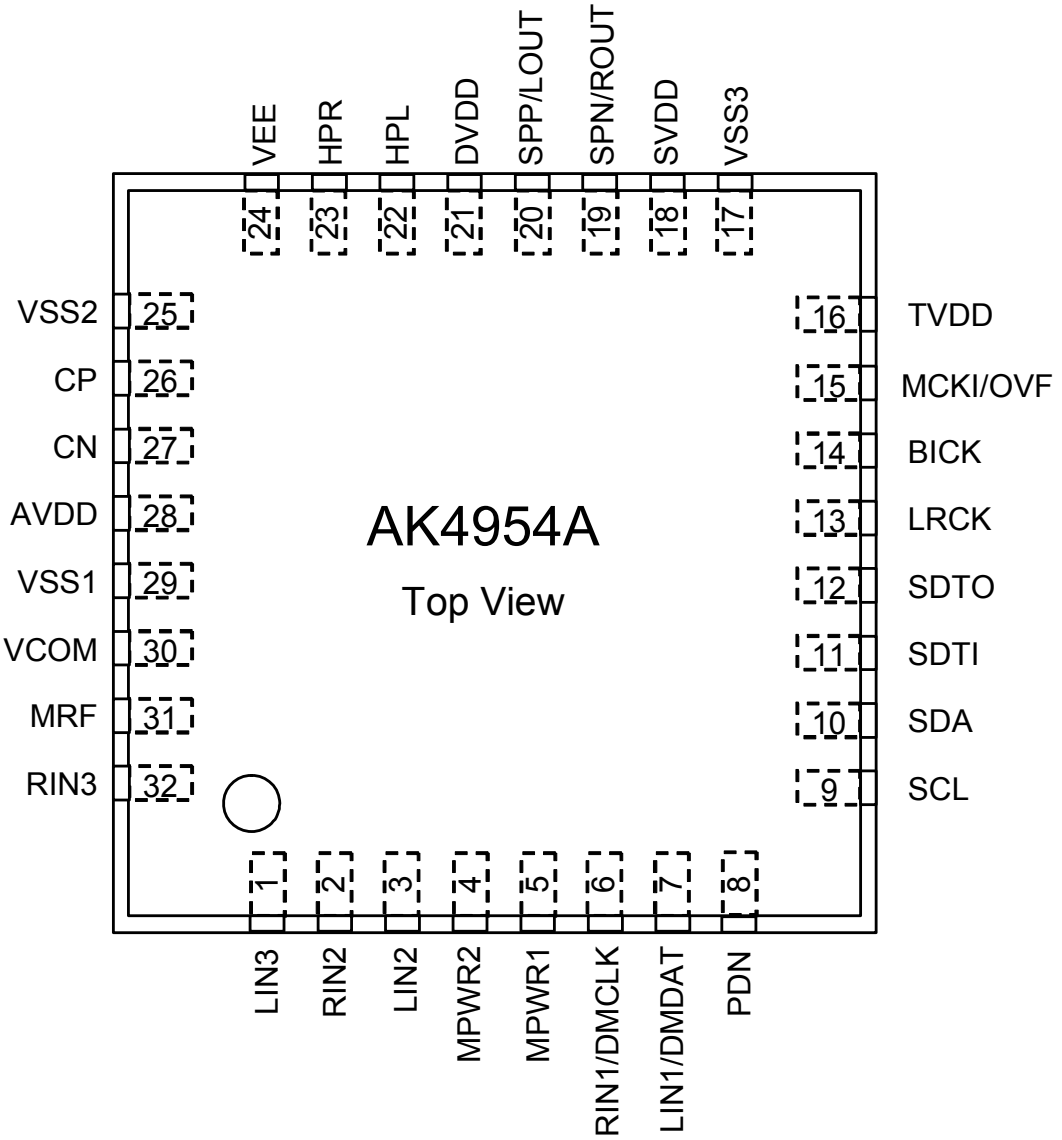


(The OVF and MCKI pins share the No. 15 pin terminal.)
Figure 1. Block Diagram

■ Ordering Guide

AK4954AEN	–30 ~ +85°C	32-pin QFN (0.4mm pitch)
AKD4954	Evaluation board for AK4954A	

■ Pin Layout



■ Comparison with AK4953A

Function	AK4953A	AK4954A
Resolution	24-bit	32-bit
AVDD	2.85V ~ 3.5V	2.5V ~ 3.5V
DVDD	1.6V ~ 2.0V	1.6V ~ 1.98V
SVDD	0.9V ~ 5.5V	←
TVDD	DVDD ~ 3.5V	1.6V or (DVDD-0.2)V ~ 3.5V
ADC DR, S/N	88dB @ MGAIN = +20dB 96dB @ MGAIN = 0dB	97dB @ MGAIN = +20dB 100dB @ MGAIN = 0dB
DAC S/N	96dB	100dB
Input level	typ. 2.4Vpp @ MIC Gain=0dB	typ. 0.8 x AVDD @ MGAIN=0dB
Output level (Headphone)	typ. 1.75Vpp @ DVOL=0dB	typ. 0.485 x AVDD @ DVOL=0dB
MIC Power Output Voltage	typ 2.3V (2 Line Outputs)	0.8 x AVDD (2 Line Outputs)
MIC Power Output Noise	-108dBV (A-weighted)	-120dBV (A-weighted)
MIC-Amp	0dB/+12dB/+16dB/+20dB/+23dB/ +26dB/+29dB	0dB/+6dB/+13dB/+20dB/+26dB
ADC Overflow Output	No	Yes (pin selectable OVF/MCKI)
Stereo Emphasis	No	Yes
Output Volume	+36dB ~ -54dB, 0.375dB Step (Note 1) & +12dB ~ -115dB, 0.5dB Step	+36dB ~ -52.5dB, 0.375dB Step (Note 1) & +6dB ~ -65.5dB, 0.5dB Step
Dynamic Range Control	No	Yes (for Playback)
Line Output Switch for Speaker-Amp	No	Yes
Master Clock Reference for PLL Mode	11.2896MHz, 12MHz, 13.5MHz, 24MHz, 27MHz	11.2896MHz, 12MHz, 12.288MHz, 13.5MHz, 24MHz, 27MHz
Serial µP Interface	3-wire Serial or I^2C Bus	I^2C Bus
Power Consumption **(Stereo Recording)** **(Headphone Playback)**	 typ. 9.4mW typ. 10.2mW	 typ. 10.4mW (Low-power operation mode) typ. 6.2mW (Low-power operation mode)
Package	36-pin QFN (5 x 5mm, 0.4mm pitch)	32-pin QFN (4 x 4mm, 0.4mm pitch)

Note 1. ALC and Volume circuits are shared by input and output. Therefore, it is impossible to use ALC and Volume control function at the same time for both recording and playback mode.

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LIN3	I	Lch Analog Input 3 Pin
2	RIN2	I	Rch Analog Input 2 Pin
3	LIN2	I	Lch Analog Input 2 pin
4	MPWR2	O	Microphone Power Supply Pin for Microphone 2
5	MPWR1	O	Microphone Power Supply Pin for Microphone 1
6	RIN1	I	Rch Analog Input 1 Pin (DMIC bit = "0": default)
	DMCLK	O	Digital Microphone Clock pin (DMIC bit = "1")
7	LIN1	I	Lch Analog Input 1 Pin (DMIC bit = "0": default)
	DMDAT	I	Digital Microphone Data Input Pin (DMIC bit = "1")
8	PDN	I	Power-down & Reset When "L", the AK4954A is in power-down mode and is held in reset. The AK4954A must be always reset upon power-up.
9	SCL	I	Control Data Clock Pin
10	SDA	I/O	Control Data Input/Output Pin
11	SDTI	I	Audio Serial Data Input Pin
12	SDTO	O	Audio Serial Data Output Pin
13	LRCK	I/O	Input/Output Channel Clock Pin
14	BICK	I/O	Audio Serial Data Clock Pin
15	MCKI	I	External Master Clock Input Pin (OVFL bit = "0": default)
	OVF	O	Over Flow Flag Output Pin (OVFL bit = "1")
16	TVDD	-	Digital I/O Power Supply Pin, 1.6 ~ 3.5V
17	VSS3	-	Ground 3 Pin
18	SVDD	-	Speaker Amplifier Power Supply Pin, 0.9 ~ 5.5V
19	SPN	O	Speaker Amplifier Negative Output Pin (LOSEL bit = "0": default)
	ROUT	O	Rch Stereo Line Output Pin (LOSEL bit = "1")
20	SPP	O	Speaker Amplifier Positive Output Pin (LOSEL bit = "0": default)
	LOUT	O	Lch Stereo Line Output Pin (LOSEL bit = "1")
21	DVDD	-	Digital Power Supply Pin, 1.6 ~1.98V
22	HPL	O	Lch Headphone Amplifier Output Pin
23	HPR	O	Rch Headphone Amplifier Output Pin
24	VEE	O	Charge-Pump Circuit Negative Voltage Output Pin This pin must be connected to VSS2 with 2.2µF±50% capacitor in series.
25	VSS2	-	Ground 2 Pin
26	CP	O	Positive Charge-Pump Capacitor Terminal Pin This pin must be connected to CN pin with 2.2µF±50% capacitor in series.
27	CN	I	Negative Charge-Pump Capacitor Terminal Pin This pin must be connected to CP pin with 2.2µF±50% capacitor in series.
27	AVDD	-	Analog Power Supply Pin, 2.5 ~ 3.5V
29	VSS1	-	Ground 1 Pin
30	VCOM	O	Common Voltage Output Pin Bias voltage of ADC inputs and DAC outputs. This pin must be connected to VSS1 with 2.2µF±50% capacitor in series.
31	MRF	O	Microphone Power Supply Ripple Filter Pin This pin must be connected to VSS1 with 2.2µF±50% capacitor in series.
32	RIN3	I	Rch Analog Input 3 Pin

Note 2. All input pins except analog input pins (LIN1, RIN1, LIN2, RIN2, LIN3, RIN3) must not be allowed to float.

■ Handling of Unused Pin

The unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	MPWR1, MPWR2, MRF, SPN, SPP, HPL, HPR, CP, CN, VEE, LIN1/DMDAT, RIN1/DMCLK, LIN2, RIN2, LIN3, RIN3	Open.
Digital	MCKI/OVF	Connect to VSS2 and set OVFL bit = "0".
	SDTI	Connect to VSS2
	SDTO	Open

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=0V; Note 3)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Digital	DVDD	–0.3	2.5	V
	Digital I/O	TVDD	–0.3	6.0	V
	Speaker Amplifier	SVDD	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 5)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 6)		VIND	–0.3	TVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 7)		Pd	-	900	mW

Note 3. All voltages are with respect to ground.

Note 4. VSS1, VSS2 and VSS3 must be connected to the same analog ground plane.

Note 5. LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins

Note 6. PDN, SCL, SDA, SDTI, LRCK, BICK and MCKI pins
Pull-up resistors at SDA and SCL pins should be connected to (TVDD+0.3)V or less voltage.

Note 7. This power is the AK4954A internal dissipation that does not include power dissipation of externally connected speakers. The maximum junction temperature is 125°C and θja (Junction to Ambient) is 42°C/W at JESD51-9 (2p2s). When Pd =900mW and the θja is 42°C/W, the junction temperature does not exceed 125°C. In this case, there is no case that the AK4954A is damaged by its internal power dissipation. Therefore, the AK4954A should be used in the condition of θja ≤ 42°C/W.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3= 0V; Note 3)

Parameter		Symbol	min	typ	max	Unit
Power Supplies	Analog	AVDD	2.5	3.3	3.5	V
(Note 8)	Digital	DVDD	1.6	1.8	1.98	V
	Digital I/O (Note 9)	TVDD	1.6 or (DVDD-0.2)	1.8	3.5	V
	SPK Amplifier	SVDD	0.9	3.3	5.5	V

Note 3. All voltages are with respect to ground.

Note 8. The power-up sequence between AVDD, DVDD, TVDD and SVDD is not critical. The PDN pin must be "L" upon power-up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.

Note 9. The minimum value is higher voltage between DVDD-0.2V and 1.6V.

*** When SVDD is powered ON and the PDN pin is "L", AVDD, DVDD or TVDD can be powered ON/OFF. When TVDD is powered ON and the PDN pin is "L", AVDD, DVDD or SVDD can be powered ON/OFF. The PDN pin must be set to "H" after all power supplies are ON when the AK4954A is powered-up from power-down state.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=SVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3=0V; fs=44.1kHz, BICK=64fs; Signal Frequency=1kHz; 24-bit Data; Measurement Bandwidth=20Hz ~ 20kHz; unless otherwise specified)

Parameter			min	typ	max	Unit
Microphone Amplifier: LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins						
Input Resistance			70	100	140	kΩ
Gain	MGAIN2-0 bits = "000"		+5	+6	+7	dB
	MGAIN2-0 bits = "001"		+12	+13	+14	dB
	MGAIN2-0 bits = "010"		+19	+20	+21	dB
	MGAIN2-0 bits = "011"		+25	+26	+27	dB
	MGAIN2-0 bits = "1xx"		-	0	-	dB
Microphone Power Supply: MPWR1, MPWR2 pins						
Output Voltage (Note 10)			2.51	2.64	2.77	V
Output Noise Level (A-weighted)			-	-120	-	dBV
PSRR (fin = 1kHz) (Note 11)			-	70	-	dB
Load Resistance			1.0	-	-	kΩ
Load Capacitance			-	-	15	pF
ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2/LIN3/RIN3 pins → ADC → Programmable Filter (IVOL=0dB, EQ=ALC=OFF) → SDTO; C_{ext1} = 1µF, C_{ext2} = 1nF (Note 12)						
Resolution			-	-	32	Bits
Input Voltage (Note 13)		(Note 14)	0.237	0.264	0.29	Vpp
		(Note 15)	2.37	2.64	2.90	Vpp
S/(N+D) (−1dBFS)	fs=44.1kHz BW=20kHz	(Note 14)	78	88	-	dBFS
		(Note 15)	-	88	-	dBFS
	fs=96kHz BW=40kHz	(Note 14)	-	85	-	dBFS
		(Note 15)	-	82	-	dBFS
D-Range (−60dBFS, A-weighted)		(Note 14)	87	97	-	dB
		(Note 15)	-	100	-	dB
S/N (A-weighted)		(Note 14)	87	97	-	dB
		(Note 15)	-	100	-	dB
Interchannel Isolation		(Note 14)	80	100	-	dB
		(Note 15)	-	100	-	dB
Interchannel Gain Mismatch		(Note 14)	-	0	0.8	dB
		(Note 15)	-	0	0.5	dB
PSRR (fin = 1kHz) (Note 11, Note 14)			-	40	-	dB

Note 10. The output voltage is proportional to AVDD. (typ. 0.8 x AVDD V)
Note 11. PSRR is applied to AVDD with 100mpVpp sine wave.
Note 12. Measured by the circuit shown below (Figure 2). (C_{ext2} can also be placed between the input pin and VSS1.)

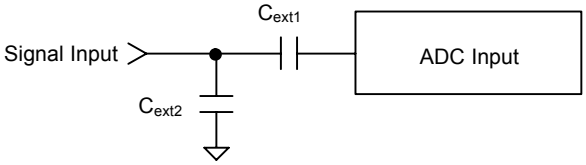


Figure 2. ADC Analog Characteristics Measurement Circuit

Note 13. The input voltage is proportional to AVDD.
typ. 0.8 x AVDD Vpp (0dB), typ. 0.08 x AVDD Vpp (+20dB)
Note 14. MGAIN2-0 bits = "010" (+20dB)
Note 15. MGAIN2-0 bits = "1xx" (0dB).

Parameter			min	typ	max	Unit
DAC Characteristics:						
Resolution			-	-	32	Bits
Headphone Amplifier Characteristics: DAC → HPL, HPR pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=16Ω						
Output Voltage (Note 16)			1.44	1.60	1.76	Vpp
S/(N+D)	(R_L=16Ω)	fs=44.1kHz, BW=20kHz	55	65	-	dB
		fs=96kHz, BW=40kHz	-	65	-	dB
	(R_L=10kΩ)	fs=44.1kHz, BW=20kHz	-	80	-	dB
S/N (A-weighted)			90	100	-	dB
Interchannel Isolation			65	80	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Output Offset Voltage			- 1	0	+ 1	mV
PSRR (fin = 1kHz) (Note 17)			-	40	-	dB
Load Resistance			16	-	-	Ω
Load Capacitance			-	-	300	pF
Speaker Amplifier Characteristics: DAC → SPP/SPN pins, ALC=OFF, IVOL=DVOL= 0dB, R_L=8Ω, BTL						
Output Voltage						
SLG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	3.18	-	Vpp
SLG1-0 bits = "01", –0.5dBFS (Po=250mW)			3.20	4.00	4.80	Vpp
SLG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	1.79	-	Vrms
SLG1-0 bits = "00", –1.5dBFS (Po=100mW) (Note 18)			-	0.9	-	Vrms
S/(N+D)						
SLG1-0 bits = "00", –0.5dBFS (Po=150mW)			-	70	-	dB
SLG1-0 bits = "01", –0.5dBFS (Po=250mW)			40	70	-	dB
SLG1-0 bits = "10", –0.5dBFS (Po=400mW)			-	20	-	dB
SLG1-0 bits = "00", –1.5dBFS (Po=100mW) (Note 18)			-	20	-	dB
Output Noise Level (A-weighted, SLG1-0 bits = "01")			-	-97	-87	dBV
Output Offset Voltage			-30	0	+30	mV
PSRR (fin = 1kHz) (Note 19)			-	50	-	dB
Load Resistance			6.8	8	-	Ω
Load Capacitance			-	-	30	pF
Stereo Line Output Characteristics: DAC → LOUT, ROUT pins, ALC=OFF, IVOL=DVOL=SLG= 0dB, R_L=10kΩ						
Output Voltage (Note 20)			-	2.24	-	Vpp
S/(N+D)			74	84	-	dB
S/N (A-weighted)			84	94	-	dB
Interchannel Isolation			-	90	-	dB
Interchannel Gain Mismatch			-	0	0.8	dB
Load Resistance			10	-	-	kΩ
Load Capacitance			-	-	30	pF

Note 16. The full-scale output voltage is proportional to AVDD. (typ. 0.485 x AVDD Vpp)
Note 17. PSRR is applied to AVDD or DVDD with 100mpVpp sine wave.
Note 18. When SVDD = 1.5V.
Note 19. PSRR is applied to AVDD or SVDD with 100mpVpp sine wave.
Note 20. The full-scale output voltage is proportional to AVDD. (typ. 0.68 x AVDD Vpp)

Parameter	min	typ	max	Unit
Beep Output Characteristics: BEEP Generator → HPL, HPR pins, SPP/SPN pins, LOUT, ROUT pins				
Output Voltage (BPLVL = 0dB)				
HPL, HPR pins (R_L=16Ω)	-	1.5	-	Vpp
SPP/SPN pins (R_L=8Ω, BTL, SLG = +4.26dB)	-	2.8	-	Vpp
LOUT, ROUT pins (R_L=10kΩ, SLG = 0dB)	-	1.4	-	Vpp
Gain				
Gain Setting	-60	-	0	dB
Step Width	-	3	-	dB
Power Supplies:				
Power-up (PDN pin = "H")				
MIC + ADC + DAC + Headphone out				
AVDD+DVDD+TVDD (Note 21)	-	9.2	13.8	mA
AVDD+DVDD+TVDD (Note 22)	-	8.2	-	mA
SVDD (No Load)	-	8	12	μA
MIC + ADC + DAC + Speaker out				
AVDD+DVDD+TVDD (Note 23)	-	8.2	12.3	mA
AVDD+DVDD+TVDD (Note 24)	-	7.2	-	mA
SVDD (No Load)	-	0.8	1.2	mA
Power-down (PDN pin = "L") (Note 25)				
AVDD+DVDD+TVDD+SVDD	-	0	10	μA
SVDD (Note 26)	-	0	10	μA

Note 21. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMHPL=PMHPR= PMVCM=PMPLL=PMBP=PMMP=M/S bits = "1", and LPMIC = LPDA bits = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 7.3mA (typ), DVDD= 1.6mA (typ), TVDD= 0.3mA (typ).

Note 22. When EXT Slave Mode (PMPLL=M/S bits ="0"), PMADL=PMADR=PMDAC=PMHPL=PMHPR= PMVCM=PMBP=PMMP bits = "1", and PMPFIL = LPMIC = LPDA bits = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 6.5mA (typ), DVDD= 1.6mA (typ), TVDD= 0.1mA (typ).

Note 23. When PLL Master Mode (MCKI=12MHz), and PMADL=PMADR=PMDAC=PMPFIL=PMSL=PMVCM= PMPLL=PMBP=PMMP=M/S bits = "1", and LPMIC = LPDA bits = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 6.5mA (typ), DVDD= 1.4mA (typ), TVDD= 0.3mA (typ).

Note 24. When EXT Slave Mode (PMPLL=M/S bits ="0"), PMADL=PMADR=PMDAC=PMSL=PMVCM= PMBP=PMMP bits = "1", and PMPFIL = LPMIC = LPDA bits = "0". In this case, the MPWR1 (MPWR2) pin outputs 0mA. AVDD= 5.7mA (typ), DVDD= 1.4mA (typ), TVDD= 0.1mA (typ).

Note 25. All digital input pins are fixed to TVDD or VSS2.

Note 26. When AVDD, DVDD, and TVDD are powered OFF.

■ Power Consumption on Each Operation Mode

Conditions: Ta=25°C; AVDD= SVDD=3.3V, TVDD=DVDD=1.8V; VSS1=VSS2=VSS3= 0V; fs=44.1kHz,
LPF, HPF, Stereo Separation, 5-band Equalizer, ALC, DRC=OFF (PMPFIL = PMDRC bits = "0"),
External Slave Mode, BICK=64fs; LIN1/RIN1 input = No input; SDTI input = No input;
Headphone & Speaker & Line output = No load.

Mode	Power Management Bit							AVDD [mA]	DVDD [mA]	TVDD [mA]	SVDD [mA]	Total Power [mW]
	PMVCM	PMSL	PMDAC	PMADL	PMADR	PMHPL	PMHPR					
All Power-down	0	0	0	0	0	0	0	0	0	0	0	0
LIN1/RIN1 → ADC (Note 27)	1	0	0	1	1	0	0	2.70	0.76	0.03	0.01	10.4
LIN1(Mono)→ADC (Note 27)	1	0	0	1	0	0	0	1.54	0.63	0.03	0.01	6.3
DAC → HP (Note 28)	1	0	1	0	0	1	1	1.49	0.69	0.01	0.01	6.2
DAC → SPK (LOSEL bit = "0")	1	1	1	0	0	0	0	1.44	0.67	0.01	0.76	8.5
LIN1/RIN1 → ADC (Note 27) & DAC → HP (Note 28)	1	0	1	1	1	1	1	4.07	1.60	0.03	0.01	16.4
LIN1/RIN1 → ADC (Note 27) & DAC → SPK (LOSEL bit = "0")	1	1	1	1	1	0	0	4.03	1.54	0.03	0.76	18.6

Note 27. Low-power consumption mode (LPMIC bit = "1").
Note 28. Low-power consumption mode (LPDA bit = "1").

Table 1. Power Consumption for Each Operation Mode (typ)

ADC SHARP ROLL-OFF FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V; SDAD bit = "0")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 29)	+0.08dB ~ –0.23dB	PB	0	-	18.8	kHz
	–0.74dB		-	19.4	-	kHz
	–1.41dB		-	19.9	-	kHz
	–8.0dB		-	22.1	-	kHz
Stopband (Note 29)		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	62	-	-	dB
Group Delay (Note 30)		GD	-	10.7	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	3.4	-	Hz
(Note 29)	–0.5dB		-	10	-	Hz
	–0.1dB		-	22	-	Hz

ADC SHARP ROLL-OFF FILTER CHARACTERISTICS (fs=96kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V; SDAD bit = "0")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 29)	+0.08dB ~ –0.23dB	PB	0	-	40.9	kHz
	–0.74dB		-	42.2	-	kHz
	–1.41dB		-	43.3	-	kHz
	–8.0dB		-	48.0	-	kHz
Stopband (Note 29)		SB	56.8	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	62	-	-	dB
Group Delay (Note 30)		GD	-	10.7	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	7.4	-	Hz
(Note 29)	–0.5dB		-	21.8	-	Hz
	–0.1dB		-	47.9	-	Hz

Note 29. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 30. A calculating delay time which induced by digital filtering. This time is from the input of an analog signal to the setting of 32-bit data of both channels to the ADC output register. For the signal through the programmable filters (First HPF + 4-band Equalizer + ALC + Equalizer), the group delay is increased 4/fs from the value above if there is no phase change by the IIR filter.

ADC SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V; SDAD bit = "1")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 33)	+0.08dB ~ –0.23dB	PB	0	-	18.8	kHz
	–0.74dB		-	19.4	-	kHz
	–1.41dB		-	19.9	-	kHz
	–8.0dB		-	22.1	-	kHz
Stopband (Note 33)		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	61	-	-	dB
Group Delay (Note 34)		GD	-	4.3	-	1/fs
Group Delay Distortion		ΔGD	-	-	±1.8	1/fs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	3.4	-	Hz
(Note 31)	–0.5dB		-	10	-	Hz
	–0.1dB		-	22	-	Hz

ADC SHORT DELAY SHARP ROLL-OFF FILTER CHARACTERISTICS (fs=96kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V; SDAD bit = "1")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 33)	+0.08dB ~ –0.23dB	PB	0	-	40.9	kHz
	–0.74dB		-	42.2	-	kHz
	–1.41dB		-	43.3	-	kHz
	–8.0dB		-	48.0	-	kHz
Stopband (Note 31)		SB	56.8	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	61	-	-	dB
Group Delay (Note 32)		GD	-	4.3	-	1/fs
Group Delay Distortion		ΔGD	-	-	±1.3	1/fs
ADC Digital Filter (HPF): HPFC1-0 bits = "00"						
Frequency Response	–3.0dB	FR	-	7.4	-	Hz
(Note 31)	–0.5dB		-	21.8	-	Hz
	–0.1dB		-	47.9	-	Hz

Note 31. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 32. A calculating delay time which induced by digital filtering. This time is from the input of an analog signal to the setting of 32-bit data of both channels to the ADC output register. For the signal through the programmable filters (First HPF + 4-band Equalizer + ALC + Equalizer), the group delay is increased 4/fs from the value above if there is no phase change by the IIR filter.

DAC FILTER CHARACTERISTICS (fs=44.1kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF):						
Passband (Note 33)	±0.05dB −6.0dB	PB	0 -	- 22.05	20.0 -	kHz kHz
Stopband (Note 33)		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 34)		GD	-	22	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 20.0kHz (Note 33)		FR	-	±1.0	-	dB

DAC FILTER CHARACTERISTICS (fs=96kHz)

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	min	typ	max	Unit
DAC Digital Filter (LPF):						
Passband (Note 33)	±0.05dB −6.0dB	PB	0 -	- 48.0	43.5 -	kHz kHz
Stopband (Note 33)		SB	52.5	-	-	kHz
Passband Ripple		PR	-	-	±0.05	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 34)		GD	-	22	-	1/fs
DAC Digital Filter (LPF) + SCF:						
Frequency Response: 0 ~ 40.0kHz (Note 33)		FR	-	±1.0	-	dB

Note 33. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 34. A calculating delay time which induced by digital filtering. This time is from setting the 32-bit data of both channels to input register to the output of analog signal. For the signal through the programmable filters (First HPF + 4-band Equalizer + ALC + Equalizer), the group delay is increased 7/fs from the value above if there is no phase change by the IIR filter.

DC CHARACTERISTICS

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V)

Parameter		Symbol	min	typ	max	Unit
Audio Interface & Serial µP Interface (SDA, SCL, PDN, BICK, LRCK, SDTI, MCKI pins)						
High-Level Input Voltage	(TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
	(TVDD < 2.2V)		80%TVDD	-	-	V
Low-Level Input Voltage	(TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
	(TVDD < 2.2V)		-	-	20%TVDD	V
Audio Interface & Serial µP Interface (SDA, BICK, LRCK, SDTO, OVF pins Output)						
High-Level Output Voltage	(Iout = −80µA)	VOH	TVDD−0.2	-	-	V
Low-Level Output Voltage						
	(Except SDA pin : Iout = 80µA)	VOL1	-	-	0.2	V
	(SDA pin, 2.0V ≤ TVDD ≤ 3.5V: Iout = 3mA)	VOL2	-	-	0.4	V
	(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Input Leakage Current		Iin	-	-	±10	µA
Digital Microphone Interface (DMDAT pin Input ; DMIC bit = "1")						
High-Level Input Voltage		VIH3	65%AVDD	-	-	V
Low-Level Input Voltage		VIL3	-	-	35%AVDD	V
Sink Current	(Vin = AVDD)	Isink	-	-	150	µA
Source Current	(Vin = 0V)	Isource	-20	-	-	µA
Digital Microphone Interface (DMCLK pin Output ; DMIC bit = "1")						
High-Level Output Voltage	(Iout=−80µA)	VOH3	AVDD-0.4	-	-	V
Low-Level Output Voltage	(Iout= 80µA)	VOL3	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta = -30 ~ 85°C; AVDD=2.5 ~ 3.5V, DVDD =1.6 ~ 1.98V, TVDD=(DVDD-0.2) ~ 3.5V, SVDD=0.9 ~ 5.5V; C_L=20pF)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing						
Frequency		fs	8	-	96	kHz
Duty Cycle		Duty	-	50	-	%
BICK Output Timing						
Period	BCKO bit = "0"	tBCK	-	1/(32fs)	-	ns
	BCKO bit = "1"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = BICK pin)						
LRCK Input Timing						
Frequency		fs	8	-	96	kHz
Duty		Duty	45	-	55	%
BICK Input Timing						
Period	PLL2-0 bits = "000"	tBCK	-	1/(32fs)	-	ns
	PLL2-0 bits = "001"	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns

Parameter			Symbol	min	typ	max	Unit
External Slave Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	2.048	-	24.576	MHz
	384fs		fCLK	3.072	-	18.432	MHz
	512fs		fCLK	4.096	-	24.576	MHz
	1024fs		fCLK	8.192	-	12.288	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Input Timing							
Frequency	256fs		fs	8	-	96	kHz
	384fs		fs	8	-	48	kHz
	512fs		fs	8	-	48	kHz
	1024fs		fs	8	-	12	kHz
Duty			Duty	45	-	55	%
BICK Input Timing							
Period			tBCK	156.25	-	-	ns
Pulse Width Low			tBCKL	65	-	-	ns
Pulse Width High			tBCKH	65	-	-	ns
External Master Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	2.048	-	24.576	MHz
	384fs		fCLK	3.072	-	18.432	MHz
	512fs		fCLK	4.096	-	24.576	MHz
	1024fs		fCLK	8.192	-	12.288	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing							
Frequency			fs	8	-	96	kHz
Duty Cycle			Duty	-	50	-	%
BICK Output Timing							
Period		BCKO bit = “0”	tBCK	-	1/(32fs)	-	ns
		BCKO bit = “1”	tBCK	-	1/(64fs)	-	ns
Duty Cycle			dBCK	-	50	-	%

Parameter	Symbol	min	typ	max	Units
Audio Interface Timing					
Master Mode					
BICK "↓" to LRCK Edge (Note 35)	tMBLR	–20	-	20	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	–35	-	35	ns
BICK "↓" to SDTO	tBSD	–35	-	35	ns
SDTI Hold Time	tSDH	25	-	-	ns
SDTI Setup Time	tSDS	20	-	-	ns
Slave Mode					
LRCK Edge to BICK "↑" (Note 35)	tLRB	25	-	-	ns
BICK "↑" to LRCK Edge (Note 35)	tBLR	25	-	-	ns
LRCK Edge to SDTO (MSB) (Except I²S mode)	tLRD	-	-	45	ns
BICK "↓" to SDTO	tBSD	-	-	45	ns
SDTI Hold Time	tSDH	25	-	-	ns
SDTI Setup Time	tSDS	20	-	-	ns
Control Interface Timing (I²C Bus Mode): (Note 36)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 37)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Capacitive Load on Bus	Cb	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 35. BICK rising edge must not occur at the same time as LRCK edge.
Note 36. I²C-bus is a trademark of NXP B.V.
Note 37. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Parameter		Symbol	min	typ	max	Unit
Digital Audio Interface Timing; fs = 8kHz ~ 48kHz, C_L=100pF						
DMCLK Output Timing						
Period		tSCK	-	1/(64fs)	-	ns
Rising Time		tSRise	-	-	10	ns
Falling Time		tSFall	-	-	10	ns
Duty Cycle		dSCK	40	50	60	%
Audio Interface Timing						
DMDAT Setup Time		tSDS	50	-	-	ns
DMDAT Hold Time		tSDH	0	-	-	ns
Power-down & Reset Timing						
PDN Accept Pulse Width	(Note 38)	tAPD	1	-	-	µs
PDN Reject Pulse Width	(Note 38)	tRPD	-	-	50	ns
PMADL or PMADR "↑" to SDTO valid	(Note 39)					
ADRST1-0 bits = "00"		tPDV	-	2115	-	1/fs
ADRST1-0 bits = "01"		tPDV	-	4227	-	1/fs
ADRST1-0 bits = "10"		tPDV	-	267	-	1/fs
ADRST1-0 bits = "11"		tPDV	-	1059	-	1/fs
PMDML or PMDMR "↑" to SDTO valid	(Note 40)					
ADRST1-0 bits = "00"		tPDV	-	2115	-	1/fs
ADRST1-0 bits = "01"		tPDV	-	4227	-	1/fs
ADRST1-0 bits = "10"		tPDV	-	267	-	1/fs
ADRST1-0 bits = "11"		tPDV	-	1059	-	1/fs

Note 38. The AK4954A can be reset by bringing the PDN pin "L" upon power-up. The PDN pin must held "L" for more than 1µs for a certain reset. The AK4954A is not reset by the "L" pulse less than 50ns.
Note 39. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".
Note 40. This is the count of LRCK "↑" from the PMDML or PMDMR bit = "1".

■ Timing Diagram

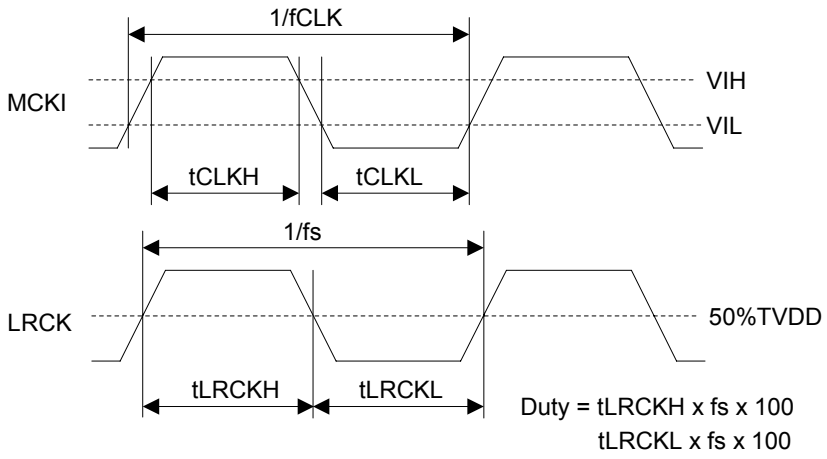


Figure 3. Clock Timing (PLL/EXT Master mode)

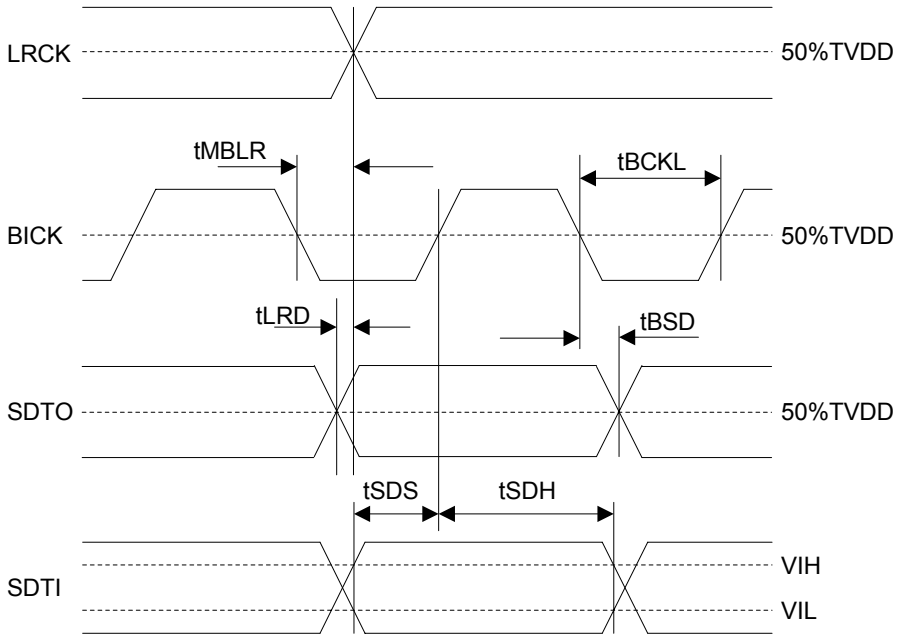


Figure 4. Audio Interface Timing (PLL/EXT Master mode)

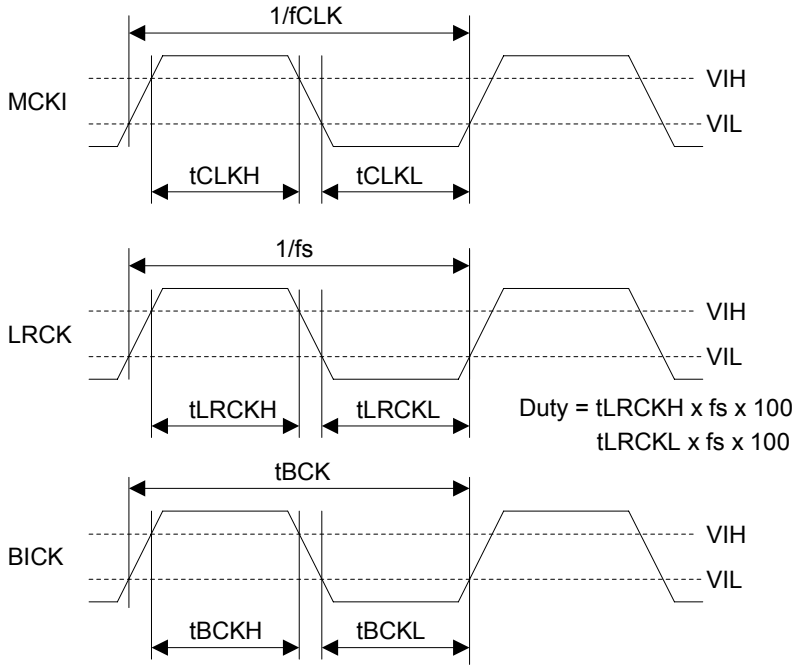


Figure 5. Clock Timing (EXT Slave mode)

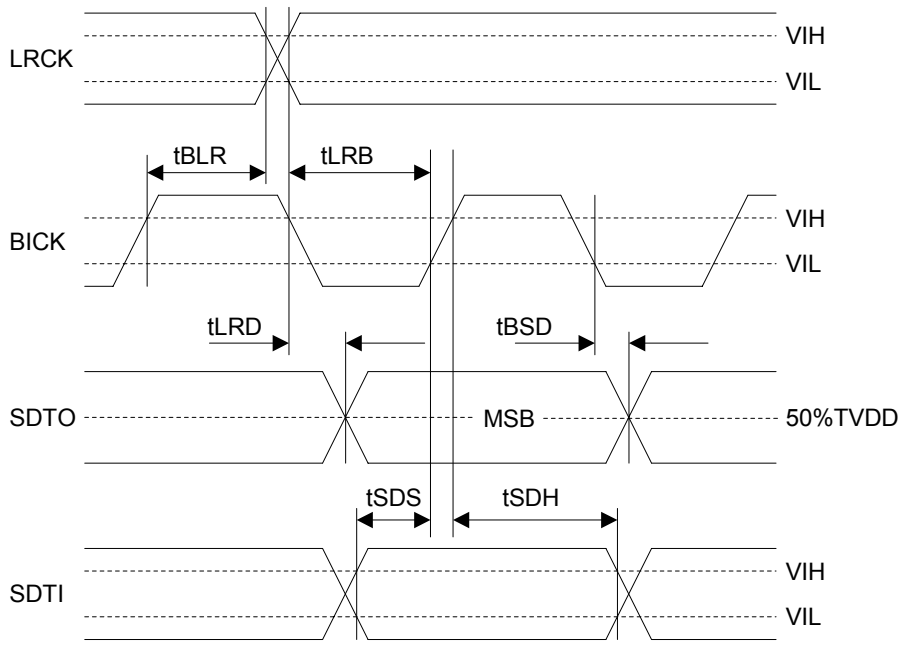


Figure 6. Audio Interface Timing (PLL/EXT Slave mode)

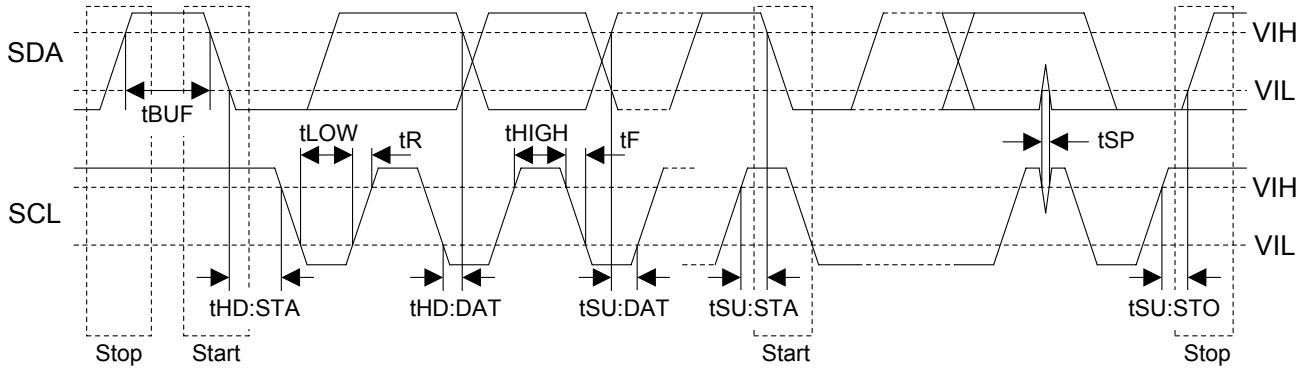
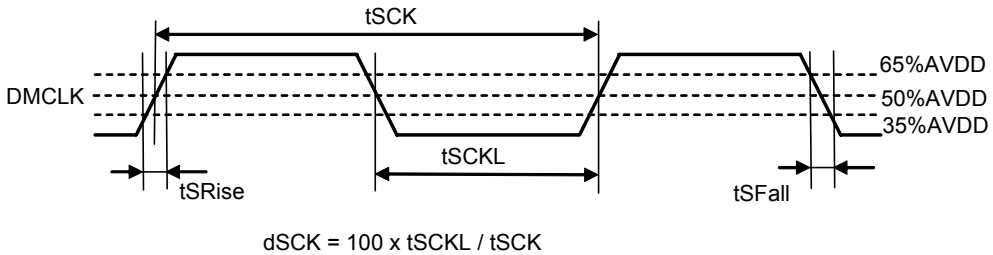


Figure 7. I^2C Bus Mode Timing



dSCK = 100 x tSCKL / tSCK

Figure 8. DMCLK Clock Timing

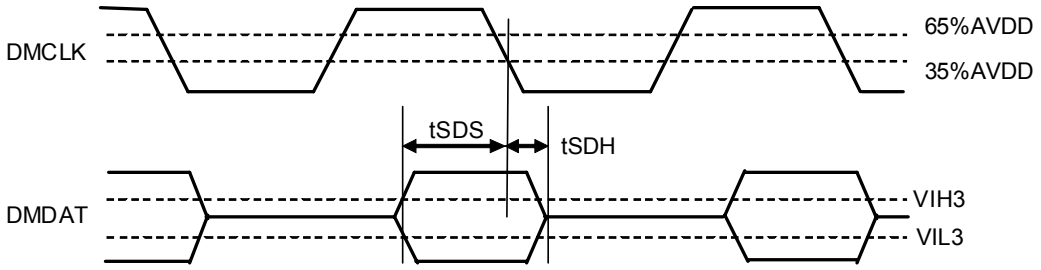


Figure 9. Audio Interface Timing (DCLKP bit = "1")

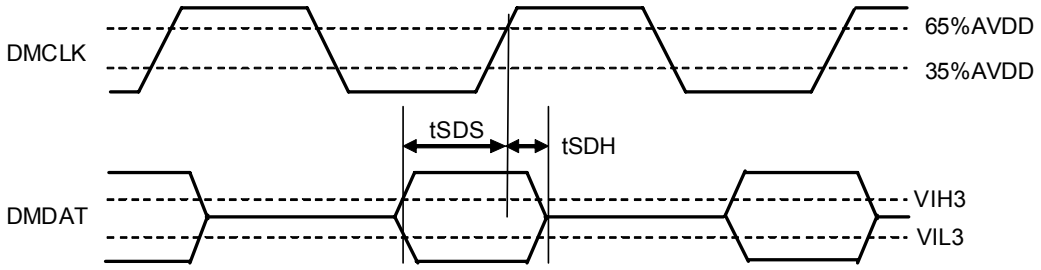


Figure 10. Audio Interface Timing (DCLKP bit = "0")

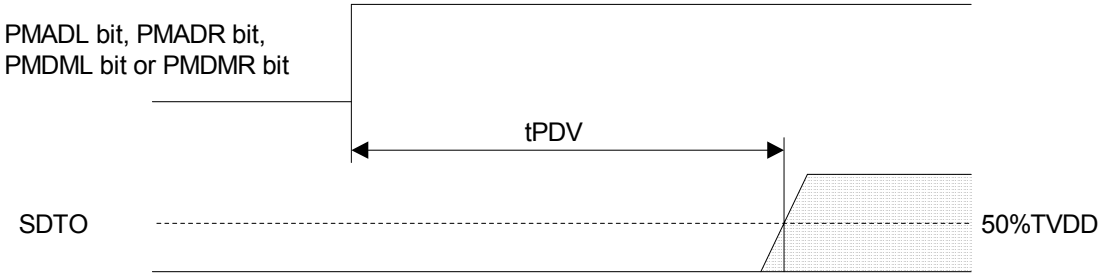


Figure 11. Power-down & Reset Timing 1

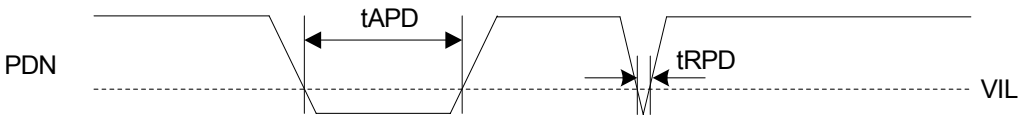


Figure 12. Power-down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following four clock modes to interface with external devices (Table 2, Table 3).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode	1	1	Table 5	Figure 13
PLL Slave Mode (PLL Reference Clock: MCKI pin)	1	0	Table 5	Figure 14
EXT Slave Mode	0	0	x	Figure 15
EXT Master Mode	0	1	x	Figure 16

Table 2. Clock Mode Setting (x: Don't care)

Mode	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	Input Frequency of Table 5 (Selected by PLL2-0 bits)	Output (Selected by BCKO bit)	Output (1fs)
PLL Slave Mode (PLL Reference Clock: BICK pin)	GND	Input (Selected by PLL2-0 bits)	Input (1fs)
EXT Slave Mode	Input Frequency of Table 5 (Selected by CM1-0 bits)	Input (≥ 32fs)	Input (1fs)
EXT Master Mode	Input Frequency of Table 5 (Selected by CM1-0 bits)	Output (Selected by BCKO bit)	Output (1fs)

Table 3. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK4954A is in power-down mode (PDN pin = "L") and when exits reset state, the AK4954A is in slave mode. After exiting reset state, the AK4954A goes to master mode by changing M/S bit = "1".

When the AK4954A is in master mode, the LRCK and BICK pins are a Hi-Z state until M/S bit becomes "1". The LRCK and BICK pins of the AK4954A must be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 4. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by the PLL2-0 and FS3-0 bits. The PLL lock times, when the AK4954A is supplied stable clocks or the sampling frequency is changed after PLL is powered-up (PMPLL bit = "0" → "1"), are shown in Table 5.

1) PLL Mode Setting

Mode	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)	
0	0	0	0	BICK pin	32fs	2ms	
1	0	0	1	BICK pin	64fs	2ms	
2	0	1	0	MCKI pin	11.2896MHz	10ms	(default)
3	0	1	1	MCKI pin	12.288MHz	10ms	
4	1	0	0	MCKI pin	12MHz	10ms	
5	1	0	1	MCKI pin	24MHz	10ms	
6	1	1	0	MCKI pin	13.5MHz	10ms	
7	1	1	1	MCKI pin	27MHz	10ms	

Table 5. PLL Mode Setting (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode

When the PLL reference clock input is the MCKI pin or the BICK pin, the sampling frequency is selected by FS3-0 bits as defined in Table 6.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (Note 41)	
0	0	0	0	0	8kHz mode	
1	0	0	0	1	11.025kHz mode	
2	0	0	1	0	12kHz mode	
4	0	1	0	0	16kHz mode	
5	0	1	0	1	22.05kHz mode	
6	0	1	1	0	24kHz mode	
8	1	0	0	0	32kHz mode	
9	1	0	0	1	44.1kHz mode	(default)
10	1	0	1	0	48kHz mode	
12	1	1	0	0	64kHz mode	
13	1	1	0	1	88.2kHz mode	
14	1	1	1	0	96kHz mode	
Others	Others				N/A	

Table 6. Setting of Sampling Frequency (N/A: Not Available)

Note 41. When the MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL2-0 bits) and sampling frequency (FS3-0 bits). Refer to Table 7 for the details of sampling frequency. In master mode, LRCK and BICK output frequency correspond to sampling frequencies shown in Table 7. When the BICK pin is the PLL reference clock input, the sampling frequency generated by PLL is the same sampling frequency of mode name.