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AK5373

24-bit Stereo ADC with USB Interface

GENERAL DESCRIPTION

The AK5373 is a stereo A/D converter with a USB 2.0 interface. The device includes an integrated USB serial interface engine, a USB transceiver, an audio class processing block, endpoints, and a 24-bit stereo audio ADC. An integrated PLL enables the use of multiple sampling frequencies. A microphone amplifier and an integrated programmable gain amplifier are available for processing low-level signals from an analog microphone element. An external EEP-ROM is used to store the descriptor information. The AK5373 is housed in a 48-pin package. It is a low power device, operating from +3.3V, and consuming just 100mW in active mode and less than 100μA in suspend mode.

FEATURES

- **USB 2.0 compliant (full speed audio class)**
- **USB audio controller**
  - **USB serial interface engine**
  - **Audio class encoder/decoder**
- **USB synchronization**
  - **Synchronous type (synchronize with 1ms SOF)**
- **24-bit stereo A/D converter with mute control**
  - **S/(N+D) = 85dB, S/N = 91dB (AVDD=3.3V, MIC-Amp = 0dB)**
  - **S/(N+D) = 70dB, S/N = 78dB (AVDD=3.3V, MIC-Amp = +30dB)**
- **Microphone amplifier gain:**
  - **0dB, +6dB, +12dB, +18dB, +24dB, +30dB, +36dB**
- **Digital programmable gain: +24dB ~ -31dB, 1dB Step**
- **Integrated PLL supports standard sampling frequencies**
  - **8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz 44.1kHz, 48kHz**
- **EEP-ROM interface for descriptors**
- **External Digital Audio Interface**
- **Power Management**
- **Low power consumption**
  - **30mA in active mode**
  - **Less than 100μA in suspend mode**
- **Power Supply:**
  - **Analog Power Supply (AVDD): 3.0 ~ 3.6V**
  - **Digital Power Supply (DVDD): 3.0 ~ 3.6V**
- **Ta = -10 ~ +70°C**
- **Package:**
  - **48pin LQFP (7 x 7 mm, 0.5mm pitch)**

■ Block Diagram

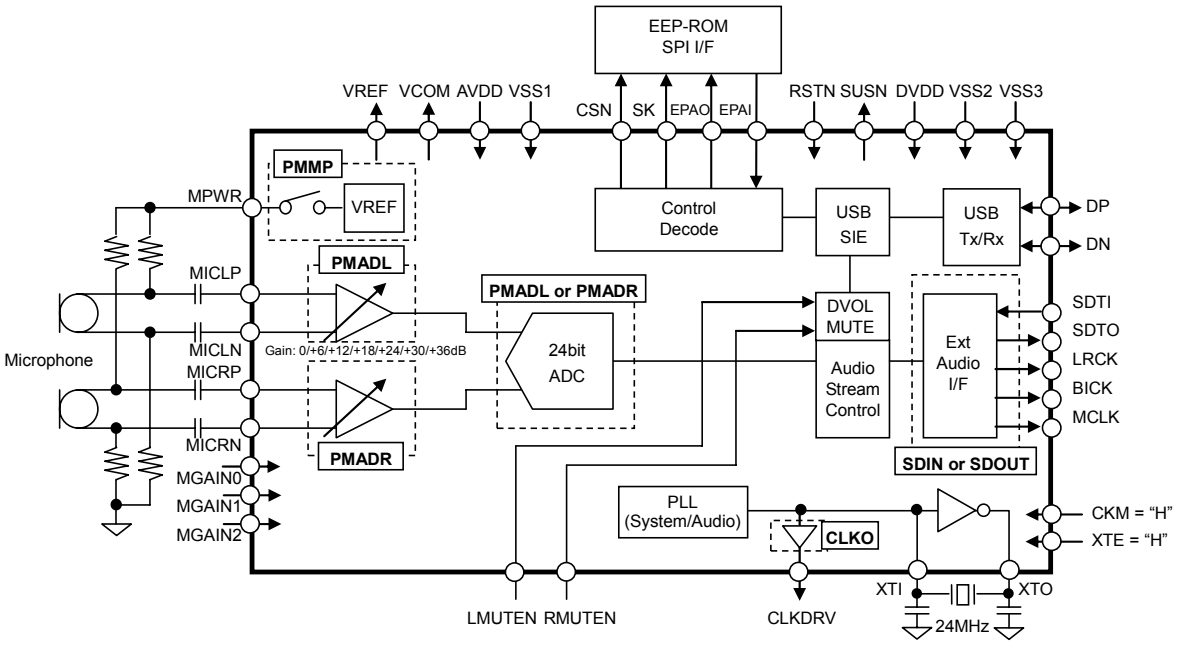
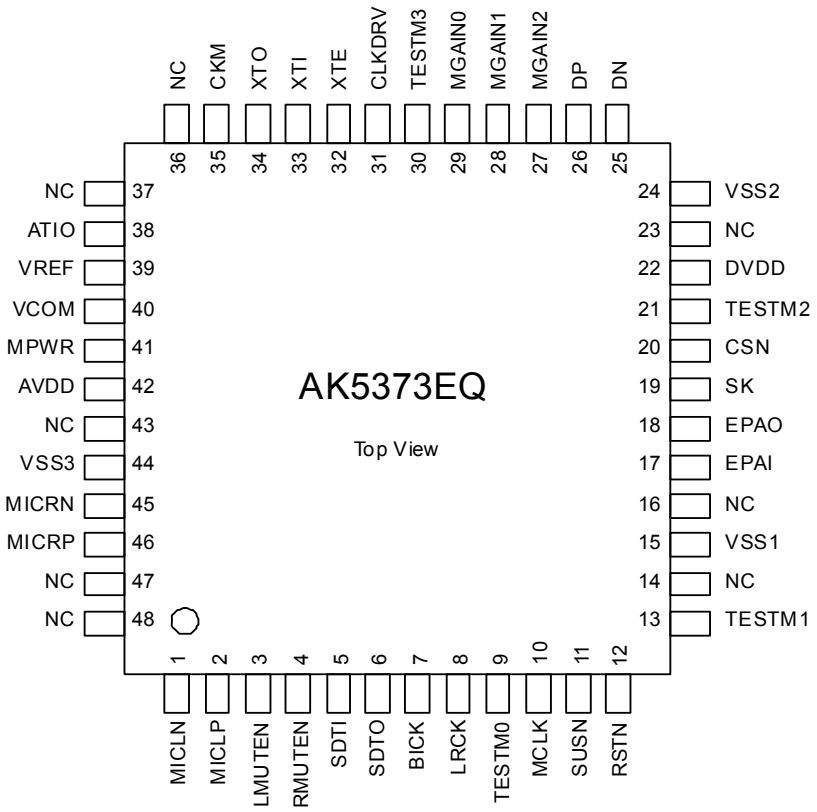


Figure 1. Block Diagram

■ Ordering Guide

AK5373EQ	−10 ~ +70°C	48pin LQFP (0.5mm pitch)
AKD5373	Evaluation board for AK5373	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function	Reset State (RSTN pin = "L")
1	MICLN	I	Left Channel Inverting Input Pin	←
2	MICLP	I	Left Channel Positive Input Pin	←
3	LMUTEN	I	Left Channel Mute Pin "L": Mute "H": Normal Operation	←
4	RMUTEN	I	Right Channel Mute Pin "L": Mute "H": Normal Operation	←
5	SDTI	I	External Audio Serial Data Input Pin	←
6	SDTO	O	External Audio Serial Data Output Pin	"L" output
7	BICK	O	External Audio Serial Clock Output Pin	"L" output
8	LRCK	O	External Audio Channel Clock Output Pin	"L" output
9	TESTM0	I	Test #0 Pin This pin must be connected to VSS1-3.	←
10	MCLK	O	External Audio Master Clock Output Pin	"L" output
11	SUSN	O	Suspend Status Output Pin "L": Suspend State "H": Normal Operation	"L" output
12	RSTN	I	Reset Pin When "L", the AK5373 is held in reset. The AK5373 must be always reset upon power-up.	←
13	TESTM1	I	Test #1 Pin This pin must be connected to VSS1-3.	←
14	NC	-	No Connect Pin No internal bonding. Normally connected to VSS1-3.	←
15	VSS1	-	Ground Pin	←
16	NC	-	No Connect Pin No internal bonding. Normally connected to VSS1-3.	←
17	EPAI	I	EEP-ROM Serial Data Input Pin	←
18	EPAO	O	EEP-ROM Serial Data Output Pin	"Hi-Z"
19	SK	O	EEP-ROM Serial Clock Output Pin	"Hi-Z"
20	CSN	O	EEP-ROM Chip Select Output Pin	"Hi-Z"
21	TESTM2	I	Test #2 Pin This pin must be connected to VSS2.	←
22	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V	←
23	NC	-	No Connect Pin No internal bonding. Normally connected to VSS1-3.	←
24	VSS2	-	Ground Pin	←
25	DN	I/O	USB Bus Inverting Pin	Input
26	DP	I/O	USB Bus Positive Pin This pin must be connected to DVDD with 1.5kΩ resistor.	Input
27	MGAIN2	I	MIC Gain Control 2 Pin	←
28	MGAIN1	I	MIC Gain Control 1 Pin	←
29	MGAIN0	I	MIC Gain Control 0 Pin	←
30	TESTM3	I	Test #3 Pin This pin must be connected to VSS1-3.	←
31	CLKDRV	O	Clock Drive Output Pin	"L" output
32	XTE	I	Crystal Oscillator Enable Pin "L": Master Clock Input Mode "H": Crystal Oscillator Mode	←

No.	Pin Name	I/O	Function	Reset State (RSTN pin = "L")
33	MCKI	I	Master Clock Input Pin (XTE pin = "L")	←
	XTI	I	Crystal Oscillator Input Pin (XTE pin = "H")	←
34	XTO	O	Crystal Oscillator Output Pin	"L" output
35	CKM	I	Crystal Mode Select Pin "L": 16MHz "H": 24MHz	←
36	NC	-	No Connect Pin No internal bonding. Normally connected to VSS1-3.	←
37	NC	-	No Connect Pin No internal bonding. Normally connected to VSS1-3.	←
38	ATIO	I/O	Test Pin This pin must be connected to VSS1-3.	"Input"
39	VREF	O	High Level Voltage Reference Output Pin	"L" output
40	VCOM	O	Analog Common Voltage Output Pin	"L" output
41	MPWR	O	Microphone Power Supply Pin	"Hi-Z"
42	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V	←
43	NC	-	No Connect Pin No internal bonding. Normally connected to VSS1-3.	←
44	VSS3	-	Ground Pin	←
45	MICRN	I	Right Channel Inverting Input Pin	←
46	MICRP	I	Right Channel Positive Input Pin	←
47	NC	-	No Connect Pin No internal bonding. Normally connected to VSS1-3.	←
48	NC	-	No Connect Pin No internal bonding. Normally connected to VSS1-3.	←

Note 1. All digital input pins (EPAI, SDTI, MGAIN0/1/2, CKM, LMUTEN, RMUTEN, XTE and TESTM0/1/2/3 pins) must not be left floating.

■ Handling of Unused Pin

The unused I/O pin must be processed appropriately as below.

Classification	Pin Name	Setting
Analog Input	MICLP, MICLN	MICLP pin is connected to MICLN pin.
	MICRP, MICRN	MICRP pin is connected to MICRN pin.
	ATIO	This pin must be connected to VSS1-3.
Analog Output	MPWR	This pin must be open.
Digital Input	SDTI, MGAIN1/2/3, CKM, XTE, TESTM0/1/2/3	These pins must be connected to VSS1-3.
	LMUTEN, RMUTEN	These pins must be connected to DVDD.
Digital Output	SUSN, MCLK, LRCK, BICK, SDTO, CLKDRV	These pins must be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=0V; Note 2)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	-0.3	4.6	V
	Digital	DVDD	-0.3	4.6	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage (Note 4)		VIND	-0.3	DVDD+0.3	V
Ambient Temperature (power applied)		Ta	-10	70	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground.
Note 3. MICLP, MICLN, MICRP and MICRN pins.
Note 4. MGAIN0/1/2, CKM, LMUTEN, RMUTEN, SDTI, EPAI, XTE and TESTM0/1/2/3 pins.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 5)	Analog	AVDD	3.0	3.3	3.6	V
	Digital	DVDD	3.0	3.3	3.6	V
	Difference	AVDD-DVDD	-0.3	0	+0.3	V

Note 2. All voltages with respect to ground.
Note 5: The power up sequence among AVDD and DVDD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.3V; VSS1=VSS2=VSS3=0V; Signal Frequency = 1kHz; Sampling Frequency = 48kHz; BW = 20Hz to 20kHz, unless otherwise specified)

Parameter			min	typ	max	Units
Microphone Amplifier: MICLP/MICLN/MICRP/MICRN pins						
Input Resistance			10	20	-	kΩ
Gain	MGAIN2-0 bits = "001"		-1	0	+1	dB
	MGAIN2-0 bits = "010"		+5	+6	+7	dB
	MGAIN2-0 bits = "011"		+11	+12	+13	dB
	MGAIN2-0 bits = "100"		+17	+18	+19	dB
	MGAIN2-0 bits = "101"		+23	+24	+25	dB
	MGAIN2-0 bits = "110"		+29	+30	+31	dB
	MGAIN2-0 bits = "111"		+35	+36	+37	dB
Microphone Power Supply: MPWR pin						
Output Voltage			1.9	2.2	2.5	V
Output Current			-	-	2.0	mA
ADC Analog Input Characteristics: MICLP/MICLN/MICRP/MICRN pins						
Resolution			-	-	24	Bits
Input Voltage		(Note 6)	±1.00	±1.20	±1.40	Vpp
		(Note 7)	-	±0.038	-	Vpp
S/(N+D) (-1dBFS)		(Note 6)	75	85	-	dB
		(Note 7)	-	70	-	dB
Dynamic Range (–60dBFS, A-weighted)		(Note 6)	81	91	-	dB
		(Note 7)	-	78	-	dB
S/N (A-weighted)		(Note 6)	81	91	-	dB
		(Note 7)	-	78	-	dB
Power Supplies:						
Power Supply Current						
	Normal operation (internal ADC mode)					
	AVDD		-	10	15	mA
	DVDD		-	20	30	mA
	Power down					
	RSTN pin = "L" (Note 8)		-	10	100	μA
	Suspend mode		-	10	100	μA

Note 6. MGAIN2-0 bits = "001" (0dB)
Note 7. MGAIN2-0 bits = "110" (+30dB)
Note 8. All digital input pins are fixed to DVDD or VSS2.

FILTER CHARACTERISTICS

(Ta=-10 ~ +70°C; AVDD=DVDD=3.0 ~ 3.6V; fs=48kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter						
Passband (Note 9)	-0.07 ~ +0.15dB	PB	0	-	18.9	kHz
	-0.2dB		-	20.3	-	kHz
	-3.0dB		-	22.9	-	kHz
	-6.0dB		-	23.9	-	kHz
Stopband		SB	28.0	-	-	kHz
Passband Ripple		PR	-0.07	-	+0.15	dB
Stopband Attenuation		SA	-	68.0	-	dB
Group Delay		GD	-	14	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF):						
Frequency Response (Note 9)	-3.0dB	FR	-	0.93	-	Hz
	-0.1dB		-	6.1	-	Hz

Note 9. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz

DC CHARACTERISTICS

(Ta=-10~+70°C; AVDD=DVDD=3.0 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	(Note 11)	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	(Note 11)	VIL	-	-	30%DVDD	V
High-Level Output Voltage	(Note 12, Iout=−200μA)	VOH	DVDD−0.2	-	-	V
Low-Level Output Voltage	(Note 12, Iout=200μA)	VOL	-	-	0.2	V
Input Leakage Current	(Note 13)	Iin	-	-	±10	μA

Note 10. All digital pins except for DP, DN pins. Schmitt hysteresis level of RSTN pin and levels of all test pins are not tested.

Note 11. EPAI, SDTI, MGAIN1/2/3, CKM, LMUTEN, RMUTEN, RSTN, XTE and TESTM0/1/2/3 pins.

Note 12. CSN, SK, EPAO, SUSN, MCLK, LRCK, BICK, SDTO and CLKDRV pins.

Note 13. Expect for EPAI pin. EPAI pin has internal pull-down device, nominally 100kΩ.

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.3V; CL=50pF)

Parameter		Symbol	min	typ	max	Units
Master Clock Frequency						
Crystal Resonator	CKM pin = "L"	fXTAL1	-	16	-	MHz
	CKM pin = "H"	fXTAL2	-	24	-	MHz
USB Interface						
DP, DN Single Ended Receiver Threshold (High-Level)		VseH	2.0	-	-	V
DP, DN Single Ended Receiver Threshold (Low-Level)		VseL	-	-	0.8	V
Time Width for USB Reset Signal Recognition (DP<VseL & DN< VseL to USB Reset mode)		Trst_rec	2.7	-	-	µs
Device Ready Time from USB Reset (Ready for transaction after reset)		Tdrr	-	-	10	ms
Time Width for Suspend Recognition (Idle state DP > VseL & DN < VseL to Suspend mode)		Tsus_rec	3.0	-	-	ms
Resume Time from Suspend (Note 14) (First flip of DP/DN from Idle sate to Device Ready)		Tresm	-	-	30	ms
USB Transmitter						
Data Rate		DR	11.97	12	12.03	MHz
Output Impedance (Hi) (Note 15) (DP, DN pins = "H", Iout = -10mA)		Roh	-	36	-	Ω
Output Impedance (Lo) (Note 15) (DP, DN pins = "L", Iout = 10mA)		Rol	-	36	-	Ω
"H" level Output Voltage (Iout = -200µA)		Vohd	2.8	-	-	V
"L" level Output Voltage (Iout = 2.2mA)		Vold	-	-	0.3	V
Tri-state Leakage Current (0 < DP, DN < 3.3V)		Iolk	-10	-	10	µA
Rise/Fall Time		Trf/Tff	4	12	20	ns
Rise/Fall Time Matching		Trfm	-	100	-	%
Crossover Point		Vcrs	-	1.65	-	V
USB Receiver						
Common Mode Range		CMR	0.8	-	2.5	V
Differential Input Sensitivity		DIS	200	-	-	mV
Schmitt High Level Voltage		Vihs	2.0	-	-	V
Schmitt Low Level Voltage		Vils	-	-	0.8	V

Note 14. VREF, X'tal oscillator, and PLL get stable and bus transaction with normal rate is ready.
Note 15. Including an external 18Ω (±1%) resistor in series.

Parameter	Symbol	min	typ	max	Units
External Audio Mode					
MCLK Output Timing					
Frequency	fMCK	2.048	-	24.576	MHz
Duty Cycle	dMCK	40	50	60	%
LRCK Output Timing					
Frequency	fs	8	-	48	kHz
Duty Cycle	Duty	-	50	-	%
BICK Output Timing					
Period	tBCK	-	1/(64fs)	-	ns
Duty Cycle	dBCK	-	50	-	%
Audio Interface Timing					
BICK "↓" to LRCK Edge (Note 16)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)	tLRD	–70	-	70	ns
BICK "↓" to SDTO	tBSD	–70	-	70	ns
SDTI Hold Time	tSDH	50	-	-	ns
SDTI Setup Time	tSDS	50	-	-	ns
SPI (EEP-ROM) Control Interface Timing					
SK Frequency	fSK	-	1.5	-	MHz
SK Duty Cycle	dSK	-	50	-	%
EPAI Delay	tCD	-	-	100	ns
CSN Edge to SK "↑"	tCSS	300	-	-	ns
SK "↓" to CSN Edge	tCSH	300	-	-	ns
CSN "H" Time	tCSW	300	-	-	ns
EPAI Setup Time	tCDS	100	-	-	ns
EPAI Hold Time	tCDH	100	-	-	ns
One Shot Mute Timing					
One Shot Mute Input Width	Wosm	10	-	-	µs
Reset Timing					
Reset Input Width (Note 17)	Wrst	1.0	-	-	µs

Note 16. BICK rising edge must not occur at the same time as LRCK edge.
Note 17. The AK5373 can be reset by the RSTN pin = "L".

■ Timing Diagrams

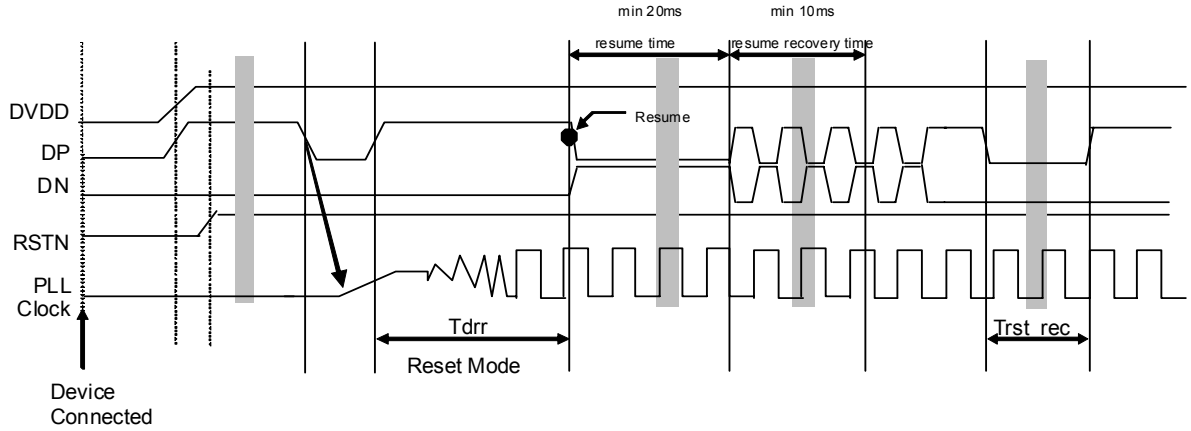


Figure 2. Mode change with respect to BUS States 1 (Power on and device connected)

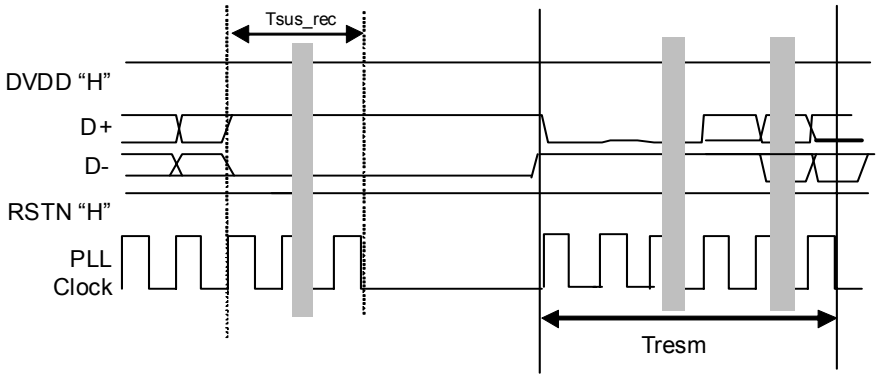


Figure 3. Mode Change with respect to Bus States 2 (Bus transactions)

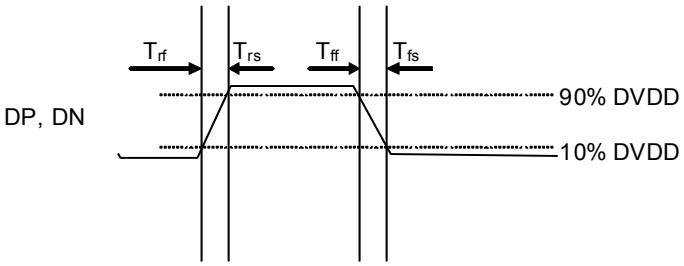


Figure 4. Rise/Fall Time

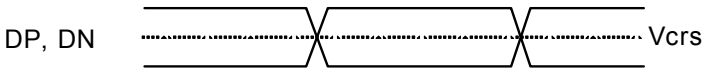


Figure 5. Crossover Point

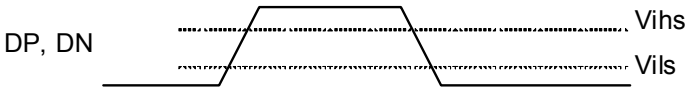


Figure 6. Schmitt Level Voltage

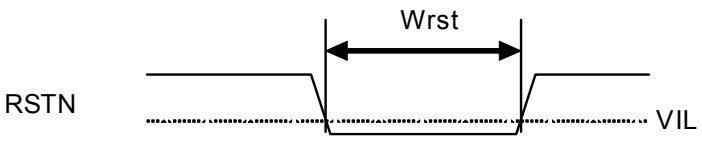


Figure 7. Power-down & Reset Timing

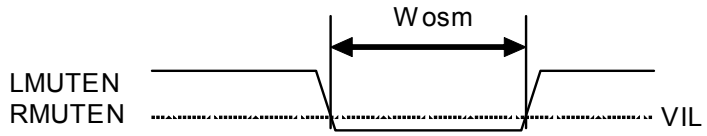


Figure 8. One Shot Mute Timing

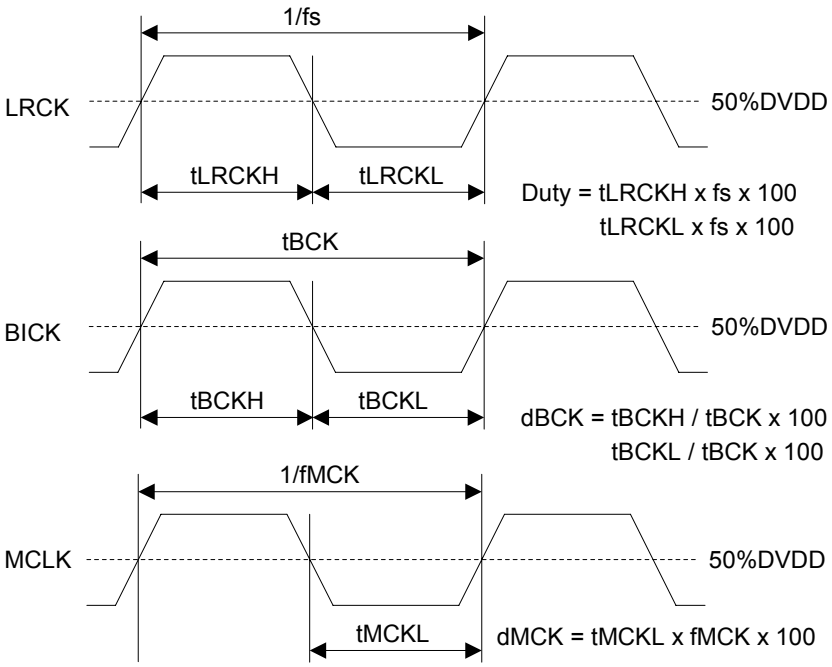


Figure 9. Audio Clock Timing

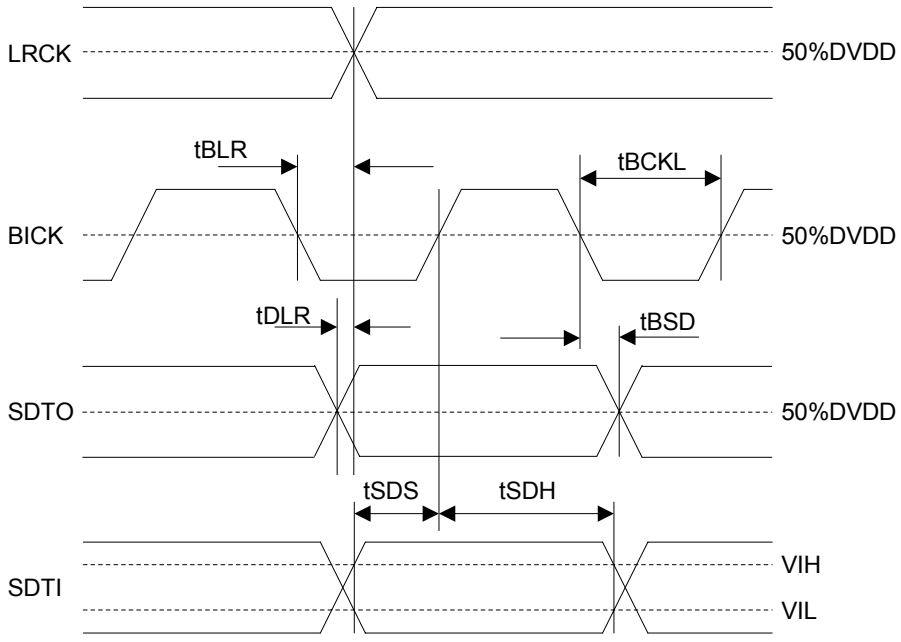


Figure 10. Audio Interface Timing

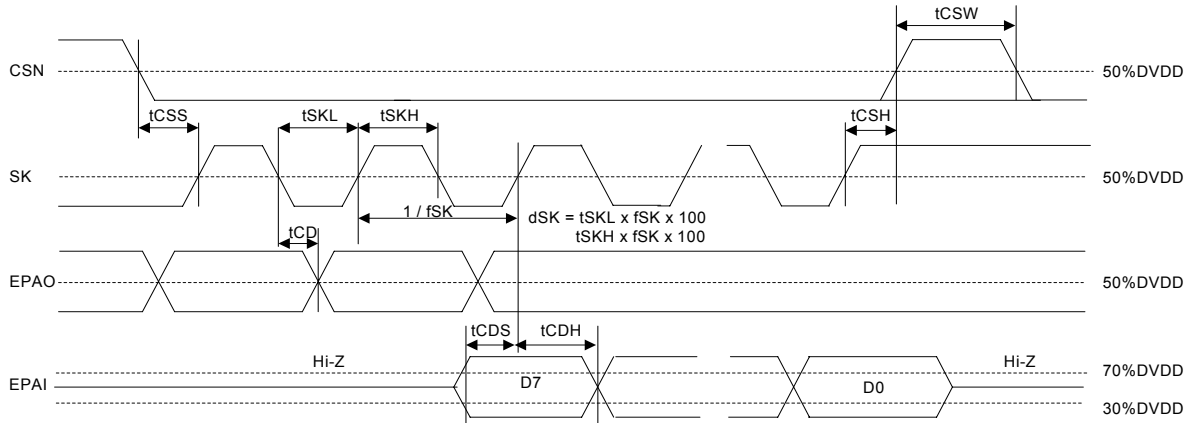


Figure 11. SPI (EEP-ROM) Control Interface Timing

OPERATION OVERVIEW

■ Overview of AK5373

The AK5373 is a stereo A/D converter with USB interface. It is easy to use since the control logic including USB audio class, stereo differential microphone amplifiers, two PLL's USB serial interface engine, and FIFO are integrated. All Descriptor contents are stored in EEP-ROM and customizable. For example, when supporting a mono microphone by 48kHz sampling rate only, what needed to be done is to prepare appropriate USB descriptor. There is no need for writing program codes.

The AK5373 also has an external audio steaming interface to connect other A/D converters or audio DSP's. When a high performance A/D converters is connected, A/D data generated by this A/D converter are transmitted via USB upstream. When an external audio DSP is connected, the output of AK5373 is processed by this DSP. The AK5373 receives this data again and transmits. I/F format is stored in the EEP-ROM header.

The AK5373 integrates the following blocks:

1. 24bit High Performance Stereo A/D Converter
   a) S/N: 91dB (MIC Gain=0dB), S/N: 78dB (MIC Gain=+30dB)
2. MIC Power Supply
   a) Output Voltage: 2.2V (typ)
3. Differential Microphone Amplifier
   a) Setting of Gain: 0dB, +6dB, +12dB, +18dB, +24dB, +30dB, +36dB
4. Digital Programmable Gain
   a) Gain Range: from +24dB to -31dB (Setting of gain: Max, Min and Initial value)
   b) Gain Step: 1dB/step (Fix)
5. PLL
   a) 16.0MHz or 24.0MHz crystal generator with output buffer (Available for External Clock input)
   b) Two PLLs
      - A/D_PLL: generate audio clock
      - System_PLL: generate USB system clock
6. Audio Synchronization Type
   a) Synchronous Type
      - Isochronous transfer uses Synchronous type synchronization which is synchronous to SOF (start of frame) packets which are issued per 1ms.
7. USB Audio Format
   a) Supports 7 Frequencies: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz, 48kHz
   b) Stereo/Mono 24bit/16bit/8bit LSB first
8. FIFO
   a) Synchronization between A/D converter and USB bus
      - Memory Size 576 bytes: 24bit (3 bytes) x 48 samples x 2 channel x 2 frames
9. USB Serial Interface Engine
   a) Process USB Standard Requests
10. Control block of Audio Device Class
    a) Translate internal A/D format to USB audio class format
    b) Process USB Audio Class Request
       - Mute
       - Gain/Attenuation
       - Sampling Frequency Control
11. USB transceiver
12. EEP-ROM I/F
    SPI™ (4-wire) type EEP-ROM can be used to customize all USB descriptors and any functions.
       - 8K bits (AK6506C) or larger
13. USB Suspend/Resume Support
14. External Digital Audio Interface
    a) 24bit I^2S or MSB justified
    b) MCLK=256fs or 512fs, BICK=64fs
15. Stand-alone Mute
    a) Zero Crossing detection mute or One Shot mute (not support HID function)

■ Clock Source

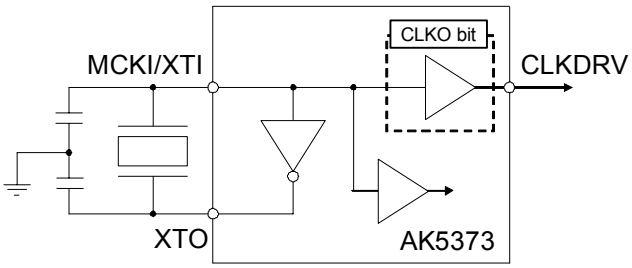
16MHz or 24 MHz crystal resonator can be used as the master clock. If the CKM pin is set to "H", the AK5373 supports 24MHz. If the CKM pin is set to "L", the AK5373 supports 16MHz. The AK5373 can drive the clock up to three external loads. The AK5373 generates 48MHz for system clock from 16MHz or 24MHz by system PLL circuit.

CKM pin	X'tal Frequency
L	16.0MHz
H	24.0MHz

Table 1. Reference X'tal frequency

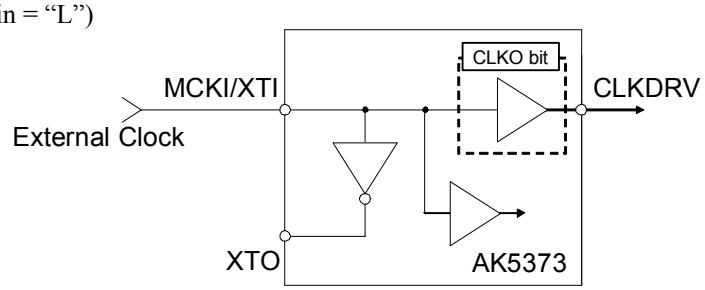
The clock for the MCKI/XTI pin can be generated by the following methods:

1) X'tal (XTE pin = "H")



Note 18. External capacitance depends on the crystal oscillator (Max. 30pF)
Figure 12. X'tal Mode

2) External clock (XTE pin = "L")



Note 19. Input clock must not exceed DVDD.
Figure 13. External clock mode

■ MIC Gain Amplifier

The AK5373 has a gain amplifier for microphone inputs. The gain of MIC-Amp is selected by the MGAIN2-0 pins or MGAIN2-0 bits (Table 2).

MGAIN2 pin	MGAIN1 pin	MGAIN0 pin	MGAIN2 bit	MGAIN1 bit	MGAIN0 bit	Input Gain
L	L	L	0	0	0	0dB
			0	0	1	0dB
			0	1	0	+6dB
			0	1	1	+12dB
			1	0	0	+18dB
			1	0	1	+24dB
			1	1	0	+30dB
			1	1	1	+36dB
L	L	H	x	x	x	0dB
L	H	L				+6dB
L	H	H				+12dB
H	L	L				+18dB
H	L	H				+24dB
H	H	L				+30dB
H	H	H				+36dB

Table 2. Mic Input Gain (x: Don't care)

■ MIC Power

When PMMP bit = "1", the MPWR pin supplies power for the microphone. This output voltage is typically 2.2V and the output current is maximum 2.0mA. In case of using two sets of stereo full-differential microphones, the load resistance is minimum 1kΩ for each channel. Any capacitor must not be connected directly to the MPWR pin (Figure 14).

PMMP bit	MPWR pin
0	Hi-Z
1	Output

Table 3. MIC Power

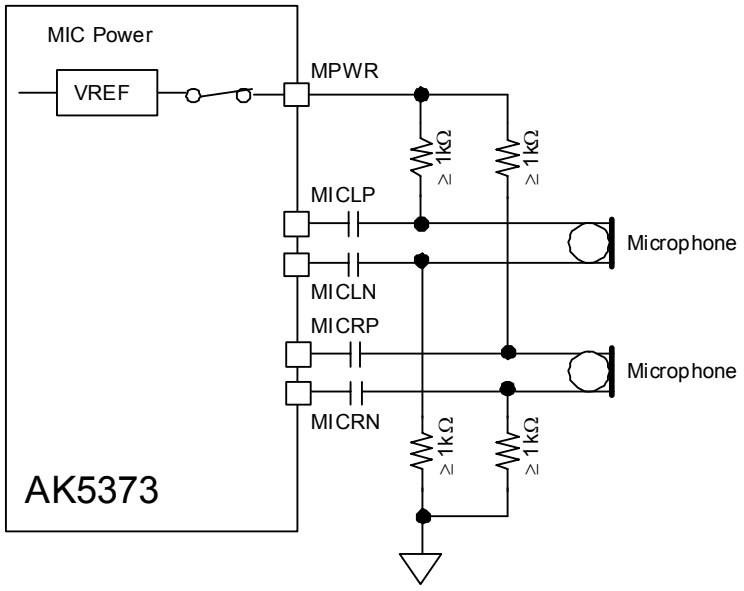


Figure 14. MIC Block Circuit

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 0.93Hz at fs=48kHz. The digital high pass filter cut-off frequency scales with the sampling rate (fs). The HPF is always enabled.

■ Audio Data Format

The AK5373 supports 8bit, 16bit and 24bit audio data format and outputs LSB first to USB bus.

1) 8bit mono data format on the USB

Sample #	#1	#2	#3	···
	mono	mono	mono	···
	8 bit	8bit	8 bit	···
bit position	0-7	0-7	0-7	···

Table 4. Audio Data Format for 8bit mono

2) 16bit stereo data format on the USB

Sample #	#1				#2				···
	L-ch data		R-ch data		L-ch data		R-ch data		···
	Lower 8 bit	Upper 8 bit	Lower 8 bit	Upper 8 bit	Lower 8 bit	Upper 8 bit	Lower 8bit	Upper 8 bit	...
bit position	0-7	8-15	0-7	8-15	0-7	8-15	0-7	8-15	···

Table 5. Audio Data Format for 16bit stereo

3) 24bit stereo data format on the USB

Sample #	#1						#2						···
	L-ch data			R-ch data			L-ch data			R-ch data			···
	Lower 8 bit	Middle 8 bit	Upper 8 bit	Lower 8 bit	Middle 8 bit	Upper 8 bit	Lower 8 bit	Middle 8 bit	Upper 8 bit	Lower 8 bit	Middle 8 bit	Upper 8 bit	···
bit position	0-7	8-15	16-23	0-7	8-15	16-23	0-7	8-15	16-23	0-7	8-15	16-23	···

Table 6. Audio Data Format for 24bit stereo

■ External Digital Audio Interface

The AK5373 has optional audio streaming interface to output A/D data, or to receive DSP data and to transmit them to the host. Because the AK5373 operates as a master device only, MCLK, LRCK, and BICK are output. The AK5373 supports two audio formats, I2S and MSB justified format. The data length of ADC outputs is 24bit only despite the USB audio formats which can be selected from 8/16/24 bit. This interface is specified in the header of EEP-ROM.

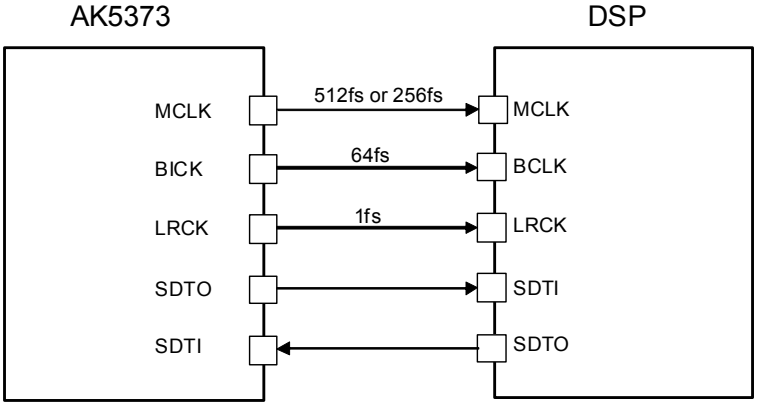


Figure 15. External Digital Audio Interface

512FS bit	MCLK pin
0	256fs
1	512fs

Table 7. MCLK Output Frequency

I2S bit	SDTO	SDTI
0	MSB justified	MSB justified
1	I^2S Compatible	I^2S Compatible

Table 8. Audio Interface Format

■ Volume & Mute Control

The AK5373 has a digital volume control which ranges from +24dB to -31dB in 1dB step. The maximum volume, the minimum and default volumes are defined by EEP-ROM header setting.

When ZCE bit = "1" (Zero cross detection enable), L-channel and R-channel volumes are changed independently on zero cross or zero cross timeout. Zero cross timeout is set by ZTM1-0 bits (Table 9). When ZCE bit = "0" (zero cross detection disable), the volume is changed immediately. Mute operation and zero cross detection have the same relation as the volume mentioned in this section.

ZTM1 bit	ZTM0 bit		Zero Crossing Timeout Period		
			8kHz	16kHz	44.1kHz
0	0	128/fs	16ms	8ms	2.9ms
0	1	256/fs	32ms	16ms	5.8ms
1	0	512/fs	64ms	32ms	11.6ms
1	1	1024/fs	128ms	64ms	23.2ms

Table 9. Zero Crossing Timeout Period

The AK3573 has the LMUTEN and RMUTEN pins, and it can control mute operation from the device side. However, because the AK5373 does not have HID function, the mute operation by these pins cannot be acknowledged by the host. There are two modes for the mute operation by LMUTEN and RMUTEN pins; one is normal mute and the other is one-shot mute.

In normal mute operation (OSME bit = "0"), mute is executed on zero cross or zero cross timeout when the LMUTEN and RMUTEN pins = "L" if zero cross detection is enabled. When zero cross detection is disabled, it is executed immediately. In case that the LMUTEN and RMUTEN pins = "H", mute is released on zero cross or zero cross timeout if the zero cross detection is enabled. When zero cross detection is disabled, it is released immediately.

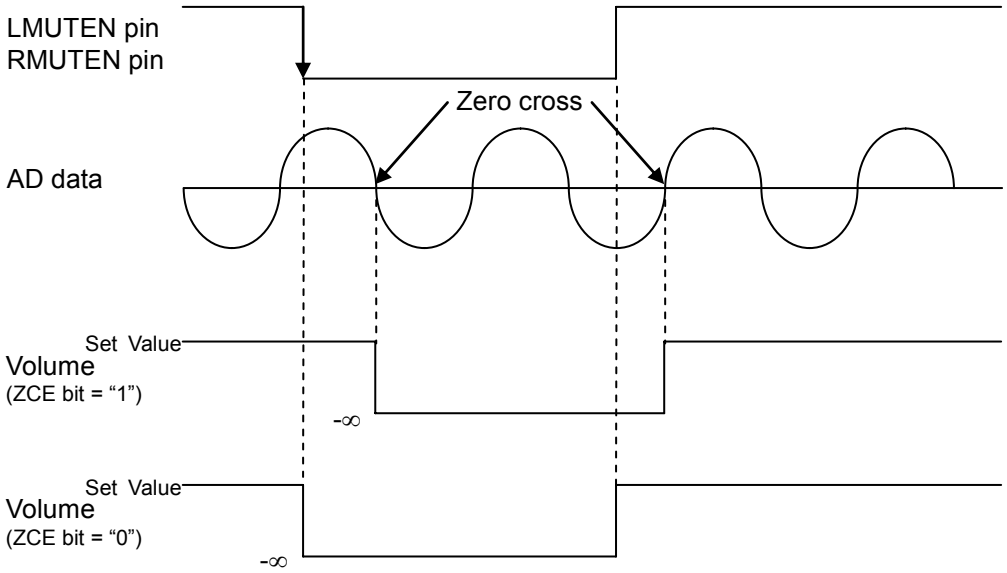


Figure 16. Normal Mute for LMUTEN, RMUTEN pins

In one-shot mute operation (OSME bit = "1"), mute is executed on zero cross or zero cross timeout after detecting a falling edge of the LMUTEN and RMUTEN pins. The AK5373 releases the mute on zero cross or zero cross timeout after mute hold period which is set by MHLD7-0 bits.

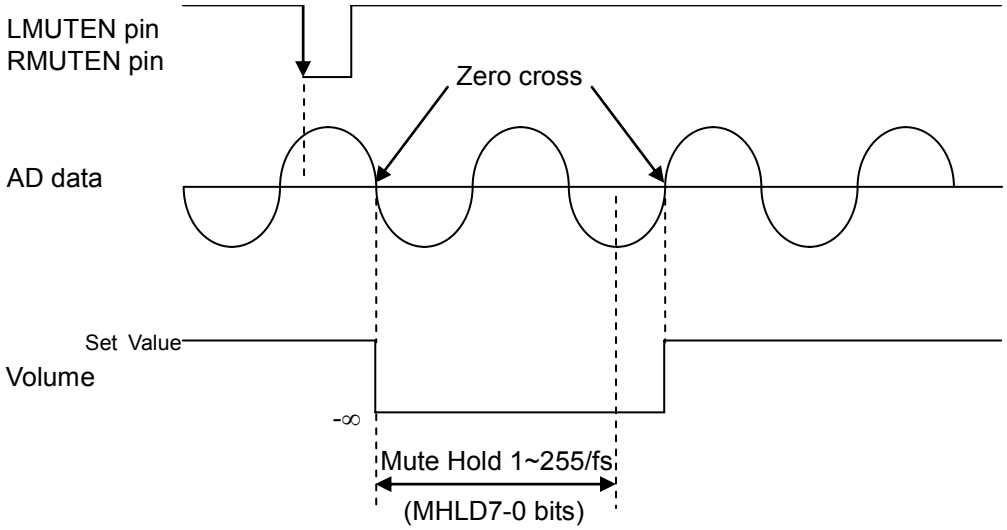


Figure 17. One Shot Mute for LMUTEN, RMUTEN pins

■ Power Management Control

USB specifies that the current at suspend mode must not exceed 500μA. When the USB host is in suspend mode, the SUSN pin also becomes to "L" in order to notify this mode to the external components like DSP's to observe USB specification.

■ Synchronization

The AK5373 supports synchronous type synchronization which is synchronous to SOF (start of frame) packets which are issued per 1ms.

■ Descriptor's Customization

USB audio class has very flexible, but complicated format. In order to keep both of the flexibility and simplicity to use, the AK5373 utilizes the precompiled control information in EEP-ROM instead of direct USB audio class decoding. Data in EEP-ROM is divided into two blocks; header information block and USB descriptor block. Header block size is fixed while USB descriptor block size is variable. Header information includes various control information such as audio format, the microphone's gain, power management information, and etc. When the device is powered up, at first the AK5373 reads the header block in EEP-ROM, and maps these values into the internal registers. Note that 8k bits or larger SPI type EEP-ROM is available.

The AK5373 does not store all of the descriptors into internal memory at the boot time. Instead, the AK5373 reads the descriptor from EEP-ROM and transmit it when it receives the "Get Descriptor" Request command. The AK5373 transmits NAK until it is ready to send data.

Header Information includes

1) Power Management Information
2) Microphone Gain
3) External Digital Audio Interface Information
4) Mute Control Information
5) Descriptor related information
    a) PCM format(stereo/mono, resolution) and the related alternate setting number
    b) Endpoint number
    c) Initial/Minimum/Maximum Volume

■ EEP-ROM Control Interface

Register information and descriptor information on EEP-ROM are read by SPI I/F (CSN, SK, EPAO and EPAI) pins. The data on the I/F consists of Instruction Byte, Address Byte (MSB first, 16bits) and Input Data Byte (MSB first, 8bits). The AK5373 outputs Instruction Byte and Address Byte on a falling edge of SK and down-loads address data from EPAI. The next address data is read by sending SK signal continuously. Data reading ends by a rising edge of CSN. SK clock speed is typically 1.5MHz. The AK5373 reads data from EEP-ROM according to a request signal from the USB host after releasing a reset.

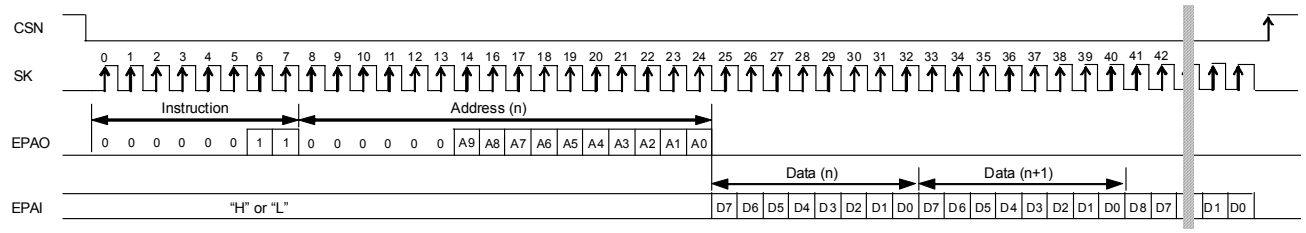


Figure 18. EEP-ROM I/F Read Sequence

■ EEP-ROM memory map

<Header Block> 32 Bytes (fixed)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
000H	Power Management	0	0	0	SELF	0	CLKO	PMADR	PMADL
001H	Microphone Gain Control	0	0	0	PMMP	0	MGAIN2	MGAIN1	MGAIN0
002H	Ext. Audio I/F Control	SDOUT	SDIN	0	0	0	0	512FS	I2S
003H	PCM Format Alt 1	INTFQ12	INTFQ11	INTFQ10	MIX1	RES11	RES10	SIGNED1	STEREO1
004H	PCM Format Alt 2	INTFQ22	INTFQ21	INTFQ20	MIX2	RES21	RES20	SIGNED2	STEREO2
005H	PCM Format Alt 3	INTFQ32	INTFQ31	INTFQ30	MIX3	RES31	RES30	SIGNED3	STEREO3
006H	PCM Format Alt 4	INTFQ42	INTFQ41	INTFQ40	MIX4	RES41	RES40	SIGNED4	STEREO4
007H	PCM Format Alt 5	INTFQ52	INTFQ51	INTFQ50	MIX5	RES51	RES50	SIGNED5	STEREO5
008H	PCM Format Alt 6	INTFQ62	INTFQ61	INTFQ60	MIX6	RES61	RES60	SIGNED6	STEREO6
009H	PCM Format Alt 7	INTFQ72	INTFQ71	INTFQ70	MIX7	RES71	RES70	SIGNED7	STEREO7
00AH	Sampling Frequency Alt 1	VALID1	FS48K1	FS44K1	FS32K1	FS22K1	FS16K1	FS11K1	FS8K1
00BH	Sampling Frequency Alt 2	VALID2	FS48K2	FS44K2	FS32K2	FS22K2	FS16K2	FS11K2	FS8K2
00CH	Sampling Frequency Alt 3	VALID3	FS48K3	FS44K3	FS32K3	FS22K3	FS16K3	FS11K3	FS8K3
00DH	Sampling Frequency Alt 4	VALID4	FS48K4	FS44K4	FS32K4	FS22K4	FS16K4	FS11K4	FS8K4
00EH	Sampling Frequency Alt 5	VALID5	FS48K5	FS44K5	FS32K5	FS22K5	FS16K5	FS11K5	FS8K5
00FH	Sampling Frequency Alt 6	VALID6	FS48K6	FS44K6	FS32K6	FS22K6	FS16K6	FS11K6	FS8K6
010H	Sampling Frequency Alt 7	VALID7	FS48K7	FS44K7	FS32K7	FS22K7	FS16K7	FS11K7	FS8K7
011H	Endpoint Number	0	0	0	0	0	EPNO2	EPNO1	EPNO0
012H	Initial Volume	INTVOL7	INTVOL6	INTVOL5	INTVOL4	INTVOL3	INTVOL2	INTVOL1	INTVOL0
013H	Minimum Volume	MINVOL7	MINVOL6	MINVOL5	MINVOL4	MINVOL3	MINVOL2	MINVOL1	MINVOL0
014H	Maximum Volume	MAXVOL7	MAXVOL6	MAXVOL5	MAXVOL4	MAXVOL3	MAXVOL2	MAXVOL1	MAXVOL0
015H	Mute Control 1	0	0	0	0	OSME	ZCE	ZTM1	ZTM0
016H	Mute Control 2	MHT7	MHT6	MHT5	MHT4	MHT3	MHT2	MHT1	MHT0
017H	Reserved	0	0	0	0	0	0	0	0
018H	Reserved	0	0	0	0	0	0	0	0
019H	Reserved	0	0	0	0	0	0	0	0
01AH	Reserved	0	0	0	0	0	0	0	0
01BH	Reserved	0	0	0	0	0	0	0	0
01CH	Reserved	0	0	0	0	0	0	0	0
01DH	Reserved	0	0	0	0	0	0	0	0
01EH	Reserved	0	0	0	0	0	0	0	0
01FH	Reserved	0	0	0	0	0	0	0	0

<Descriptor Block>

Addr	Descriptor	Size
020H ~ 023H	Language ID String Descriptor	4 bytes
024H ~ 0A3H	iManufacturer String Descriptor	128 bytes (max)
0A4H ~ 123H	iProduct String Descriptor	128 bytes (max)
124H ~ 1A3H	iSerial Number String Descriptor	128 bytes (max)
1A4H ~ 1B5H	Device Descriptor	18 bytes
1B6H ~ 1BEH	Configuration Descriptor	9 bytes
1BFH ~ 1C7H	Standard Audio Control Interface Descriptor	9 bytes
1C8H ~ 1D0H	Class-specific Audio Control Interface Descriptor	9 bytes
1D1H ~ 1DCH	Input Terminal Descriptor	12 bytes
1DDH ~ 1E5H	Output Terminal Descriptor	9 bytes
1E6H ~	Feature Unit Descriptor	8 or 10 bytes
	Zero-bandwidth Alternate Setting 0	
	Standard AS Interface Descriptor	9 bytes
	Alternate Setting 1	
	Standard AS Interface Descriptor	9 bytes
	Class-specific AS General Interface Descriptor	6 bytes
	Type 1 Format Type Descriptor	11 ~ 29 bytes
	Standard Endpoint Descriptor	9 bytes
	Class-specific Isochronous Audio Data Endpoint Descriptor	7 bytes
	Alternate Setting 2	
	Standard AS Interface Descriptor	9 bytes
	Class-specific AS General Interface Descriptor	6 bytes
	Type 1 Format Type Descriptor	11 ~ 29 bytes
	Standard Endpoint Descriptor	9 bytes
	Class-specific Isochronous Audio Data Endpoint Descriptor	7 bytes
	Alternate Setting 3	
	Standard AS Interface Descriptor	9 bytes
	Class-specific AS General Interface Descriptor	6 bytes
	Type 1 Format Type Descriptor	11 ~ 29 bytes
	Standard Endpoint Descriptor	9 bytes
	Class-specific Isochronous Audio Data Endpoint Descriptor	7 bytes
	Alternate Setting 4	
	Standard AS Interface Descriptor	9 bytes
	Class-specific AS General Interface Descriptor	6 bytes
	Type 1 Format Type Descriptor	11 ~ 29 bytes
	Standard Endpoint Descriptor	9 bytes
	Class-specific Isochronous Audio Data Endpoint Descriptor	7 bytes
	Alternate Setting 5	
	Standard AS Interface Descriptor	9 bytes
	Class-specific AS General Interface Descriptor	6 bytes
	Type 1 Format Type Descriptor	11 ~ 29 bytes
	Standard Endpoint Descriptor	9 bytes
	Class-specific Isochronous Audio Data Endpoint Descriptor	7 bytes
	Alternate Setting 6	
	Standard AS Interface Descriptor	9 bytes
	Class-specific AS General Interface Descriptor	6 bytes
	Type 1 Format Type Descriptor	11 ~ 29 bytes
	Standard Endpoint Descriptor	9 bytes
	Class-specific Isochronous Audio Data Endpoint Descriptor	7 bytes
	Alternate Setting 7	
	Standard AS Interface Descriptor	9 bytes
	Class-specific AS General Interface Descriptor	6 bytes
	Type 1 Format Type Descriptor	11 ~ 29 bytes
	Standard Endpoint Descriptor	9 bytes
	Class-specific Isochronous Audio Data Endpoint Descriptor	7 bytes

Note 20. Read address after a reset release: 000H~016H, 024H, 0A4H, 124H, 1B8H~1B9H (Total 28bytes)

Note 21. The data address must be written slide forward if the number of bytes is less than the data size above in the address after 1E6H.

Note 22. The setting of 003H~011H and the setting after 1F9H must be matched.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	SELF	0	CLKO	PMADR	PMADL

PMADL: MIC-Amp Lch and ADC Lch Power Management
"0": Power-up
"1": Power-down

PMADR: MIC-Amp Rch and ADC Rch Power Management
"0": Power-up
"1": Power-down

CLKO: Master Clock Output Driver Power Management
"0": Power-up
"1": Power-down

SELF: Self Power Mode Enable
"0": Bus Power Mode
"1": Self Power Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Microphone Gain Control	0	0	0	PMMP	0	MGAIN2	MGAIN1	MGAIN0

MGAIN2-0: MIC-Amp Gain Control (Enabled when the MGAIN2 pin = MGAIN1 pin = MGAIN0 pin = "L")
"000": 0dB
"001": 0dB
"010": +6dB
"011": +12dB
"100": +18dB
"101": +24dB
"110": +30dB
"111": +36dB

PMMP: MPWR pin Power Management
"0": Power-up
"1": Power-down: Hi-z

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Ext. Audio I/F Control	SDOUT	SDIN	0	0	0	0	512FS	I2S

I2S: Audio Format
"0": MSB justified
"1": I2S

512FS: Master Clock Output Frequency
"0": 256fs
"1": 512fs

SDIN: Ext. Audio Input Interface Enable
"0": Power-down and Disable: SDTI pin must be connected to VSS1-3.
"1": Power-up and Enable
If this bit is set to "1", the AK5373 receives audio data via the external digital audio interface and transmits them to the host instead of the A/D data generated by the AK5373.

SDOUT: Ext. Audio Output Interface Enable
"0": Power-down and Disable: SDTO pin = "L"
"1": Power-up and Enable
If this bit is set to "1", the A/D data is output via this Interface.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	PCM Format Alt 1	INTFQ12	INTFQ11	INTFQ10	MIX1	RES11	RES10	SIGNED1	STEREO1
04H	PCM Format Alt 2	INTFQ22	INTFQ21	INTFQ20	MIX2	RES21	RES20	SIGNED2	STEREO2
05H	PCM Format Alt 3	INTFQ32	INTFQ31	INTFQ30	MIX3	RES31	RES30	SIGNED3	STEREO3
06H	PCM Format Alt 4	INTFQ42	INTFQ41	INTFQ40	MIX4	RES41	RES40	SIGNED4	STEREO4
07H	PCM Format Alt 5	INTFQ52	INTFQ51	INTFQ50	MIX5	RES51	RES50	SIGNED5	STEREO5
08H	PCM Format Alt 6	INTFQ62	INTFQ61	INTFQ60	MIX6	RES61	RES60	SIGNED6	STEREO6
09H	PCM Format Alt 7	INTFQ72	INTFQ71	INTFQ70	MIX7	RES71	RES70	SIGNED7	STEREO7

STEREO: Mono/Stereo Mode Select
"0": Mono
"1": Stereo

SIGNED: Unsigned/Signed Mode Select
"0": Unsigned ("0" is valid only when the resolution is 8 bit)
"1": Signed

RES1-0: ADC Resolution Mode Select
"00": 8bit
"01": 16bit
"10": 24bit

MIX: ADC Data Mix Control
"0": Lch and Rch are not mixed.
"1": Lch and Rch are mixed. Dynamic range and S/N can be improved by approximately 3dB when the same analog signal is inputted to left and right channels.

INTFQ2-0: Initial Sampling Frequency
"000": 8kHz, "001": 11.025kHz
"010": 16kHz, "011": 22.05kHz
"100": 32kHz, "101": 44.1kHz
"110": 48kHz

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Sampling Frequency Alt 1	VALID1	FS48K1	FS44K1	FS32K1	FS22K1	FS16K1	FS11K1	FS8K1
0BH	Sampling Frequency Alt 2	VALID2	FS48K2	FS44K2	FS32K2	FS22K2	FS16K2	FS11K2	FS8K2
0CH	Sampling Frequency Alt 3	VALID3	FS48K3	FS44K3	FS32K3	FS22K3	FS16K3	FS11K3	FS8K3
0DH	Sampling Frequency Alt 4	VALID4	FS48K4	FS44K4	FS32K4	FS22K4	FS16K4	FS11K4	FS8K4
0EH	Sampling Frequency Alt 5	VALID5	FS48K5	FS44K5	FS32K5	FS22K5	FS16K5	FS11K5	FS8K5
0FH	Sampling Frequency Alt 6	VALID6	FS48K6	FS44K6	FS32K6	FS22K6	FS16K6	FS11K6	FS8K6
10H	Sampling Frequency Alt 7	VALID7	FS48K7	FS48K7	FS32K7	FS22K7	FS16K7	FS11K7	FS8K7

FS8K: Sampling Frequency 8kHz Enable
"0": Disable
"1": Enable

FS11K: Sampling Frequency 11.025kHz Enable
"0": Disable
"1": Enable

FS16K: Sampling Frequency 16kHz Enable
"0": Disable
"1": Enable

FS22K: Sampling Frequency 22.05kHz Enable
"0": Disable
"1": Enable

FS32K: Sampling Frequency 32kHz Enable
"0": Disable
"1": Enable

FS44K: Sampling Frequency 44.1kHz Enable
"0": Disable
"1": Enable

FS48K: Sampling Frequency 48kHz Enable
"0": Disable
"1": Enable

VALID: Alternate Setting Enable
"0": Disable
"1": Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	Endpoint Number	0	0	0	0	0	EPNO2	EPNO1	EPNO0

EPNO2-0: Endpoint Number (1~7)