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AK5388A

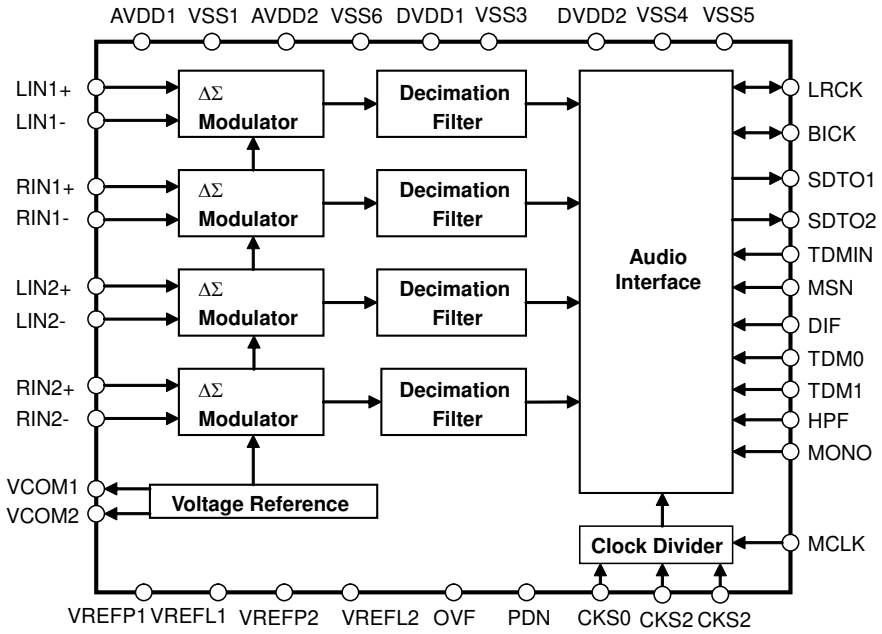
120dB 24-bit 192kHz 4-Channel ADC

GENERAL DESCRIPTION

The AK5388A is a 24bit, 216kHz sampling 4-channel A/D converter for high-end audio systems. The modulator in the AK5388A uses AKM's Enhanced Dual Bit architecture, enabling the AK5388A to realize high accuracy and low cost. The AK5388A achieves 120dB dynamic range and 110dB S/(N+D), and an optional mono mode extends dynamic range to 123dB. The AK5388A's digital filter features a modified FIR architecture that minimizes group delay while maintaining excellent linear phase response. So the device is suitable for professional audio applications including recording, sound reinforcement, effects processing, sound cards, and high-end A/V receivers. The AK5388A is available in 44pin LQFP package.

FEATURES

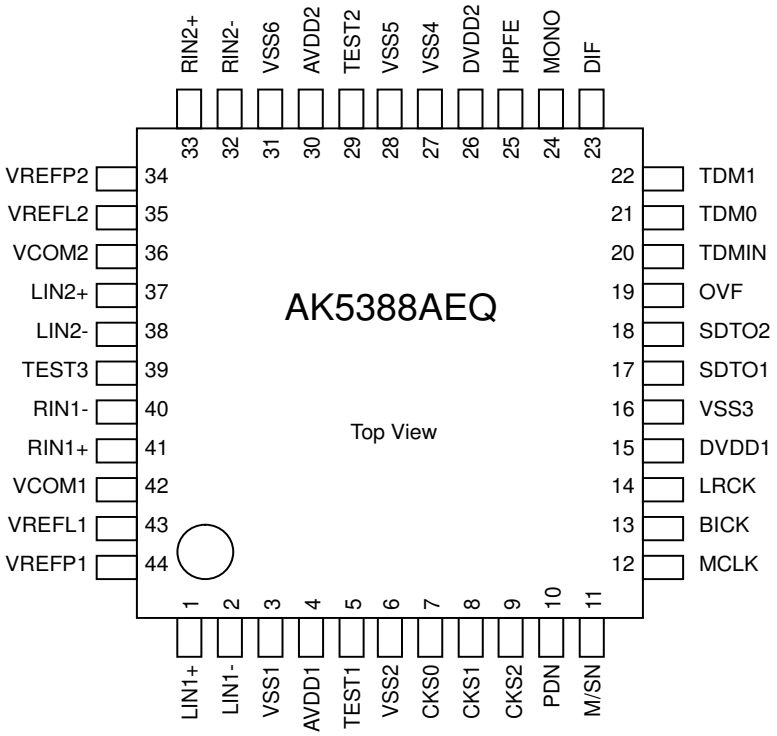
- **Sampling Rate: 8kHz ~ 216kHz**
- **Full Differential Inputs**
- **S/(N+D): 110dB**
- **DR, S/N: 120dB(Mono Mode: 123dB)**
- **Short Delay Digital Filter (GD=12.6/fs)**
  - **Passband: 0~21.648kHz (@fs=48kHz)**
  - **Ripple: 0.01dB**
  - **Stopband: 80dB**
- **Digital HPF**
- **Power Supply: 4.75 ~ 5.25V(Analog), 3.0 ~ 3.6V(Digital)**
- **Output format: 24bit MSB justified, I^2S or TDM**
- **Cascade TDM I/F: 8ch/48kHz, 4ch/96kHz, 4ch/192kHz**
- **Master & Slave Mode**
- **Overflow Flag**
- **Power Dissipation: 575 mW (@fs=48kHz)**
- **Package: 44pin LQFP**



■ Ordering Guide

AK5388AEQ	–10 ~ +70°C	44pin LQFP (0.8mm pitch)
AKD5388A	Evaluation Board for AK5388A	

■ Pin Layout



PIN / FUNCTION

No.	Pin Name	I/O	Function
1	LIN1+	I	ADC1 Lch Positive Analog Input Pin
2	LIN1−	I	ADC1 Lch Negative Analog Input Pin
3	VSS1	-	Ground Pin
4	AVDD1	-	Analog Power Supply Pin, 4.75 ~ 5.25V
5	TEST1	I	Test Pin (Connected to VSS1-6)
6	VSS2		Ground pin
7	CKS0	I	Clock Mode Select #0 Pin
8	CKS1	I	Clock Mode Select #1 Pin
9	CKS2	I	Clock Mode Select #2 Pin
10	PDN	I	Power-Down Mode Pin When "L", the circuit is in power-down mode. The AK5388A should always be reset upon power-up.
11	MSN	I	Master/Slave mode Select Pin "L": Slave mode, "H": Master mode
12	MCLK	I	Master Clock Input Pin
13	BICK	I/O	Audio Serial Data Clock Pin "L" Output in Master Mode at Power-down mode.
14	LRCK	I/O	Output Channel Clock Pin "L" Output in Master Mode at Power-down mode.
15	DVDD1	-	Digital Power Supply Pin, 3.0 ~ 3.6V
16	VSS3	-	Ground Pin
17	SDTO1	O	ADC1 Audio Serial Data Output Pin "L" Output at Power-down mode.
18	SDTO2	O	ADC2 Audio Serial Data Output Pin "L" Output at Power-down mode.
19	OVF	O	Analog Input Overflow Detect Pin This pin goes to "H" if any analog inputs overflows. "L" Output at Power-down mode.
20	TDMIN	I	TDM Data Input Pin
21	TDM0	I	TDM I/F Format Enable Pin "L" : Normal Mode, "H" : TDM Mode
22	TDM1	I	TDM I/F BICK Frequency Select Pin "L" : Normal Mode, "H" : TDM Mode
23	DIF	I	Audio Interface Format Pin "L": 24BitMSB justified, "H": 24BitI^2S Compatible
24	MONO	I	Stereo/Mono mode Select Pin "L": Stereo mode, "H": Mono mode
25	HPFE	I	HPF Enable Pin "L": Disable, "H" Enable
26	DVDD2	-	Digital Power Supply Pin, 3.0 ~ 3.6V
27	VSS4	-	Ground Pin
28	VSS5		Ground pin

No.	Pin Name	I/O	Function
29	TEST2	I	Test Pin (Connected to VSS1-6)
30	AVDD2	-	Analog Power Supply Pin, 4.75 ~ 5.25V
31	VSS6	-	Ground Pin
32	RIN2−	I	ADC2 Rch Negative Analog Input Pin
33	RIN2+	I	ADC2 Rch Positive Analog Input Pin
34	VREFP2	I	ADC2 High Level Voltage Reference Input Pin
35	VREFL2	I	ADC2 Low Level Voltage Reference Input Pin
36	VCOM2	O	Common Voltage Output Pin, (AVDD2)/2 Normally connected to AVSS2 with a 0.1μF ceramic capacitor in parallel with an electrolytic capacitor less than 2.2μF.
37	LIN2+	I	ADC2 Lch Positive Analog Input Pin
38	LIN2−	I	ADC2 Lch Negative Analog Input Pin
39	TEST3	I	Test Pin (Connected to VSS1-6)
40	RIN1−	I	ADC1 Rch Negative Analog Input Pin
41	RIN1+	I	ADC1 Rch Positive Analog Input Pin
42	VCOM1	O	Common Voltage Output Pin, (AVDD1)/2 Normally connected to AVSS1 with a 0.1μF ceramic capacitor in parallel with an electrolytic capacitor less than 2.2μF.
43	VREFL1	I	ADC1 Low Level Voltage Reference Input Pin
44	VREFP1	I	ADC1 High Level Voltage Reference Input Pin

Note: All digital input pins should not be allowed to float.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LIN1+/–, RIN1+/–	These pins should be connected to VSS1-6
	LIN2+/–, RIN+/–	These pins should be connected to VSS1-6
Digital	OVF	This pin should be open.
	TEST1	This pin should be connected to VSS1-6
	TEST2	This pin should be connected to VSS1-6
	TEST3	This pin should be connected to VSS1-6

ABSOLUTE MAXIMUM RATINGS

(VSS1-6=0V; Note 1)

Parameter		**Symbol**	**min**	**max**	**Unit**
Power Supplies:	Analog	AVDD1	–0.3	6.0	V
	Analog	AVDD2	–0.3	6.0	V
	Digital	DVDD1	–0.3	6.0	V
	Digital Output Buffer	DVDD2	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	–	±10	mA
Analog Input Voltage (Note 2)		VINA	–0.3	AVDD1+0.3	V
		VINA	–0.3	AVDD2+0.3	
Digital Input Voltage (Note 3)		VIND	–0.3	DVDD1+0.3	V
		VIND	–0.3	DVDD2+0.3	
Ambient Temperature (power applied)		Ta	–10	70	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to VSS1-6 pins.
Note 2. VREFP1, VREFP2, VREFL1, VREFL2, AINL1/2+, AINL1/2-, AINR1/2+ and AINR1/2- pins
Note 3. PDN, CKS0, CKS1, CKS2, TDMIN, MCLK, BICK, LRCK, DIF, TDM0, TDM1, HPFE, MONO and TST1/2/3 pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1-6=0V; Note 1)

Parameter		Symbol	min	typ	max	Unit
Power Supplies:	Analog	AVDD1	4.75	5.0	5.25	V
	Analog	AVDD2	4.75	5.0	5.25	V
(Note 4)	Digital	DVDD1/2	3.0	3.3	3.6	V
Voltage Reference	"H" voltage Reference	VREFP1	AVDD1-0.5	-	AVDD1	V
(Note 5)		VREFP2	AVDD2-0.5	-	AVDD2	V
	"L" voltage reference	VREFL1	VSS1-6	-	-	V
		VREFL2	VSS1-6	-	-	V
	VREFP1 – VREFL1	ΔVREF	AVDD1-0.5	-	AVDD1	V
	VREFP2 – VREFL2	ΔVREF	AVDD2-0.5	-	AVDD2	V

Note 1. All voltages with respect to VSS1-6 pins.

Note 4. The power up sequence between AVDD1/2 and DVDD1/2 is not critical.

Note 5. VREFL– and VREFR– pins should be connected to VSS1-6 pins.

Analog input voltage scales with voltage of {(VREFP) – (VREFL)}.

Vin (typ, @ 0dB) = ±2.8 x {(VREF+) – (VREF–)} / 5 [V].

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta = 25°C; AVDD1/2=5.0V; DVDD1/2=3.3V; VSS1-6=0V; VREFP1=VREFP2=AVDD, VREFL1 = VREFL2 = VSS1-6; fs=48kHz, 96kHz, 192kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=10Hz ~ 20kHz at fs = 48kHz, 40Hz ~ 40kHz at fs = 96kHz, 40Hz ~ 40kHz at fs = 192kHz; unless otherwise specified)

Parameter			min	typ	max	Unit
Analog Input Characteristics:						
Resolution			-	-	24	Bits
Input Voltage		(Note 6)	±2.7	±2.8	±2.9	Vpp
S/(N+D)	fs=48kHz BW=20kHz	−1dBFS	100	110	-	dB
		−20dBFS	-	97	-	dB
		−60dBFS	-	57	-	dB
	fs=96kHz BW=40kHz	−1dBFS	97	107	-	dB
		−20dBFS	-	90	-	dB
		−60dBFS	-	50	-	dB
	fs=192kHz BW=40kHz	−1dBFS	-	107	-	dB
		−20dBFS	-	90	-	dB
		−60dBFS	-	50	-	dB
Dynamic Range (−60dBFS with A-weighted)		Stereo Mode	114	120	-	dB
		Mono Mode	-	123	-	
S/N (A-weighted)		Stereo Mode	114	120	-	dB
		Mono Mode	-	123	-	
Input Resistance			3.15	3.7	4.25	kΩ
Interchannel Isolation			110	120		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Power Supply Rejection		(Note 7)		60	-	dB
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H")						
AVDD1/2				105	130	mA
DVDD	(fs=48kHz)			15	22	mA
DVDD	(fs=96kHz)			27	39	mA
DVDD	(fs=192kHz)			20	29	mA
Power down mode (PDN pin = "L")		(Note 8)				
AVDD+DVDD				10	100	μA

Note 6. This value is (LIN+)−(LIN−) and (RIN+)−(RIN−). Input voltage is proportional to VREF voltage. Vin = 0.56 x VREF1/2 (Vpp).

Note 7. PSR is applied to AVDD1/2 and DVDD1/2 with 1kHz, 20mVpp. The VREFP1 and VREFP2 pins held a constant voltage.

Note 8. All digital input pins are held DVDD1/2 or VSS3/4.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta=25°C; AVDD1/2=4.75 ~ 5.25V; DVDD1/2=3.0 ~ 3.6V; DFS1 = "L", DFS0 = "L")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 9)	−0.01dB	PB	0		21.6	kHz
	−0.1dB		-	22.0	-	kHz
	−3.0dB		-	23.8	-	kHz
	−6.0dB		-	24.4	-	kHz
Stopband		SB	27.9			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 10)		GD		12.6		1/fs
Group Delay Distortion		ΔGD		±0.01		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 9)	−3dB	FR		1.0		Hz
	−0.1dB			6.5		Hz

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=25°C; AVDD1/2=4.75 ~ 5.25V; DVDD1/2=3.0 ~ 3.6V; DFS1 = "L", DFS0 = "H")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 9)	−0.01dB	PB	0		43.3	kHz
	−0.1dB		-	44.2	-	kHz
	−3.0dB		-	47.6	-	kHz
	−6.0dB		-	48.9	-	kHz
Stopband		SB	55.9			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 10)		GD		12.6		1/fs
Group Delay Distortion		ΔGD		±0.013		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 9)	−3dB	FR		1.0		Hz
	−0.1dB			6.5		Hz

Note 9. The passband and stopband frequencies scale with fs. The reference frequency of these responses is 1kHz.

Note 10. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

FILTER CHARACTERISTICS (fs=192kHz)

(Ta=25°C; AVDD1/2=4.75 ~ 5.25V; DVDD1/2=3.0 ~ 3.6V; DFS1 = "H", DFS0 = "L")

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 11)	−0.08dB	PB	-	-	83.0	kHz
	−0.1dB		-	83.4	-	kHz
	−3.0dB		-	99.9	-	kHz
	−6.0dB		-	106.5	-	kHz
Stopband		SB	141.1			kHz
Passband Ripple		PR			±0.08	dB
Stopband Attenuation		SA	80			dB
Group Delay (Note 12)		GD		9.8		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 11)	−3dB	FR		1.0		Hz
	−0.1dB			6.5		Hz

Note 11. The passband and stopband frequencies scale with fs. The reference frequency of these responses is 1kHz.

Note 12. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

DC CHARACTERISTICS

(Ta=25°C; AVDD1/2=4.75 ~ 5.25V; DVDD1/2=3.0 ~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
High-Level Input Voltage		VIH	70%DVDD1	-	-	V
			70%DVDD2	-		V
Low-Level Input Voltage		VIL	-	-	30%DVDD1	V
				-	30%DVDD2	V
High-Level Output Voltage	(Iout=−400μA)	VOH	DVDD1−0.4	-	-	V
			DVDD2−0.4	-		V
Low-Level Output Voltage	(Iout=400μA)	VOL	-	-	0.4	V
Input Leakage Current		Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD1/2=4.75 ~ 5.25V; DVDD1/2=3.0 ~ 3.6V; C_L=20pF)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
Master Clock 128fs:	fCLK	1.024	24.576	27.648	MHz
Pulse Width Low	tCLKL	0.4fCLK			ns
Pulse Width High	tCLKH	0.4fCLK			ns
192fs:	fCLK	1.536	36.864	41.472	MHz
Pulse Width Low	tCLKL	0.4fCLK			ns
Pulse Width High	tCLKH	0.4fCLK			ns
256fs:	fCLK	2.048	12.288	27.648	MHz
Pulse Width Low	tCLKL	0.4fCLK			ns
Pulse Width High	tCLKH	0.4fCLK			ns
384fs:	fCLK	3.072	18.432	41.472	MHz
Pulse Width Low	tCLKL	0.4fCLK			ns
Pulse Width High	tCLKH	0.4fCLK			ns
512fs:	fCLK	4.096	24.576	27.648	MHz
Pulse Width Low	tCLKL	0.4fCLK			ns
Pulse Width High	tCLKH	0.4fCLK			ns
768fs:	fCLK	6.144	36.864	41.472	MHz
Pulse Width Low	tCLKL	0.4fCLK			ns
Pulse Width High	tCLKH	0.4fCLK			ns
LRCK Timing (Slave Mode)					
Normal mode (TDM1="L", TDM0="L")					
LRCK Frequency	fs	8		216	kHz
Duty Cycle	Duty	45		55	%
TDM256 MODE (TDM1="L", TDM0="H")					
LRCK Frequency	fs	8		54	kHz
"H" time	tLRH	1/256fs			ns
"L" time	tLRL	1/256fs			ns
TDM128 MODE (TDM1="H", TDM0="H")					
LRCK Frequency	fs	8		216	kHz
"H" time	tLRH	1/128fs			ns
"L" time	tLRL	1/128fs			ns
LRCK Timing (Master Mode)					
Normal mode (TDM1="L", TDM0="L")					
LRCK Frequency	fs	8		216	kHz
Duty Cycle	Duty		50		%
TDM256 MODE (TDM1="L", TDM0="H")					
LRCK Frequency	fs	8		54	kHz
"H" time (Note 13)	tLRH		1/8fs		ns
TDM128 MODE (TDM1="H", TDM0="H")					
LRCK Frequency	fs	8		216	kHz
"H" time (Note 13)	tLRH		1/4fs		ns

Note 13. "L" time at I^2S format

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Slave mode)					
Normal mode (TDM1="L", TDM0="L")					
BICK Period					
Normal Speed Mode	TBCK	1/128fs			ns
Double , Quad Speed Mode	TBCK	1/64fs			ns
Duty Cycle	Duty	40		60	%
LRCK Edge to BICK "↑" (Note 14)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 14)	tBLR	20			ns
LRCK to SDTO1/2 (MSB) (Except I^2S mode)	tLRS				ns
BICK "↓" to SDTO1/2	tBSD			20	ns
TDM256 mode (TDM1="L", TDM0="H")					
BICK Period	tBCK	1/256fs			ns
Duty Cycle	Duty	40		60	%
LRCK Edge to BICK "↑" (Note 14)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 14)	tBLR	20			ns
BICK "↓" to SDTO1/2 (Note 15)	tBSD			20	ns
TDMIN Setup time	tTDMS	16			ns
TDM128 mode (TDM1="H", TDM0="H") (8KHz ≤ fs < 108KHz)					
BICK Period	tBCK	1/128fs			ns
Duty Cycle	Duty	40		60	%
LRCK Edge to BICK "↑" (Note 14)	tLRB	20			ns
BICK "↑" to LRCK Edge (Note 14)	tBLR	20			ns
BICK "↓" to SDTO1 (Note 15)	tBSD			20	ns
TDM128 mode (TDM1="H", TDM0="H") (108KHz < fs ≤ 216KHz)					
BICK Period	tBCK	1/128fs			ns
Duty Cycle	Duty	40		60	%
LRCK Edge to BICK "↑" (Note 14)	tLRB	10			ns
BICK "↑" to LRCK Edge (Note 14)	tBLR	10			ns
SDTO1 Setup time BICK "↑ " (Note 15)	tBSS	10			ns
SDTO1 Hold time BICK "↑ " (Note 15)	tBSH	5			ns

Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Master mode)					
Normal mode (TDM1="L", TDM0="L")					
BICK Frequency	fBCK		64fs		Hz
BICK Duty	dBCK		50		%
BICK "↓" to LRCK	tMBLR	−20		20	ns
BICK "↓" to SDTO1/2	tBSD	−20		20	ns
TDM256 mode (TDM1="L", TDM0="H")					
BICK Frequency	fBCK		256fs		Hz
BICK Duty (Note 16)	dBCK		50		%
BICK "↓" to LRCK	tMBLR	−12		12	ns
BICK "↓" to SDTO1 (Note 15)	tBSD	−20		20	ns
TDM128 mode (TDM1="H", TDM0="H") (8KHz ≤ fs < 108KHz)					
BICK Frequency	fBCK		128fs		Hz
BICK Duty	dBCK		50		%
BICK "↓" to LRCK	tMBLR	−12		12	ns
BICK "↓" to SDTO1 (Note 15)	tBSD	−20		20	ns
TDM128 mode (TDM1="H", TDM0="H") (108KHz < fs ≤ 216KHz)					
BICK Frequency	fBCK		128fs		Hz
BICK Duty	dBCK		50		%
BICK "↓" to LRCK	tMBLR	−6		6	ns
BICK "↓" to SDTO1	tBSD	−10		10	ns
Power-Down & Reset Timing					
PDN Pulse Width (Note 17)	tPD	150			ns
PDN "↑" to SDTO1/2 valid (Note 18)	tPDV		516		1/fs

Note 14. BICK rising edge must not occur at the same time as LRCK edge.
Note 15. SDTO2 output is fixed to "L".
Note 16. This value is MCLK=512fs. Duty cycle is not guaranteed when MCLK=256fs/384fs.
Note 17. The AK5388A can be reset by bringing the PDN pin = "L".
Note 18. This cycle is the number of LRCK rising edges from the PDN pin = "H". The value is when the AK5388A is in master mode. In case of in slave mode, the value will be 1LRCK clock cycle (1/fs) longer.

■ Timing Diagram

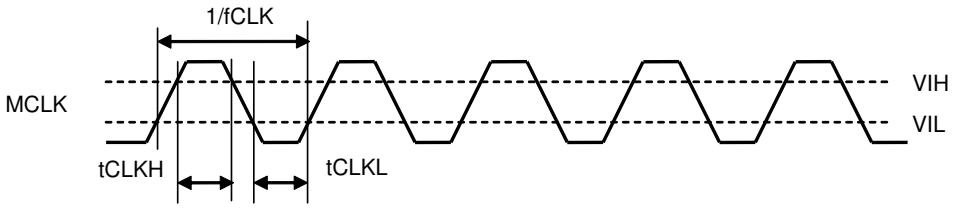


Figure 1. MCLK Timing (TDM0 pin = "L" or "H")

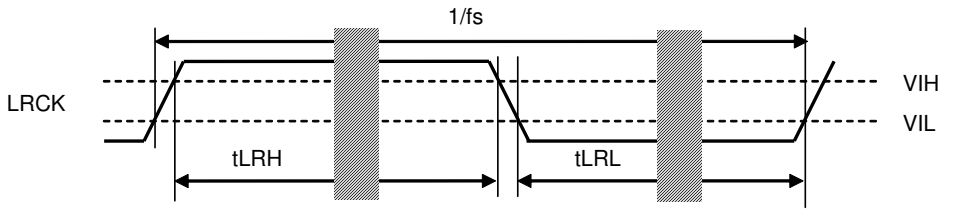


Figure 2. LRCK Timing (TDM0 pin = "L" or "H")

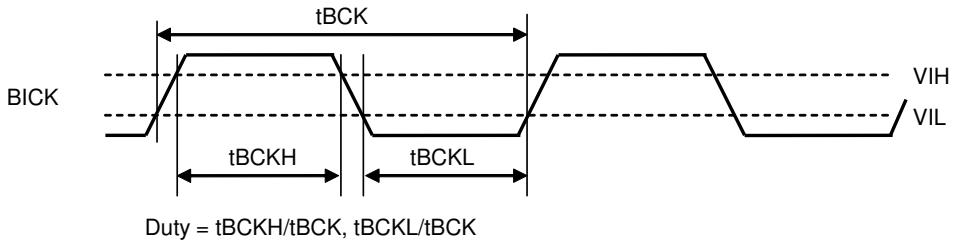


Figure 3.BICK Timing (TDM0 pin = "L" or "H")

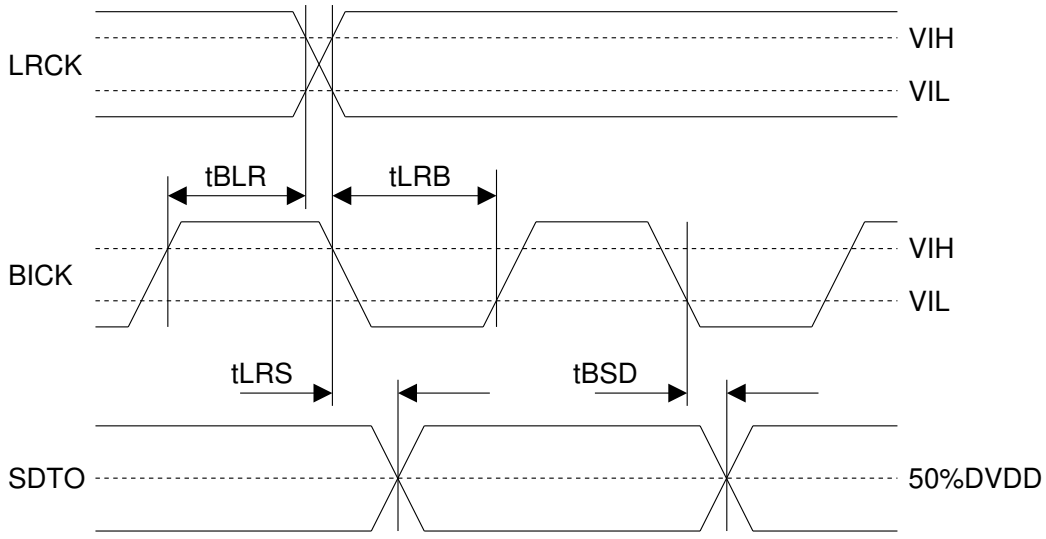


Figure 4. Audio Interface Timing (Slave mode, TDM0 pin = "L")

Note: SDTO shows SDTO1 and SDTO2.

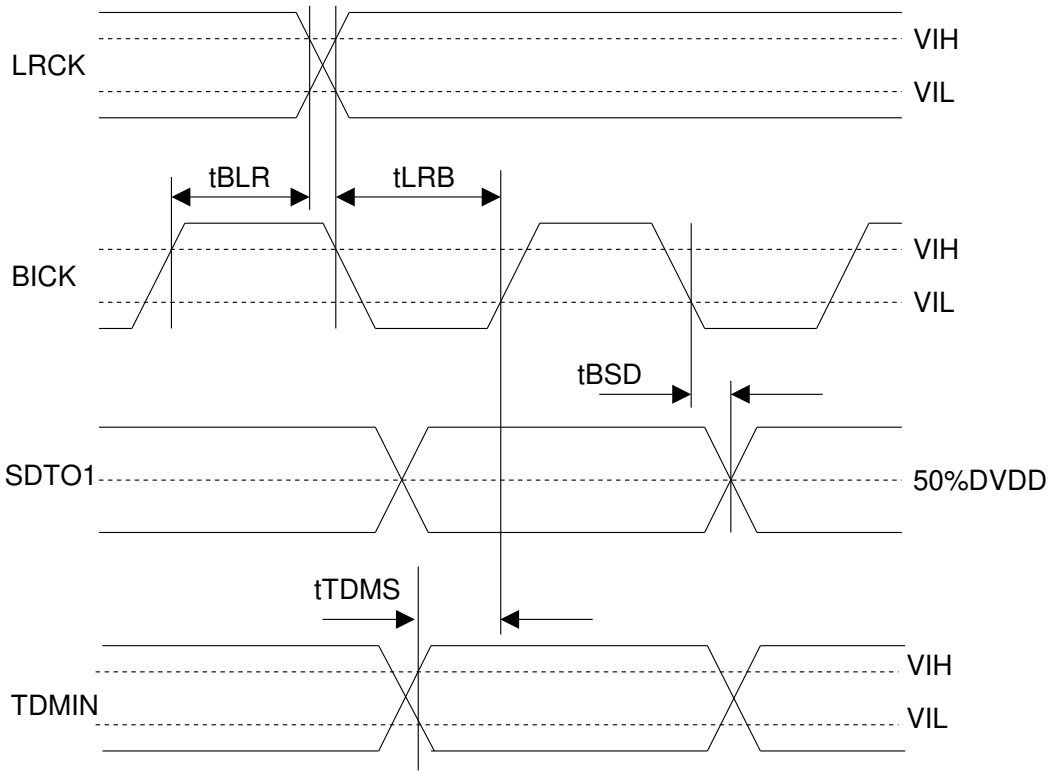


Figure 5. Audio Interface Timing (Slave mode, TDM0 pin = "H")

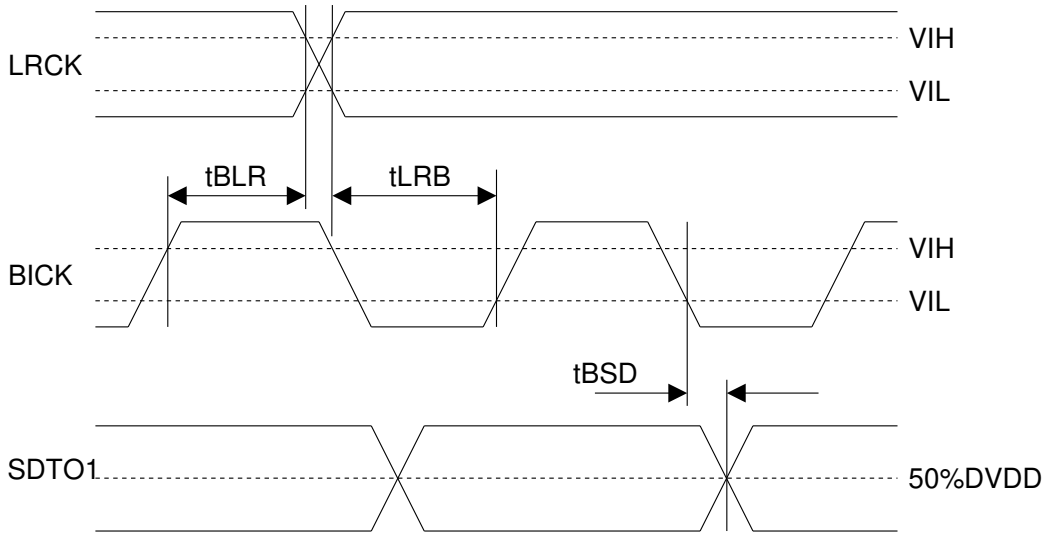


Figure 6. Audio Interface Timing (Slave mode, TDM0 pin = "H", TDM1 pin = "H", 8KHz ≤ fs < 108KHz)

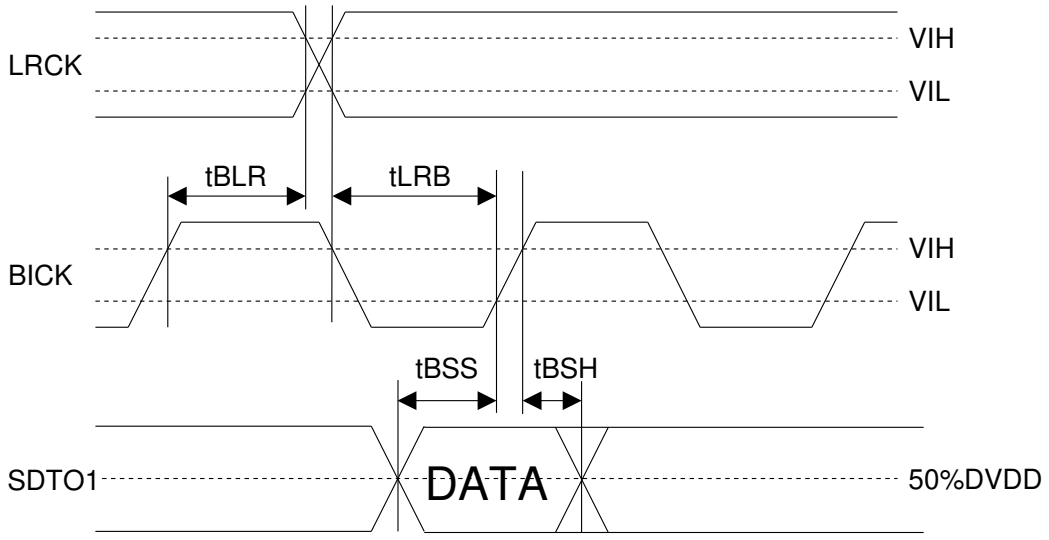


Figure 7. Audio Interface Timing (Slave mode, TDM0 pin = "H", TDM1 pin = "H", 108KHz < fs ≤ 216KHz)

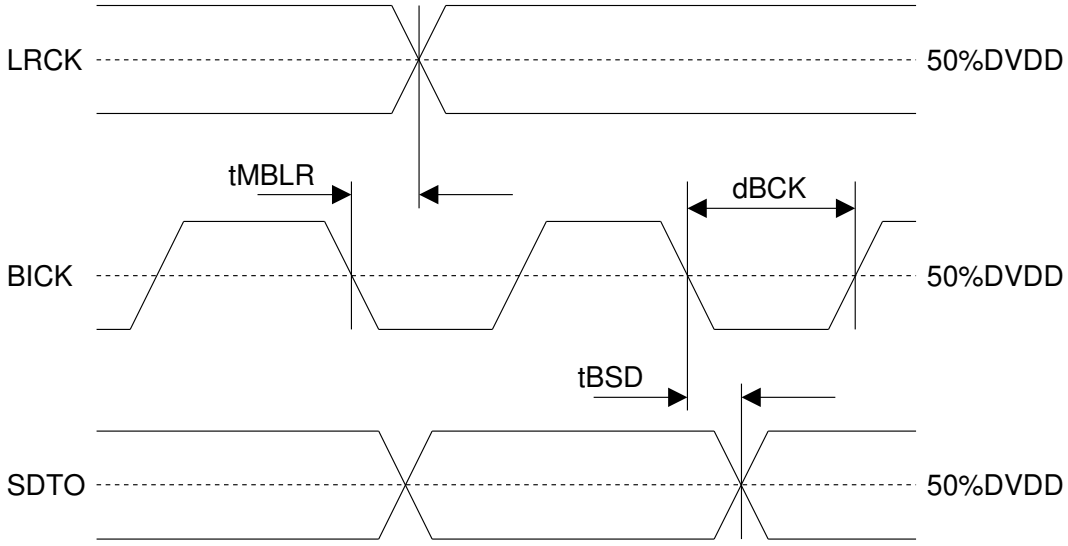


Figure 8. Audio Interface Timing (Master mode)

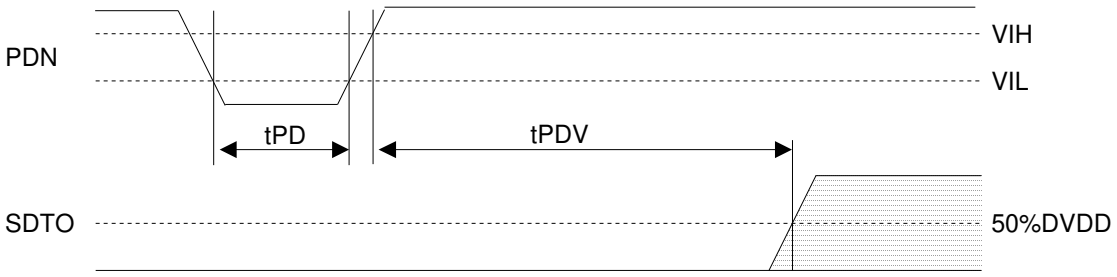


Figure 9. Power Down & Reset Timing

Note: SDTO shows SDTO1 and SDTO2.

OPERATION OVERVIEW

■ System Clock

MCLK (128fs/192fs/256fs/384fs/512fs/768fs), BICK (48fs~) and LRCK (fs) clocks are required in slave mode. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Table 1, Table 2 and Table 3 show the relationship of typical sampling frequency and the system clock frequency. MCLK frequency is selected by CKS1-0 pins as shown in Table 4.

Since the AK5388A includes a phase detection circuit for LRCK, the AK5388A is reset automatically when the synchronization is out of phase after changing the clock frequencies.

All external clocks (MCLK, BICK and LRCK) must be present unless the PDN pin = "L". If these clocks are not provided, the AK5388A may draw excess current due to its use of internal dynamically refreshed logic. If the external clocks are not present, place the AK5388A in power-down mode (PDN pin = "L"). In master mode, the master clock (MCLK) must be provided unless the PDN pin = "L". In case of using two or more devices, the AK5388A should be reset by the PDN pin when changing clocks, changing clock modes and switching digital interfaces for a synchronization. Clock or mode changes should be made during the reset, and a stable clock is needed after the reset.

fs	MCLK					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	N/A	N/A	8.192MHz	12.288MHz	16.384MHz	24.576MHz
48kHz	N/A	N/A	12.288MHz	18.432MHz	24.576MHz	36.864MHz
96kHz	N/A	N/A	24.576MHz	N/A	N/A	N/A
192kHz	24.576MHz	36.864MHz	N/A	N/A	N/A	N/A

(N/A: Not available)

Table 1. System Clock Example (Slave Mode)

fs	MCLK					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	N/A	N/A	8.192MHz	12.288MHz	16.384MHz	24.576MHz
48kHz	N/A	N/A	12.288MHz	18.432MHz	24.576MHz	36.864MHz
96kHz	N/A	N/A	24.576MHz	36.864MHz	N/A	N/A
192kHz	24.576MHz	36.864MHz	N/A	N/A	N/A	N/A

(N/A: Not available)

Table 2. System Clock Example (Master Mode)

fs	MCLK					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	N/A	N/A	N/A	N/A	16.384MHz	24.576MHz
48kHz	N/A	N/A	N/A	N/A	24.576MHz	36.864MHz
96kHz	N/A	N/A	24.576MHz	36.864MHz	N/A	N/A
192kHz	24.576MHz	36.864MHz	N/A	N/A	N/A	N/A

(N/A: Not available)

Table 3. System Clock Example (Auto Mode)

CKS2 pin	CKS1 pin	CKS0 pin	M/S Pin	MCLK Frequency
L	L	L	L	Quad Speed Mode
			H	128fs (108KHz < fs ≤ 216KHz)
L	L	H	L	Quad Speed Mode
			H	192fs (108KHz < fs ≤ 216KHz)
L	H	L	L	Normal Speed Mode
			H	256fs (8KHz ≤ fs ≤ 54KHz)
L	H	H	L	Double Speed Mode
			H	256fs (54KHz < fs ≤ 108KHz)
H	L	L	L	Auto (8KHz ≤ fs ≤ 216KHz)
			H	Double Speed Mode
				384fs (54KHz < fs ≤ 108KHz)
H	L	H	L	Normal Speed Mode
			H	384fs (8KHz ≤ fs ≤ 54KHz)
H	H	L	L	Normal Speed Mode
			H	512fs (8KHz < fs ≤ 54KHz)
H	H	H	L	Normal Speed Mode
				768fs (8KHz ≤ fs ≤ 54KHz)

Table 4. MCLK Frequency

When changing MCLK frequency in master/slave mode, the AK5388A should reset by PDN pin = "L". (ex. 12.288MHz(@fs=48kHz) at CKS1 pin = CKS0 pin = "L".

■ Audio Interface Format

12 different audio data interface formats can be selected using the TDM1-0, M/S and DIF pins as shown in Table 5. The audio data format can be selected by the DIF pin. In all formats the serial data is MSB-first, 2's compliment format. The SDTO1/2 is clocked out on the falling edge of BICK.

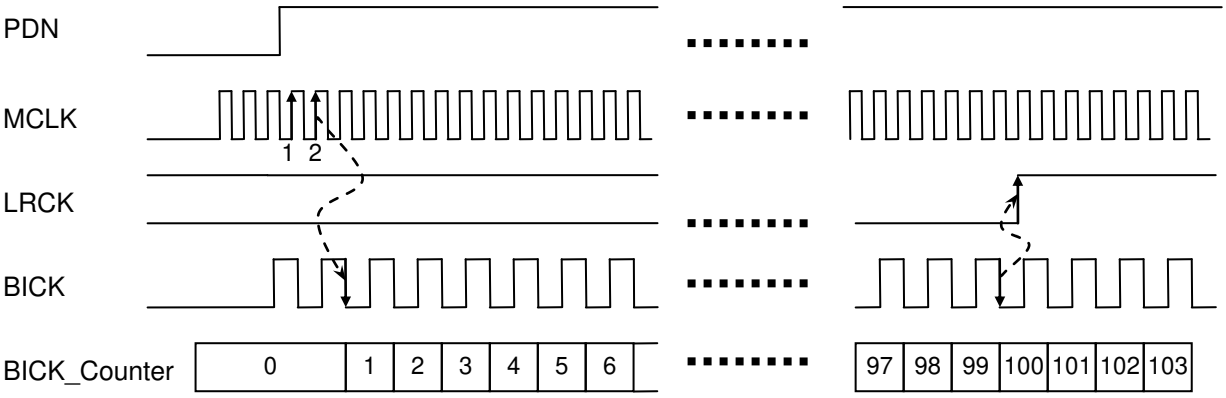
In normal mode, Mode 0-1 are the slave mode, and BICK is available up to 128fs at fs=48kHz. BICK outputs 64fs clock in Mode 2-3.

In TDM256 mode, all of the ADC's serial data (four channels) is output from the SDTO1 pins. The SDTO2 output is fixed to "L". BICK should be fixed to 256fs. In slave mode, "H" time and "L" time of LRCK should be at least 1/256fs. In master mode, "H" time ("L" time at I^2S mode) of LRCK is 1/8fs (typ). TDM256 mode only supports 48kHz sampling.

In TDM128 mode, all of the ADC's serial data (four channels) is output from the SDTO1 pin. The SDTO2 output is fixed to "L". BICK should be fixed to 128fs. In the slave mode, "H" time and "L" time of LRCK should be at least 1/128fs. In master mode, "H" time ("L" time at I^2S mode) of LRCK is 1/4fs (typ). TDM128 mode supports up to 192kHz sampling.

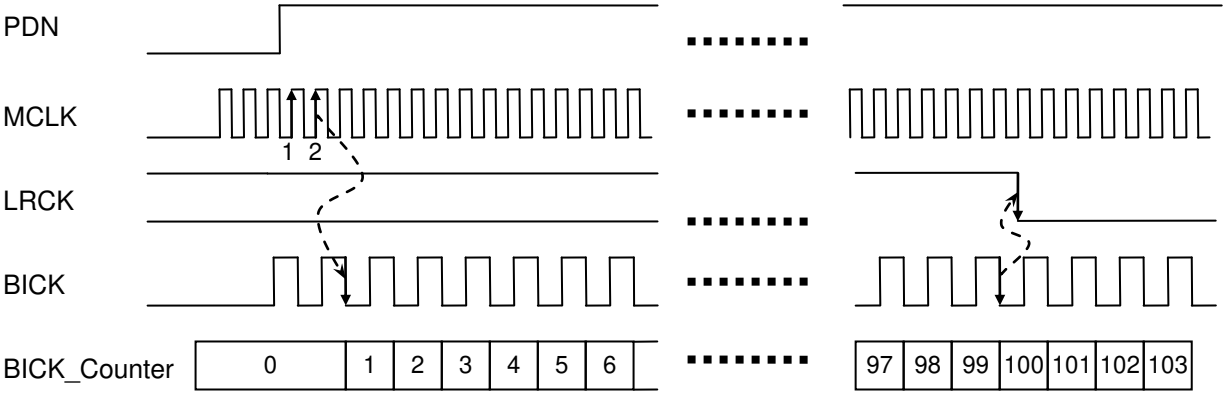
Cautions for when using TDM128 mode in slave mode

When setting the AK5388A to TDM128 mode while it is operated in slave mode, the BICK falling edge must not occur more than 100 times during the period from the second rising edge of MCLK after releasing a PDN reset to the first LRCK rising edge (in MSB justified) or falling edge (in I^2S compatible). The data to the SDTO1 pin may shift the timing against LRCK if BICK falls more than 123 times in this period. The AK5388A must be reset by the PDN pin when changing the clock frequency in TDM128 mode while it is operated in slave mode. When releasing this reset, BICK falling edge must also not occur more than 100 times during the period from the second rising edge of MCLK to the first LRCK rising edge (in MSB justified) or falling edge (in I^2S compatible).



BICK falling edge must be less than 100 times during the period from the second rising edge of MCLK after releasing PDN reset to the first rising edge of LRCK

Figure 10. Clock Input Timing (TDM128, Slave mode, MSB justified)



BICK falling edge must be less than 100 times during the period from the second rising edge of MCLK after releasing PDN reset to the first falling edge of LRCK

Figure 11. Clock Input Timing (TDM128, Slave mode, I^2S Compatible)

Mode		TDM1	TDM0	M/S	DIF	SDTO	LRCK		BICK	
								I/O		I/O
0	Normal	L	L	L	L	24bit, MSB justified	H/L	I	48-128fs	I
1					H	24bit, I^2S Compatible	L/H	I	48-128fs	I
2				H	L	24bit, MSB justified	H/L	O	64fs	O
3					H	24bit, I^2S Compatible	L/H	O	64fs	O
4	TDM256	L	H	L	L	24bit, MSB justified	↑	I	256fs	I
5					H	24bit, I^2S Compatible	↓	I	256fs	I
6				H	L	24bit, MSB justified	↑	O	256fs	O
7					H	24bit, I^2S Compatible	↓	O	256fs	O
8	TDM128	H	H	L	L	24bit, MSB justified	↑	I	128fs	I
9					H	24bit, I^2S Compatible	↓	I	128fs	I
10				H	L	24bit, MSB justified	↑	O	128fs	O
11					H	24bit, I^2S Compatible	↓	O	128fs	O
12	N/A	H	L	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 5. Audio Interface Formats (N/A: Not available)

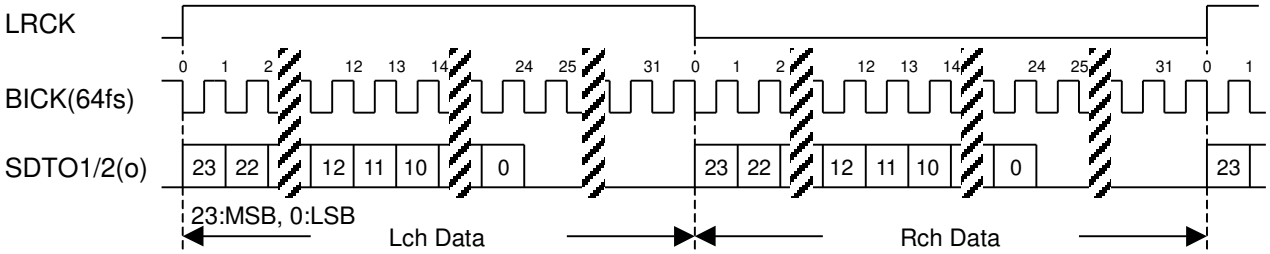


Figure 12. Mode 0/2 Timing (Normal mode, MSB justified)

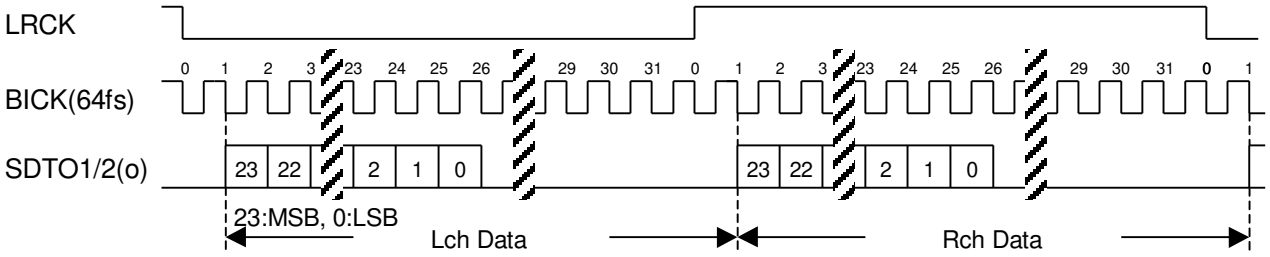


Figure 13. Mode 1/3 Timing (Normal mode, I^2S Compatible)

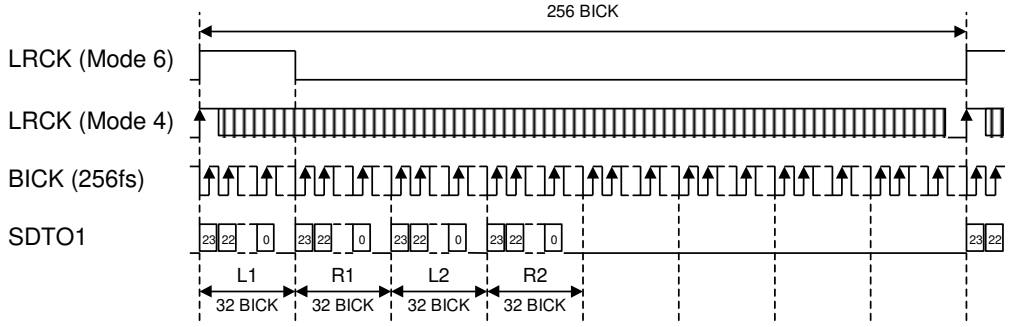


Figure 14. Mode 4/6 Timing (TDM256 mode, MSB justified)

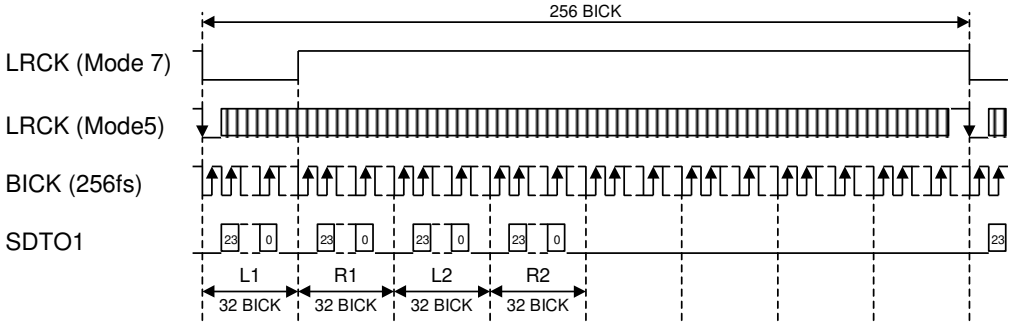


Figure 15. Mode 5/7 Timing (TDM256 mode, I^2S Compatible)

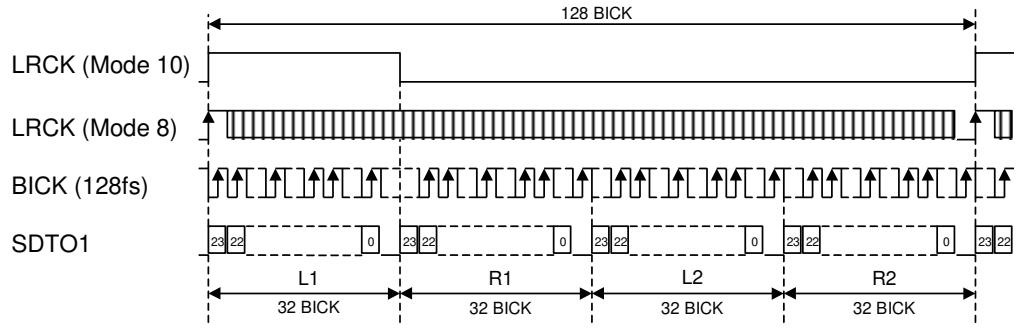


Figure 16. Mode 8/10 Timing (TDM128 mode, MSB justified)

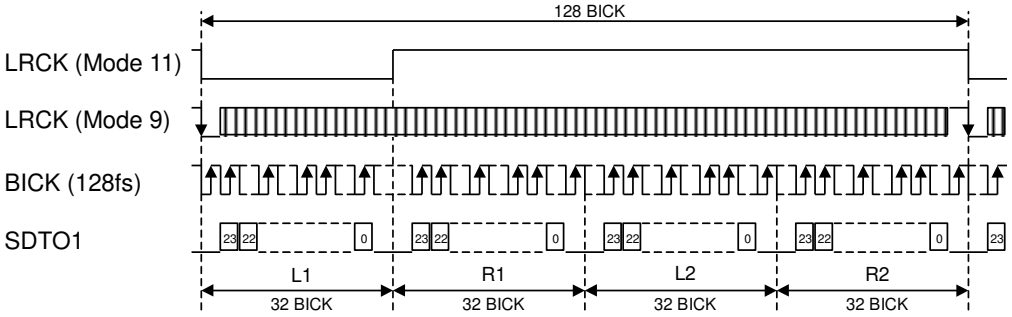


Figure 17. Mode 9/11 Timing (TDM128 mode, I^2S Compatible)

■ Digital High Pass Filter (HPF)

The ADC has a digital high pass filter for DC offset cancellation. The HPF is controlled by the HPFE pin. If the HPF setting (ON/OFF) is changed during operation, a click noise occurs due to the change in DC offset. The HPF setting should only be changed when the PDN pin = "L".

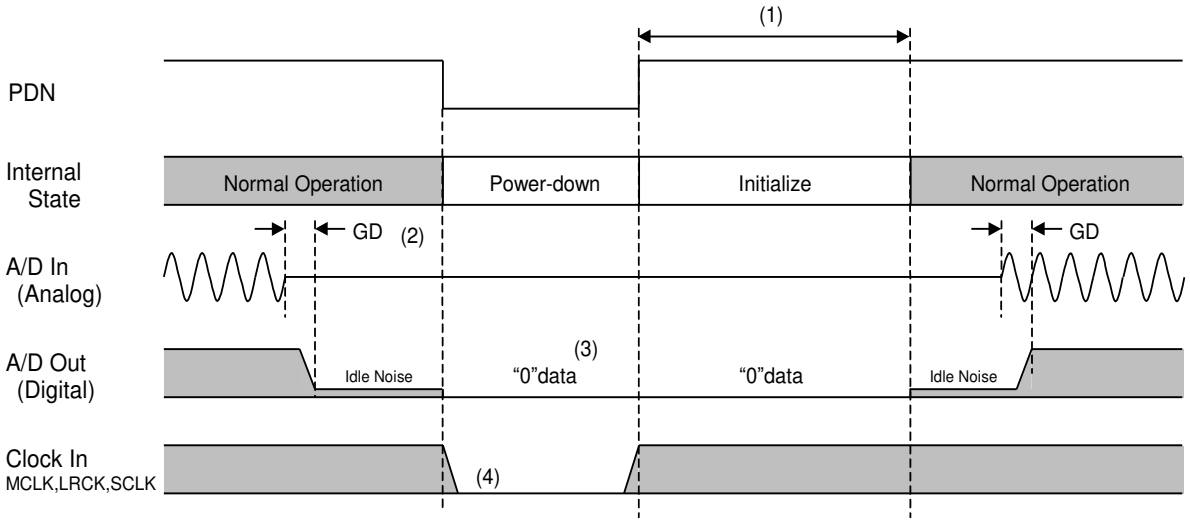
■ Overflow Detection

The AK5388A has an overflow detect function for the analog input. The OVF pin goes to "H" if either channel overflows (more than –0.3dBFS). OVF output for overflowed analog input has the same group delay as the ADC (GD=13/fs=0.27ms@fs=48kHz). OVF is "L" for 516/fs (=10.75ms@fs=48kHz) after the PDN pin = "↑", and then overflow detection is enabled.

■ Power Down and Reset

The AK5388A is placed in the power-down mode by bringing PDN pin "L" and the digital filter is also reset at the same time. This reset should always be done after power-up. In the power-down mode, the VCOM is AGND level. An analog initialization cycle starts after exiting the power-down mode. The output data SDTO is valid after 516 cycles of LRCK clock in master mode (517 cycles in slave mode). During initialization, the ADC digital data outputs of both channels are forced to "0". The ADC outputs settle to data correspondent to the input signals after the end of initialization (Settling takes approximately the group delay time).

The AK5388A should be reset once by bringing the PDN pin "L" after power-up. The internal timing starts clocking by the rising edge (falling edge at Mode 1) of LRCK after exiting from reset and power down state by MCLK.



Notes:
(1) 517/fs in slave mode and 516/fs in master mode.
(2) Digital output corresponding to analog input has group delay (GD).
(3) A/D output is "0" data in power-down state.
(4) When the external clocks (MCLK, SCLK, LRCK) are stopped, the AK5388A should be in the power-down state.

Figure 18. Power-down/up sequence example

■ Cascade TDM Mode

The AK5388A supports cascading of up to two devices in a daisy chain configuration in TDM256 mode. In this mode, SDTO1 pin of device #1 is connected to TDMIN pin of device #2. The SDTO1 pin of device #2 can output 8-chnnels of TDM data multiplexed with 4-chnnel of TDM data from device #1 and 4-channel of TDM data from device #2. Figure 19 shows a connection example of a daisy chain.
When using two AK5388A's in slave mode by cascade connection, the internal timing between device #1 and #2 may differ for 1MCLK clock cycle. BICK falling edge must me more than ±10ns from a MICK rising edge to prevent this phase difference between two devices. (Table 6)
BICK must be divided by two on a MCLK falling edge (Figure 21) when MCLK=2 x BICK (Normal speed 512fs mode or Double speed 256fs mode), and BICK must be in-phase signal to MCLK (Figure 22) when MCLK = BICK (Normal speed 256fs mode or Quad speed 128fs mode) to achieve this internal timing synchronization.

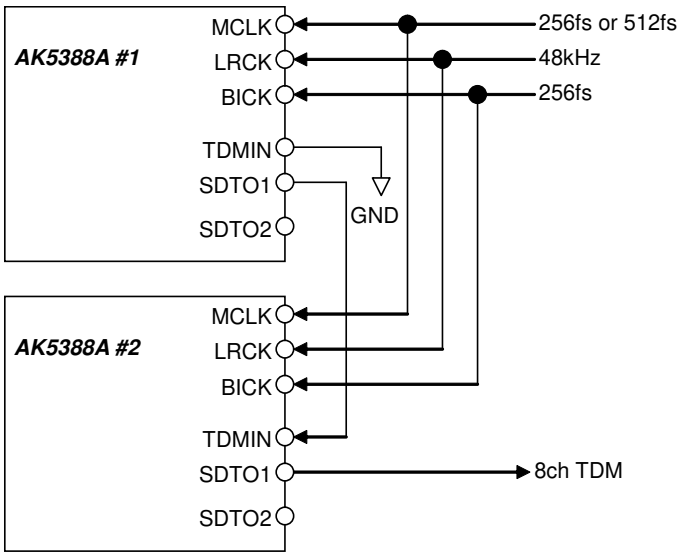


Figure 19. Cascade TDM Connection Diagram

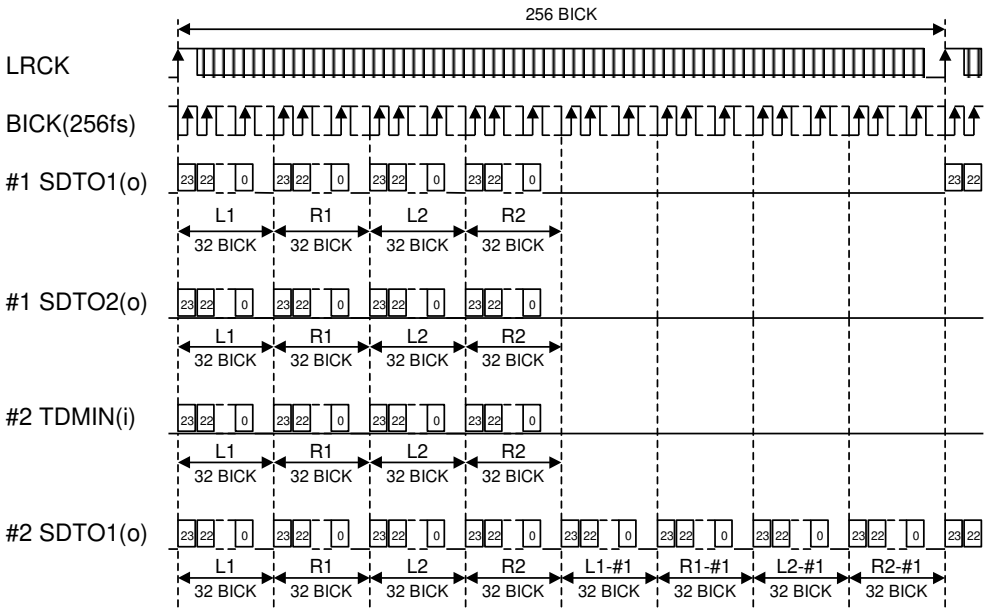


Figure 20. Cascade TDM Timing

Parameter	Symbol	min	typ	max	Units
MCLK "↑" to BICK "↓" BICK "↓" to MCLK"↑"	tMCB tBIM	10 10			ns ns

Table 6 TDM Mode Clock Timing

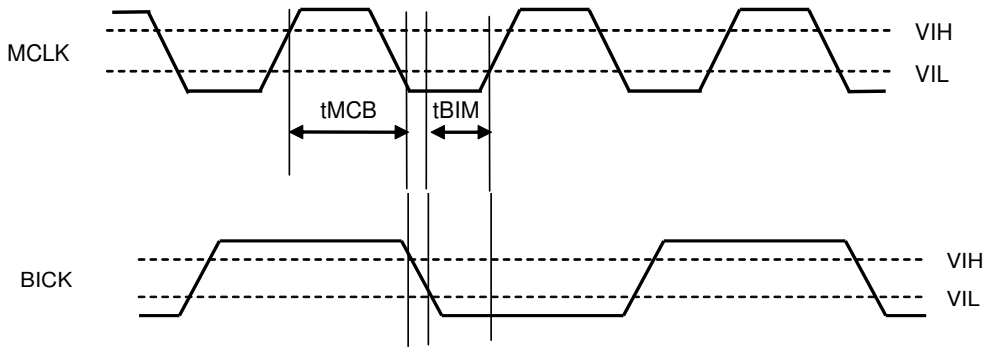


Figure 21. Audio Interface timing (Slave mode, TDM0 Mode MCLK=2 x BICK)

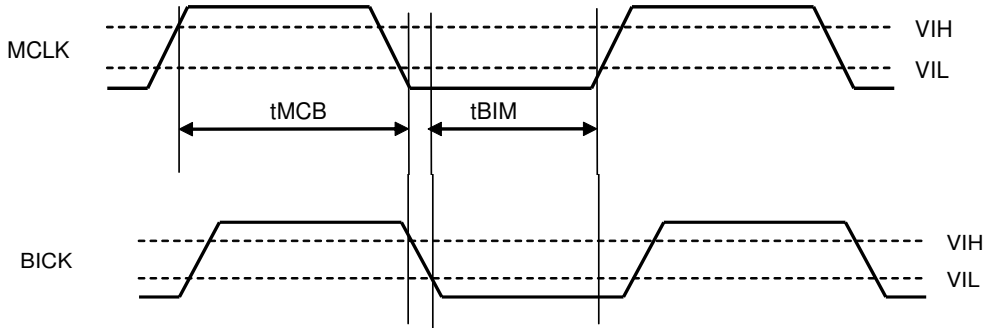


Figure 22. Audio Interface Timing (Slave mode, TDM0 Mode MCLK=BICK)

■ Mono Mode

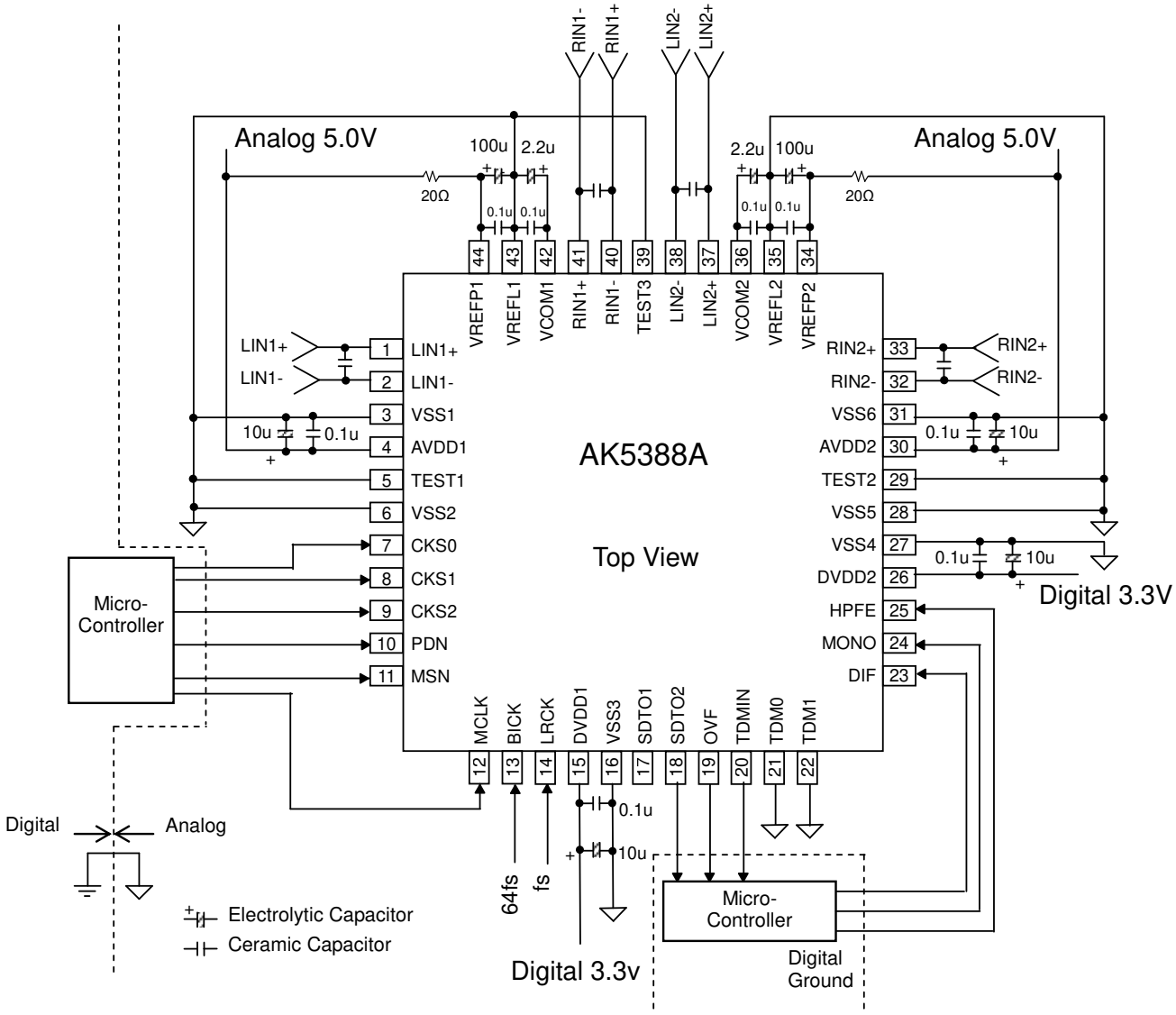
When the MONO pin is set to "H", the AK5388A is in Mono mode. In this mode, dynamic range and S/N can be improved by approximately 3dB when the same analog signal is inputted to LIN1 and RIN1, LIN2 and RIN2. The LIN1 and RIN1 data are summed and the amplitude is attenuated into half to be output from the SDTO1 pin. The LIN2 and RIN2 data are summed and the amplitude is attenuated into half to be output from the SDTO2 pin.

MONO pin	SDTO1/2 Output Data
L	Stereo Mode
H	Mono Mode

Table 7. Setup of MONO mode

SYSTEM DESIGN

Figure 23 and Figure 24 show the system connection diagram. The evaluation board demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



Note:

- VSS1-6 should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- All digital input pins should not be left floating.

Figure 23. Typical Connection Diagram