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AK5522

Differential Input Stereo 32-bit ΔΣ ADC with Excellent PSRR

1. General Description

The AK5522 is a 32-bit, from 8kHz to 192kHz sampling A/D converter for line and microphone inputs of digital audio systems. It achieves 108dB dynamic range and 98dB S/(N+D) while keeping low power consumption performance. Four types of digital filters are integrated and selectable according to the sound quality preference.

The AK5522 has great power supply rejection ratio, (PSRR), and common mode rejection ratio, (CMRR), enabling to maintain sufficient characteristics when connecting USB bus power or DCDC converter output as a power supply. It is suitable for applications with noisy power supply such as USB audio interface, wireless speakers and car audio equipment.

In addition, the AK5522 integrates a regulator with high PSRR for DAC power supply. Using the AK5522 with a DAC such as the AK4432 or the AK4452, it is enable to bring maximum DAC performance even in a poor power supply condition. Moreover, the AK5522 integrates low-jitter PLL circuit that generates a master clock for DAC from LRCK or BICK. It provides a low-EMI solution by avoiding unnecessary drawing of the master clock that has high frequency, on the board.

The AK5522 helps reducing components and a mounting space with these features for environmental noise.

2. Features

- ☐ **Sampling Rate:** 8kHz - 192kHz
- ☐ **Input:** Full Differntial, Pseudo Differential, Single-Ended
- ☐ **S/(N+D):** 98dB typ.
- ☐ **DR, S/N:** 108dB typ.
- ☐ **PSRR:** 80dB typ.
- ☐ **CMRR:** 80dB typ.
- ☐ **Internal Filter:** Four types of LPF, Digital HPF
- ☐ **Short Group Delay:** 4.4/fs (Short Delay Slow roll-off)
- ☐ **Output Format:** 32-bit MSB justified, I^2S or TDM (Cascade Connection available)
- ☐ **Operation Mode:** Master or Slave Modes
- ☐ **Programmable Gain Amp:** –3dB - +12dB/1dB (Fixed at 0dB in Parallel Control mode)
- ☐ **Integrated PLL:** Generates the master clock from BICK or LRCK
- ☐ **Master Clock Output:** Output master clock generated by the PLL
- ☐ **Voltage Regulator for External DAC Power:** Generates 3.3V from 5V applied to AVDD pin.
- ☐ **Power Supply:** Analog 4.5 - 5.5V or 3.0 - 3.6V, Digital 3.0 - 3.6V or 1.7 - 1.98V
- ☐ **Control Mode:** Parallel Control mode (Pin setting)
  Serial Control mode (I^2C Bus setting)
- ☐ **Power Consumption:** 76 mW (@AVDD=5.0V, DVDD=3.3V, fs=48kHz)
- ☐ **Operation Temperature:** –40 - 105°C
- ☐ **Package:** 24-pin QFN 4mmx4mm, 0.5mm pitch

3. Table of Contents

4. Block Diagram

■ Block Diagram

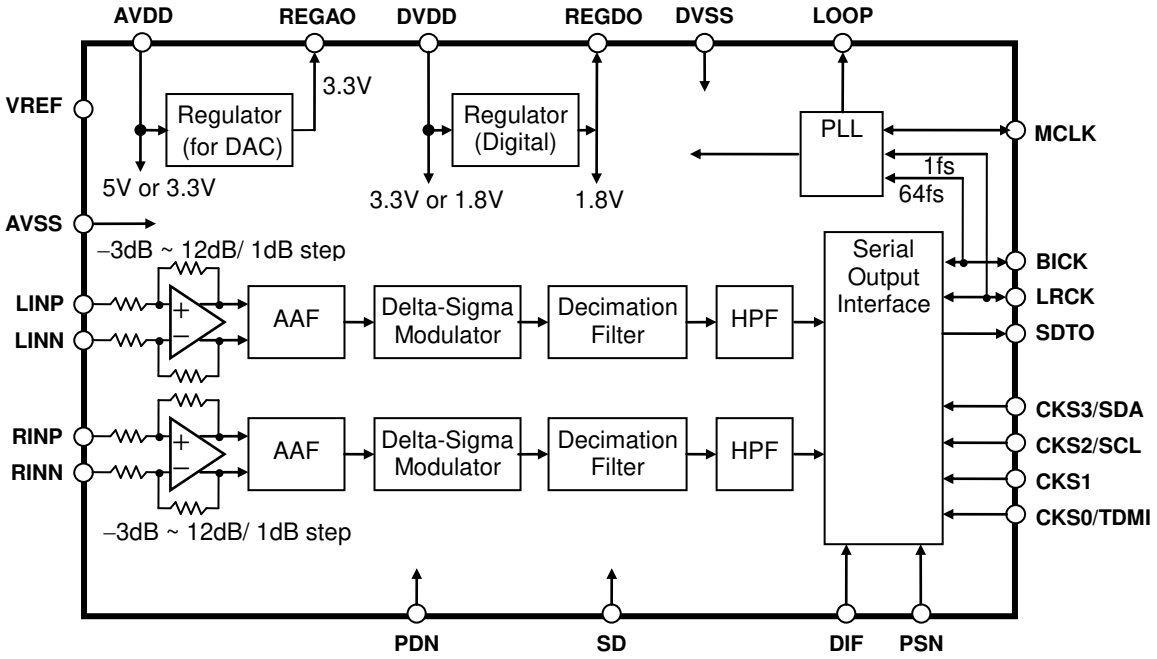

Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations

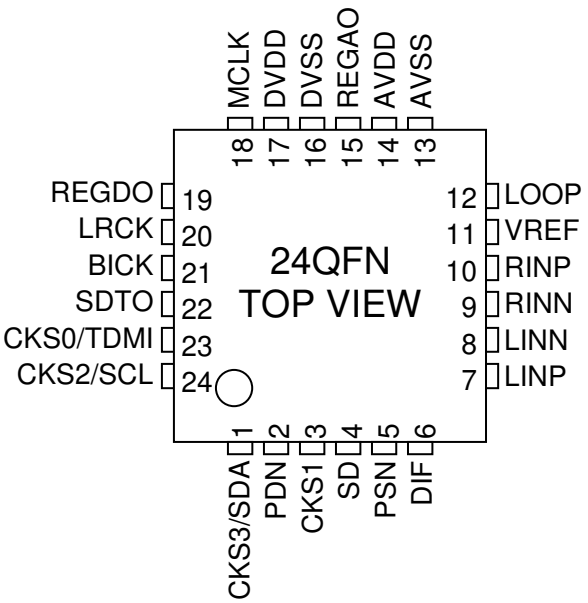

Figure 2. Pin Configurations

■ Pin Functions

No.	Pin Name	I/O	Function	Power Down Status
1	CKS3	I	Clock Mode Select Pin in Parallel Control mode	Hi-Z
	SDA	IO	Control Data I/O Pin for I^2C Bus in Serial Control mode	Hi-Z
2	PDN	I	Reset and Power Down Pin	Hi-Z
3	CKS1	I	Clock Mode Select Pin	Hi-Z
4	SD	I	Digital Filter Select Pin in Parallel Control mode "L": Sharp Roll-Off, "H": Short Delay Sharp Roll-Off	Hi-Z
5	PSN	I	Control Mode Select Pin "L": Serial Control mode, "H": Parallel Control mode	Hi-Z
6	DIF	I	Data Format Select Pin in Parallel Control mode "L": MSB Justified, "H": I^2S Compatible	Hi-Z
7	LINP	I	L Channel Positive Signal Input Pin	Hi-Z
8	LINN	I	L Channel Negative Signal Input Pin	Hi-Z
9	RINN	I	R Channel Negative Signal Input Pin	Hi-Z
10	RINP	I	R Channel Positive Signal Input Pin	Hi-Z
11	VREF	O	Internal Reference Voltage Decoupling Pin Decouple this pin to AVSS with a 1μF±50% capacitor.	Hi-Z, Pulled-down with 0.7kΩ
12	LOOP	O	PLL Loop Filter Connect Pin Connect this pin to AVSS with a 0.01μF±50% capacitor.	Hi-Z
13	AVSS	P	Analog Ground Pin	-
14	AVDD	P	Analog Power Supply Pin. 3.0 - 3.6V or 4.5 - 5.5V	-
15	REGAO	O	Regulator for External DAC Output Pin AVDD=4.5V - 5.5V: 3.3V typ. AVDD=3.0V - 3.6V: Low (External capacitor is not necessary) Connect to AVSS with a 10μF±50% capacitor. Additionally, this pin must be decoupled to the power supply pin of an external DAC with a 10μF±50% and a 0.1μF±50% capacitors in parallel. (Figure 81, Figure 82)	Hi-Z, Pulled-down with 0.5kΩ
16	DVSS	P	Digital Ground Pin	-
17	DVDD	P	Digital Power Supply Pin. 3.0 - 3.6V	-
18	MCLK	I	Master Clock Input Pin in EXT Master / EXT Slave / PLL Master mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	Hi-Z (Input mode)
		O	Master Clock Output Pin in PLL Slave mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	
19	REGDO	O	Regulator Stabilization Capacitor Connect Pin DVDD=3.0V - 3.6V: Output 1.8V typ. Connect to DVSS with a 1μF±50% capacitor.	Hi-Z
		I	DVDD=1.7V - 1.98V: Connect to DVDD	-
20	LRCK	I	Channel Clock Input Pin in Slave mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	Hi-Z (Input mode)
		O	Channel Clock Output Pin in Master mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	
21	BICK	I	Audio Serial Data Clock Input Pin in Slave mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	Hi-Z (Input mode)
		O	Audio Serial Data Clock Output Pin in Master mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	
22	SDTO	O	Audio Serial Data Output Pin	L
23	CKS0	I	Clock Mode Select Pin in Parallel Control mode	Hi-Z
	TDMI	I	TDM Data Input Pin in TDM mode	Hi-Z
24	CKS2	I	Clock Mode Select Pin in Parallel Control mode	Hi-Z
	SCL	I	Control Clock Input Pin for I^2C Bus in Serial Control mode	Hi-Z

I/O I: Input, O: Output, IO: Input and Output, P: Power Supply

Note 1. All digital input pins must not be allowed to float.

■ Handling of Unused Pin

The unused I/O pins should be connected appropriately.

Classification	Pin Name	Setting
Analog	LINP, LINN, RINP, RINN	Open
	REGAO (AVDD = 4.5V - 5.5V, Regulator for DAC = Enable)	Decouple with a 10 μF capacitor to AVSS
	REGAO (AVDD = 4.5V - 5.5V, Regulator for DAC = Disable)	Open
	REGAO (AVDD = 3.0V - 3.6V)	Open
	LOOP	Open
Digital	CKS1, CKS0, SD, DIF (Serial Control mode)	Connect to DVSS
	TDMI (TDM mode)	Connect to DVSS
	MCLK (PLL Slave mode)	Open

6. Absolute Maximum Ratings

(AVSS=DVSS=0V; Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog (AVDD pin) Digital (DVDD pin) Digital (REGDO pin)	VA VD VRD	−0.3 −0.3 −0.3	6.0 6.0 2.5	V V V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
Analog Input Voltage (LINP/N, RINP/N pins) (Note 3)		VINA	VDM−0.3	VDP+0.3 or 6.0 (Note 4)	V
Digital Input Voltage (Note 5)		VIND	−0.3	VD+0.3 or 6.0 (Note 6)	V
Ambient Temperature (Power applied)		Ta	−40	105	°C
Storage Temperature		Tstg	−65	150	°C

Note 2. All voltages with respect to ground.
Note 3. VDM and VDP are the voltages generated internally.
Note 4. The maximum value of input voltage is lower value between (VDP+0.3) V or 6.0 V.
Note 5. PDN, SD, LRCK, BICK, MCLK, PSN, CKS0/TDMI, CKS1, CKS2/SCL, CKS3/SDA and DIF pins
Note 6. The maximum value of input voltage is lower value between (VD+0.3) V or 6.0 V.

Mode	AVDD	VDM	VDP
Power-down	3.0 - 3.6V, 4.5 - 5.5V	AVSS	AVDD
Normal operation	4.5 - 5.5V	−0.75V	5.25V
	3.0 - 3.6V	−1.50V	4.50V

Table 1. VDM, VDP Voltage

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(AVSS=DVSS=0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog (AVDD)	VA	4.5	5.0	5.5	V
	Analog (AVDD)	VA	3.0	3.3	3.6	V
	Using internal regulator Digital (DVDD)	VD	3.0	3.3	3.6	V
	Not using internal regulator Digital (DVDD) Digital (REGDO)	VD VRD	1.7	1.8	1.98	V

Note 2. All voltages with respect to ground.
Note 7. The power up sequence between AVDD and DVDD is not critical. If DVDD is 1.7V to 1.98V then the DVDD pin should be connect to the REGDO pin.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Analog Characteristics

■ Analog Power Supply=5.0V

(Ta=25°C; AVDD=5.0V; DVDD=3.3V, fs=48kHz, 96kHz; 192kHz, BICK=64fs; Signal Frequency=1kHz; 32-bit Data; Measurement frequency=20Hz - 20kHz at fs=48kHz, 40Hz - 40kHz at fs=96kHz and 192kHz, Gain=0dB, unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Analog Input Characteristics:						
Resolution (Note 8)			-	-	32	Bit
Input Voltage			2.0	2.1	2.2	Vrms
S/(N+D)	fs=48kHz BW=20kHz	−1dBFS	92	98	-	dB
		−20dBFS	-	86	-	dB
		−60dBFS	-	46	-	dB
	fs=96kHz BW=40kHz	−1dBFS	-	97	-	dB
		−20dBFS	-	83	-	dB
		−60dBFS	-	43	-	dB
	fs=192kHz BW=40kHz	−1dBFS	-	97	-	dB
		−20dBFS	-	83	-	dB
		−60dBFS	-	43	-	dB
Dynamic Range (−60dBFS with A-weighted)	fs=48kHz, BW=20kHz		103	108	-	dB
Dynamic Range (−60dBFS)	fs=96kHz, 192kHz, BW=40kHz		98	103	-	dB
S/N (A-weighted)	fs=48kHz, BW=20kHz		103	108	-	dB
S/N	fs=96kHz, 192kHz, BW=40kHz		98	103	-	dB
Input Resistance	Full Differential	Gain= +12dB	5	8.5	-	kΩ
		0dB	10	20.7	-	kΩ
		−3dB	10	23.8	-	kΩ
	Pseudo Differential Single End	Gain= +12dB	5	14.0	-	kΩ
		0dB	10	27.3	-	kΩ
		−3dB	10	30.3	-	kΩ
Interchannel Isolation			110	120		dB
Interchannel Gain Mismatch			-	0	0.5	dB
Power Supply Rejection Ratio (PSRR) (Note 9)			-	80	-	dB
Common Mode Rejection Ratio (CMRR)			55	80	-	dB
VREF pin Output Voltage			3.72	3.92	4.12	V
Regulator for External DAC						
Output Voltage			3.0	3.3	3.6	V
Output Current			-	-	15	mA
Power Supply Rejection Ratio (Note 9)			-	80	-	dB
Output Noise (Flat)			-	−101	-	dBV
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = “H”) (Note 10)						
AVDD			-	12	18	mA
DVDD	(fs=48kHz)		-	4.7	8	mA
DVDD	(fs=96kHz)		-	8.1	13	mA
DVDD	(fs=192kHz)		-	7.6	12	mA
Power down mode (PDN pin = “L”) (Note 11)						
AVDD+DVDD			-	0	10	μA

Note 8. ADC full-scale input voltage at Gain=0dB. The signal input amplitude can’t exceed 2.1Vrms (typ.) even if the gain is from −3dB to −1dB.

Note 9. PSRR is applied to AVDD, DVDD with 20Hz - 20kHz sine wave.

Note 10. PLL Master mode. PLL3-0 bits = “0101b”

Note 11. All digital inputs are fixed to DVDD or DVSS.

■ Analog Power Supply=3.3V

(Ta=25°C; VA=3.3V; VD=3.3V, fs=48kHz, 96kHz, 192kHz, BICK=64fs; Signal Frequency=1kHz; 32-bit Data; Measurement frequency=20Hz - 20kHz at fs=48kHz, 40Hz - 40kHz at fs=96kHz and 192kHz, Gain=0dB, unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Analog Input Characteristics:						
Resolution			-	-	32	Bit
Input Voltage		(Note 8)	2.0	2.1	2.2	Vrms
S/(N+D)	fs=48kHz BW=20kHz	−1dBFS	87	93	-	dB
		−20dBFS	-	83	-	dB
		−60dBFS	-	43	-	dB
	fs=96kHz BW=40kHz	−1dBFS	-	92	-	dB
		−20dBFS	-	80	-	dB
		−60dBFS	-	40	-	dB
	fs=192kHz BW=40kHz	−1dBFS	-	92	-	dB
		−20dBFS	-	80	-	dB
		−60dBFS	-	40	-	dB
Dynamic Range (−60dBFS with A-weighted)	fs=48kHz, BW=20kHz		99	104	-	dB
Dynamic Range (−60dBFS)	fs=96kHz, 192kHz, BW=40kHz		94	99	-	dB
S/N (A-weighted)	fs=48kHz, BW=20kHz		99	104	-	dB
S/N	fs=96kHz, 192kHz, BW=40kHz		94	99	-	dB
Input Resistance	Full Differential	Gain= +12dB	5	12.0	-	kΩ
		0dB	10	25.2	-	kΩ
		−3dB	10	29.4	-	kΩ
	Pseudo Differential Single End	Gain= +12dB	5	18.4	-	kΩ
		0dB	10	30.9	-	kΩ
		−3dB	10	32.4	-	kΩ
Interchannel Isolation			110	120		dB
Interchannel Gain Mismatch			-	0	0.5	dB
Power Supply Rejection Ratio		(Note 9)	-	80	-	dB
Common Mode Rejection Ratio (CMRR)			55	80	-	dB
VREF pin Output Voltage			2.34	2.47	2.60	V
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = “H”)		(Note 10)				
AVDD			-	11	16	mA
DVDD	(fs=48kHz)		-	4.7	8	mA
DVDD	(fs=96kHz)		-	8.1	13	mA
DVDD	(fs=192kHz)		-	7.6	12	mA
Power down mode (PDN pin = “L”)		(Note 11)				
AVDD+DVDD			-	0	10	μA

Note 8. ADC full-scale input voltage at Gain=0dB. The signal input amplitude can’t exceed 2.1Vrms (typ.) even if the gain is from −3dB to −1dB.
Note 9. PSRR is applied to AVDD, DVDD with 20Hz - 20kHz sine wave.
Note 10. PLL Master mode. PLL3-0 bits = “0101b”
Note 11. All digital inputs are fixed to DVDD or DVSS.

9. Filter Characteristics

■ ADC Filter Characteristics (fs= 48kHz)

(Ta= −40 - +105°C, AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 3) (Parallel Control mode: SD pin="L", Serial Control mode: SD bit="0", SLOW bit="0")						
Passband (Note 12)	+0.001/−0.06dB −6.0dB	PB	0 -	- 24.4	22.0 -	kHz kHz
Stopband (Note 12)		SB	27.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	18.8	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 4) (Parallel Control mode: Not Available, Serial Control mode: SD bit="0", SLOW bit="1")						
Passband (Note 12)	+0.001/−0.076dB −6.0dB	PB	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 12)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	6.7	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (Figure 5) (Parallel Control mode: SD pin="H", Serial Control mode: SD bit="1", SLOW bit="0")						
Passband (Note 12)	+0.001/−0.06dB −6.0dB	PB	0 -	- 24.4	22.0 -	kHz kHz
Stopband (Note 12)		SB	27.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	-	2.8	1/fs
Group Delay (Note 13)		GD	-	4.9	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (Figure 6) (Parallel Control mode: Not Available, Serial Control mode: SD bit="1", SLOW bit="1")						
Passband (Note 12)	+0.001/−0.076dB −6.0dB	PB -	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 12)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 13)		GD	-	4.4	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 12)	−3.0dB −0.5dB −0.1dB	FR	- - -	1.0 2.5 6.5	- - -	Hz Hz Hz

Note 12. The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/−0.06dB) =0.46 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/−0.076dB) =0.26 × fs (SLOW ROLL-OFF).

Note 13. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces. The signal frequency is 1kHz.

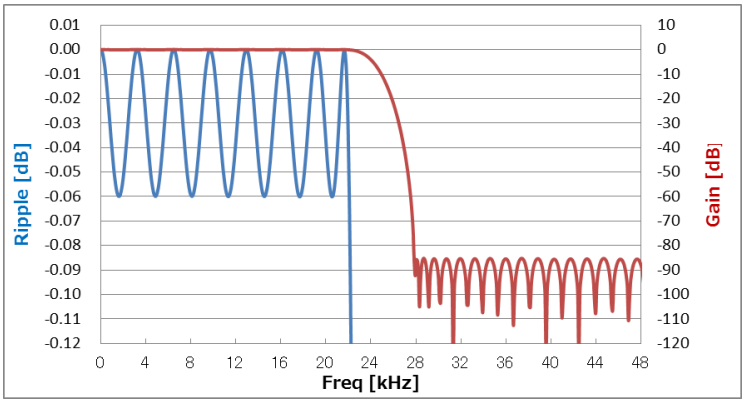

Figure 3. SHARP ROLL-OFF (fs=48kHz)

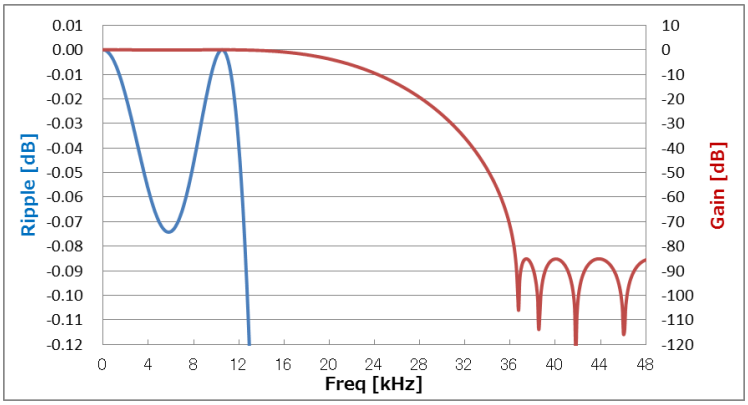

Figure 4. SLOW ROLL-OFF (fs=48kHz)

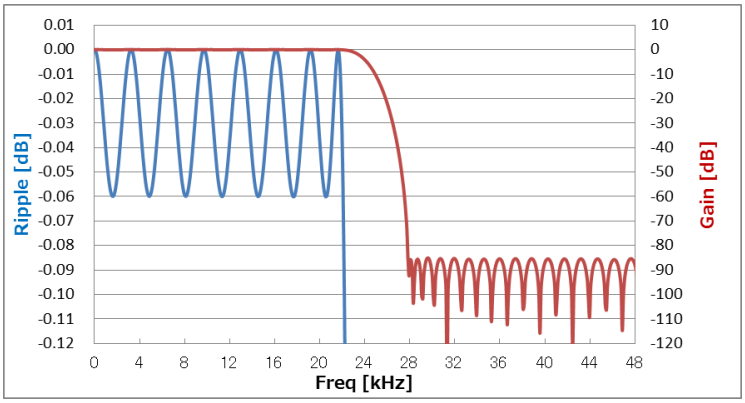

Figure 5. SHORT DELAY SHARP ROLL-OFF (fs=48kHz)

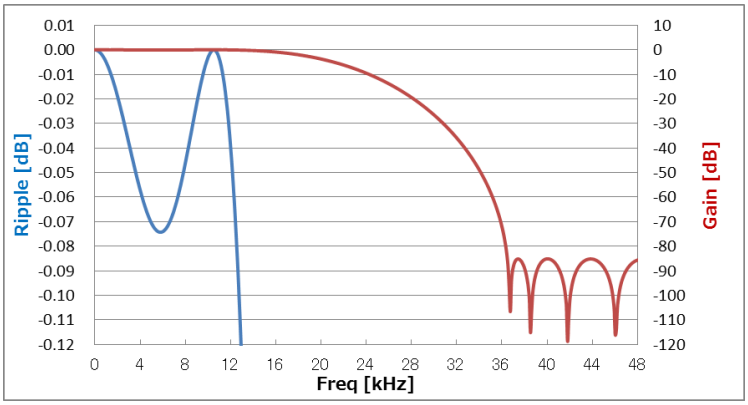

Figure 6. SHORT DELAY SLOW ROLL-OFF (fs=48kHz)

■ **ADC Filter Characteristics (fs= 96kHz)**

(Ta= −40 - +105°C, AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 7) (Parallel Control mode: SD pin="L", Serial Control mode: SD bit="0", SLOW bit="0")						
Passband (Note 12)	+0.001/−0.06dB −6.0dB	PB	0	- 48.8	44.1	kHz kHz
Stopband (Note 12)		SB	55.7	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	18.8	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 8) (Parallel Control mode: Not Available, Serial Control mode: SD bit="0", SLOW bit="1")						
Passband (Note 12)	+0.001/−0.076dB −6.0dB	PB	0 -	- 43.8	25	kHz kHz
Stopband (Note 12)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	6.7	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF (Figure 9) (Parallel Control mode: SD pin="H", Serial Control mode: SD bit="1", SLOW bit="0")						
Passband (Note 12)	+0.001/−0.06dB −6.0dB	PB	0 -	- 48.8	44.1 -	kHz kHz
Stopband (Note 12)		SB	55.7	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	2.8	1/fs
Group Delay (Note 13)		GD	-	4.9	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (Figure 10) (Parallel Control mode: Not Available, Serial Control mode: SD bit="1", SLOW bit="1")						
Passband (Note 12)	+0.001/−0.076dB −6.0dB	PB	0 -	- 43.8	25 -	kHz kHz
Stopband (Note 12)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 13)		GD	-	4.4	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 12)	−3.0dB −0.5dB −0.1dB	FR	- - -	1.0 2.5 6.5	- - -	Hz Hz Hz

Note 12. The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/−0.06dB) = 0.46 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/−0.076dB) = 0.26 × fs (SLOW ROLL-OFF).

Note 13. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces. The signal frequency is 1kHz.

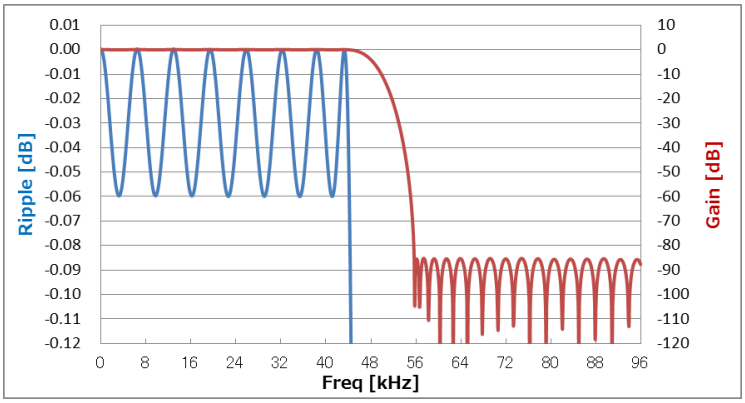

Figure 7. SHARP ROLL-OFF (fs=96kHz)

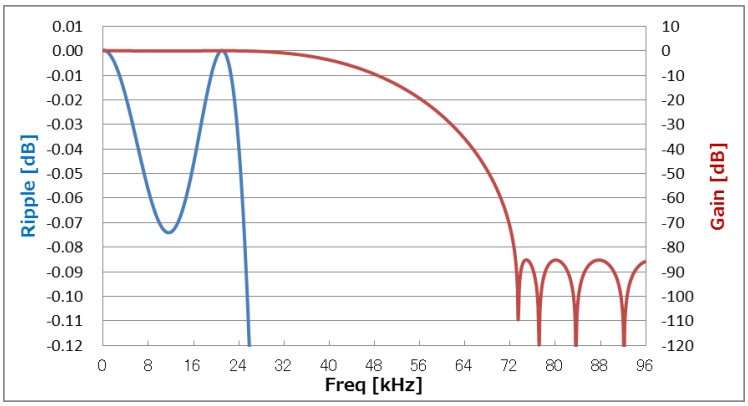

Figure 8. SLOW ROLL-OFF (fs=96kHz)

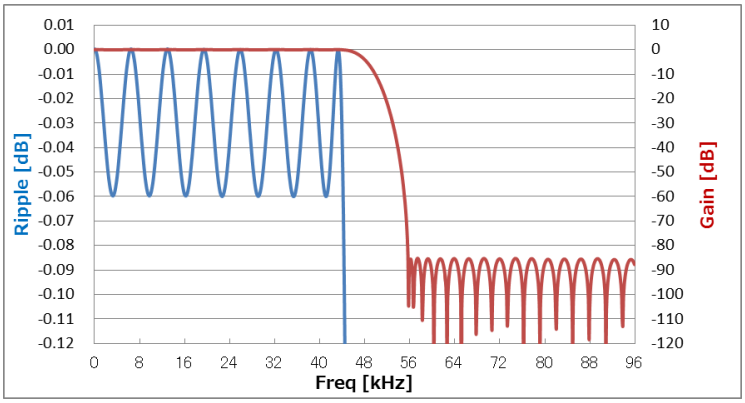

Figure 9. SHORT DELAY SHARP ROLL-OFF (fs=96kHz)

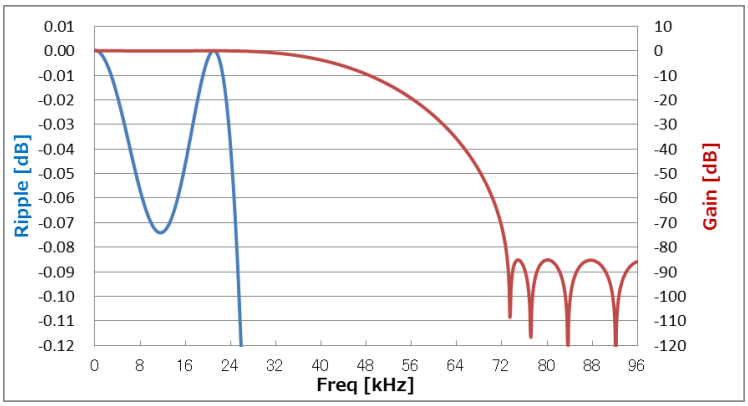

Figure 10. SHORT DELAY SLOW ROLL-OFF (fs=96kHz)

■ ADC Filter Characteristics (fs= 192kHz)

(Ta= −40 - +105°C, AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 11) (Parallel Control mode: SD pin="L", Serial Control mode: SD bit="0", SLOW bit="0")						
Passband (Note 12)	+0.001/−0.037dB −6.0dB	PB	0	- 100.2	83.7	kHz kHz
Stopband (Note 12)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	14.9	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 12) (Parallel Control mode: Not Available, Serial Control mode: SD bit="0", SLOW bit="1")						
Passband (Note 12)	+0.001/−0.1dB −6.0dB	PB	0	- 75.2	31.5	kHz kHz
Stopband (Note 12)		SB	146	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	7.9	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (Figure 13) (Parallel Control mode: SD pin="H", Serial Control mode: SD bit="1", SLOW bit="0")						
Passband (Note 12)	+0.001/−0.037dB −6.0dB	PB	0 -	- 100.2	83.7 -	kHz kHz
Stopband (Note 12)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	0.3	1/fs
Group Delay (Note 13)		GD	-	6.4	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF FILTER (Figure 14) (Parallel Control mode: Not Available, Serial Control mode: SD bit="1", SLOW bit="1")						
Passband (Note 12)	+0.001/−0.1dB −6.0dB	PB	0 -	- 75.2	31.5 -	kHz kHz
Stopband (Note 12)		SB	146	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	0.4	1/fs
Group Delay (Note 13)		GD	-	6.4	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 12)	−3.0dB −0.5dB −0.1dB	FR	- - -	1.0 2.5 6.5	- - -	Hz Hz Hz

Note 12. The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/−0.037dB) =0.436 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/−0.1dB) =0.164 × fs (SLOW ROLL-OFF).

Note 13. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces. The signal frequency is 1kHz.

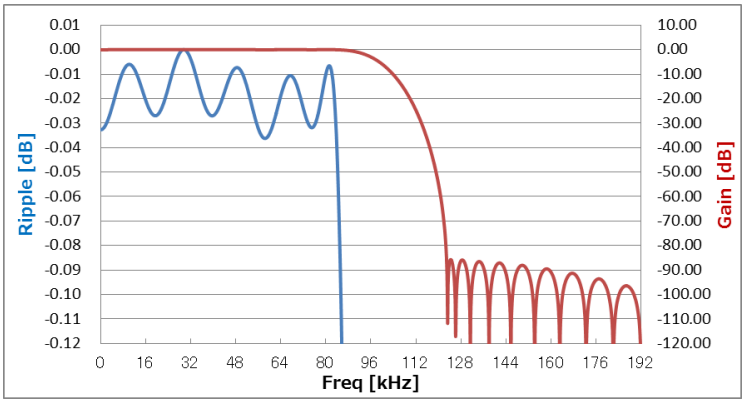

Figure 11. SHARP ROLL-OFF (fs=192kHz)

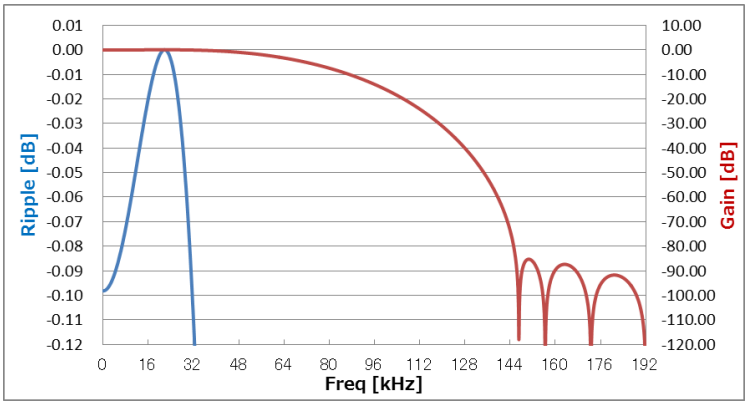

Figure 12. SLOW ROLL-OFF (fs=192kHz)

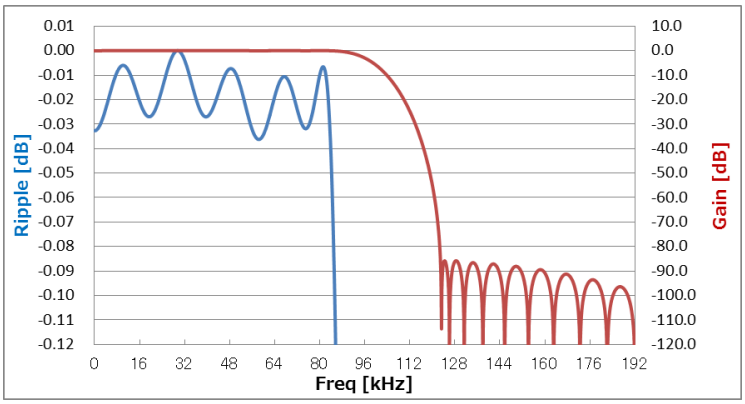

Figure 13. SHORT DELAY SHARP ROLL-OFF (fs=192kHz)

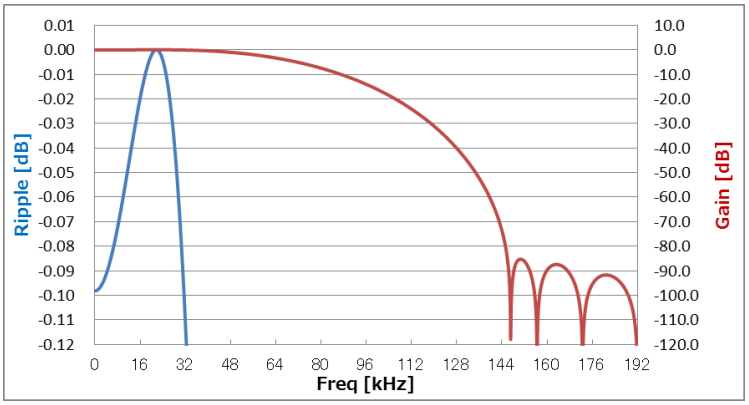

Figure 14. SHORT DELAY SLOW ROLL-OFF (fs=192kHz)

10. DC Characteristics

(Ta=−40 - 105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DVDD=1.7V - 1.98V					
High-Level Input Voltage (Note 14)	VIH	80%DVDD	-	-	V
Low-Level Input Voltage (Note 14)	VIL	-	-	20% DVDD	V
DVDD=3.0V - 3.6V					
High-Level Input Voltage (Note 14)	VIH	70% DVDD	-	-	V
Low-Level Input Voltage (Note 14)	VIL	-	-	30% DVDD	V
High-Level Output Voltage (Note 15) (Iout=−100μA)	VOH	DVDD −0.5	-	-	V
Low-Level Output Voltage (Note 15) (Iout= 100μA)	VOL	-	-	0.5	V
Low-Level Output Voltage (Note 16)	VOL				
(DVDD=1.7V - 1.98V: Iout=3mA)		-	-	20% DVDD	V
(DVDD=3.0V - 3.6V: Iout=3mA)		-	-	0.4	V
Input Leakage Current (Note 14)	Iin	-	-	±10	μA

Note 14. PDN, SD, LRCK (Slave mode), BICK (Slave mode), MCLK (Input), PSN, CKS0/TDMI, CKS1, CKS2/SCL, CKS3/SDA (Input), DIF

Note 15. SDTO, LRCK (Master mode), BICK (Master mode), MCLK (Output)

Note 16. SDA (Output)

11. Switching Characteristics (Parallel Control Mode)

■ System Clocks

□ External Master Mode (Parallel Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
MCLK=256fsn					
Frequency	fMCLK	2.048	-	13.824	MHz
Pulse Width Low	tMCLKL	32	-	-	ns
Pulse Width High	tMCLKH	32	-	-	ns
MCLK=512fsn, 256fsd, 128fsq					
Frequency	fMCLK	4.096	-	27.648	MHz
Pulse Width Low	tMCLKL	16	-	-	ns
Pulse Width High	tMCLKH	16	-	-	ns
LRCK Output Timing					
Stereo Mode					
Frequency (fs)					
Normal Speed	fsn				
MCLK 256fs, 512fs		8	-	54	kHz
Double Speed	fsd				
MCLK 256fs		54	-	108	kHz
Quad Speed	fsq				
MCLK 128fs		108	-	216	kHz
Duty Cycle	dLRCK	-	50	-	%
BICK Output Timing					
Stereo Mode					
Period	tBICK	-	1/(64fs)	-	s
Duty Cycle	dBICK	-	50	-	%

□ **External Slave Mode (Parallel Control Mode)**

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
MCLK=256fsn					
Frequency	fMCLK	2.048	-	13.824	MHz
Pulse Width Low	fMCLKL	29	-	-	ns
Pulse Width High	fMCLKH	29	-	-	ns
MCLK=384fsn					
Frequency	fMCLK	3.072	-	18.432	MHz
Pulse Width Low	fMCLKL	22	-	-	ns
Pulse Width High	fMCLKH	22	-	-	ns
MCLK=512fsn, 256fsd, 128fsq					
Frequency	fMCLK	4.096	-	27.648	MHz
Pulse Width Low	fMCLKL	15	-	-	ns
Pulse Width High	fMCLKH	15	-	-	ns
MCLK=768fsn, 384fsd, 192fsq					
Frequency	fMCLK	6.144	-	36.864	MHz
Pulse Width Low	fMCLKL	11	-	-	ns
Pulse Width High	fMCLKH	11	-	-	ns
LRCK Input Timing					
Stereo Mode					
Frequency (fs)					
Normal Speed	fsn				
MCLK 256fs, 512fs		8	-	54	kHz
MCLK 384fs, 768fs		8	-	48	kHz
MCLK 1024fs		8	-	32	kHz
Double Speed	fsd				
MCLK 256fs		54	-	108	kHz
MCLK 384fs		48	-	96	kHz
Quad Speed	fsq				
MCLK 128fs		108	-	216	kHz
MCLK 192fs		96	-	192	kHz
Duty Cycle	dLRCK	45	-	55	%
TDM256 Mode					
Frequency	fs				Hz
Normal Speed	fsn	8	-	48	kHz
Pulse Width Low	tLRCKL	1/(256fs)	-	-	s
Pulse Width High	tLRCKH	1/(256fs)	-	-	s
BICK Input Timing					
Stereo Mode					
Period	tBICK				
Normal Speed		1/(256fsn)	-	-	s
Double Speed		1/(128fsd)	-	-	s
Quad Speed		1/(64fsq)	-	-	s
Pulse Width Low	tBICKL	32	-	-	ns
Pulse Width High	tBICKH	32	-	-	ns
TDM256 Mode					
Period	tBICK	-	1/(256fs)	-	s
Pulse Width Low	tBICKL	14	-	-	ns
Pulse Width High	tBICKH	14	-	-	ns

□ PLL Slave Mode (PLL Reference Clock = BICK pin) (Parallel Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Output Timing					
Stereo Mode					
Frequency					
512fs	fMCLK	-	512fs	-	Hz
256fs		-	256fs	-	Hz
128fs		--	128fs	--	Hz
Duty Cycle	dMCLK	45	50	55	%
Pulse Width Low (@24.576MHz)	tMCLK20	16	-	-	ns
Pulse Width High (@24.576MHz)	tMCLK80	16	-	-	ns
LRCK Input Timing (Note 17)					
Stereo Mode					
Frequency (fs)					
Normal Speed	fsn				
MCLK 256fs, 512fs		-	44.1	-	kHz
		-	48	-	kHz
Double Speed	fsd				
MCLK 256fs		-	88.2	-	kHz
		-	96	-	kHz
Quad Speed	fsq				
MCLK 128fs		-	176.4	-	kHz
		-	192	-	kHz
Duty Cycle	dLRCK	45	-	55	%
BICK Input Timing					
Stereo Mode					
Period	tBICK	-	1/(64fs)	-	s
Pulse Width Low	tBICKL	0.4 x tBICK	-	-	s
Pulse Width High	tBICKH	0.4 x tBICK	-	-	s

Note 17. The PLL mode does not support variable pitch mode.

□ PLL Slave Mode (PLL Reference Clock = LRCK pin) (Parallel Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Output Timing					
Stereo Mode					
Frequency					
512fs	fMCLK	-	512fs	-	Hz
256fs		-	256fs	-	Hz
128fs		-	128fs	-	Hz
Duty Cycle	dMCLK	45	50	55	%
Pulse Width Low (@24.576MHz)	tMCLK20	16	-	-	ns
Pulse Width High (@24.576MHz)	tMCLK80	16	-	-	ns
LRCK Input Timing (Note 17)					
Stereo Mode					
Frequency (fs)					
Normal Speed	fsn				
MCLK 256fs, 512fs		-	44.1	-	kHz
		-	48	-	kHz
Double Speed	fsd				
MCLK 256fs		-	88.2	-	kHz
		-	96	-	kHz
Quad Speed	fsq				
MCLK 128fs		-	176.4	-	kHz
		-	192	-	kHz
Duty Cycle	dLRCK	45	-	55	%
BICK Input Timing					
Stereo Mode					
Period	tBICK				
Normal Speed		1/(256fsn)	-	-	s
Double Speed		1/(128fsd)	-	-	s
Quad Speed		1/(64fsq)	-	-	s
Pulse Width Low	tBICKL	0.4 x tBICK	-	-	s
Pulse Width High	tBICKH	0.4 x tBICK	-	-	s

Note 17. The PLL mode does not support variable pitch mode.

■ Audio Interface

□ External Master Mode (Parallel Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Stereo Mode					
Normal Speed , Double Speed, Quad Speed Mode					
DVDD=1.7V - 1.98V					
BICK "↓" to LRCK	tMBLR	−14	-	14	ns
LRCK to SDTO (MSB justified)	tLRS	−24	-	24	ns
BICK "↓" to SDTO	tBSD	−24	-	24	ns
DVDD=3.0V - 3.6V					
BICK "↓" to LRCK	tMBLR	−7	-	7	ns
LRCK to SDTO (MSB justified)	tLRS	−20	-	20	ns
BICK "↓" to SDTO	tBSD	−20	-	20	ns

□ PLL Slave Mode, External Slave Mode (Parallel Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Stereo Mode					
Normal Speed , Double Speed, Quad Speed Mode					
DVDD=1.7V - 1.98V					
LRCK to BICK "↑" (Note 18)	tLRB	58	-	-	ns
BICK "↑" to LRCK (Note 18)	tBLR	58	-	-	ns
LRCK to SDTO (MSB Justified)	tLRS	-	-	48	ns
BICK "↓" to SDTO	tSLR	-	-	48	ns
DVDD=3.0V - 3.6V					
LRCK to BICK "↑" (Note 18)	tLRB	33	-	-	ns
BICK "↑" to LRCK (Note 18)	tBLR	33	-	-	ns
LRCK to SDTO (MSB Justified)	tLRS	-	-	28	ns
BICK "↓" to SDTO	tSLR	-	-	28	ns
TDM256 Mode					
Normal Speed Mode					
LRCK to BICK "↑" (Note 18)	tLRB	23	-	-	ns
BICK "↑" to LRCK (Note 18)	tBLR	23	-	-	ns
BICK "↑" to SDTO	tBSDD	5	-	36	ns
TDMI Setup time to BICK "↑"	tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"	tSDH	5	-	-	ns

Note 18. BICK rising edge must not occur at the same time as LRCK edge.

■ Power-down, Reset (Parallel Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 19)	tPD	150	-	-	ns
PDN Reject Pulse Width	tRPD	-	-	30	ns

Note 19. The AK5522 can be reset by setting the PDN pin to “L” upon power-up. The PDN pin must held “L” for more than 150ns for a certain reset. The AK5522 is not reset by the “L” pulse less than 30ns.

■ Timing Diagram (Parallel Control Mode)

Clock Timings (Parallel Control Mode)

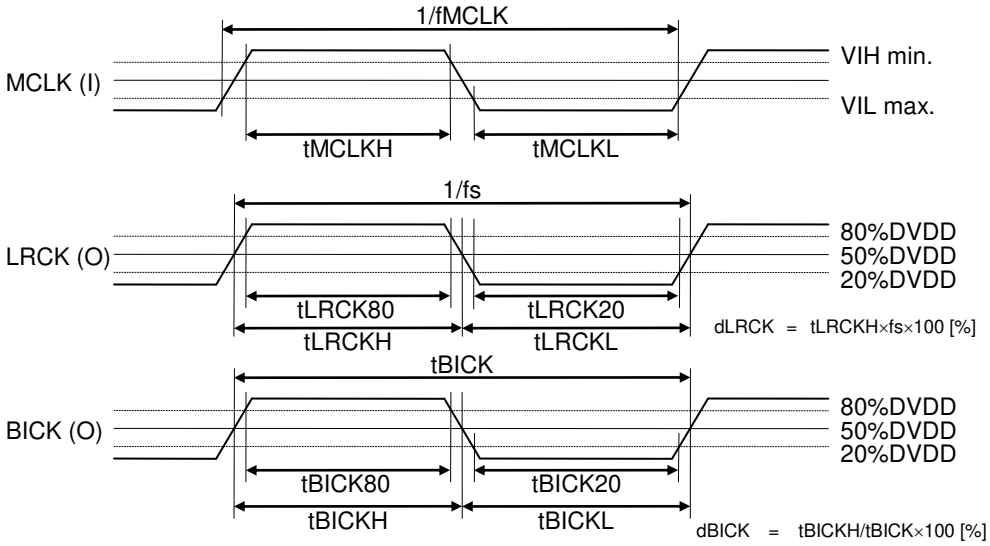

Figure 15. Clock Timing (External Master Mode)

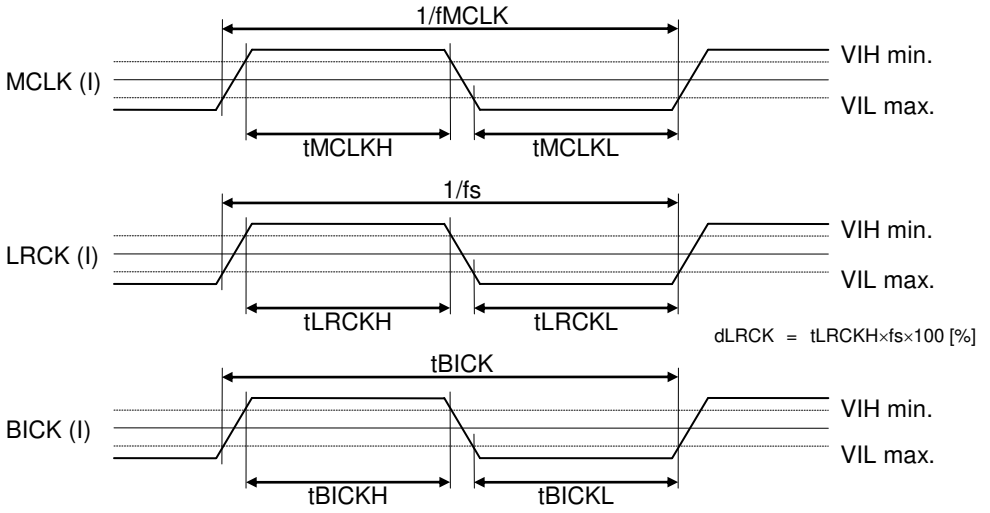

Figure 16. Clock Timing (External Slave Mode)

Clock Timings (Parallel Control Mode) (continued)

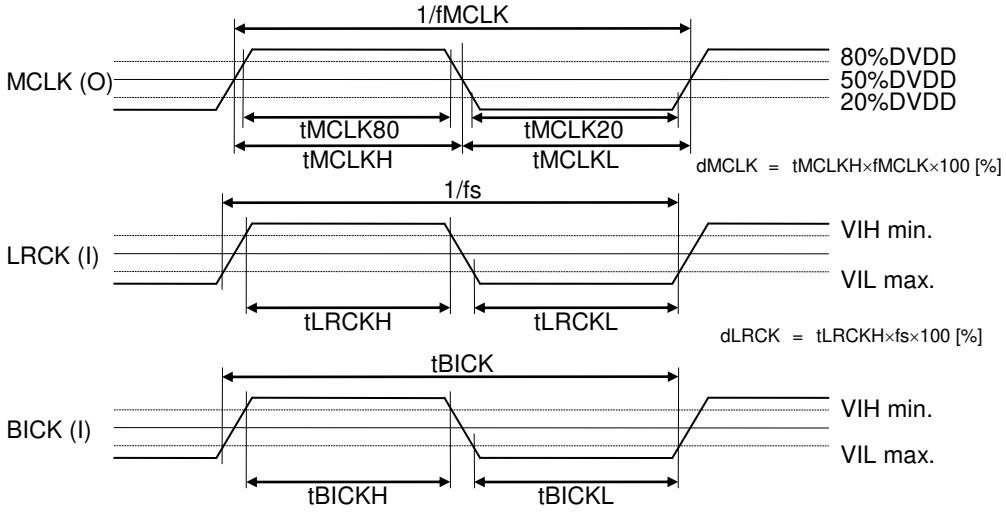

Figure 17. Clock Timing (PLL Slave Mode)

Audio Interface Timings (Parallel Control Mode)

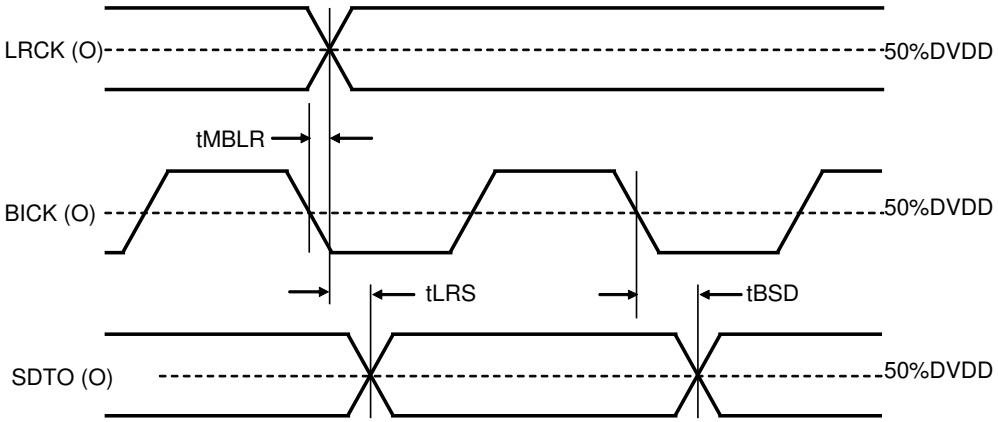

Figure 18. Audio Interface Timing (External Master Mode)

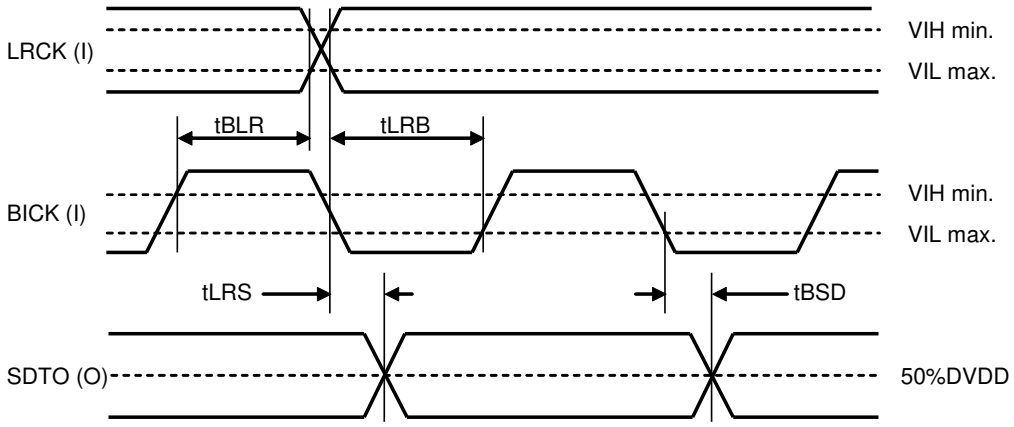

Figure 19. Audio Interface Timing (PLL Slave Mode, External Slave Mode)

Audio Interface Timings (Parallel Control Mode) (continued)

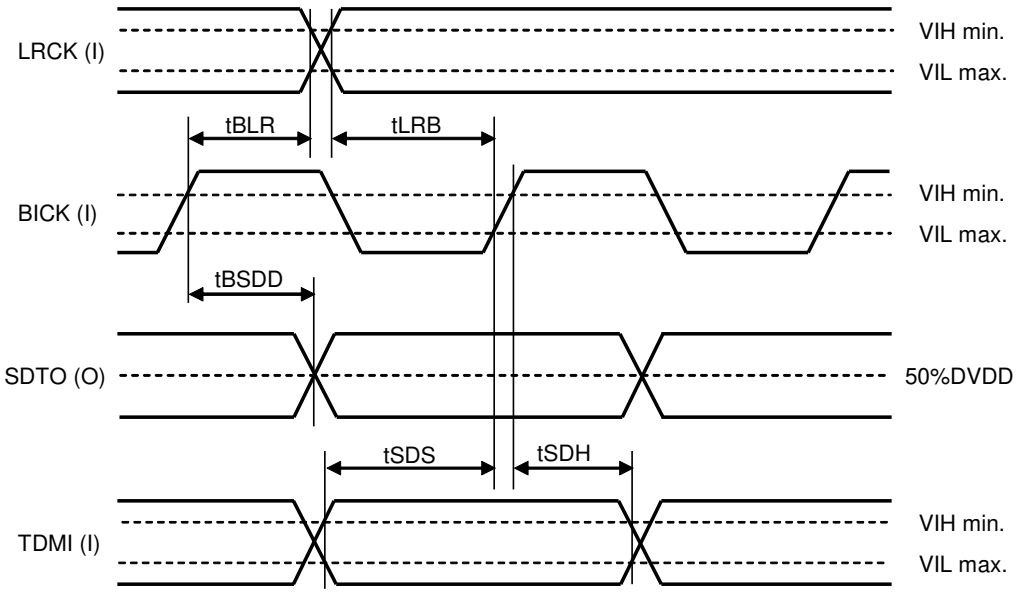

Figure 20. Audio Interface Timing (TDM mode & Slave Mode)

Power-down Timing

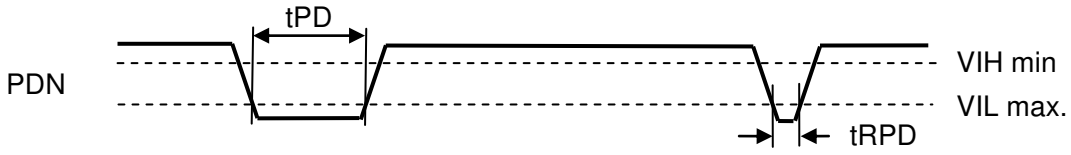

Figure 21. Power-down & Reset Timing

12. Switching Characteristics (Serial Control Mode)

■ System Clocks

□ External Master Mode (Serial Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
MCLK=256fsn					
Frequency	fMCLK	2.048	-	13.824	MHz
Pulse Width Low	tMCLKL	32	-	-	ns
Pulse Width High	tMCLKH	32	-	-	ns
MCLK=512fsn, 256fsd, 128fsq					
Frequency	fMCLK	4.096	-	27.648	MHz
Pulse Width Low	tMCLKL	16	-	-	ns
Pulse Width High	tMCLKH	16	-	-	ns
LRCK Output Timing					
Stereo Mode					
Frequency (fs)					
Normal Speed					
MCLK 256fs, 512fs	fsn	8	-	54	kHz
Double Speed					
MCLK 256fs	fsd	54	-	108	kHz
Quad Speed					
MCLK 128fs	fsq	108	-	216	kHz
Duty Cycle	dLRCK	-	50	-	%
TDM256 Mode					
Frequency (fs)					
Normal Speed	fsn	8	-	48	kHz
Double Speed	fsd	48	-	96	kHz
Pulse Width Low	tLRCKL	-	1/(8fs)	-	s
Pulse Width High	tLRCKH	-	1/(8fs)	-	s
TDM128 Mode					
Frequency (fs)					
Quad Speed	fsq	96	-	192	kHz
Pulse Width Low	tLRCKL	-	1/(4fs)	-	s
Pulse Width High	tLRCKH	-	1/(4fs)	-	s