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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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AK5558

8-Channel Differential 32-bit ΔΣ ADC

1. General Description

The AK555x series is a 32-bit, 768 kHz sampling, differential input A/D converter for digital audio systems. It achieves 115 dB dynamic range and 106 dB S/(N+D) while maintaining low power consumption performance.

The AK5558 integrates a 8-channel A/D converter, suitable for mixers and multi-channel recorders. Four types of digital filters are integrated and selectable according to the sound quality preference. The AK5558 can be easily connected to a DSP by supporting TDM audio formats. Additionally, it supports DSD output up to 11.2MHz. The channel summation improves the dynamic range to 118 dB in 8-to-4 mode, to 121 dB in 8-to-2 mode and to 124 dB in 8-to-1 mode.

2. Features

- ☐ **Sampling Rate: 8 kHz-768 kHz**
- ☐ **Input: Full Differential Inputs**
- ☐ **S/(N+D): 106 dB**
- ☐ **DR: 115 dB (8-to-4 mode: 118 dB, 8-to-2 mode: 121 dB, 8-to-1 mode: 124 dB)**
- ☐ **S/N: 115 dB (8-to-4 mode: 118 dB, 8-to-2 mode: 121 dB, 8-to-1 mode: 124 dB))**
- ☐ **Internal Filter: Four types of LPF, Digital HPF**
- ☐ **Power Supply: 4.5-5.5 V (Analog), 1.7-1.98 V or 3.0-3.6 V (Digital)**
- ☐ **Output Format:**
  - **PCM mode: 24/32-bit MSB justified, I^2S or TDM**
  - **DSD mode: DSD Native 64, 128, 256**
  - **Maximized Slot Efficiency in TDM Mode by Optimal Data Placed Mode**
- ☐ **Cascade TDM I/F:**
  - **TDM512: fs= 48 kHz**
  - **TDM256: fs= 96 kHz or 48 kHz**
  - **TDM128: fs= 192 kHz, 96 kHz or 48 kHz**
- ☐ **Operation Mode: Master Mode & Slave Mode**
- ☐ **Detection Function: Input Overflow Flag**
- ☐ **Serial Interface: 3-wire Serial and I^2C µP I/F (Pin setting is also available)**
- ☐ **Power Consumption: 261 mW (@AVDD= 5.0 V, TVDD= 3.3 V, fs= 48 kHz)**
- ☐ **Package: 64-pin QFN**

3. Table of Contents

4. Block Diagram

■ Block Diagram

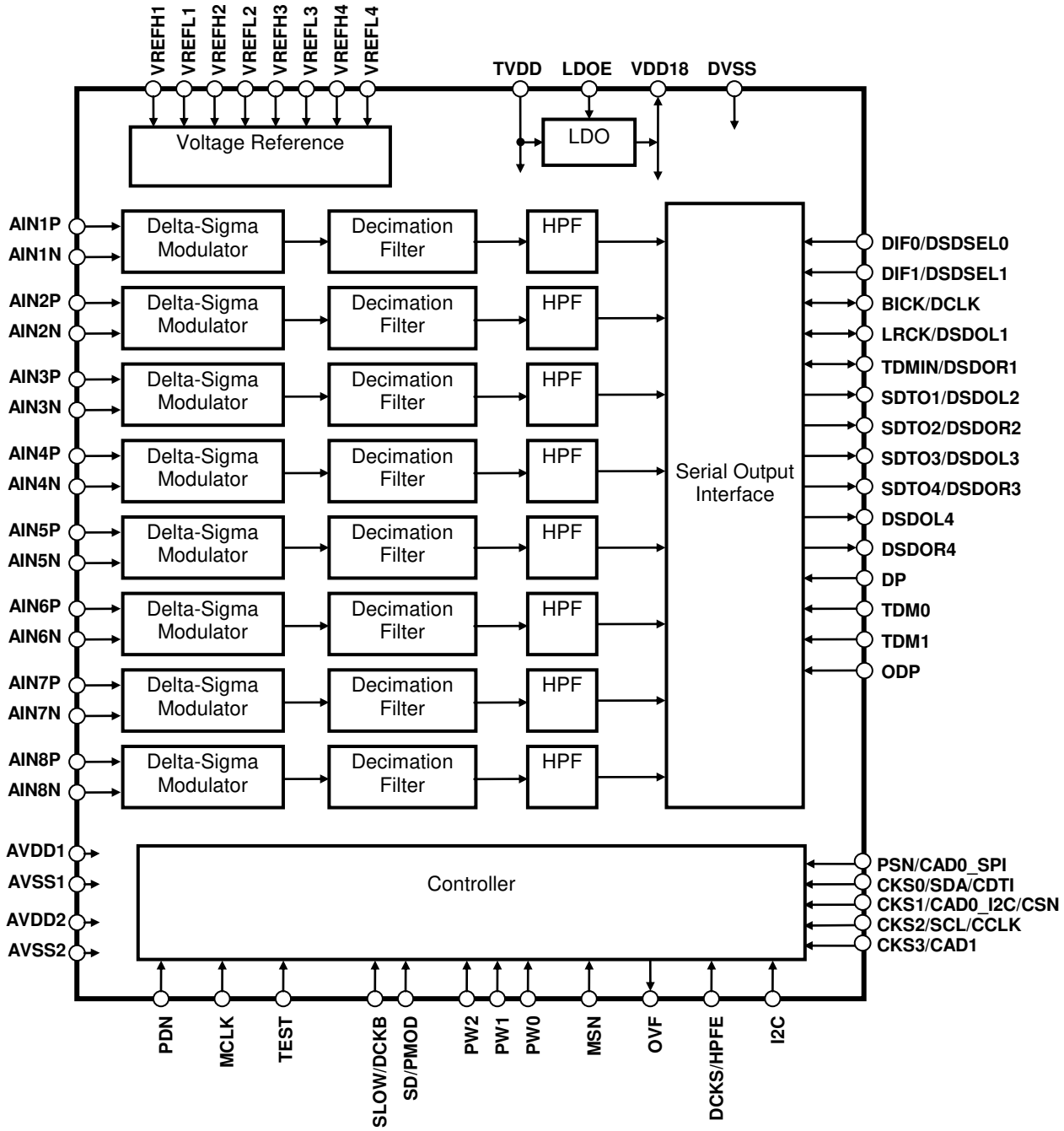
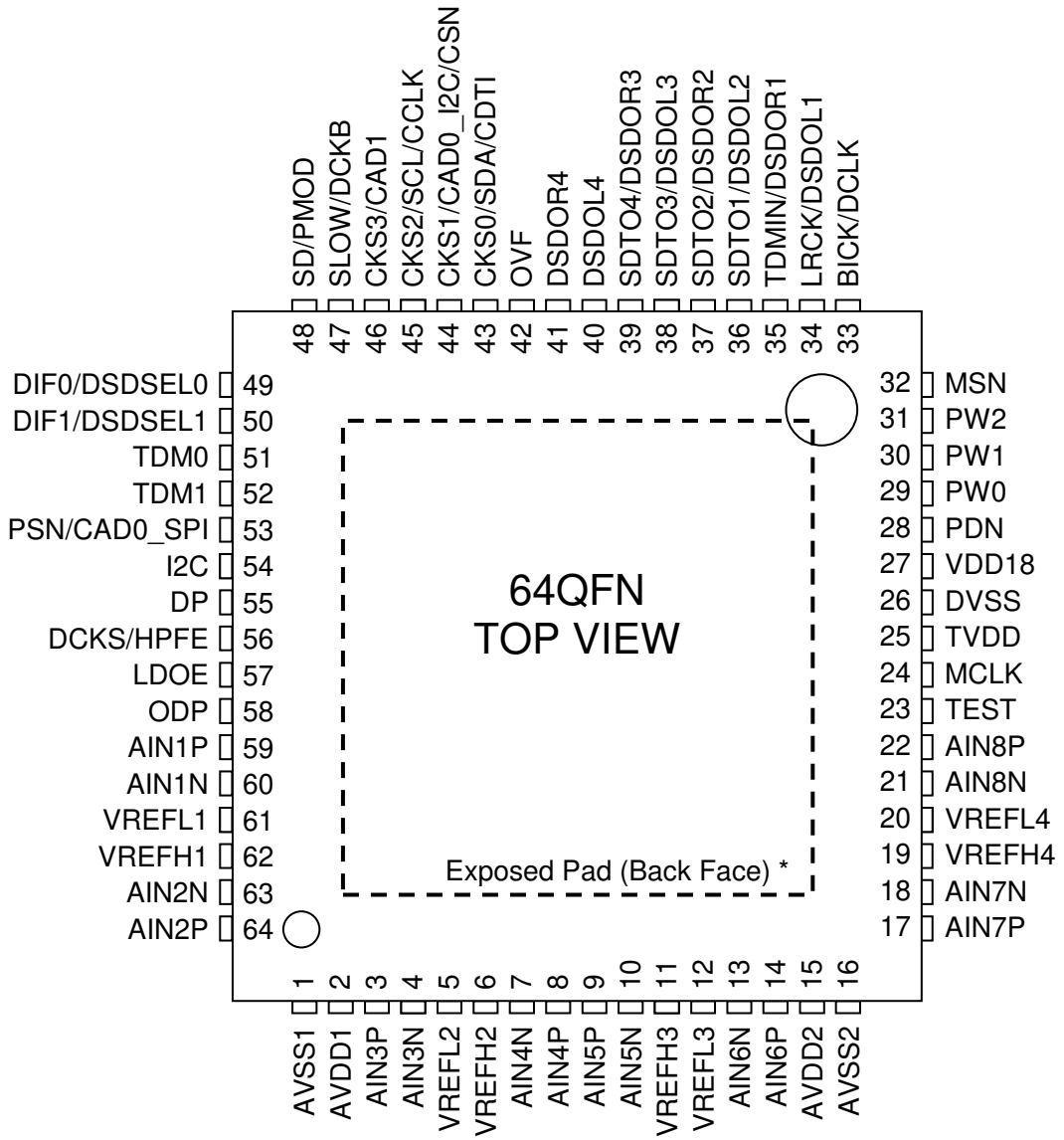


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations



* The exposed pad at back face of the package must be open or connected to the ground of the board.

Figure 2. Pin Configurations

■ Pin Functions

No.	Pin Name	I/O	Function	Power Down Status
1	AVSS1	-	Analog Ground Pin(AIN1-4)	-
2	AVDD1	-	Analog Power Supply Pin(AIN1-4), 4.5-5.5 V	-
3	AIN3P	I	Channel 3 Positive Input Pin	-
4	AIN3N	I	Channel 3 Negative Input Pin	-
5	VREFL2	I	ADC Low Level Voltage Reference Input Pin	-
6	VREFH2	I	ADC High Level Voltage Reference Input Pin	-
7	AIN4N	I	Channel 4 Negative Input Pin	-
8	AIN4P	I	Channel 4 Positive Input Pin	-
9	AIN5P	I	Channel 5 Positive Input Pin	-
10	AIN5N	I	Channel 5 Negative Input Pin	-
11	VREFH3	I	ADC High Level Voltage Reference Input Pin	-
12	VREFL3	I	ADC Low Level Voltage Reference Input Pin	-
13	AIN6N	I	Channel 6 Negative Input Pin	-
14	AIN6P	I	Channel 6 Positive Input Pin	-
15	AVDD2	-	Analog Power Supply Pin(AIN5-8), 4.5-5.5 V	-
16	AVSS2	-	Analog Ground Pin(AIN5-8)	-
17	AIN7P	I	Channel 7 Positive Input Pin	-
18	AIN7N	I	Channel 7 Negative Input Pin	-
19	VREFH4	I	ADC High Level Voltage Reference Input Pin	-
20	VREFL4	I	ADC Low Level Voltage Reference Input Pin	-
21	AIN8N	I	Channel 8 Negative Input Pin	-
22	AIN8P	I	Channel 8 Positive Input Pin	-
23	TEST	I	TEST Enable Pin. This pin is pull down by 100kΩ internally	-
24	MCLK	I	Master Clock Input Pin	-
25	TVDD	-	Digital I/O Buffers and LDO Power Supply Pin 1.7-1.98 V (LDOE pin= “L”) or 3.0-3.6 V (LDOE pin= “H”).	-
26	DVSS	-	Digital Ground Pin	-
27	VDD18	I	Digital Core Power Supply Pin, 1.7-1.98 V (LDOE pin= “L”)	-
		O	LDO Stabilization Capacitor Connect Pin. (LDOE pin= “H”)	Hi-z & Pull Down with 500 Ω
28	PDN	I	Reset & Power Down Pin “L”: Reset & Power down, “H” : Normal operation	-
29	PW0	I	Power Management Pin, Channel Summation select Pin	-
30	PW1	I	Power Management Pin, Channel Summation select Pin	-
31	PW2	I	Power Management Pin, Channel Summation select Pin	-
32	MSN	I	Master/Slave Select Pin “L”: Slave Mode, “H” : Master Mode	-
33	BICK	I	Audio Serial Data Clock Input Pin in PCM & Slave Mode. This pin is pulled down by 100 kΩ internally	-
		O	Audio Serial Data Clock Output Pin in PCM & Master Mode This pin is pulled down by 100 kΩ internally	Hi-z
	DCLK	O	DSD Clock Output Pin in DSD Mode This pin is pulled down by 100 kΩ internally	Hi-z
34	LRCK	I	Channel Clock Input Pin in PCM & Slave Mode This pin is pulled down by 100 kΩ internally	-
		O	Channel Clock Output Pin in PCM & Master Mode This pin is pulled down by 100 kΩ internally	Hi-z
	DSDOL1	O	Audio Serial Data Output Pin for AIN1 in DSD Mode This pin is pulled down by 100 kΩ internally	Hi-z

No.	Pin Name	I/O	Function	Power Down Status
35	TDMIN	I	TDM Data Input Pin in PCM Mode This pin is pulled down by 100 kΩ internally	-
	DSDOR1	O	Audio Serial Data Output Pin for AIN2 in DSD Mode This pin is pulled down by 100 kΩ internally	Hi-z
36	SDTO1	O	Audio Serial Data Output Pin for AIN1 and AIN2 in PCM Mode	L
	DSDOL2	O	Audio Serial Data Output Pin for AIN3 in DSD Mode	L
37	SDTO2	O	Audio Serial Data Output Pin for AIN3 and AIN4 in PCM Mode	L
	DSDOR2	O	Audio Serial Data Output Pin for AIN4 in DSD Mode	L
38	SDTO3	O	Audio Serial Data Output Pin for AIN5 and AIN6 in PCM Mode	L
	DSDOL3	O	Audio Serial Data Output Pin for AIN5 in DSD Mode	L
39	SDTO4	O	Audio Serial Data Output Pin for AIN7 and AIN8 in PCM Mode	L
	DSDOR3	O	Audio Serial Data Output Pin for AIN6 in DSD Mode	L
40	DSDOL4	O	Audio Serial Data Output Pin for AIN7 in DSD Mode	L
41	DSDOR4	O	Audio Serial Data Output Pin for AIN8 in DSD Mode	L
42	OVF	O	Analog Input Over Flow Flag Output Pin	L
43	CKS0	I	Clock Mode Select Pin	-
	SDA	I/O	Control Data I/O Pin in I^2C Bus Serial Control Mode	Hi-z
	CDTI	I	Control Data Input Pin in 3-wire Serial Control Mode	-
44	CKS1	I	Clock Mode Select Pin	-
	CAD0_I2C	I	Chip Address 0 Pin in I^2C Bus Serial Control Mode	-
	CSN	I	Chip Select Pin in 3-wire Serial Control Mode	-
45	CKS2	I	Clock Mode Select Pin	-
	SCL	I	Control Data Clock Pin in I^2C Bus Serial Control Mode	-
	CCLK	I	Control Data Clock Pin in 3-wire Serial Control Mode	-
46	CKS3	I	Clock Mode Select Pin	-
	CAD1	I	Chip Address 1 Pin in I^2C Bus or 3-wire Serial Control Mode	-
47	SLOW	I	Slow Roll-OFF Digital Filter Select Pin in PCM Mode	-
	DCKB	I	Polarity of DCLK Pin in DSD Mode	-
48	SD	I	Short Delay Digital Filter Select Pin in PCM Mode	-
	PMOD	I	DSD Phase Modulation Mode Select Pin in DSD Mode	-
49	DIF0	I	Audio Data Format Select Pin in PCM Mode "L": MSB justified, "H": I^2S	-
	DSDSEL0	I	DSD Sampling Rate Control Pin in DSD Mode	-
50	DIF1	I	Audio Data Format Select Pin in PCM Mode "L": 24-bit Mode, "H": 32-bit Mode	-
	DSDSEL1	I	DSD Sampling Rate Control Pin in DSD Mode	-
51	TDM0	I	TDM I/F Format Select Pin * This pin must be fixed to "L" when using DSD mode.	-
52	TDM1	I	TDM I/F Format Select Pin * This pin must be fixed to "L" when using DSD mode.	-
53	PSN	I	Control Mode Select Pin (I2C pin = "H") "L":I^2C Bus Serial Control Mode, "H" :Parallel Control Mode	-
	CAD0_SPI	I	Chip Address 0 Pin in 3-wire Serial Control Mode (I2C pin = "L")	-
54	I2C	I	Control Mode Select Pin "L": 3-wire Serial Control Mode "H": I^2C Bus Serial Control Mode or Parallel Control Mode	-
55	DP	I	DSD Mode Enable Pin "L": PCM Mode, "H": DSD Mode	-

No.	Pin Name	I/O	Function	Power Down Status
56	HPFE	I	High Pass Filter Enable Pin "L": HPF Disable, "H": HPF Enable	-
	DCKS	I	Master Clock Frequency Select at DSD Mode (DSD Only)	
57	LDOE	I	LDO Enable Pin "L": LDO Disable, "H": LDO Enable This pin is pulled down by 100 kΩ internally.	-
58	ODP	I	Optimal Data Placement Mode Select Pin	-
59	AIN1P	I	Channel 1 Positive Input Pin	-
60	AIN1N	I	Channel 1 Negative Input Pin	-
61	VREFL1	I	ADC Low Level Voltage Reference Input Pin	-
62	VREFH1	I	ADC High Level Voltage Reference Input Pin	-
63	AIN2N	I	Channel 2 Negative Input Pin	-
64	AIN2P	I	Channel 2 Positive Input Pin	-

Note 1. All digital input pins must not be allowed to float.

■ Handling of Unused Pin

The unused I/O pins should be connected appropriately.

1. PCM Mode

Classification	Pin Name	Setting
Analog	AIN1-8P, AIN1-8N	Open
	VREFH1-4	Connect to AVDD
	VREFL1-4	Connect to AVSS
Digital	TDMIN, TEST	Connect to DVSS
	SDTO1-4, DSDOL4, DSDOR4, OVF	Open

2. DSD Mode

Classification	Pin Name	Setting
Analog	AIN1-8P, AIN1-8N	Open
	VREFH1-4	Connect to AVDD
	VREFL1-4	Connect to AVSS
Digital	TDM0, TDM1, TEST	Connect to DVSS
	DSDOL1-4, DSDOR1-4, OVF	Open

Note 2. Unused channels must be powered down.

6. Absolute Maximum Ratings

(VSS= 0 V; Note 3)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies:	Analog (AVDD pin)	AVDDam	−0.3	6.0	V
	Digital Interface (TVDD pin)	TVDDam	−0.3	4.0	V
	Digital Core (VDD18 pin) (Note 4)	VDD18am	−0.3	2.5	V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
Analog Input Voltage (AIN1-4P, AIN1-4N pins)		VINA	−0.3	AVDD+0.3	V
Digital Input Voltage		VIND	−0.3	TVDD+0.3	V
Ambient Temperature (Power applied)					
When the back tab is connected to VSS		Ta	−40	105	°C
When the back tab is open		Ta	−40	70	°C
Storage Temperature		Tstg	−65	150	°C

Note 3. All voltages with respect to ground.
Note 4. The 1.8 V LDO is off (LDOE pin = “L”) and an external power is supplied to the VDD18 pin.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(VSS= 0 V; Note 3)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog (AVDD pin)	AVDD	4.5	5.0	5.5	V
	(LDOE pin= “L”) (Note 5)					
	Digital Interface (TVDD pin) (Note 6)	TVDD	1.7	1.8	1.98	V
	Digital Core (VDD18 pin)	VDD18	1.7	1.8	1.98	V
	(LDOE pin= “H”) (Note 7)					
	Digital Interface (TVDD pin)	TVDD	3.0	3.3	3.6	V
Voltage Reference	“H” voltage Reference (Note 8)	VREFH1-4	4.5	5.0	5.5	V
	“L” voltage reference (Note 9)	VREFL1-4	-	AVSS	-	V

Note 3. All voltages with respect to ground.
Note 5. TVDD pin must be powered up before or at the same time with the VDD18 pin when the LDOE pin = “L”. The power up sequence between AVDD pin and TVDD pin or between AVDD pin and VDD18 pin is not critical.
Note 6. TVDD must not exceed VDD18±0.1 V when LDOE pin= “L”.
Note 7. When LDOE pin = “H”, the internal LDO supplies 1.8 V (typ). The power up sequences between AVDD pin and TVDD pin is not critical.
Note 8. VREFH1-4 must not exceed AVDD+0.1 V.
Note 9. VREFL1-4 must be connected to AVSS.
Analog Input Voltage is proportional to {(VREFH) – (VREFL)}.
Vin (typ, @ 0dB) = ±2.8 × {(VREFH) – (VREFL)} / 5 [V].

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Analog Characteristics

(Ta= 25 °C; AVDD= 5.0 V; TVDD= 3.3 V, fs= 48 kHz, BICK= 64fs;
Signal Frequency= 1 kHz; 24-bit Data; Measurement frequency= 20 Hz-20 kHz at fs= 48 kHz,
40 Hz-40 kHz at fs= 96 kHz, 40 Hz-40 kHz at fs= 192 kHz, unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Analog Input Characteristics:						
Resolution			-	-	32	bit
Input Voltage		(Note 10)	±2.7	±2.8	±2.9	Vpp
S/(N+D)	fs= 48 kHz BW=20 kHz	–1 dBFS	100	106	-	dB
		–20 dBFS	-	92	-	dB
		–60 dBFS	-	52	-	dB
	fs= 96 kHz BW= 40 kHz	–1 dBFS	-	106	-	dB
		–20 dBFS	-	89	-	dB
		–60 dBFS	-	49	-	dB
	fs= 192 kHz BW= 40 kHz	–1 dBFS	-	106	-	dB
		–20 dBFS	-	89	-	dB
		–60 dBFS	-	49	-	dB
Dynamic Range (–60 dBFS with A-weighted)		Not-Sum. mode	110	115	-	dB
		8-to-4 mode	-	118	-	dB
		8-to-2 mode	-	121	-	dB
		8-to-1 mode	-	124	-	dB
S/N (A-weighted)		Not-Sum. mode	110	115	-	dB
		8-to-4 mode	-	118	-	dB
		8-to-2 mode	-	121	-	dB
		8-to-1 mode	-	124	-	dB
Input Resistance These values will be doubled in DSD 64fs mode. (Values in DSD128 or DSD256 modes are as shown here)			8.8	10.4	12.0	kΩ
Interchannel Isolation (AIN1↔AIN2, AIN3↔AIN4, AIN5↔AIN6, AIN7↔AIN8)			110	120	-	dB
Interchannel Gain Mismatch			-	0	0.5	dB
Power Supply Rejection		(Note 11)	-	60	-	dB
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H", LDOE pin = "H")						
AVDD + VREFHm (m=1-4)			-	41	54	mA
TVDD	(fs= 48 kHz)		-	17	22	mA
TVDD	(fs= 96 kHz)		-	28	36	mA
TVDD	(fs= 192 kHz)		-	25	32	mA
Power Down mode (PDN pin = "L")		(Note 12)				
AVDD+TVDD			-	10	100	μA

Note 10. This value is (AINnP)–(AINnN) that the ADC output becomes full-scale (n=1-8).
Vin = 0.56 × (VREFHm–VREFLm) [Vpp]. (m=1-4)
Note 11. PSRR is applied to AVDD, TVDD with 1 kHz, 20 mVpp sine wave. The VREFH1-4 are held to the fixed voltage.
Note 12. All digital inputs are fixed to TVDD or TVSS.

9. Filter Characteristics

■ ADC Filter Characteristics (fs= 48 kHz)

(Ta= −40 - +105°C; AVDD= 4.5-5.5 V, TVDD=1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin= "L"))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 3) (SD pin= "L", SLOW pin= "L")						
Passband (Note 13)	+0.001/−0.06 dB	PB	0	-	22.0	kHz
	−6.0 dB		-	24.4	-	kHz
Stopband (Note 13)		SB	27.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0 kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	19	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 4) (SD pin= "L", SLOW pin= "H")						
Passband (Note 13)	+0.001/−0.076 dB	PB	0	-	12.5	kHz
	−6.0 dB		-	21.9	-	kHz
Stopband (Note 13)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0 kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	7	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (Figure 5) (SD pin= "H", SLOW pin= "L")						
Passband (Note 13)	+0.001/−0.06 dB	PB	0	-	22.0	kHz
	−6.0 dB		-	24.4	-	kHz
Stopband (Note 13)		SB	27.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0 kHz		ΔGD	-	-	2.8	1/fs
Group Delay (Note 14)		GD	-	5	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (Figure 6) (SD pin= "H",SLOW pin= "H")						
Passband (Note 13)	+0.001/−0.076 dB	PB	0	-	12.5	kHz
	−6.0 dB		-	21.9	-	kHz
Stopband (Note 13)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0 kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 14)		GD	-	5	-	1/fs
Digital Filter (HPF):						
Frequency Response	−3.0 dB	FR	-	1.0	-	Hz
	−0.5 dB		-	2.5	-	Hz
(Note 13)	−0.1 dB		-	6.5	-	Hz

Note 13. The Passband and Stopband Frequencies scale with fs.
For Example, PB (+0.001 dB/−0.06 dB) = 0.46 × fs (SHARP ROLL-OFF).
For Example, PB (+0.001 dB/−0.076 dB) = 0.26 × fs (SLOW ROLL-OFF).

Note 14. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces.

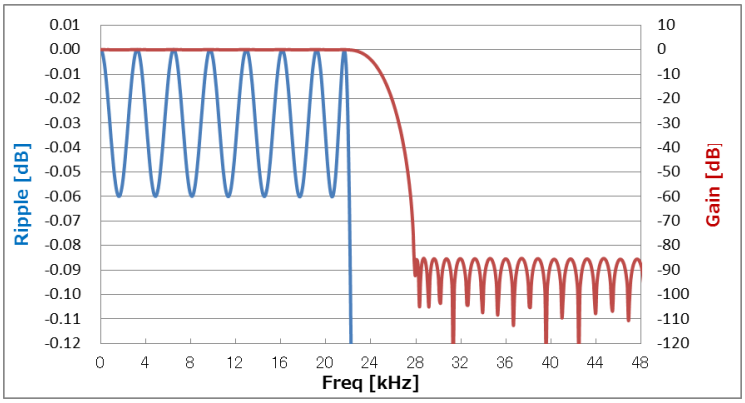


Figure 3. SHARP ROLL-OFF (fs= 48 kHz)

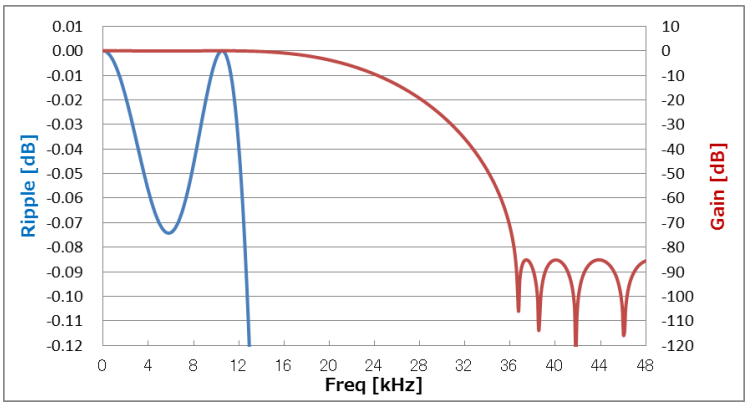


Figure 4. SLOW ROLL-OFF (fs= 48 kHz)

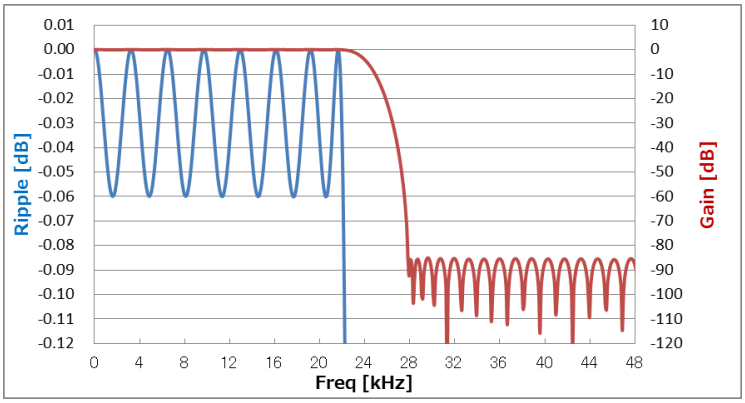


Figure 5. SHORT DELAY SHARP ROLL-OFF (fs= 48 kHz)

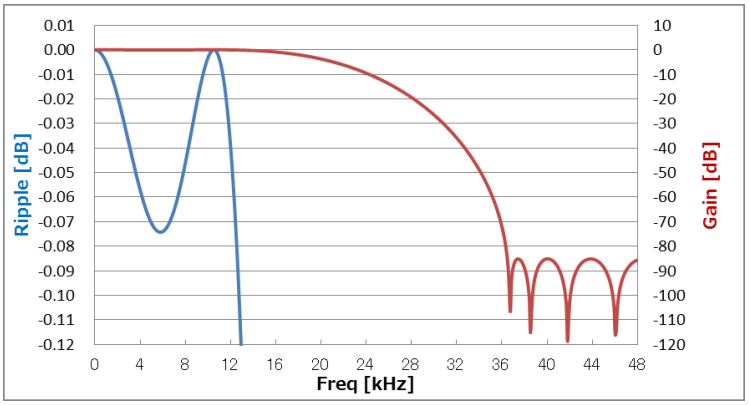


Figure 6. SHORT DELAY SLOW ROLL-OFF (fs= 48 kHz)

■ ADC Filter Characteristics (fs= 96 kHz)

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD=1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin= "L"))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 7) (SD pin= "L", SLOW pin= "L")						
Passband (Note 13)	+0.001/−0.06 dB −6.0 dB	PB	0 -	- 48.8	44.1 -	kHz kHz
Stopband (Note 13)		SB	55.7	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0 kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	19	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 8) (SD pin= "L", SLOW pin= "H")						
Passband (Note 13)	+0.001/−0.076 dB −6.0 dB	PB	0 -	- 43.8	25	kHz kHz
Stopband (Note 13)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0 kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	7	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF (Figure 9) (SD pin= "H",SLOW pin= "L")						
Passband (Note 13)	+0.001/−0.06 dB −6.0 dB	PB	0 -	- 48.8	44.1 -	kHz kHz
Stopband (Note 13)		SB	55.7	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0 kHz		ΔGD	-	-	2.8	1/fs
Group Delay (Note 14)		GD	-	5	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (Figure 10) (SD pin="H", SLOW pin= "H")						
Passband (Note 13)	+0.001/−0.076 dB −6.0dB	PB	0 -	- 43.8	25 -	kHz kHz
Stopband (Note 13)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0 kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 14)		GD	-	5	-	1/fs
Digital Filter (HPF):						
Frequency Response	−3.0 dB −0.5 dB	FR	- -	1.0 2.5	- -	Hz Hz
(Note 13)	−0.1 dB		-	6.5	-	Hz

Note 13. The Passband and Stopband Frequencies scale with fs.
For example, PB (+0.001 dB/−0.06 dB) = 0.46 × fs (SHARP ROLL-OFF).
For example, PB (+0.001 dB/−0.076 dB) = 0.26 × fs (SLOW ROLL-OFF).

Note 14. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces.

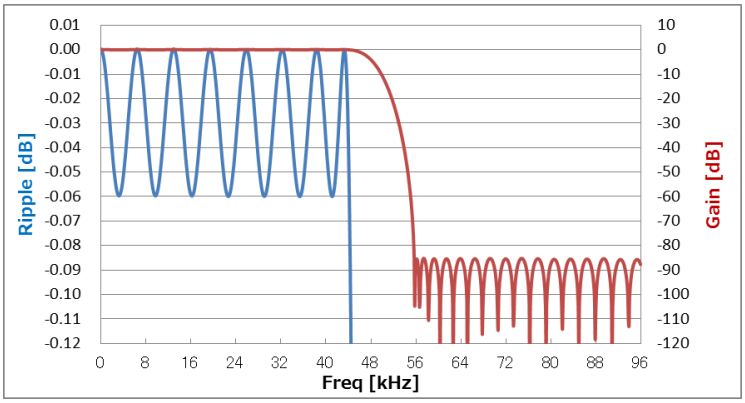


Figure 7. SHARP ROLL-OFF (fs= 96 kHz)

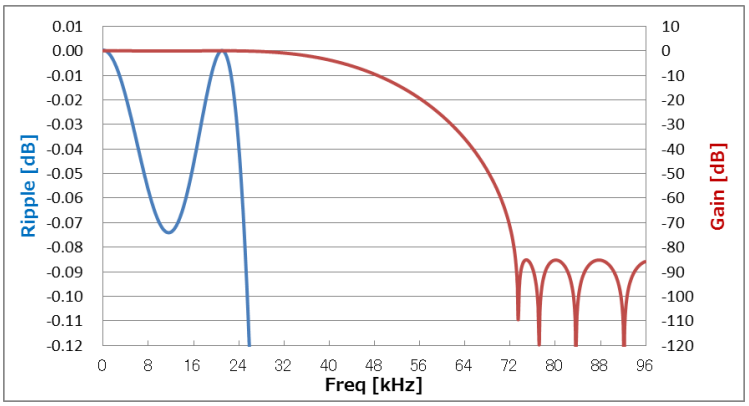


Figure 8. SLOW ROLL-OFF (fs= 96 kHz)

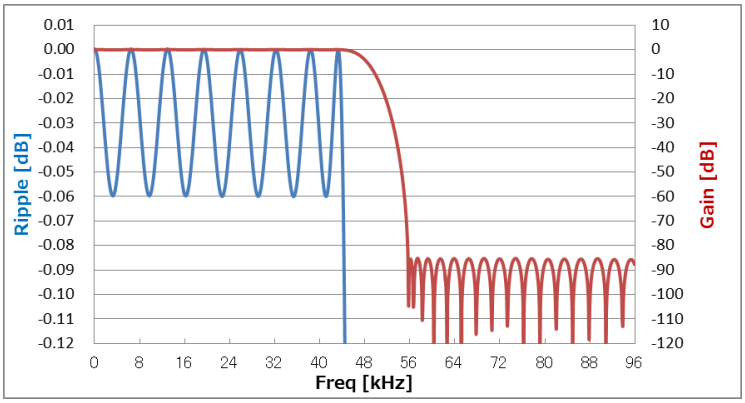


Figure 9. SHORT DELAY SHARP ROLL-OFF (fs= 96 kHz)

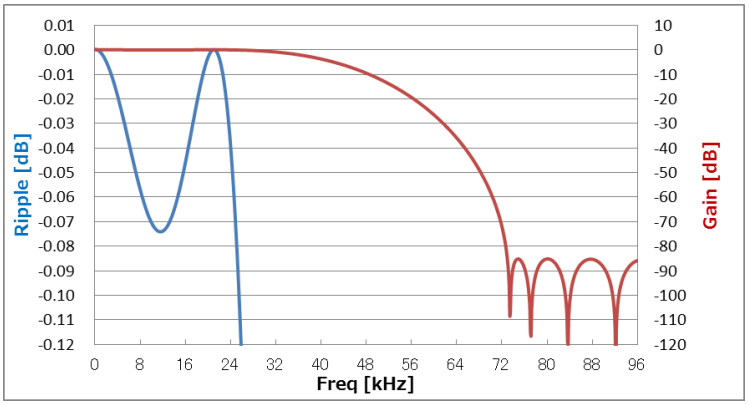


Figure 10. SHORT DELAY SLOW ROLL-OFF (fs= 96 kHz)

■ ADC Filter Characteristics (fs= 192 kHz)

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD=1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin= "L"))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 11) (SD pin="L", SLOW pin= "L")						
Passband (Note 13)	+0.001/−0.037 dB	PB	0	-	83.7	kHz
	−6.0 dB		-	100.2	-	kHz
Stopband (Note 13)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0 kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	15	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 12) (SD pin="L", SLOW pin= "H")						
Passband (Note 13)	+0.001/−0.1 dB	PB	0	-	31.5	kHz
	−6.0 dB		-	75.2	-	kHz
Stopband (Note 13)		SB	146	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0 kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	8	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (Figure 13) (SD pin="H", SLOW pin= "L")						
Passband (Note 13)	+0.001/−0.037 dB	PB	0	-	83.7	kHz
	−6.0 dB		-	100.2	-	kHz
Stopband (Note 13)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0 kHz		ΔGD	-	-	0.3	1/fs
Group Delay (Note 14)		GD	-	6	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF FILTER (Figure 14) (SD pin="H", SLOW pin= "H")						
Passband (Note 13)	+0.001/−0.1 dB	PB	0	-	31.5	kHz
	−6.0 dB		-	75.2	-	kHz
Stopband (Note 13)		SB	146	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0 kHz		ΔGD	-	-	0.4	1/fs
Group Delay (Note 14)		GD	-	6	-	1/fs
Digital Filter (HPF):						
Frequency Response	−3.0 dB	FR	-	1.0	-	Hz
	−0.5 dB		-	2.5	-	Hz
(Note 13)	−0.1 dB		-	6.5	-	Hz

Note 13. The Passband and Stopband Frequencies scale with fs.
For Example, PB (+0.001 dB/−0.037 dB) = 0.436 × fs (SHARP ROLL-OFF).
For Example, PB (+0.001 dB/−0.1 dB) = 0.164 × fs (SLOW ROLL-OFF).

Note 14. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces.

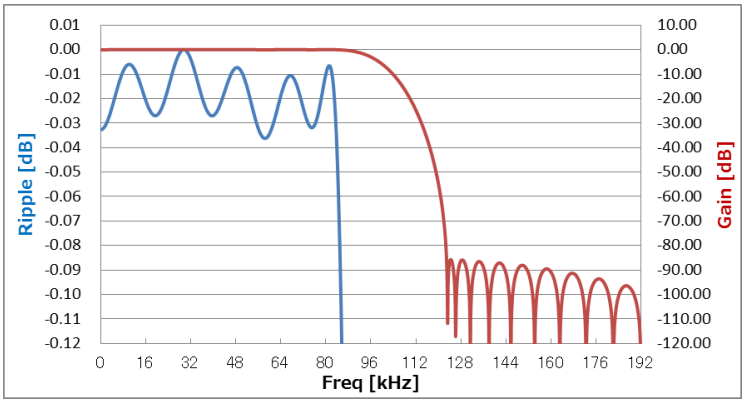


Figure 11. SHARP ROLL-OFF (fs= 192 kHz)

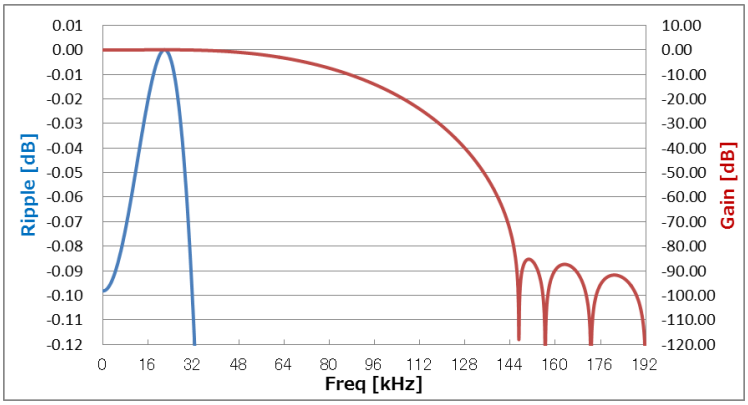


Figure 12. SLOW ROLL-OFF (fs= 192 kHz)

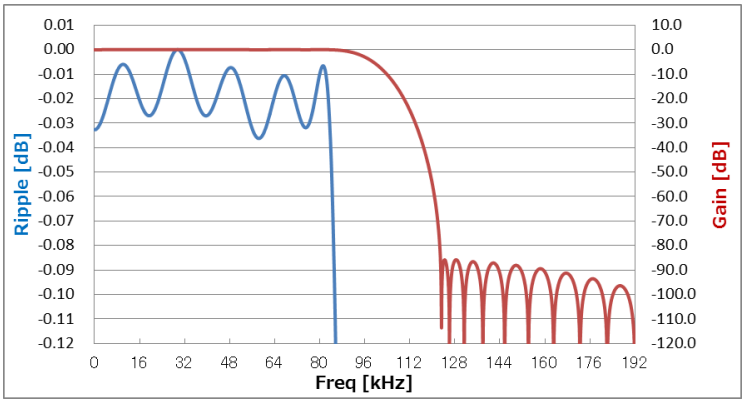


Figure 13. SHORT DELAY SHARP ROLL-OFF (fs= 192 kHz)

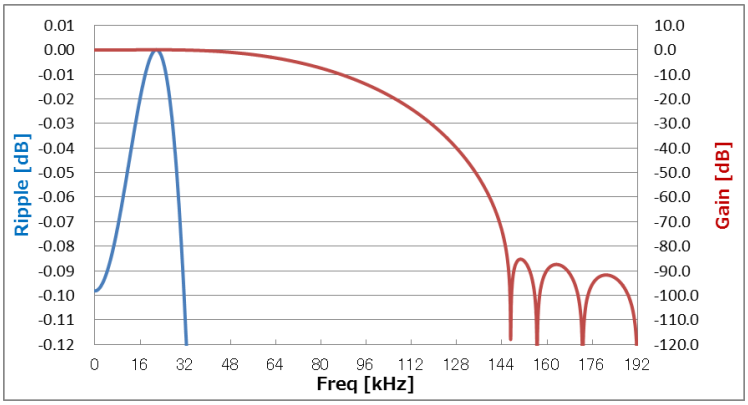


Figure 14. SHORT DELAY SLOW ROLL-OFF (fs= 192 kHz)

■ ADC Filter Characteristics (fs= 384 kHz)

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD=1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin= "L"))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF) (Figure 15) (SD pin = "X", SLOW pin = "X") * It does not depend on the SD pin and Slow pin.						
Frequency Response (Note 13)	−0.1 dB −1.0 dB −3.0 dB −6.0 dB	FR	- - - -	81.75 114 137.63 157.2	- - - -	kHz kHz kHz kHz
Stopband (Note 13)		SB	277.4	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0 kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	7	-	1/fs

Note 13. The Passband and Stopband Frequencies scale with fs.

Note 14. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces.

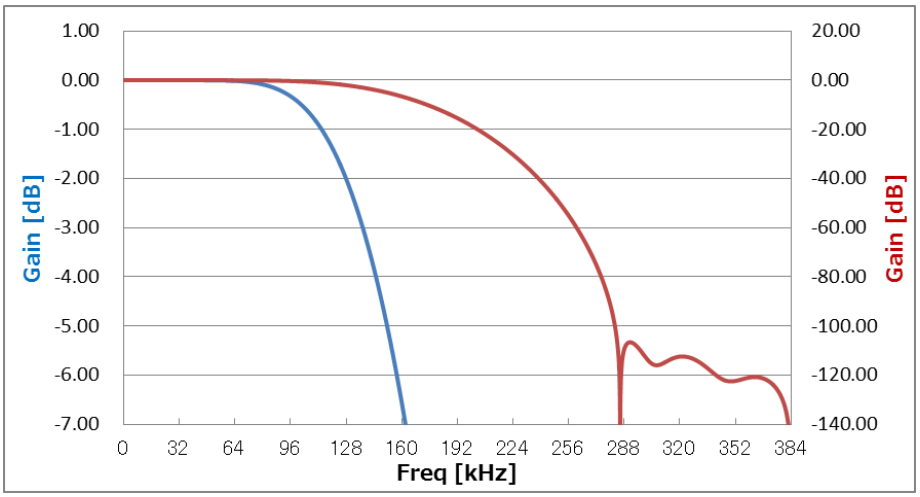


Figure 15. Frequency Response (fs= 384 kHz)

■ ADC Filter Characteristics (fs= 768 kHz)

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD=1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin= "L"))

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF) (Figure 16) (SD pin = "X", SLOW pin = "X") * It does not depend on the SD pin and SLOW pin.						
Frequency Response (Note 13)	−0.1 dB −1.0 dB −3.0 dB −6.0 dB	FR	- - - -	26.25 83.75 144.5 203.1	- - - -	kHz kHz kHz kHz
Stopband (Note 13)		SB	640.3	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0 kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 14)		GD	-	5	-	1/fs

Note 13. The Passband and Stopband Frequencies scale with fs.

Note 14. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces.

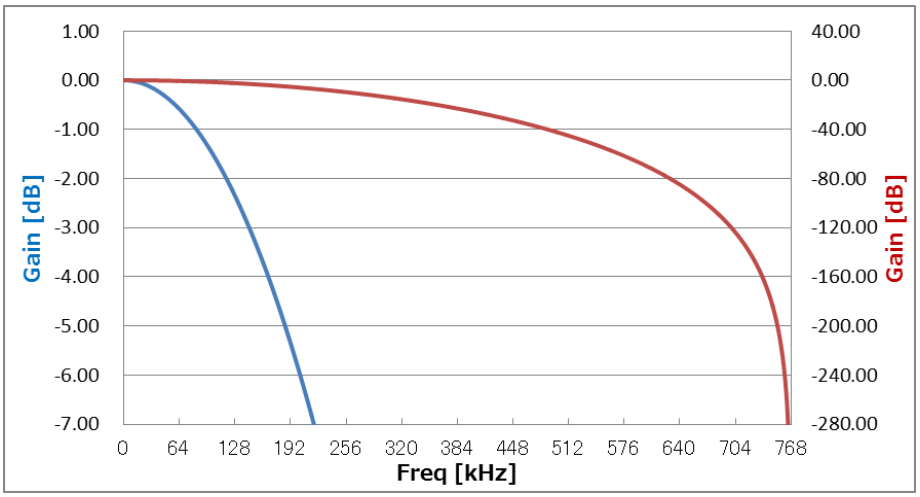


Figure 16. Frequency Response (fs= 768 kHz)

10. DC Characteristics

(Ta= −40-105 °C; AVDD= 4.5-5.5 V, VDD18= 1.7-1.98 V (LDOE pin="L"))

Parameter		Symbol	Min.	Typ.	Max.	Unit
TVDD= 3.0-3.6 V (LDOE pin="H")						
High-Level Input Voltage	(Note 15)	VIH	70%TVDD	-	-	V
Low-Level Input Voltage	(Note 15)	VIL	-	-	30%TVDD	V
High-Level Output Voltage (Iout= −100 µA)	(Note 16)	VOH	TVDD−0.5	-	-	V
Low-Level Output Voltage	(Note 17)					
(except SDA pin: Iout= 100 µA)		VOL	-	-	0.5	V
(SDA pin: Iout= 3 mA)		VOL	-	-	0.4	V
TVDD= 1.7-1.98 V (LDOE pin="L")						
High-Level Input Voltage	(Note 15)	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	(Note 15)	VIL	-	-	20%TVDD	V
High-Level Output Voltage (Iout= −100 µA)	(Note 16)	VOH	TVDD−0.3	-	-	V
Low-Level Output Voltage	(Note 17)					
(except SDA pin: Iout= 100 µA)		VOL	-	-	0.3	V
(SDA pin: Iout= 3 mA)		VOL	-	-	20%TVDD	V
Input Leakage Current		Iin	-	-	±10	µA

Note 15. MCLK, PDN, PW0-2, MSN, BICK (Slave Mode), LRCK (Slave Mode), TDMIN, SLOW/DCKB, SD/PMOD, CKS0/SDA (Write)/CDTI, CKS1/CAD_I2C/CSN, CKS2/SCL/CCLK, CKS3/CAD1, DIF0/DSDSEL0, DIF1/DSDSEL1, TDM0, TDM1, PSN/CAD0_SPI, I2C, DP, DCKS/HPFE, LDOE, ODP and TEST pins.

Note 16. BICK (Master Mode)/DCLK, LRCK (Master Mode)/DSDOL1, DSDOR1, SDTO1/DSDOL2, SDTO2/DSDOR2, SDTO3/DSDOL3, SDTO4/DSDOR3, DSDOL4, DSDOR4 and OVF pins.

Note 17. Pins shown in Note.16 and SDA (Read) pin.
The external pull-up resistors should be connected to TVDD+0.3 V or less.

11. Switching Characteristics

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD= 1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin="L"), C_L= 10 pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Clock (MCLK)Timing (Figure 17, Figure 18)					
Frequency	fCLK	2.048	-	49.152	MHz
Duty Cycle	dCLK	45	-	55	%
LRCK Timing (Slave mode) (Figure 17)					
Normal mode (TDM1-0 bits = "00")					
Frequency	fs				
Normal Speed mode	fsn	8	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
Quad Speed mode	fsq	108	-	216	kHz
Oct speed mode	fso	-	384	-	kHz
Hex speed mode	fsh	-	768	-	kHz
Duty Cycle	Duty	45	-	55	%
TDM128 mode (TDM1-0 bits = "01")					
Frequency	fs				
Normal Speed mode	fsn	8	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
Quad Speed mode	fsq	108	-	216	kHz
High time	tLRH	1/128fs	-	-	ns
Low time	tLRL	1/128fs	-	-	ns
TDM256 mode (TDM1-0 bits = "10")					
Frequency	fs				
Normal Speed mode	fsn	8	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
High time	tLRH	1/256fs	-	-	ns
Low time	tLRL	1/256fs	-	-	ns
TDM512 mode (TDM1-0 bits = "11")					
Frequency	fs				
Normal Speed mode	fsn	8	-	54	kHz
High time	tLRH	1/512fs	-	-	ns
Low time	tLRL	1/512fs	-	-	ns
LRCK Timing (Master mode) (Figure 18)					
Normal mode (TDM1-0 bits = "00")					
Frequency	fs				
Normal Speed mode	fsn	8	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
Quad Speed mode	fsq	108	-	216	kHz
Oct speed mode	fso	-	384	-	kHz
Hex speed mode	fsh	-	768	-	kHz
Duty Cycle	Duty	-	50	-	%
TDM128 mode (TDM1-0 bits = "01")					
Frequency	fs				
Normal Speed mode	fsn	8	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
Quad Speed mode	fsq	108	-	216	kHz
High time	tLRH	-	1/4fs	-	ns
TDM256 mode (TDM1-0 bits = "10")					
Frequency	fs				
Normal Speed mode	fsn	8	-	54	kHz
Double Speed mode	fsd	54	-	108	kHz
High time	tLRH	-	1/8fs	-	ns
TDM512 mode (TDM1-0 bits = "11")					
Frequency	fs				
Normal Speed mode	fsn	8	-	54	kHz
High time	tLRH	-	1/16fs	-	ns

Note 18. When the 1024fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK5558 should be reset by the PDN pin or RSTN bit.

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD= 1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin="L"), C_L= 10 pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Slave mode)					
Normal mode (TDM1-0 bits = "00") (8 kHz ≤ fs ≤ 216 kHz) (Figure 19) (LDOE pin = "H")					
BICK Period					
Normal Speed mode	tBCK	1/128fsn	-	-	ns
Double Speed mode	tBCK	1/128fsd	-	-	ns
Quad Speed mode	tBCK	1/64fsq	-	-	ns
BICK Pulse Width Low	tBCKL	32	-	-	ns
BICK Pulse Width High	tBCKH	32	-	-	ns
LRCK Edge to BICK "↑" (Note 19)	tLRB	25	-	-	ns
BICK "↑" to LRCK Edge (Note 19)	tBLR	25	-	-	ns
LRCK to SDTO (MSB) (Except I^2S mode)	tLRS	-	-	25	ns
BICK "↓"to SDTO1/2/3/4	tBSD	-	-	25	ns
Normal mode (TDM1-0 bits = "00") (8 kHz ≤ fs ≤ 216 kHz) (Figure 19) (LDOE pin = "L")					
BICK Period					
Normal Speed mode (8 kHz ≤ fs ≤ 48 kHz)	tBCK	1/128fsn	-	-	ns
Double Speed mode (48 kHz ≤ fs ≤ 96 kHz)	tBCK	1/128fsd	-	-	ns
Quad Speed mode (96 kHz ≤ fs ≤ 192 kHz)	tBCK	1/64fsq	-	-	ns
BICK Pulse Width Low	tBCKL	36	-	-	ns
BICK Pulse Width High	tBCKH	36	-	-	ns
LRCK Edge to BICK "↑" (Note 19)	tLRB	30	-	-	ns
BICK "↑" to LRCK Edge (Note 19)	tBLR	30	-	-	ns
LRCK to SDTO (MSB) (Except I^2S mode)	tLRS	-	-	30	ns
BICK "↓" to SDTO1/2/3/4	tBSD	-	-	30	ns
Normal mode (TDM1-0 bits = "00") (fs = 384 kHz, 768 kHz) (Figure 20)					
BICK Period					
Oct Speed mode	tBCK	1/64fso	-	-	ns
Hex Speed mode	tBCK	1/48fsh	-	-	ns
BICK Pulse Width Low	tBCKL	12	-	-	ns
BICK Pulse Width High	tBCKH	12	-	-	ns
LRCK Edge to BICK "↑" (Note 19)	tLRB	12	-	-	ns
BICK "↑" to LRCK Edge (Note 19)	tBLR	12	-	-	ns
BICK "↑" to SDTO1/2/3/4	tBSDD	5	-	22	ns

Note 18. When the 1024fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK5558 should be reset by the PDN pin or RSTN bit.

Note 19. BICK rising edge must not occur at the same time as LRCK edge.

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD= 1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin="L"), C_L= 10 pF)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Slave mode) (Figure 21)						
TDM128 mode (TDM1-0 bits = "01")						
BICK Period						
Normal Speed mode		tBCK	1/128fsn	-	-	ns
Double Speed mode		tBCK	1/128fsd	-	-	ns
Quad Speed mode		tBCK	1/128fsq	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 19)	tLRB	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 19)	tBLR	14	-	-	ns
BICK "↑" to SDTO1/2/3/4		tBSDD	5	-	30	ns
TDMIN Hold Time		tSDH	5	-	-	ns
TDMIN Setup Time		tSDS	5	-	-	ns
TDM256 mode (TDM1-0 bits = "10")						
BICK Period						
Normal Speed mode		tBCK	1/256fsn	-	-	ns
Double Speed mode		tBCK	1/256fsd	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 19)	tLRB	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 19)	tBLR	14	-	-	ns
BICK "↑" to SDTO1/2/3/4		tBSDD	5	-	30	ns
TDMIN Hold Time		tSDH	5	-	-	ns
TDMIN Setup Time		tSDS	5	-	-	ns
TDM512 mode (TDM1-0 bits = "11")						
BICK Period						
Normal Speed mode		tBCK	1/512fsn	-	-	ns
BICK Pulse Width Low		tBCKL	14	-	-	ns
BICK Pulse Width High		tBCKH	14	-	-	ns
LRCK Edge to BICK "↑"	(Note 19)	tLRB	14	-	-	ns
BICK "↑" to LRCK Edge	(Note 19)	tBLR	14	-	-	ns
BICK "↑" to SDTO1/2/3/4		tBSDD	5	-	30	ns
TDMIN Hold Time		tSDH	5	-	-	ns
TDMIN Setup Time		tSDS	5	-	-	ns

Note 18. When the 1024fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK5558 should be reset by the PDN pin or RSTN bit.

Note 19. BICK rising edge must not occur at the same time as LRCK edge.

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD= 1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin="L"), C_L= 10 pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Master mode) (Figure 22)					
Normal mode (TDM1-0 bits = "00")					
(8 kHz ≤ fs ≤ 216 kHz)					
BICK Period					
Normal Speed mode	tBCK	-	1/64fsn	-	ns
Double Speed mode	tBCK	-	1/64fsd	-	ns
Quad Speed mode	tBCK	-	1/64fsq	-	ns
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK Edge	tMBLR	−20	-	20	ns
BICK "↓"to SDTO1/2/3/4	tBSD	−20	-	20	ns
Normal mode (TDM1-0 bits = "00")					
(fs = 384kHz, 768 kHz)					
(LDOE pin = "H")					
BICK Period					
Oct speed mode	tBCK	-	1/64fso	-	ns
Hex speed mode	tBCK	-	1/64fsh	-	ns
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK Edge	tMBLR	−4	-	4	ns
BICK "↓" to SDTO1/2/3/4	tBSD	−4	-	4	ns
Normal mode (TDM1-0 bits = "00")					
(fs = 384 kHz,768 kHz)					
(LDOE pin = "L")					
BICK Period					
Oct speed mode	tBCK	-	1/64fso	-	ns
Hex speed mode	tBCK	-	1/48fsh	-	ns
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK Edge	tMBLR	−5	-	5	ns
BICK "↓" to SDTO1/2/3/4	tBSD	−5	-	5	ns

Note 18. When the 1024fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK5558 should be reset by the PDN pin or RSTN bit.

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD= 1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin="L"), C_L= 10 pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Master mode) (Figure 22)					
TDM128 mode (TDM1-0 bits = "01")					
BICK Period					
Normal Speed mode	tBCK	-	1/128fsn	-	ns
Double Speed mode	tBCK	-	1/128fsd	-	ns
Quad Speed mode	tBCK	-	1/128fsq	-	ns
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK Edge	tMBLR	−5	-	5	ns
BICK "↓" to SDTO1/2	tBSD	−5	-	5	ns
TDMIN Hold Time	tSDH	5	-	-	ns
TDMIN Setup Time	tSDS	5	-	-	ns
TDM256 mode (TDM1-0 bits = "10")					
BICK Period					
Normal Speed mode	tBCK	-	1/256fsn	-	ns
Double Speed mode	tBCK	-	1/256fsd	-	ns
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK Edge	tMBLR	−5	-	5	ns
BICK "↓" to SDTO1	tBSD	−5	-	5	ns
TDMIN Hold Time	tSDH	5	-	-	ns
TDMIN Setup Time	tSDS	5	-	-	ns
TDM512 mode (TDM1-0 bits = "11")					
BICK Period					
Normal Speed mode	tBCK	-	1/512fsn	-	ns
BICK Duty	dBCK	-	50	-	%
BICK "↓" to LRCK Edge	tMBLR	−5	-	5	ns
BICK "↓" to SDTO1	tBSD	−5	-	5	ns
TDMIN Hold Time	tSDH	5	-	-	ns
TDMIN Setup Time	tSDS	5	-	-	ns

Note 18. When the 1024fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK5558 should be reset by the PDN pin or RSTN bit.

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD= 1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin="L"), C_L= 10 pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (Master mode) (Figure 23)					
DSD Audio Interface Timing (64fs mode, DSDSEL 1-0 bits = "00")					
DCLK Period	tDCK	-	1/64fs	-	ns
DCLK Pulse Width Low	tDCKL	144	-	-	ns
DCLK Pulse Width High	tDCKH	144	-	-	ns
DCLK Edge to DSDOL/R (Note 20)	tDDD	−20	-	20	ns
DSD Audio Interface Timing (128fs mode, DSDSEL 1-0 bits = "01")					
DCLK Period	tDCK	-	1/128fs	-	ns
DCLK Pulse Width Low	tDCKL	72	-	-	ns
DCLK Pulse Width High	tDCKH	72	-	-	ns
DCLK Edge to DSDOL/R (Note 20)	tDDD	−10	-	10	ns
DSD Audio Interface Timing (256fs mode, DSDSEL 1-0 bits = "10")					
DCLK Period	tDCK	-	1/256fs	-	ns
DCLK Pulse Width Low	tDCKL	36	-	-	ns
DCLK Pulse Width High	tDCKH	36	-	-	ns
DCLK Edge to DSDOL/R (Note 20)	tDDD	−10	-	10	ns

Note 18. When the 1024fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs are switched, the AK5558 should be reset by the PDN pin or RSTN bit.

Note 20. tDDD is defined from a falling edge of DCLK "↓" to a DSDOL/R edge when DCKB bit = "0" and it is defined from a rising edge of DCLK "↑" to a DSDOL/R edge when DCKB bit = "1".

(Ta= −40 - +105 °C; AVDD= 4.5-5.5 V, TVDD= 1.7-1.98 V (LDOE pin="L") or 3.0-3.6 V (LDOE pin="H"), VDD18= 1.7-1.98 V (LDOE pin="L"), C_L= 10 pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (3-Wire Serial mode): (Figure 25) (Figure 26)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Timing	tCDS	40	-	-	ns
CDTI Hold Timing	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
Control Interface Timing (I^2C Bus mode): (Figure 27)					
SCL CLOCK Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Tune (Prior to First Clock Pulse)	tHD STA	0.6	-	-	µs
Clock Low Time	tLow	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 21)	tHD DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	1.0	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive Load on Bus	Cb	-	-	400	pF
Power Down & Reset Timing (Figure 28)					
PDN Pulse Width (Note 22)	tPD	150	-	-	ns
PDN Reject Pulse Width (Note 22)	tRPD	-	-	30	ns
PDN "↑" to SDTO1-4 valid (Note 23)	tPDV	-	583	-	1/fs

Note 21. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 22. The AK5558 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 150 ns for a certain reset. The AK5558 is not reset by the "L" pulse less than 30 ns.

Note 23. This cycle is the number of LRCK rising edges from the PDN pin = "H".