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AK5701

16-Bit ΔΣ Stereo ADC with PLL & MIC-AMP

GENERAL DESCRIPTION

The AK5701 features a 16-bit stereo ADC. Input circuits include a Microphone-Amplifier and an ALC (Auto Level Control) circuit that is suitable for portable application with recording function. On-chip PLL supports base-band clock of mobile phone, therefore it is easy to connect with DSP. The AK5701 is available in a 24-pin QFN, utilizing less board space than competitive offerings.

FEATURES

1. **Resolution: 16bits**
2. **Recording Function**
   - **2 Stereo Input Selector**
   - **Full-differential or Single-ended Input**
   - **MIC Amplifier (+30dB/+15dB or 0dB)**
   - **Input Voltage: 1.8Vpp@VA=3.0V (= 0.6 x AVDD)**
   - **ADC Performance: S/(N+D): 78dB, DR, S/N: 89dB@MGAIN=0dB**
     S/(N+D): 77dB, DR, S/N: 87dB@MGAIN=+15dB
     S/(N+D): 72dB, DR, S/N: 77dB@MGAIN=+30dB
   - **Digital HPF for DC-offset cancellation (fc=3.4Hz@fs=44.1kHz)**
   - **Digital ALC (Automatic Level Control)**
     (+36dB ~ –54dB, 0.375dB Step, Mute)
3. **Sampling Rate:**
   - **PLL Slave Mode (EXLRCK pin): 7.35kHz ~ 48kHz**
   - **PLL Slave Mode (EXBCLK pin): 7.35kHz ~ 48kHz**
   - **PLL Slave Mode (MCKI pin):**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **PLL Master Mode:**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **EXT Slave Mode:**
     7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)
4. **PLL Input Clock:**
   - **MCKI pin:**
     27MHz, 26MHz, 24MHz, 19.2MHz, 13.5MHz, 13MHz, 12.288MHz, 12MHz, 11.2896MHz
   - **EXLRCK pin: 1fs**
   - **EXBCLK pin: 32fs/64fs**
5. **Master/Slave mode**
6. **Audio Interface Format: MSB First, 2's compliment**
   - **DSP Mode, 16bit MSB justified, I^2S**
7. **μP I/F: 3-wire Serial**
8. **Power Supply:**
   - **AVDD: 2.4 ~ 3.6V**
   - **DVDD: 1.6 ~ 3.6V**
9. **Power Supply Current: 8mA**
10. **AK5701VN: Ta = –30 ~ 85°C**
    AK5701KN: Ta = –40 ~ 85°C
11. **Package: 24-pin QFN (4mm x 4mm)**
12. **AEC-Q100 Qualified (AK5701KN)**

■ Block Diagram

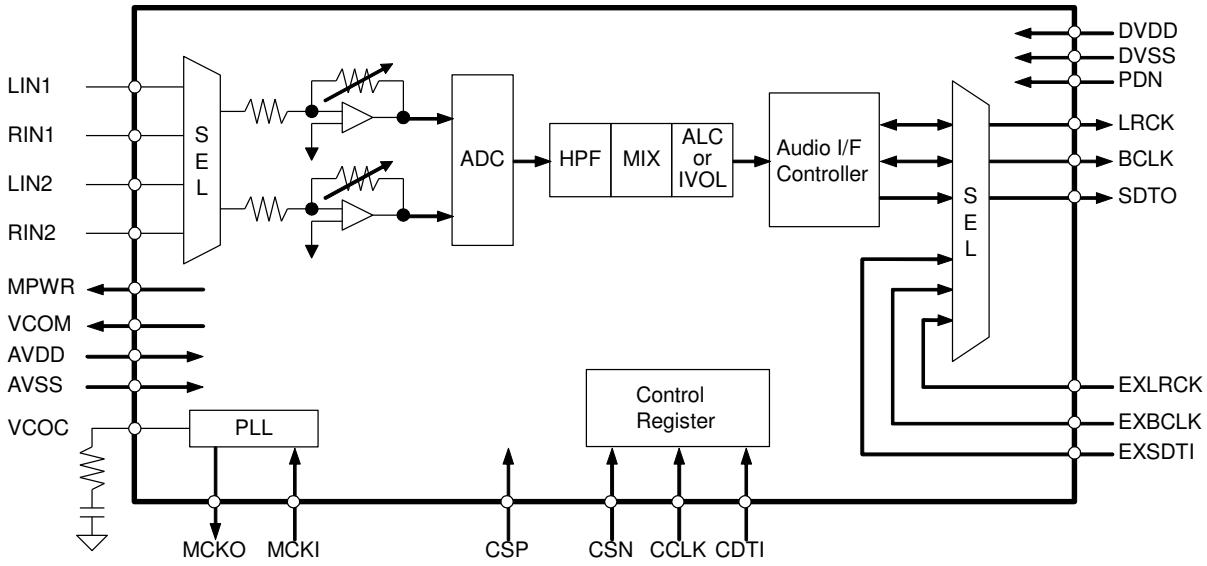
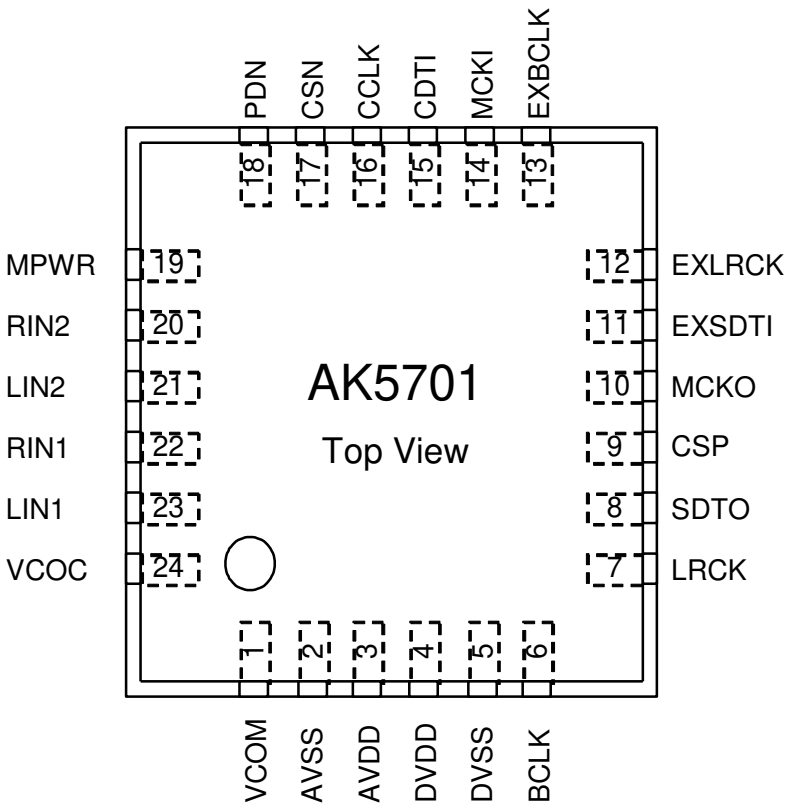


Figure 1. Block Diagram

■ Ordering Guide

AK5701VN	−30 ~ +85°C	24-pin QFN (0.5mm pitch)
AK5701KN	−40 ~ +85°C	24-pin QFN (0.5mm pitch)
AKD5701	Evaluation board for AK5701	

■ Pin Layout



■ Comparison with AK5355VN

Function	AK5355VN	AK5701
Input Selector	No	Yes
Input Gain	+15dB/0dB	+30dB/+15dB/0dB
Mic Bias	No	Yes
ALC	No	Yes
Mono Mic Mode	No	Yes
Audio I/F Format	Left justified, I^2S	DSP Mode, Left justified, I^2S
PLL	No	Yes
Master Mode	No	Yes
Output Data Selector	No	Yes
Serial Control	No	Yes
Power Supply	2.1 ~ 3.6V	AVDD=2.4 ~ 3.6V DVDD=1.6 ~ 3.6V
Package	20-pin QFN (4.2mm x 4.2mm)	24-pin QFN (4mm x 4mm)
Ambient Temperature	−40 ~ +85°C	AK5701VN : −30 ~ +85°C AK5701KN : −40 ~ +85°C

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD Bias voltage of ADC inputs.
2	AVSS	-	Analog Ground Pin
3	AVDD	-	Analog Power Supply Pin
4	DVDD	-	Digital Power Supply Pin
5	DVSS	-	Digital Ground Pin
6	BCLK	O	Audio Serial Data Clock Pin
7	LRCK	O	Input / Output Channel Clock Pin
8	SDTO	O	Audio Serial Data Output Pin
9	CSP	I	Chip Select Polarity Pin "H": CSN pin = "H" active, C1-0 = "01" "L": CSN pin = "L" active, C1-0 = "10"
10	MCKO	O	Master Clock Output Pin
11	EXSDTI	I	External Audio Serial Data Input Pin
12	EXLRCK	I	External Input / Output Channel Clock Pin
13	EXBCLK	I	External Audio Serial Data Clock Pin
14	MCKI	I	External Master Clock Input Pin
15	CDTI	I	Control Data Input Pin
16	CCLK	I	Control Data Clock Pin (Internal Pull-down at CSP pin = "H")
17	CSN	I	Chip Select Pin
18	PDN	I	Power-Down Mode Pin "H": Power-up, "L": Power-down, reset and initializes the control register.
19	MPWR	O	MIC Power Supply Pin
20	RIN2	I	Rch Analog Input 2 Pin (MDIF2 bit = "0")
	RIN+	I	Rch Positive Input Pin (MDIF2 bit = "1")
21	LIN2	I	Lch Analog Input 2 Pin (MDIF2 bit = "0")
	RIN–	I	Rch Negative Input Pin (MDIF2 bit = "1")
22	RIN1	I	Rch Analog Input 1 Pin (MDIF1 bit = "0")
	LIN–	I	Lch Negative Input Pin (MDIF1 bit = "1")
23	LIN1	I	Lch Analog Input 1 Pin (MDIF1 bit = "0")
	LIN+	I	Lch Positive Input Pin (MDIF1 bit = "1")
24	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to AVSS with one resistor and capacitor in series.

Note 1. All input pins except analog input pins (LIN1, RIN1, LIN2, RIN2) should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, VCOC, LIN1/LIN+, RIN1/LIN–, LIN2/RIN–, RIN2/RIN+	These pins should be open.
Digital	BCLK, LRCK, SDTO, MCKO	These pins should be open.
	MCKI, EXBCLK, EXLRCK, EXSDTI	These pins should be connected to DVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 2)

Parameter			Symbol	Min.	Max.	Unit
Power Supplies:	Analog		AVDD	–0.3	4.6	V
	Digital		DVDD	–0.3	4.6	V
	|AVSS – DVSS| (Note 3)		ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies			IIN	-	±10	mA
Analog Input Voltage (Note 4)			VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 5)			VIND	–0.3	DVDD+0.3	V
Ambient Temperature		AK5701VN	Ta	–30	85	°C
(powered applied)		AK5701KN	Ta	–40	85	°C
Storage Temperature			Tstg	–65	150	°C

Note 2. All voltages with respect to ground.
Note 3. AVSS and DVSS must be connected to the same analog ground plane.
Note 4. LIN1/LIN+, RIN1/LIN–, LIN2/RIN–, RIN2/RIN+ pins
Note 5. PDN, CSN, CCLK, CDTI, CSP, MCKI, EXSDTI, EXLRCK, EXBCLK pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog	AVDD	2.4	3.0	3.6	V
(Note 6)	Digital	DVDD	1.6	3.0	AVDD	V

Note 2. All voltages with respect to ground.
Note 6. The power-up sequence between AVDD and DVDD is not critical. When only AVDD is powered OFF, the power supply current of DVDD at power-down mode may be increased. DVDD should not be powerd OFF while AVDD is powered ON.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=3.0V; AVSS=DVSS=0V; PLL Master Mode; MCKI=12MHz, fs=44.0995kHz, BCLK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter		Min.	Typ.	Max.	Unit
MIC Amplifier: LIN1, RIN1, LIN2, RIN2 pins; MDIF1 = MDIF2 bits = "0" (Single-ended inputs)					
Input Resistance	MGAIN1-0 bits = "00"	40	60	80	kΩ
	MGAIN1-0 bits = "01" or "10"	20	30	40	kΩ
Gain	MGAIN1-0 bits = "00"	-	0	-	dB
	MGAIN1-0 bits = "01"	-	+15	-	dB
	MGAIN1-0 bits = "10"	-	+30	-	dB
MIC Amplifier: LIN+, LIN−, RIN+, RIN− pins; MDIF1 = MDIF2 bits = "1" (Full-differential input)					
Input Voltage (Note 7)					
	MGAIN1-0 bits = "01"	-	-	0.37	Vpp
	MGAIN1-0 bits = "10"	-	-	0.066	Vpp
MIC Power Supply: MPWR pin					
Output Voltage (Note 8)		2.02	2.25	2.48	V
Load Resistance		0.5	-	-	kΩ
Load Capacitance		-	-	30	pF
ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2 pins (Single-ended inputs) → ADC → IVOL, MGAIN=+15dB, IVOL=0dB, ALC=OFF					
Resolution		-	-	16	Bits
Input Voltage (Note 9)	MGAIN=+30dB	-	0.057	-	Vpp
	MGAIN=+15dB	0.27	0.32	0.37	Vpp
	MGAIN=0dB	1.53	1.80	2.07	Vpp
S/(N+D) (−0.5dBFS) (Note 10)		67	77	-	dB
D-Range (−60dBFS, A-weighted) (Note 11)		79	87	-	dB
S/N (A-weighted) (Note 11)		79	87	-	dB
Interchannel Isolation (Note 12)		80	90	-	dB
Interchannel Gain Mismatch	MGAIN=+30dB	-	0.2	-	dB
	MGAIN=+15dB	-	0.2	1.0	dB
	MGAIN=0dB	-	0.2	0.5	dB
Power Supplies:					
Power Supply Current: AVDD+DVDD					
Power Up (PDN pin = "H") (Note 13)		-	8	12	mA
Power Down (PDN pin = "L") (Note 14)		-	1	20	μA

Note 7. The voltage difference between LIN+/RIN+ and LIN−/RIN− pins. AC coupling capacitor should be connected in series at each input pin. Full-differential input is not available at MGAIN1-0 bits = "00". Maximum input voltage of LIN+, LIN−, RIN+ and RIN− pins is proportional to AVDD voltage, respectively.
Vin = |(L/RIN+) − (L/RIN−)| = 0.123 x AVDD (max)@MGAIN1-0 bits = "01", 0.022 x AVDD (max)@MGAIN1-0 bits = "10".
When the signal larger than above value is input to LIN+, LIN−, RIN+ or RIN− pin, ADC does not operate normally.

Note 8. Output voltage is proportional to AVDD voltage. Vout = 0.75 x AVDD (typ).

Note 9. Input voltage is proportional to AVDD voltage. Vin = 0.107 x AVDD (typ)@MGAIN1-0 bits = "01" (+15dB), Vin = 0.6 x AVDD(typ)@MGAIN1-0 bits = "00" (0dB).

Note 10. 80dB(typ)@MGAIN=0dB, 70dB(typ)@MGAIN=+30dB

Note 11. 89dB(typ)@MGAIN=0dB, 77dB(typ)@MGAIN=+30dB

Note 12. 100dB(typ)@MGAIN=0dB, 80dB(typ)@MGAIN=+30dB

Note 13. PLL Master Mode (MCKI=12MHz), PMADL = PMADR = PMVCM = PMPLL = PMMP = M/S bits = "1" and MCKO bit = "0". MPWR pin outputs 0mA. AVDD=6.4mA(typ), DVDD=1.6mA(typ).
EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=5.7mA(typ), DVDD=1.3mA(typ).
Bypass Mode (THR bit = "1", PMADL = PMADR = M/S bits = "0"), fs=8kHz: AVDD=1μA(typ), DVDD=150μA(typ).

Note 14. All digital input pins are fixed to DVDD or DVSS.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V; fs=44.1kHz)

Parameter		Symbol	Min.	Typ.	Max.	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 15)	±0.1dB	PB	0	-	17.4	kHz
	−1.0dB		-	20.0	-	kHz
	−3.0dB		-	21.1	-	kHz
Stopband (Note 15)		SB	25.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	65	-	-	dB
Group Delay (Note 16)		GD	-	18	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPF1-0 bits = "00"						
Frequency Response (Note 15)	−3.0dB	FR	-	3.4	-	Hz
	−0.5dB		-	10	-	Hz
	−0.1dB		-	22	-	Hz

Note 15. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.454*fs (@−1.0dB). Each response refers to that of 1kHz.

Note 16. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF.

DC CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage						
Except CSP pin; 2.2V≤ DVDD ≤3.6V		VIH	70%DVDD	-	-	V
Except CSP pin; 1.6V≤ DVDD <2.2V		VIH	80%DVDD	-	-	V
CSP pin		VIH	90%DVDD	-	-	V
Low-Level Input Voltage						
Except CSP pin; 2.2V≤ DVDD ≤3.6V		VIL	-	-	30%DVDD	V
Except CSP pin; 1.6V≤ DVDD <2.2V		VIL	-	-	20%DVDD	V
CSP pin		VIL	-	-	10%DVDD	V
High-Level Output Voltage	(Iout= −200μA)	VOH	DVDD−0.2	-	-	V
Low-Level Output Voltage	(Iout= 200μA)	VOL	-	-	0.2	V
Input Leakage Current (Note 17)		Iin	-	-	±10	μA

Note 17. When CSP pin is "H", CCLK pin has internal pull-down device, normally 100kΩ.

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)					
MCKI Input Timing					
Frequency	fCLK	11.2896	-	27	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing					
Frequency	fMCK	0.2352	-	12.288	MHz
Duty Cycle					
Except 256fs at fs=32kHz, 29.4kHz	dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz	dMCK	-	33	-	%
LRCK Output Timing					
Frequency					
Except DSP Mode 1	fs	7.35	-	48	kHz
DSP Mode 1 (Note 18)	fsd	14.7	-	96	kHz
DSP Mode: Pulse Width High	tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle	Duty	-	50	-	%
BCLK Output Timing					
Period BCKO1-0 bit = "01"	tBCK	-	1/(32fs)	-	ns
Period BCKO1-0 bit = "10"	tBCK	-	1/(64fs)	-	ns
Duty Cycle	dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)					
MCKI Input Timing					
Frequency	fCLK	11.2896	-	27	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing					
Frequency	fMCK	0.2352	-	12.288	MHz
Duty Cycle					
Except 256fs at fs=32kHz, 29.4kHz	dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz	dMCK	-	33	-	%
EXLRCK Input Timing					
Frequency	fs	7.35	-	48	kHz
DSP Mode: Pulse Width High	tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle	Duty	45	-	55	%
EXBCLK Input Timing					
Period	tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns
PLL Slave Mode (PLL Reference Clock = EXLRCK pin)					
EXLRCK Input Timing					
Frequency	fs	7.35	-	48	kHz
DSP Mode: Pulse Width High	tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle	Duty	45	-	55	%
EXBCLK Input Timing					
Period	tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns

Note 18. Sampling frequency is 7.35kHz ~ 48kHz.

Parameter			Symbol	Min.	Typ.	Max.	Unit
PLL Slave Mode (PLL Reference Clock = EXBCLK pin)							
EXLRCK Input Timing							
Frequency			fs	7.35	-	48	kHz
DSP Mode: Pulse Width High			tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle			Duty	45	-	55	%
EXBCLK Input Timing							
Period	PLL3-0 bits = “0010”		tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = “0011”		tBCK	-	1/(64fs)	-	ns
Pulse Width Low			tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High			tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	1.8816	-	12.288	MHz
	512fs		fCLK	3.7632	-	13.312	MHz
	1024fs		fCLK	7.5264	-	13.312	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
EXLRCK Input Timing							
Frequency	256fs		fs	7.35	-	48	kHz
	512fs		fs	7.35	-	26	kHz
	1024fs		fs	7.35	-	13	kHz
DSP Mode: Pulse Width High			tLRCKH	tBCK−60	-	1/fs − tBCK	ns
Except DSP Mode: Duty Cycle			Duty	45	-	55	%
EXBCLK Input Timing							
Period			tBCK	312.5	-	-	ns
Pulse Width Low			tBCKL	130	-	-	ns
Pulse Width High			tBCKH	130	-	-	ns
External Master Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	1.8816	-	12.288	MHz
	512fs		fCLK	3.7632	-	13.312	MHz
	1024fs		fCLK	7.5264	-	13.312	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	ns
Pulse Width High			tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing							
Frequency			fs	7.35	-	48	kHz
DSP Mode: Pulse Width High			tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle			Duty	-	50	-	%
BCLK Output Timing							
Period	BCKO1-0 bit = “01”		tBCK	-	1/(32fs)	-	ns
	BCKO1-0 bit = “10”		tBCK	-	1/(64fs)	-	ns
Duty Cycle			dBCK	-	50	-	%

Parameter	Symbol	Min.	Typ.	Max.	Unit
Audio Interface Timing (DSP Mode)					
Master Mode					
LRCK "↑" to BCLK "↑" (Note 19)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
LRCK "↑" to BCLK "↓" (Note 20)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
BCLK "↑" to SDTO (BCKP bit = "0")	tBSD	–70	-	70	ns
BCLK "↓" to SDTO (BCKP bit = "1")	tBSD	–70	-	70	ns
Slave Mode					
EXLRCK "↑" to EXBCLK "↑" (Note 19)	tLRB	0.4 x tBCK	-	-	ns
EXLRCK "↑" to EXBCLK "↓" (Note 20)	tLRB	0.4 x tBCK	-	-	ns
EXBCLK "↑" to EXLRCK "↑" (Note 19)	tBLR	0.4 x tBCK	-	-	ns
EXBCLK "↓" to EXLRCK "↑" (Note 20)	tBLR	0.4 x tBCK	-	-	ns
EXBCLK "↑" to SDTO (BCKP bit = "0")	tBSD	-	-	80	ns
EXBCLK "↓" to SDTO (BCKP bit = "1")	tBSD	-	-	80	ns
Audio Interface Timing (Left justified & I^2S)					
Master Mode					
BCLK "↓" to LRCK Edge (Note 21)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)	tLRD	–70	-	70	ns
BCLK "↓" to SDTO	tBSD	–70	-	70	ns
Slave Mode					
EXLRCK Edge to EXBCLK "↑" (Note 21)	tLRB	50	-	-	ns
EXBCLK "↑" to EXLRCK Edge (Note 21)	tBLR	50	-	-	ns
EXLRCK Edge to SDTO (MSB) (Except I^2S mode)	tLRD	-	-	80	ns
EXBCLK "↓" to SDTO	tBSD	-	-	80	ns

Note 19. MSBS, BCKP bits = "00" or "11"
Note 20. MSBS, BCKP bits = "01" or "10"
Note 21. EXBCLK rising edge must not occur at the same time as EXLRCK edge.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (CSP pin = "L")					
CCLK Period	tCCK	142	-	-	ns
CCLK Pulse Width Low	tCCKL	56	-	-	ns
Pulse Width High	tCCKH	56	-	-	ns
CDTI Setup Time	tCDS	28	-	-	ns
CDTI Hold Time	tCDH	28	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 22)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 22)	tCSH	50	-	-	ns
Control Interface Timing (CSP pin = "H")					
CCLK Period	tCCK	142	-	-	ns
CCLK Pulse Width Low	tCCKL	56	-	-	ns
Pulse Width High	tCCKH	56	-	-	ns
CDTI Setup Time	tCDS	28	-	-	ns
CDTI Hold Time	tCDH	28	-	-	ns
CSN "L" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 22)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 22)	tCSH	50	-	-	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 23)	tPD	150	-	-	ns
PMADL or PMADR "↑" to SDTO valid (Note 24)					
HPF1-0 bits = "00"	tPDV	-	3088	-	1/fs
HPF1-0 bits = "01"	tPDV	-	1552	-	1/fs
HPF1-0 bits = "10"	tPDV	-	784	-	1/fs

Note 22. CCLK rising edge must not occur at the same time as CSN edge.
Note 23. The AK5701 can be reset by the PDN pin = "L".
Note 24. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

■ Timing Diagram

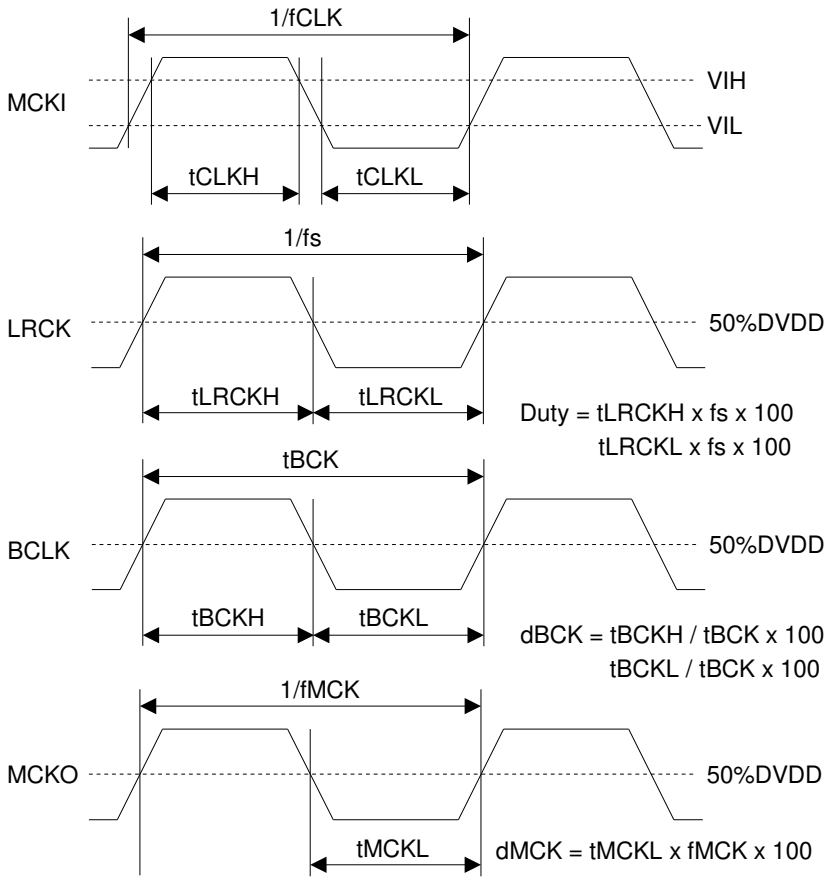


Figure 2. Clock Timing (PLL/EXT Master mode)

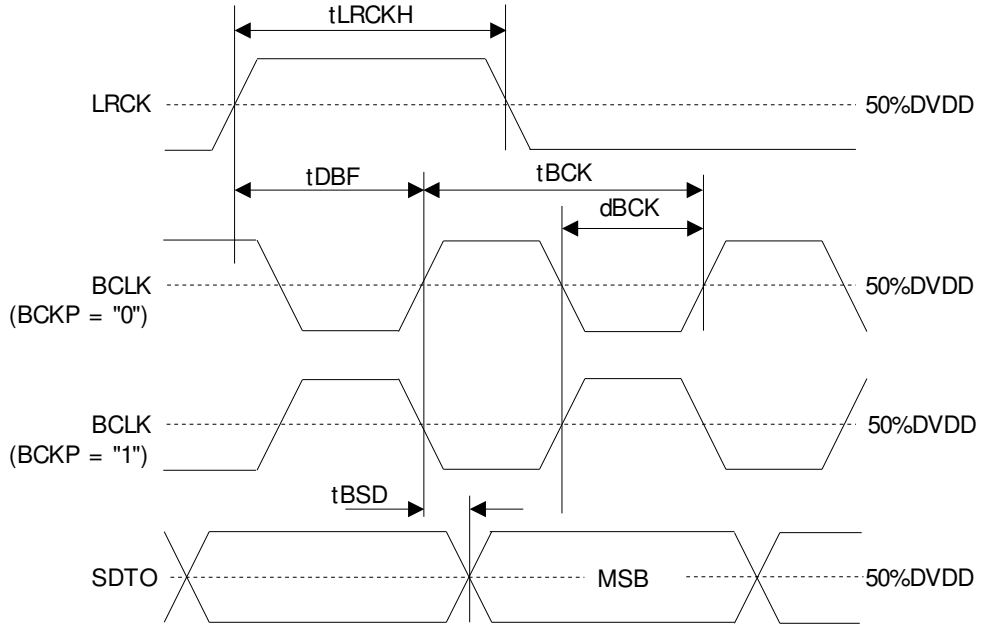


Figure 3. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS = “0”)

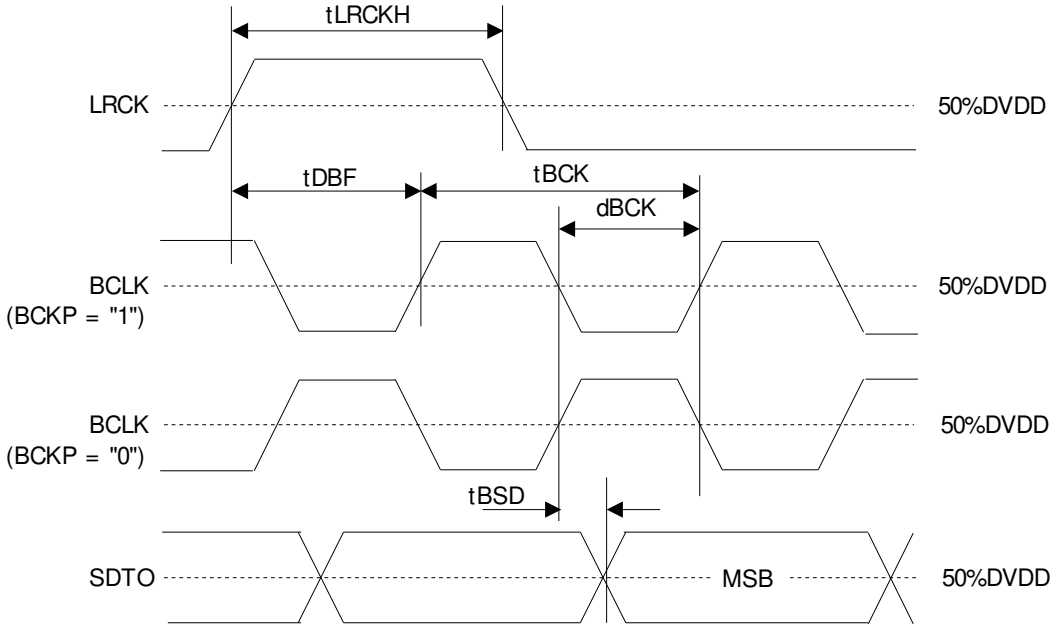


Figure 4. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS = "1")

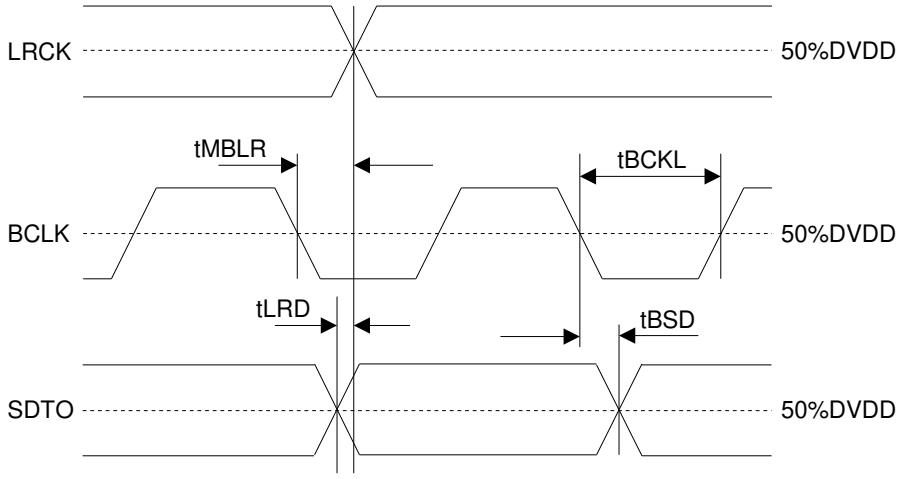


Figure 5. Audio Interface Timing (PLL/EXT Master mode & Except DSP mode)

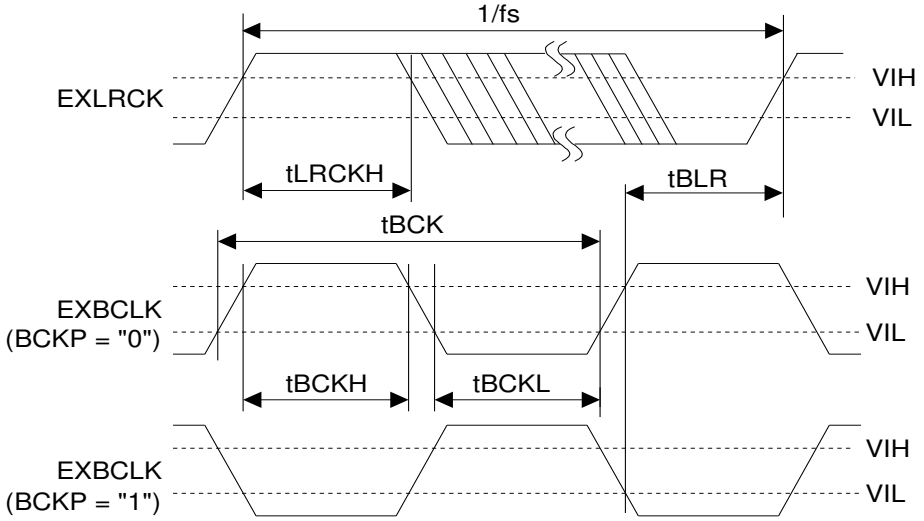


Figure 6. Clock Timing (PLL Slave mode; PLL Reference Clock = EXLRCK or EXBCLK pin & DSP mode; MSBS = 0)

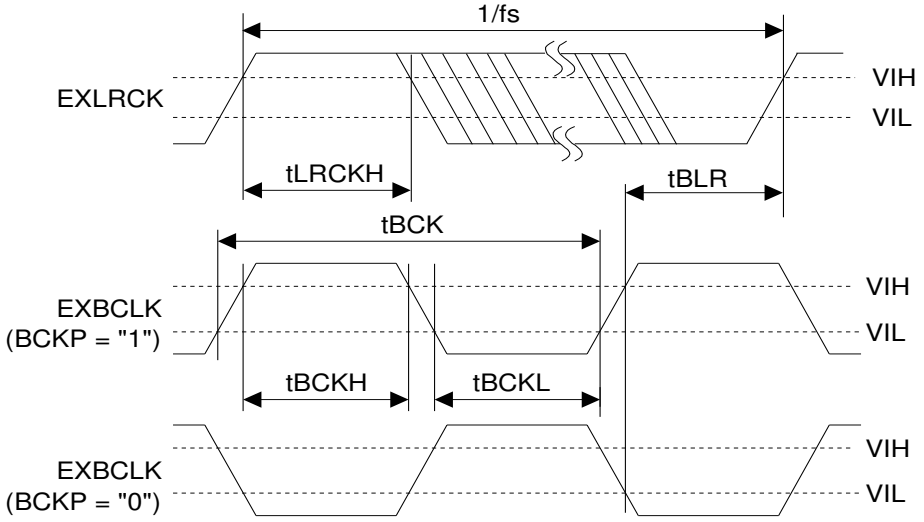


Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = EXLRCK or EXBCLK pin & DSP mode; MSBS = 1)

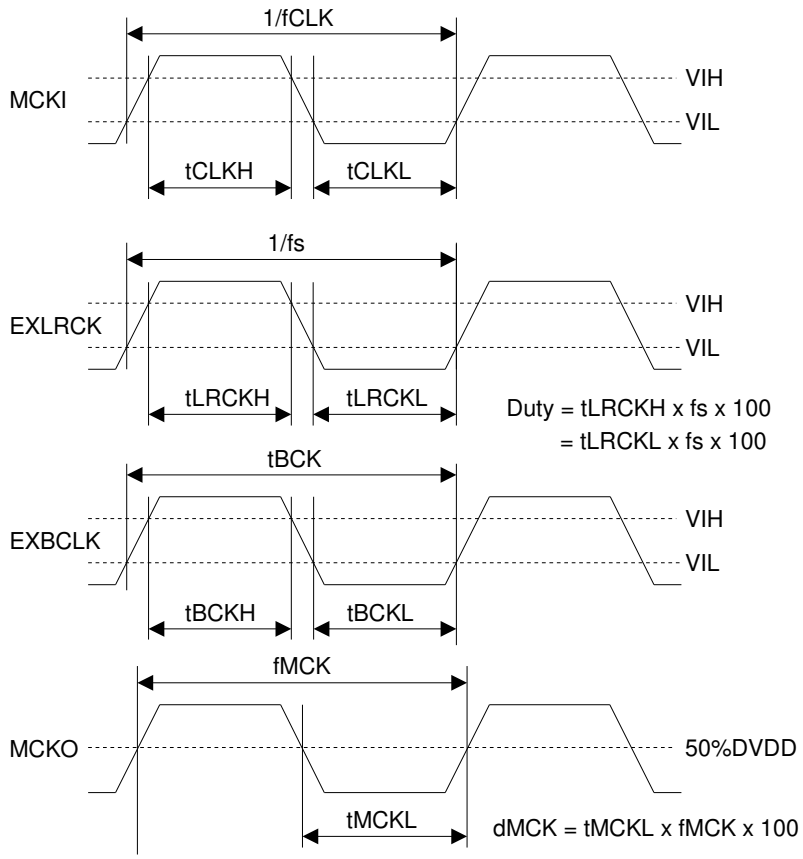


Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin & Except DSP mode)

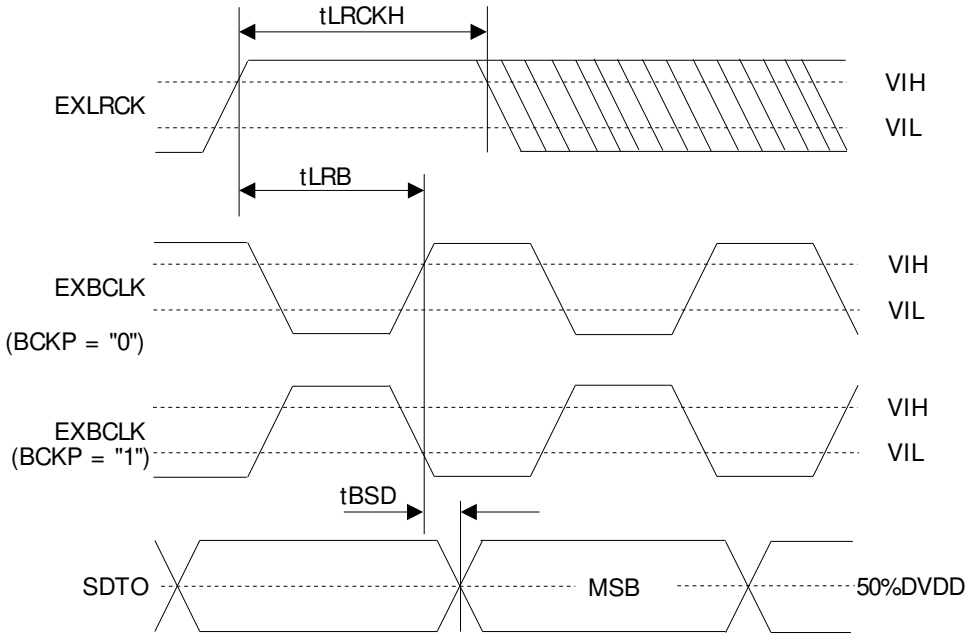


Figure 9. Audio Interface Timing (PLL Slave mode & DSP mode; MSBS = 0)

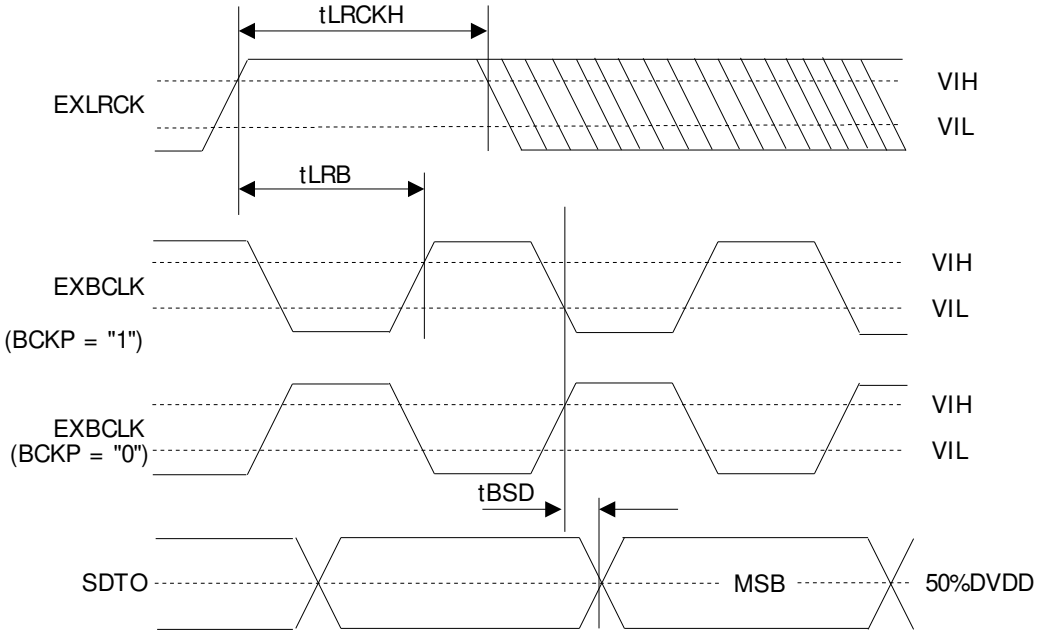


Figure 10. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = 1)

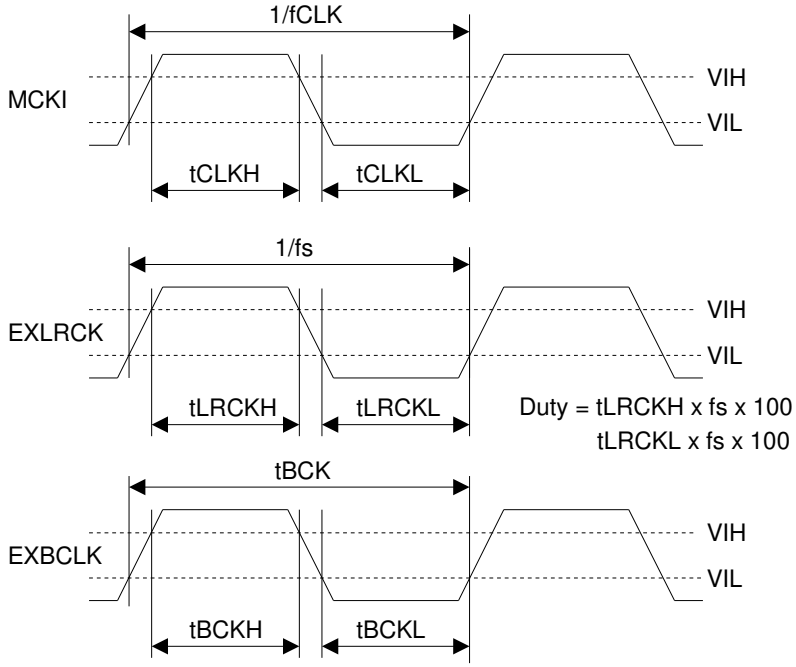


Figure 11. Clock Timing (EXT Slave mode)

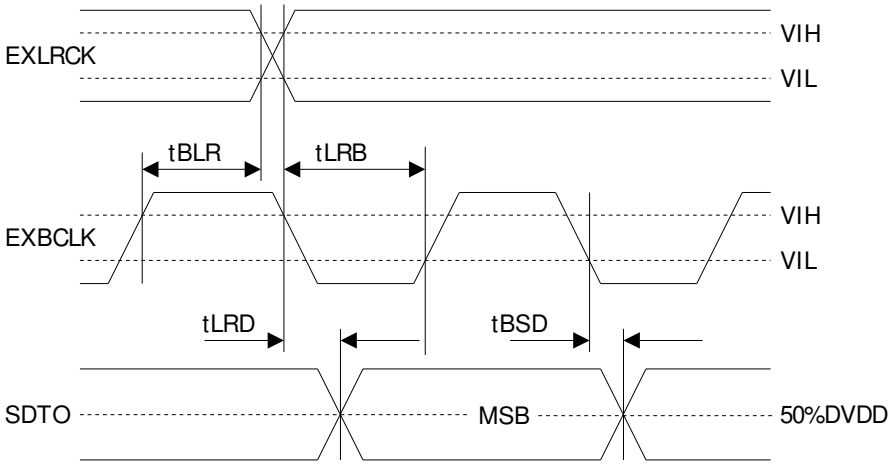


Figure 12. Audio Interface Timing (PLL/EXT Slave mode)

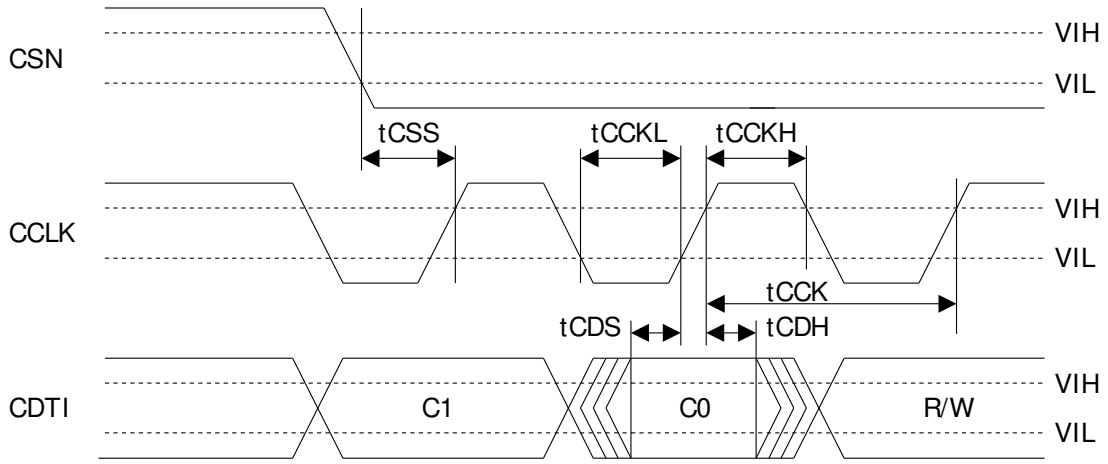


Figure 13. WRITE Command Input Timing (CSP pin = "L")

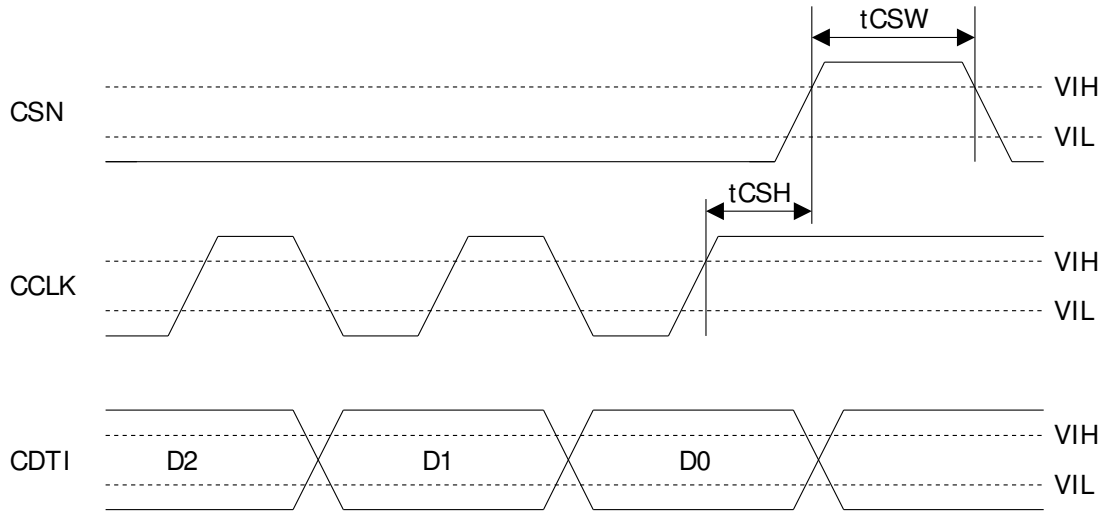


Figure 14. WRITE Data Input Timing (CSP pin = "L")

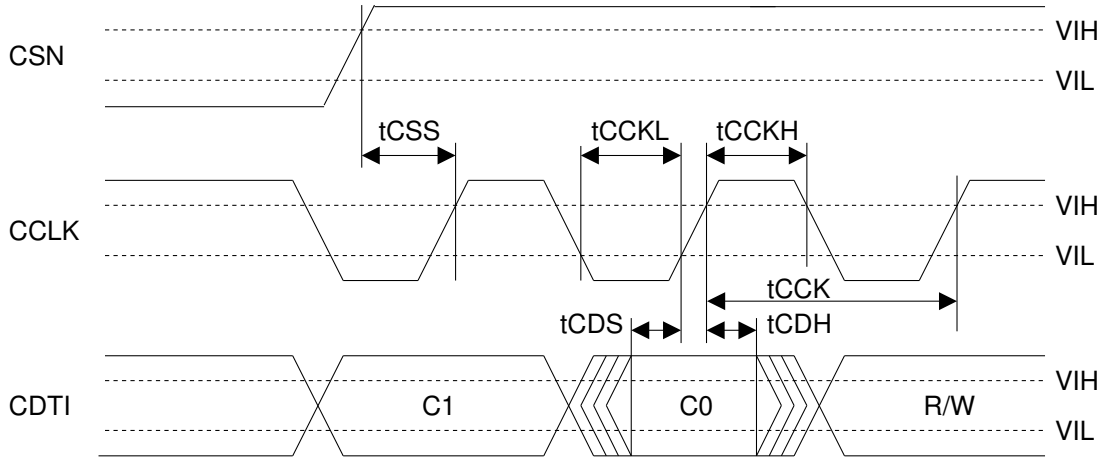


Figure 15. WRITE Command Input Timing (CSP pin = "H")

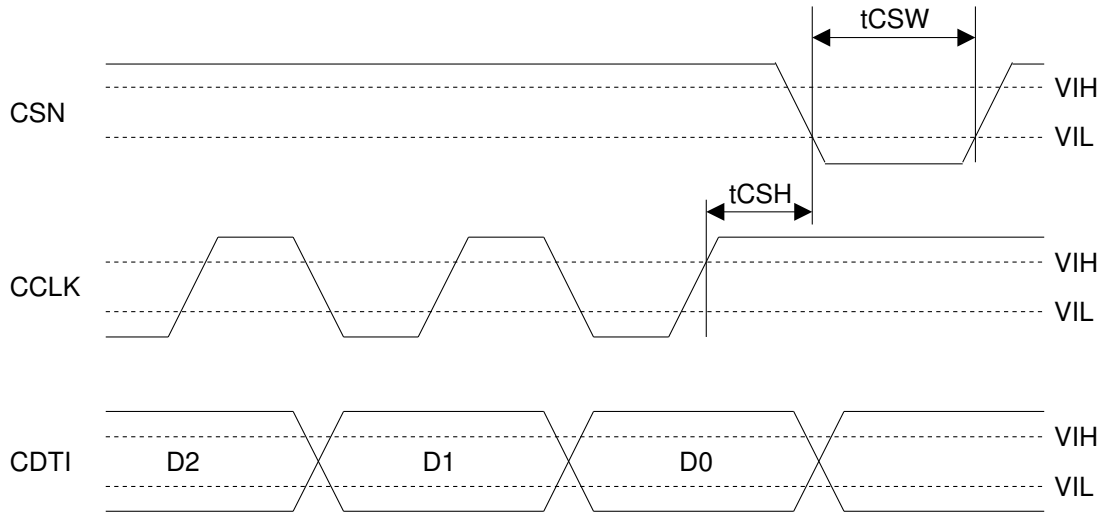


Figure 16. WRITE Data Input Timing (CSP pin = "H")

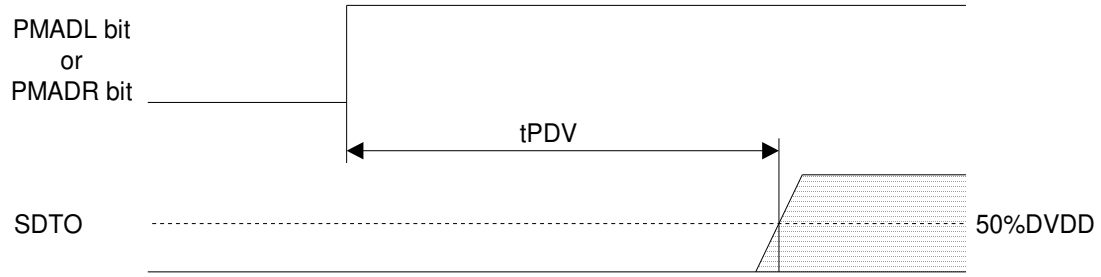


Figure 17. Power Down & Reset Timing 1

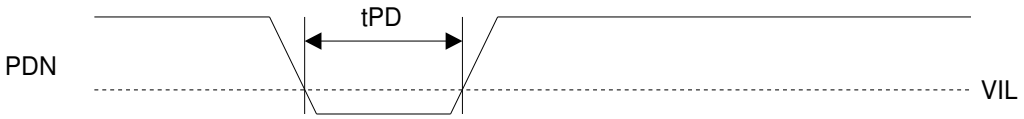


Figure 18. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 1 and Table 2)

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 25)	1	1	See Table 4	Figure 19
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	See Table 4	Figure 20
PLL Slave Mode 2 (PLL Reference Clock: EXLRCK or EXBCLK pin)	1	0	See Table 4	Figure 21
EXT Slave Mode	0	0	x	Figure 22
EXT Master Mode (Note 26)	0	0	x	Figure 23

Note 25. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from the MCKO pin when MCKO bit is "1".

Note 26. In case of EXT Master Mode, the register should be set as Figure 49.

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BCLK pin, EXBCLK pin	LRCK pin, EXLRCK pin
PLL Master Mode	0	L	Selected by PLL3-0 bits	BCLK pin (Selected by BCKO1-0 bits)	LRCK pin (1fs) (Note 27)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	L	Selected by PLL3-0 bits	EXBCLK pin (≥ 32fs)	EXLRCK pin (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: EXLRCK or EXBCLK pin)	0	L	GND	EXBCLK pin (Selected by PLL3-0 bits)	EXLRCK pin (1fs)
EXT Slave Mode	0	L	Selected by FS1-0 bits	EXBCLK pin (≥ 32fs)	EXLRCK pin (1fs)
EXT Master Mode	0	L	Selected by FS1-0 bits	BCLK pin (Selected by BCKO1-0 bits)	LRCK pin (1fs)

Note 27. LRCK becomes 2fs at PLL Master Mode & DSP Mode 1.

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK5701 is power-down mode (PDN pin = "L") and exits reset state, the AK5701 is slave mode. After exiting reset state, the AK5701 goes to master mode by changing M/S bit = "1".

M/S bit	Mode	Used pins	
0	Slave Mode	EXBCLK, EXLRCK	(default)
1	Master Mode	BCLK, LRCK	

Table 3. Select Master/Salve Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, whenever the AK5701 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes.

1) Setting of PLL Mode

Mode	PLL3 bit	PLL2 Bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	EXLRCK pin	1fs	6.8k	220n	80ms	
2	0	0	1	0	EXBCLK pin	32fs	10k	4.7n	2ms	
							10k	10n	4ms	
3	0	0	1	1	EXBCLK pin	64fs	10k	4.7n	2ms	
							10k	10n	4ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	40ms	
5	0	1	0	1	MCKI pin	12.288MHz	10k	4.7n	40ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	40ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	40ms	
8	1	0	0	0	MCKI pin	19.2MHz	10k	4.7n	40ms	
9	1	0	0	1	MCKI pin	12MHz (Note 28)	10k	4.7n	40ms	(default)
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	40ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	40ms	
14	1	1	1	0	MCKI pin	13MHz	10k	220n	60ms	
15	1	1	1	1	MCKI pin	26MHz	10k	220n	60ms	
Others	Others				N/A					

Note 28. Please see Table 5 regarding the difference between PLL3-0 bits = "0110"(Mode 6) and "1001"(Mode 9).

Table 4. Setting of PLL Mode (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz 7.349918kHz (Note 29)	
5	0	1	0	1	11.025kHz 11.024877kHz (Note 29)	
6	0	1	1	0	14.7kHz 14.69984kHz (Note 29)	
7	0	1	1	1	22.05kHz 22.04975kHz (Note 29)	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz 29.39967kHz (Note 29)	
15	1	1	1	1	44.1kHz 44.0995kHz (Note 29)	(default)
Others	Others				N/A	

Note 29. In case of PLL3-0 bits = "1001"

Table 5. Setting of Sampling Frequency at PMPLL bit = "1" and Reference Clock=MCKI pin

When PLL reference clock input is EXLRCK or EXBCLK pin, the sampling frequency is selected by FS3 and FS2 bits (Table 6).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	x	x	7.35kHz ≤ fs ≤ 12kHz	
1	0	1	x	x	12kHz < fs ≤ 24kHz	
2	1	x	x	x	24kHz < fs ≤ 48kHz	(default)
Others	Others				N/A	

(x: Don't acre, N/A: Not available)

Table 6. Setting of Sampling Frequency at PMPLL bit = "1" and Reference=EXLRCK/EXBCLK

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, LRCK and BCLK pins go to "L" and irregular frequency clock is output from the MCKO pin at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin changes to "L" (Table 7).

In DSP Mode 0 and 1, BCLK and LRCK start to output corresponding to Lch data after PLL goes to lock state by setting PMPLL bit = "0" → "1". When MSBS and BCKP bits are "01" or "10" in DSP Mode 0 and 1, BCLK "H" time of the first pulse becomes 1/(256fs) shorter than "H" time except for the first pulse.

When sampling frequency is changed, BCLK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BCLK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After that PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except above case)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	See Table 9	See Table 10	1fs Output (Note 30)

Note 30. LRCK becomes 2fs at DSP Mode 1.

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". After that, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal should be muted by writing "0" to DACL, DACH and DACS bits.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock (except above case)	"L" Output	Invalid
PLL Lock	"L" Output	See Table 9

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to MCKI pin, the MCKO, BCLK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BCLK output frequency is selected among 32fs or 64fs, by BCKO1-0 bits (Table 10).

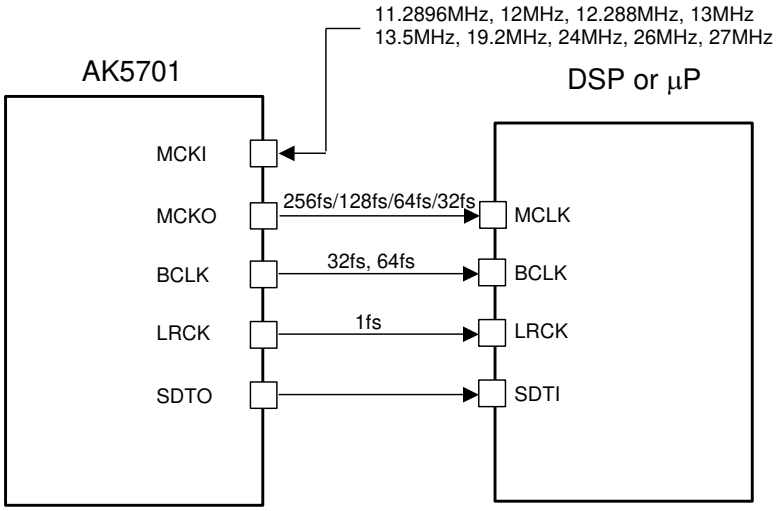


Figure 19. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO1 bit	BCKO0 bit	BCLK Output Frequency	
0	0	N/A	
0	1	32fs	(default)
1	0	64fs	
1	1	N/A	

Table 10. BCLK Output Frequency at Master Mode (N/A: Not available)

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to the MCKI, EXBCLK or EXLRCK pin. The required clock to the AK5701 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL reference clock: MCKI pin

EXBCLK and EXLRCK inputs should be synchronized with MCKO output. The phase between MCKO and EXLRCK is not important. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

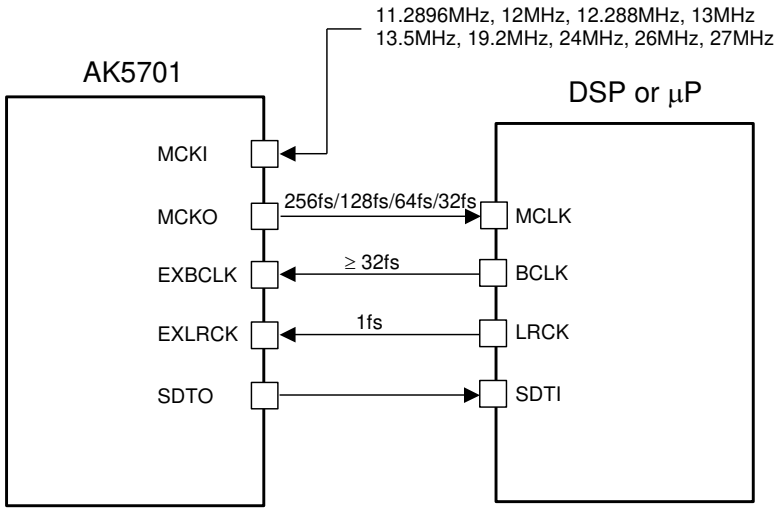


Figure 20. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

The external clocks (MCKI, EXBCLK and EXLRCK) should always be present whenever the ADC is in operation (PMADL bit = "1" or PMADR bit = "1"). If these clocks are not provided, the AK5701 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC should be in the power-down mode (PMADL=PMADR bits = "0").

b) PLL reference clock: EXBCLK or EXLRCK pin

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits (Table 6).

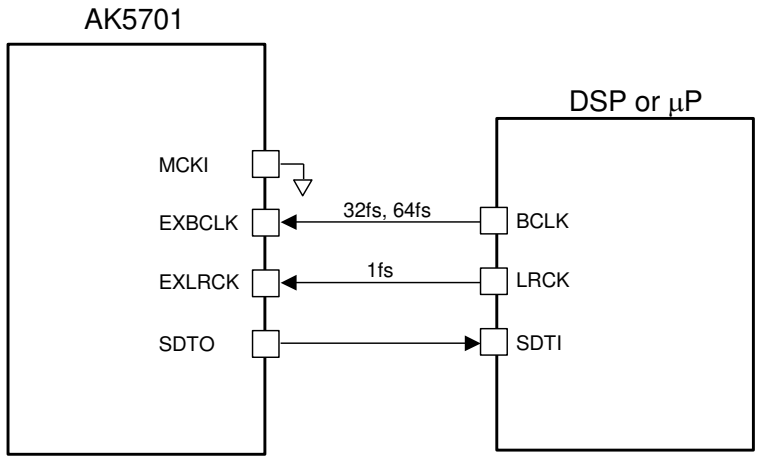


Figure 21. PLL Slave Mode 2 (PLL Reference Clock: EXLRCK or EXBCLK pin)