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AK5703

4-Channel 24-bit ADC with PLL & MIC-AMP

GENERAL DESCRIPTION

The AK5703 is a 4-channel 24-bit A/D converter with programmable microphone amplifiers and ALC (Automatic Level Control) circuit. It is designed for consumer microphone array applications. An integrated PLL operates from a wide variety of clocks, enabling high design flexibility. Microphone power outputs are included for biasing external microphones. Wide dynamic range is achieved, at 83dB with a microphone gain setting of +30dB. The AK5703 is packaged in a space-saving 28-pin QFN package.

FEATURES

1. **Recording Function**
   - **4-Channel ADC**
   - **Full-differential or Single-ended Input**
   - **Microphone Amplifier (+36dB/+30dB/+24dB/+18dB/+15dB/+12dB/+8dB/0dB)**
   - **Input Voltage: 1.8Vpp@AVDD=3.0V (= 0.6 x AVDD)**
   - **ADC Performance:**
     S/(N+D): 85dB, DR, S/N: 96dB@MGAIN=0dB, Single-ended Input
     S/(N+D): 78dB, DR, S/N: 83dB@MGAIN=+30dB, Full Differential Input
   - **Digital HPF for DC-offset cancellation (fc=3.4Hz@fs=44.1kHz)**
   - **Microphone Sensitivity Correction (+3dB ~ –3dB, 0.75dB Step)**
   - **Digital ALC (Automatic Level Control)**
   - **Input Digital Volume (+36dB ~ –52.5dB, 0.375dB Step, Mute)**
   - **Programmable Output Data Delay**
     Delay Time: 0 to 64/64fs (1/64fs Step)
2. **Sampling Frequency:**
   - **PLL Slave Mode (BICK pin): 8kHz ~ 48kHz**
   - **PLL Slave Mode (MCKI pin):**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **PLL Master Mode:**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **EXT Master/Slave Mode:**
     8kHz ~ 48kHz (256fs), 8kHz ~ 24kHz (512fs), 8kHz ~ 12kHz (1024fs)
3. **PLL Input Clock:**
   - **MCKI pin:**
     27MHz, 26MHz, 24MHz, 19.2MHz, 13.5MHz, 13MHz, 12.288MHz, 12MHz, 11.2896MHz
   - **BICK pin: 32fs/64fs**
4. **Master/Slave Mode**
5. **Audio Interface Format: MSB First, 2's complement**
   - **24/16-bit MSB justified, 24/16-bit I^2S, TDM Mode**
6. **μP I/F: 3-wire Serial Control or I^2C Bus (Ver 1.0, 400kHz Mode)**
7. **Power Supply:**
   - **AVDD: 2.4 ~ 3.6V**
   - **DVDD: 1.6 ~ 1.98V**
   - **TVDD: 1.6 or (DVDD-0.2) ~ 3.6V**
8. **Power Supply Current: 9.0mA (EXT Slave Mode)**
9. **Ta = –30 ~ 85°C**
10. **Package: 28pin QFN (4mm x 4mm, 0.4mm pitch)**

■Block Diagram

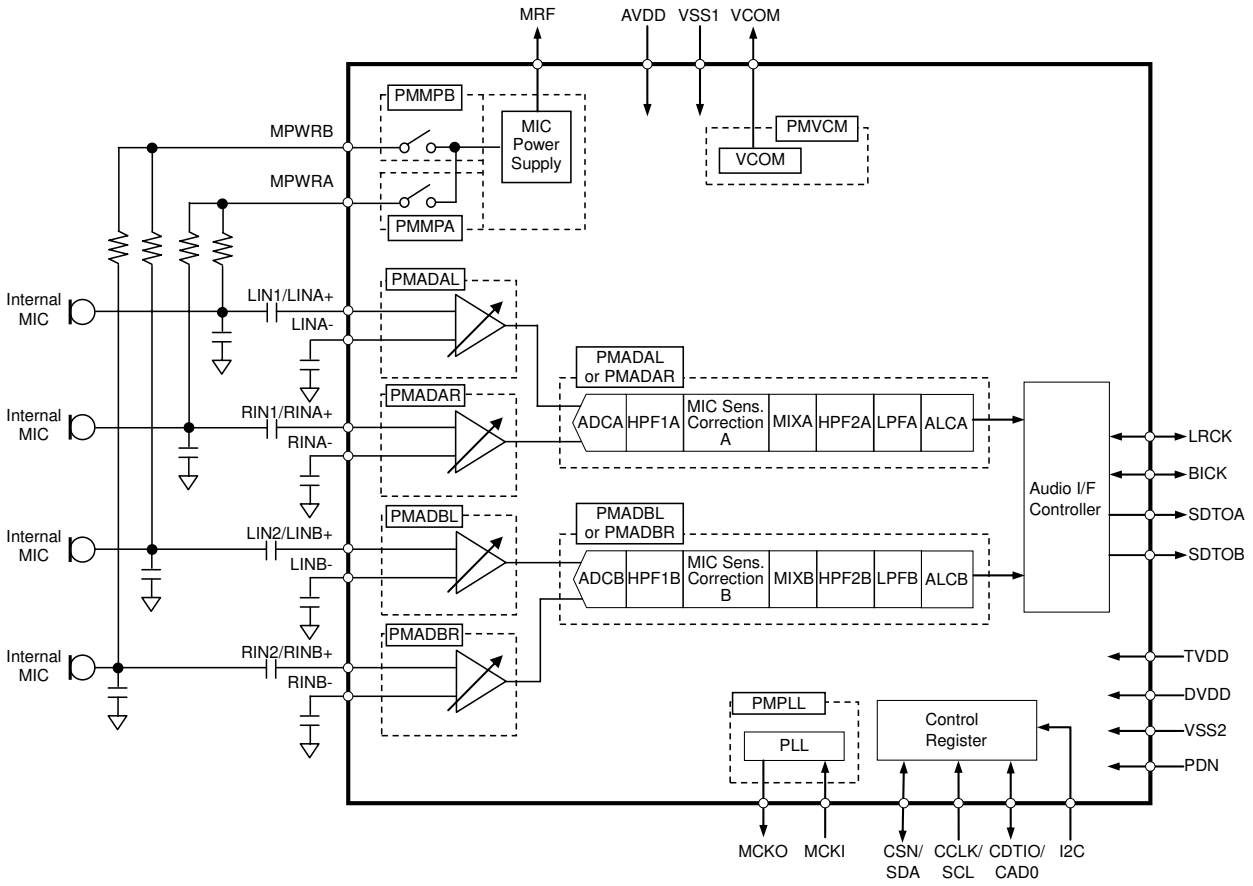
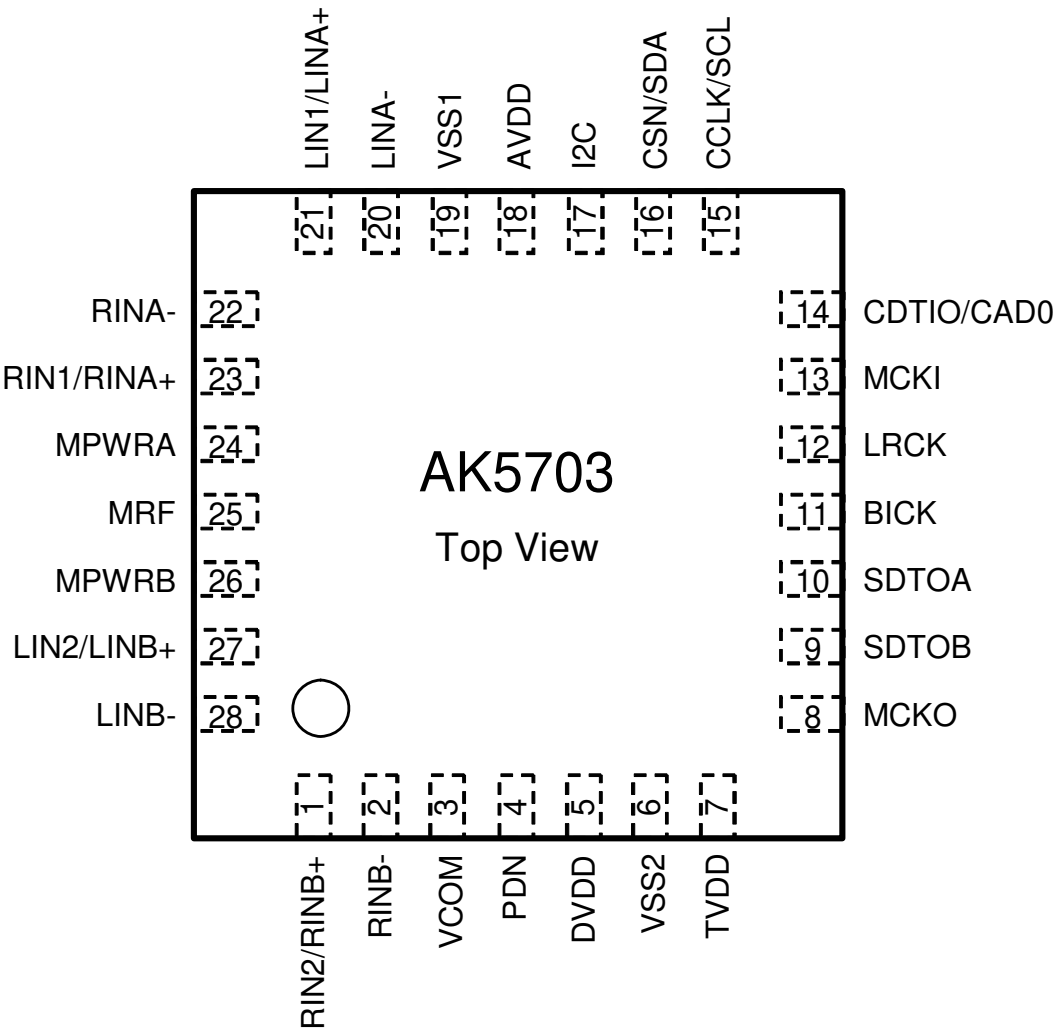


Figure 1. Block Diagram

■ Ordering Guide

AK5703EN	-30 ~ +85°C	28pin QFN (0.4mm pitch)
AKD5703	Evaluation Board for AK5703	

■ Pin Layout



■ Comparison with AK5702

Function		AK5702	AK5703
ADC Resolution		16-bit	24-bit
3:1 Stereo Input Selector		Yes	No
MIC Amplifier	Gain	+36dB, +30dB, +15dB, 0dB	+36dB, +30dB, +24dB, +18dB, +15dB, +12dB, +8dB, 0dB
	Input Resistance	30kΩ @MGAIN=+15dB, +30dB, +36dB	100kΩ
DR, S/N (Full Differential Input)		74dB@MGAIN=+30dB	83dB@MGAIN=+30dB
Audio Interface	DSP Mode	Yes	No
	TDM Mode	Yes	Yes
	Cascade TDM Mode	Yes	No
MIC Sensitivity Correction		No	Yes (+3dB ~ -3dB)
Programmable Output Data Delay		No	Yes (0 ~ 64/64fs)
PLL	LRCK Reference	Yes	No
	VCOC pin	Yes	No
Package		32pin QFN (5mm x 5mm, 0.5mm pitch)	28pin QFN (4mm x 4mm, 0.4mm pitch)

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	RIN2	I	Rch Analog Input 2 Pin (MDIFB bit = "0": Single-ended Input)
	RINB+	I	Rch Positive Input B Pin (MDIFB bit = "1": Full-differential Input)
2	RINB-	I	Rch Negative Input B Pin (MDIFB bit = "0": Single-ended Input) This pin must be connected to VSS1 with a capacitor in series. (Refer to Figure 50)
			Rch Negative Input B Pin Rch Negative Input B Pin
3	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD Bias voltage of ADC inputs. This pin must be connected to VSS1 with 1µF±50% capacitor in series.
4	PDN	I	Power-Down Mode Pin "H": Power-up, "L": Power-down, reset and initializes the control register.
5	DVDD	-	Digital Power Supply Pin, 1.6 ~ 1.98V
6	VSS2	-	Digital Ground Pin
7	TVDD	-	Digital I/O Power Supply Pin, 1.6 ~ 3.6V
8	MCKO	O	Master Clock Output Pin
9	SDTOB	O	ADCB/TDM Audio Serial Data Output Pin
10	SDTOA	O	ADCA Audio Serial Data Output Pin
11	BICK	I/O	Audio Serial Data Clock Pin
12	LRCK	I/O	Input / Output Channel Clock Pin
13	MCKI	I	External Master Clock Input Pin
14	CDTIO	I/O	Control Data Input/Output Pin (I2C pin = "L": 3-wire Serial Mode)
	CAD0	I	Chip Address 0 Select Pin (I2C pin = "H": I^2C Bus Mode)
15	CCLK	I	Control Data Clock Pin (I2C pin = "L": 3-wire Serial Mode)
	SCL	I	Control Data Clock Pin (I2C pin = "H": I^2C Bus Mode)
16	CSN	I	Chip Select Pin (I2C pin = "L": 3-wire Serial Mode)
	SDA	I/O	Control Data Input Pin (I2C pin = "H": I^2C Bus Mode)
17	I2C	I	Control Mode Select Pin "H": I^2C, "L": 3-wire serial
18	AVDD	-	Analog Power Supply Pin, 2.4 ~ 3.6V
19	VSS1	-	Analog Ground Pin
20	LINA-	I	Lch Negative Input A Pin (MDIFA bit = "0": Single-ended Input) This pin must be connected to VSS1 with a capacitor in series. (Refer to Figure 50)
			Lch Negative Input A Pin (MDIFA bit = "1": Full-differential Input)
21	LIN1	I	Lch Analog Input 1 Pin (MDIFA bit = "0": Single-ended Input)
	LINA+	I	Lch Positive Input A Pin (MDIFA bit = "1": Full-differential Input)
22	RINA-	I	Rch Negative Input A Pin (MDIFA bit = "0": Single-ended Input) This pin must be connected to VSS1 with a capacitor in series. (Refer to Figure 50)
			Rch Negative Input A Pin (MDIFB bit = "1": Full-differential Input)
23	RIN1	I	Rch Analog Input 1 Pin (MDIFA bit = "0": Single-ended Input)
	RINA+	I	Rch Positive Input A Pin (MDIFA bit = "1": Full-differential Input)
24	MPWRA	O	Microphone Power Supply A Pin
25	MRF	O	Microphone Power Supply Ripple Filter Pin This pin must be connected to VSS1 with 1µF±50% capacitor in series.
26	MPWRB	O	Microphone Power Supply B Pin
27	LIN2	I	Lch Analog Input 2 Pin (MDIFB bit = "0": Single-ended Input)
	LINB+	I	Lch Positive Input B Pin (MDIFB bit = "1": Full-differential Input)
28	LINB-	I	Lch Negative Input B Pin (MDIFB bit = "0": Single-ended Input) This pin must be connected to VSS1 with a capacitor in series. (Refer to Figure 50)
			Lch Negative Input B Pin (MDIFB bit = "1": Full-differential Input)

Note 1. All input pins except analog input pins (LIN1-2, RIN1-2, LINA+/-, RINA+/-, LINB+/-, RINB+/-) must not be allowed to float.

■Handling of Unused Pin

The unused I/O pins must be connected appropriately.

Classification	Pin Name	Setting
Analog	MPWRA, MPWRB, MRF, LIN1/LINA+, LINA−, RIN1/RINA+, RINA−, LIN2/LINB+, LINB−, RIN2/RINB+, RINB−	Open
	LINA−, RINA−, LINB−, RINB− (When single-ended inputs are used.)	Connect to VSS1 with a capacitor in series.
Digital	SDTOA, SDTOB, MCKO	Open
	MCKI	Connect to VSS2

ABSOLUTE MAXIMUM RATINGS

(VSS1, VSS2 = 0V; Note 2)

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog	AVDD	−0.3	6.0	V
	Digital	DVDD	−0.3	2.5	V
	Digital I/O	TVDD	−0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	−0.3	AVDD+0.3	V
Digital Input Voltage (Note 4)		VIND	−0.3	TVDD+0.3	V
Ambient Temperature (powered applied)		Ta	−30	85	°C
Storage Temperature		Tstg	−65	150	°C

Note 2. All voltages are with respect to ground. VSS1 and VSS2 must be connected to the same analog ground plane.
Note 3. LIN1/LINA+, LINA−, RIN1/RINA+, RINA−, LIN2/LINB+, LINB−, RIN2/RINB+, RINB− pins
Note 4. PDN, CSN/SDA, CCLK/SCL, CDTIO/CAD0, MCKI, LRCK, BICK, I2C pins
Pull-up resistors at SDA and SCL pins should be connected to (TVDD+0.3)V or less voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1, VSS2=0V; Note 2)

Parameter		Symbol	min	typ	max	Unit
Power Supplies (Note 5)	Analog	AVDD	2.4	3.0	3.6	V
	Digital	DVDD	1.6	1.8	1.98	V
	Digital I/O (Note 6)	TVDD	1.6 or DVDD-0.2	3.0	3.6	V

Note 2. All voltages are with respect to ground. VSS1 and VSS2 must be connected to the same analog ground plane.
Note 5. The power-up sequence between AVDD, DVDD and TVDD is not critical. The PDN pin must be "L" upon power-up, and should be changed to "H" after all power supplies are supplied to avoid an internal circuit error.
Note 6. The minimum value is higher voltage between DVDD-0.2V and 1.6V.

*** When TVDD is powered ON and the PDN pin is "L", AVDD or DVDD can be powered ON/OFF. The PDN pin must be set to "H" after all power supplies are ON when the AK5703 is powered-up from power-down state.**

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=TVDD=3.0V, DVDD=1.8V; VSS1=VSS2=0V; EXT Slave Mode; MCKI=11.2896MHz, fs=44.1kHz, BICK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement bandwidth =20Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
Microphone Amplifier: LIN1/RIN1/LIN2/RIN2 pins					
Input Resistance		70	100	130	kΩ
Gain	MGAIN2-0 bits = "000"	-1	0	+1	dB
	MGAIN2-0 bits = "001"	+7	+8	+9	dB
	MGAIN2-0 bits = "010"	+11	+12	+13	dB
	MGAIN2-0 bits = "011"	+14	+15	+16	dB
	MGAIN2-0 bits = "100"	+17	+18	+19	dB
	MGAIN2-0 bits = "101"	+23	+24	+25	dB
	MGAIN2-0 bits = "110"	+29	+30	+31	dB
	MGAIN2-0 bits = "111"	+35	+36	+37	dB
Microphone Power Supply: MPWRA, MPWRB pins					
Output Voltage (Note 7)		2.16	2.40	2.64	V
Output Noise Level (A-weighted)		-	-114	-	dBV
PSRR (fin = 1kHz) (Note 8)		-	70	-	dB
Load Resistance		0.5	-	-	kΩ
Load Capacitance		-	-	30	pF
ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2 pins (Single-ended Input) → ADC → Programmable Filter (IVOL=0dB, ALC=OFF) → SDTOA/SDTOB					
Resolution		-	-	24	Bits
Input Voltage (Note 9)	MGAIN= +30dB	0.048	0.057	0.065	Vpp
	MGAIN= 0dB	1.53	1.80	2.07	Vpp
S/(N+D) (−1dBFS)	MGAIN= +30dB	68	78	-	dB
	MGAIN= 0dB	-	85	-	dB
	MGAIN= +30dB (Full Differential Input)	-	78	-	dB
D-Range (−60dBFS, A-weighted)	MGAIN= +30dB	73	83	-	dB
	MGAIN= 0dB	-	96	-	dB
	MGAIN= +30dB (Full Differential Input)	-	83	-	dB
S/N (A-weighted)	MGAIN= +30dB	73	83	-	dB
	MGAIN= 0dB	-	96	-	dB
	MGAIN= +30dB (Full Differential Input)	-	83	-	dB
Interchannel Isolation	MGAIN= +30dB	70	80	-	dB
	MGAIN= 0dB	-	100	-	
Interchannel Gain Mismatch	MGAIN= +30dB	-	0	1.0	dB
	MGAIN= 0dB	-	0	0.5	dB

Note 7. The output voltage is proportional to AVDD. (typ. 0.8 x AVDD V)
Note 8. PSRR is applied to AVDD with 100mpVpp sine wave.
Note 9. The full-scale input voltage is proportional to AVDD.
Single-ended Input: Vin = 0.6 x AVDD Vpp(typ)
Full Differential Input: Vin = (IN+) – (IN-) = 0.6 x AVDD Vpp(typ)

Parameter			min	typ	max	Unit
Power Supply Current:						
Power Up (PDN pin = "H", All Circuits Power-up)						
	AVDD + DVDD + TVDD	(Note 10)	-	9.0	-	mA
		(Note 11)	-	12.0	18.0	mA
Power Down (PDN pin = "L") (Note 12)						
	AVDD + DVDD + TVDD		-	0	10	μA

Note 10. When EXT Slave Mode (MCKI=11.2896MHz, fs=44.1kHz), and PMADAL = PMADAR = PMADBL = PMADBR = PMVCM = PMMPA = PMMPB bits = "1", PMPLL = M/S = MCKO bits = "0", TDM1-0 bits = "00". In this case, the MPWRA and MPWRB pins output 0mA.
AVDD=7.1mA(typ), DVDD=1.7mA(typ), TVDD=0.2mA(typ).

Note 11. When PLL Master Mode (MCKI=12MHz, fs=44.1kHz), and PMADAL = PMADAR = PMADBL = PMADBR = PMVCM = PMMPA = PMMPB = PMPLL = M/S = MCKO bits = "1", TDM1-0 bits = "11". In this case, the MPWRA and MPWRB pins output 0mA.
AVDD=7.7mA(typ), DVDD=1.8mA(typ), TVDD=2.5mA(typ).

Note 12. All digital input pins are fixed to TVDD or VSS2.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 1.98V; TVDD=1.6 ~ 3.6V; fs=44.1kHz)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 13)	±0.16dB	PB	0	-	17.3	kHz
	–0.66dB		-	19.4	-	kHz
	–1.1dB		-	19.9	-	kHz
	–7.1dB		-	22.1	-	kHz
Stopband (Note 13)		SB	26.1	-	-	kHz
Passband Ripple		PR	-	-	±0.16	dB
Stopband Attenuation		SA	73	-	-	dB
Group Delay (Note 14)		GD	-	19	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPFADA=HPFADB bits = "1", HPFA1-0= HPFB1-0 bits = "00"						
Frequency Response (Note 13)	–3.0dB	FR	-	3.4	-	Hz
	–0.5dB		-	10	-	Hz
	–0.1dB		-	22	-	Hz

Note 13. The passband and stopband frequencies scale with fs (system sampling rate). Each response refers to that of 1kHz.

Note 14. A calculating delay time which induced by digital filtering. This time is from the input of an analog signal to the setting of 24-bit data of both channels to the ADC output register.

DC CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 1.98V; TVDD=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
Audio Interface & Serial μP Interface (CDTIO/CAD0, CSN/SDA, CCLK/SCL, I2C, PDN, BICK, LRCK, MCKI pins)						
High-Level Input Voltage	(TVDD ≥ 2.2V)	VIH	70%TVDD	-	-	V
	(TVDD < 2.2V)		80%TVDD	-	-	V
Low-Level Input Voltage	(TVDD ≥ 2.2V)	VIL	-	-	30%TVDD	V
	(TVDD < 2.2V)		-	-	20%TVDD	V
Audio Interface & Serial μP Interface (CDTIO, SDA, MCKO, BICK, LRCK, SDTOA, SDTOB pins Output)						
High-Level Output Voltage	(Iout = –80μA)	VOH	TVDD–0.2	-	-	V
Low-Level Output Voltage						
	(Except SDA pin : Iout = 80μA)	VOL1	-	-	0.2	V
	(SDA pin, 2.0V ≤ TVDD ≤ 3.6V: Iout = 3mA)	VOL2	-	-	0.4	V
	(SDA pin, 1.6V ≤ TVDD < 2.0V: Iout = 3mA)	VOL2	-	-	20%TVDD	V
Input Leakage Current		Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 1.98V; TVDD=1.6 ~ 3.6V; C_L=20pF)

Parameter		Symbol	min	typ	max	Unit
PLL Master Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
MCKO Output Timing						
Frequency		fMCK	0.256	-	12.288	MHz
Duty Cycle		dMCK	40	50	60	%
LRCK Output Timing						
Frequency		fs	-	Table 6	-	kHz
Stereo Mode: Duty Cycle		Duty	-	50	-	%
TDM64, TDM128 Mode:						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(4fs)	-	s
MSB justified: Pulse Width High		tLRCKH	-	1/(4fs)	-	s
BICK Output Timing						
Period	BCKO1-0 bits = "00"	tBCK	-	1/(32fs)	-	s
	BCKO1-0 bits = "01"	tBCK	-	1/(64fs)	-	s
	BCKO1-0 bits = "10" (TDM128 Mode)	tBCK	-	1/(128fs)	-	s
Duty Cycle		dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)						
MCKI Input Timing						
Frequency		fCLK	11.2896	-	27	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
MCKO Output Timing						
Frequency		fMCK	0.256	-	12.288	MHz
Duty Cycle		dMCK	40	50	60	%
LRCK Input Timing						
Frequency		fs	-	Table 6	-	kHz
Stereo Mode: Duty Cycle		Duty	45	-	55	%
TDM64 Mode:						
I^2S compatible: Pulse Width Low		tLRCKL	1/(64fs)	-	63/(64fs)	s
MSB justified: Pulse Width High		tLRCKH	1/(64fs)	-	63/(64fs)	s
TDM128 Mode:						
I^2S compatible: Pulse Width Low		tLRCKL	1/(128fs)	-	127/(128fs)	s
MSB justified: Pulse Width High		tLRCKH	1/(128fs)	-	127/(128fs)	s
BICK Input Timing						
Period	Stereo Mode	tBCK	1/(64fs)	-	1/(32fs)	s
	TDM64 Mode	tBCK	-	1/(64fs)	-	s
	TDM128 Mode	tBCK	-	1/(128fs)	-	s
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	s
Pulse Width High		tBCKH	0.4 x tBCK	-	-	s

Parameter			Symbol	min	typ	max	Unit
PLL Slave Mode (PLL Reference Clock = BICK pin)							
MCKO Output Timing							
Frequency			fMCK	0.256	-	12.288	MHz
Duty Cycle			dMCK	40	50	60	%
LRCK Input Timing							
Frequency			fs	8	-	48	kHz
Stereo Mode: Duty Cycle			Duty	45	-	55	%
TDM64 Mode:							
I^2S compatible: Pulse Width Low			tLRCKL	1/(64fs)	-	63/(64fs)	s
MSB justified: Pulse Width High			tLRCKH	1/(64fs)	-	63/(64fs)	s
TDM128 Mode:							
I^2S compatible: Pulse Width Low			tLRCKL	1/(128fs)	-	127/(128fs)	s
MSB justified: Pulse Width High			tLRCKH	1/(128fs)	-	127/(128fs)	s
BICK Input Timing							
Period	Stereo Mode						
	PLL3-0 bits = "0010"		tBCK	-	1/(32fs)	-	s
	PLL3-0 bits = "0011"		tBCK	-	1/(64fs)	-	s
	TDM64 Mode						
	PLL3-0 bits = "0011"		tBCK	-	1/(64fs)	-	s
	TDM128 Mode						
	PLL3-0 bits = "0001"		tBCK	-	1/(128fs)	-	s
Pulse Width Low			tBCKL	0.4 x tBCK	-	-	s
Pulse Width High			tBCKH	0.4 x tBCK	-	-	s
External Slave Mode							
MCKI Input Timing							
Frequency	256fs		fCLK	2.048	-	12.288	MHz
	512fs		fCLK	4.096	-	12.288	MHz
	1024fs		fCLK	8.192	-	12.288	MHz
Pulse Width Low			tCLKL	0.4/fCLK	-	-	s
Pulse Width High			tCLKH	0.4/fCLK	-	-	s
LRCK Input Timing							
Frequency	256fs		fs	8	-	48	kHz
	512fs		fs	8	-	24	kHz
	1024fs		fs	8	-	12	kHz
Stereo Mode: Duty Cycle			Duty	45	-	55	%
TDM64 Mode:							
I^2S compatible: Pulse Width Low			tLRCKL	1/(64fs)	-	63/(64fs)	s
MSB justified: Pulse Width High			tLRCKH	1/(64fs)	-	63/(64fs)	s
TDM128 Mode:							
I^2S compatible: Pulse Width Low			tLRCKL	1/(128fs)	-	127/(128fs)	s
MSB justified: Pulse Width High			tLRCKH	1/(128fs)	-	127/(128fs)	s
BICK Input Timing							
Period		Stereo Mode	tBCK	325.52	-	-	ns
		TDM Mode	tBCK	162.76	-	-	ns
Pulse Width Low		Stereo Mode	tBCKL	130	-	-	ns
		TDM Mode	tBCKL	65	-	-	ns
Pulse Width High		Stereo Mode	tBCKH	130	-	-	ns
		TDM Mode	tBCKH	65	-	-	ns

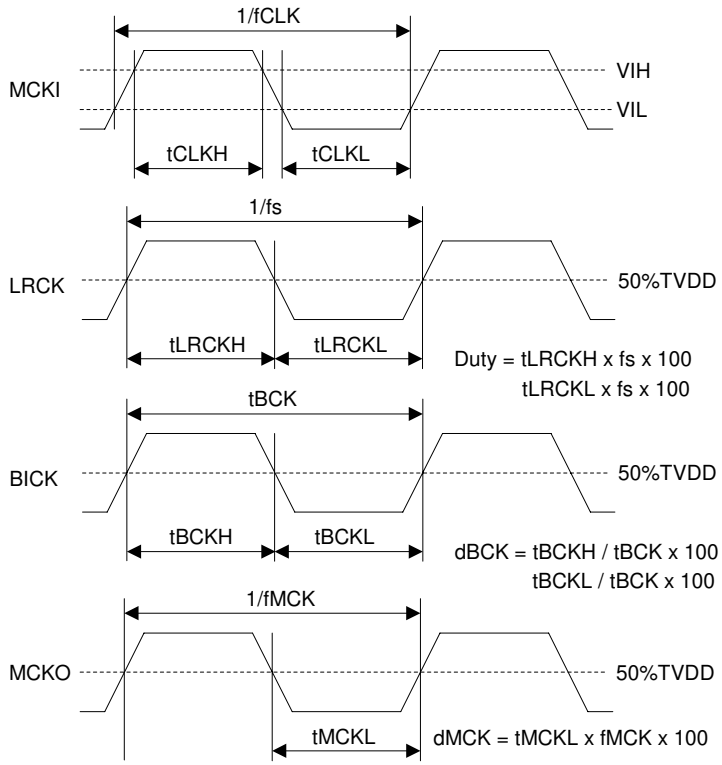
Parameter		Symbol	min	typ	max	Unit
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	2.048	-	12.288	MHz
	512fs	fCLK	4.096	-	12.288	MHz
	1024fs	fCLK	8.192	-	12.288	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	s
Pulse Width High		tCLKH	0.4/fCLK	-	-	s
LRCK Output Timing						
Frequency		fs	8	-	48	kHz
Stereo Mode: Duty Cycle		Duty	-	50	-	%
TDM64, TDM128 Mode:						
I^2S compatible: Pulse Width Low		tLRCKL	-	1/(4fs)	-	s
MSB justified: Pulse Width High		tLRCKH	-	1/(4fs)	-	s
BICK Output Timing						
Period	BCKO1-0 bits = "00"	tBCK	-	1/(32fs)	-	s
	BCKO1-0 bits = "01"	tBCK	-	1/(64fs)	-	s
	BCKO1-0 bits = "10" (TDM128 Mode)	tBCK	-	1/(128fs)	-	s
Duty Cycle		dBCK	-	50	-	%
Audio Interface Timing (Left justified & I^2S)						
Master Mode						
BICK "↓" to LRCK Edge (Note 15)		tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)		tLRD	–70	-	70	ns
BICK "↓" to SDTO		tBSD	–70	-	70	ns
Slave Mode						
LRCK Edge to BICK "↑" (Note 15)		tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 15)		tBLR	50	-	-	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)		tLRD	-	-	80	ns
BICK "↓" to SDTO		tBSD	-	-	80	ns
Audio Interface Timing (TDM64 Mode)						
Master Mode						
BICK "↓" to LRCK		tMBLR	-40	-	40	ns
BICK "↓" to SDTOB (Note 16)		tBSD	-70	-	70	ns
Slave Mode						
LRCK Edge to BICK "↑" (Note 15)		tLRB	50	-	-	ns
BICK "↑" to LRCK Edge (Note 15)		tBLR	50	-	-	ns
BICK "↓" to SDTOB (Note 16)		tBSD	-	-	80	ns
Audio Interface Timing (TDM128 Mode)						
Master Mode						
BICK "↓" to LRCK		tMBLR	-24	-	24	ns
BICK "↓" to SDTOB (Note 16)		tBSD	-40	-	40	ns
Slave Mode						
LRCK Edge to BICK "↑" (Note 15)		tLRB	40	-	-	ns
BICK "↑" to LRCK Edge (Note 15)		tBLR	40	-	-	ns
BICK "↓" to SDTOB (Note 16)		tBSD	-	-	50	ns

Note 15. BICK rising edge must not occur at the same time as LRCK edge.
Note 16. SDTOA is fixed to "L".

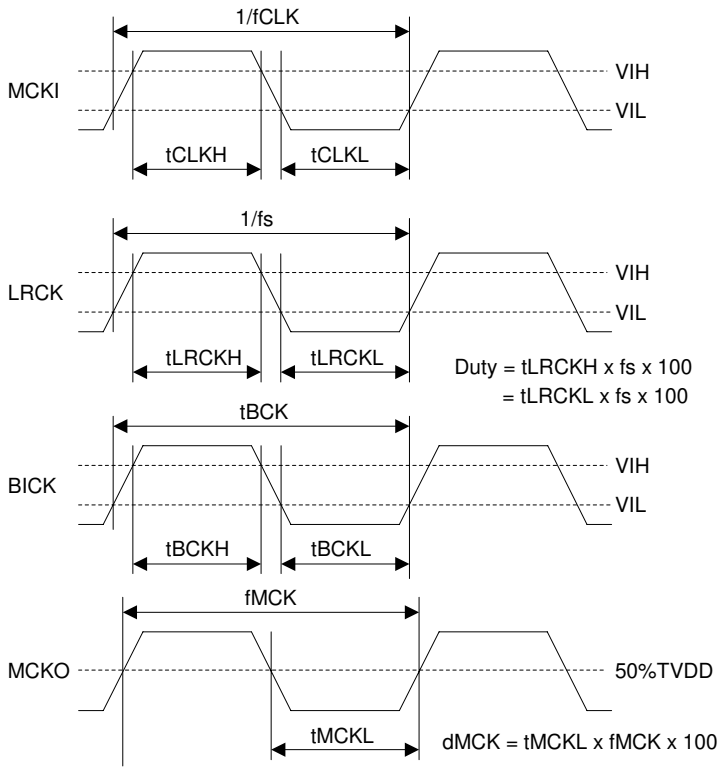
Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (3-wire mode):					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTIO Setup Time	tCDS	40	-	-	ns
CDTIO Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN Edge to CCLK "↑" (Note 17)	tCSS	50	-	-	ns
CCLK "↑" to CSN Edge (Note 17)	tCSH	50	-	-	ns
CCLK "↓" to CDTIO (at Read Command)	tDCD	-	-	70	ns
CSN "↑" to CDTIO (Hi-Z) (at Read Command) (Note 19)	tCCZ	-	-	70	ns
Control Interface Timing (I^2C Bus mode) (Note 18)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling (Note 20)	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Capacitive Load on Bus	Cb	-	-	400	pF
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 21)	tAPD	1.0	-	-	µs
PDN Reject Pulse Width (Note 21)	tRPD	-	-	50	ns
PMADAL or PMADAR or PMADBL or PMADBR "↑" to SDTO valid (Note 22)					
ADRSTA/B1-0 bits = "00"	tPDV	-	1059	-	1/fs
ADRSTA/B1-0 bits = "01"	tPDV	-	267	-	1/fs
ADRSTA/B1-0 bits = "10"	tPDV	-	2115	-	1/fs
ADRSTA/B1-0 bits = "11"	tPDV	-	531	-	1/fs

Note 17. CCLK rising edge must not occur at the same time as CSN edge.
Note 18. I^2C-bus is a trademark of NXP B.V.
Note 19. R_L=1kΩ/10% change (pull-up to TVDD)
Note 20. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 21. The AK5703 can be reset by bringing the PDN pin "L" upon power-up. The PDN pin must held "L" for more than 1µs for a certain reset. The AK5703 is not reset by the "L" pulse less than 50ns.
Note 22. This is the count of LRCK "↑" from the PMADAL, PMADAR, PMADBL or PMADBR bit = "1".

■ Timing Diagram



Note 23. MCKO is not available at EXT Master Mode.
Figure 2. Clock Timing (PLL/EXT Master mode)



Note 24. The MCKI pin is “L” level when PLL reference clock is the BICK pin.
Figure 3. Clock Timing (PLL Slave mode)

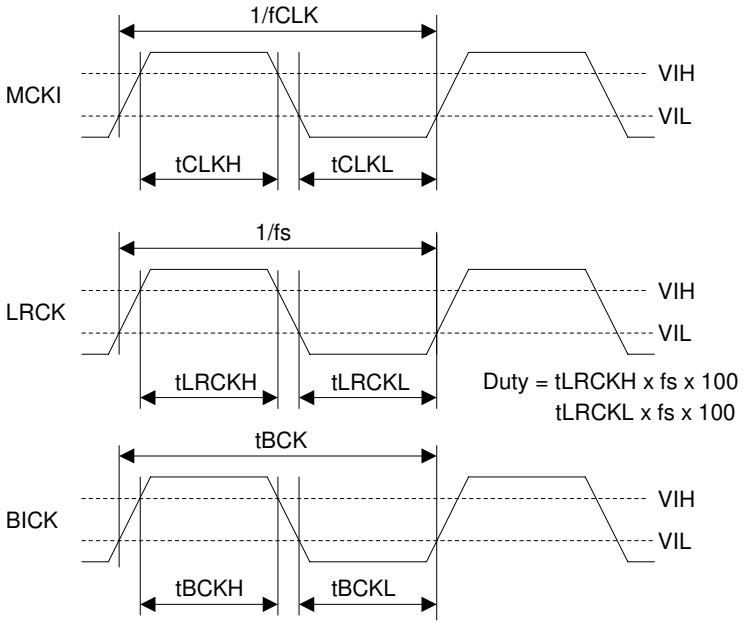


Figure 4. Clock Timing (EXT Slave mode)

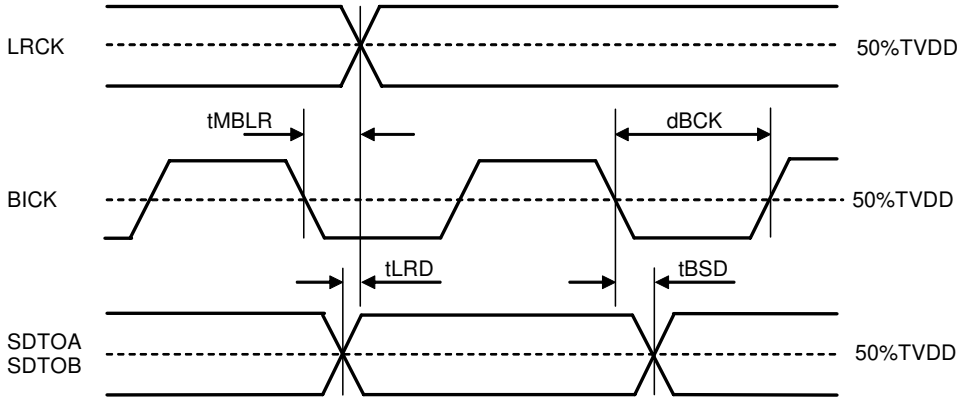


Figure 5. Audio Interface Timing (PLL/EXT Master mode & Normal Mode)

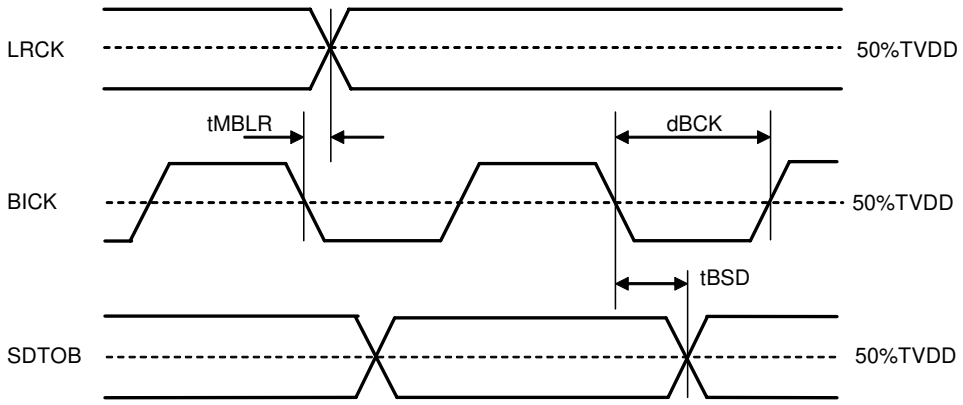


Figure 6. Audio Interface Timing (PLL/EXT Master mode & TDM mode)

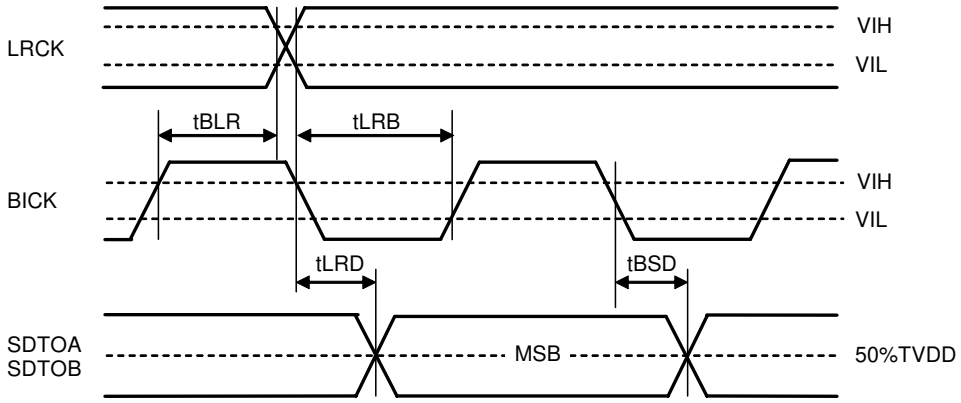


Figure 7. Audio Interface Timing (PLL/EXT Slave mode & Normal mode)

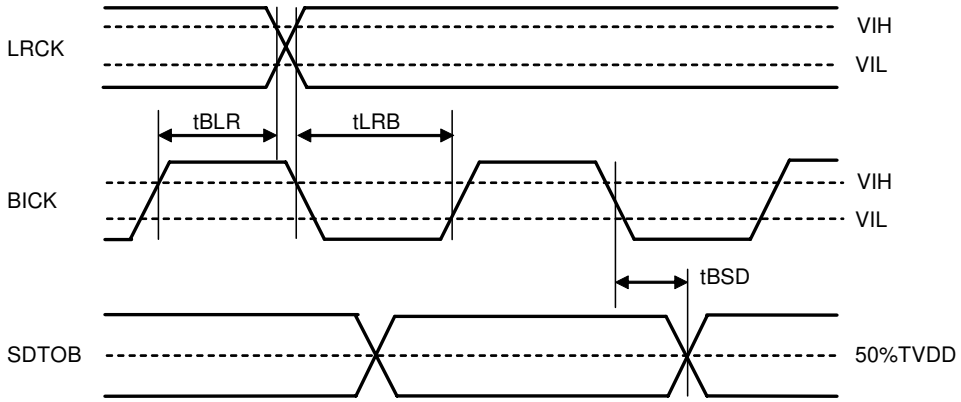


Figure 8. Audio Interface Timing (PLL/EXT Slave mode & TDM mode)

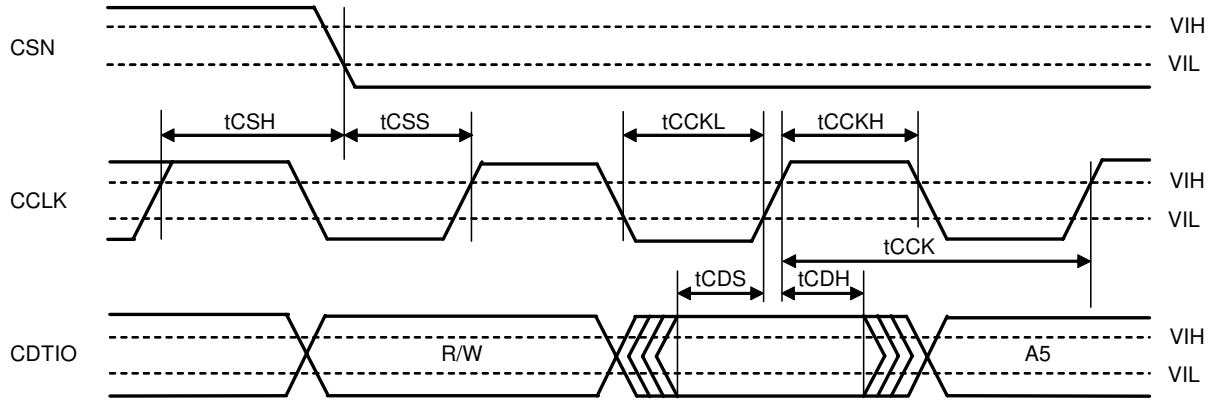


Figure 9. WRITE Command Input Timing

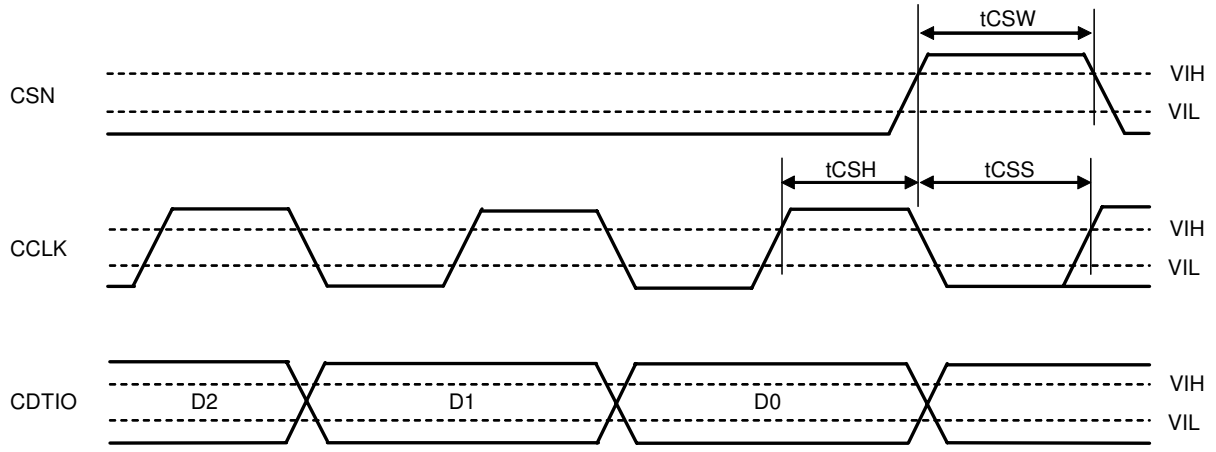


Figure 10. WRITE Data Input Timing

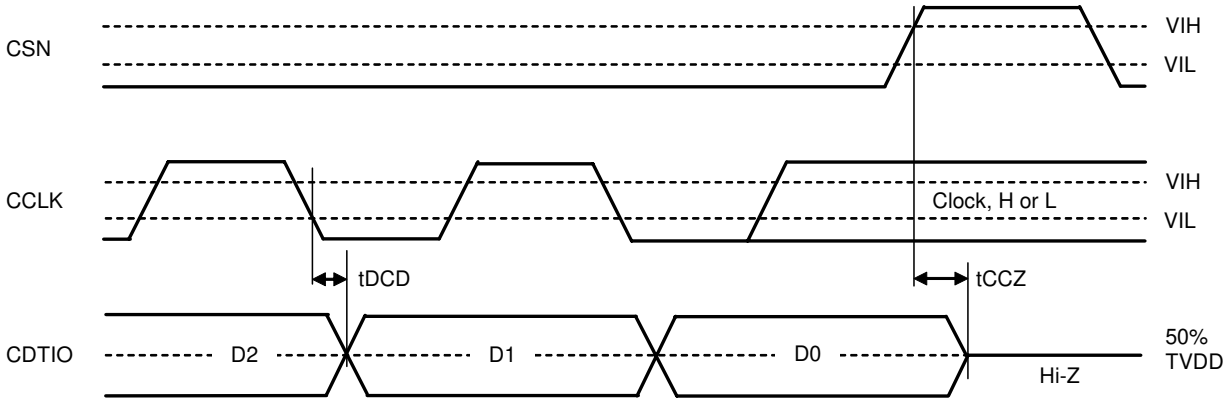


Figure 11. Read Data Output Timing

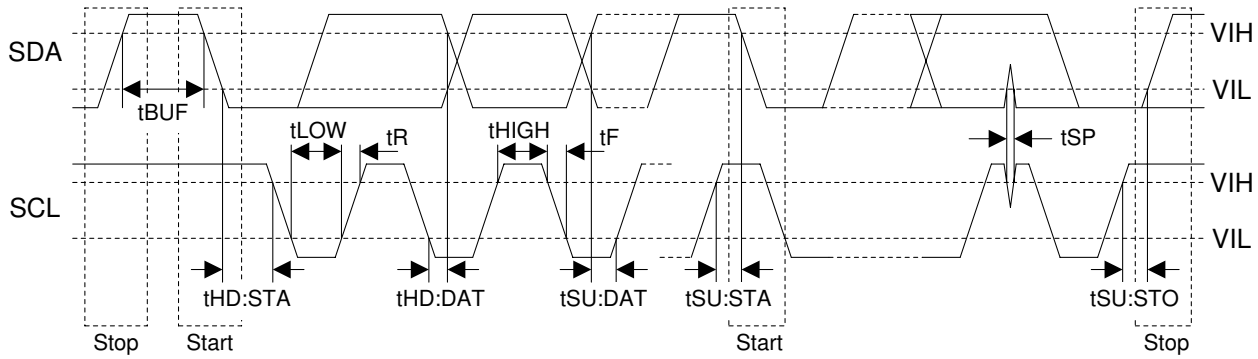


Figure 12. I^2C Bus Mode Timing

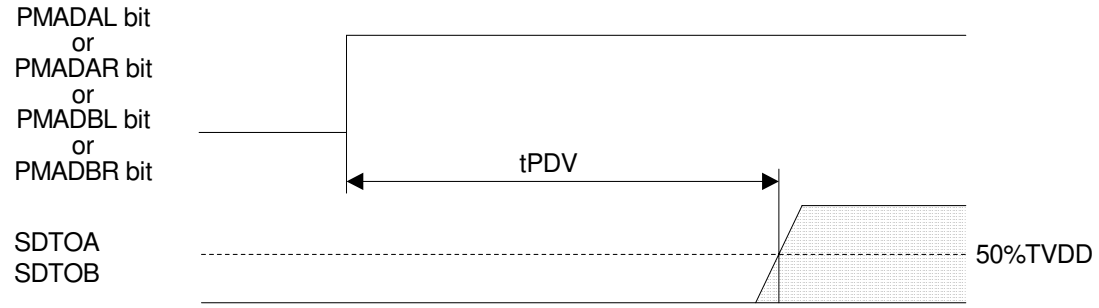


Figure 13. Power Down & Reset Timing 1

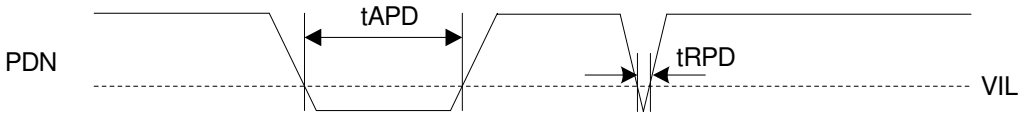


Figure 14. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (Table 1, Table 2).

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 25)	1	1	Table 4	Figure 15
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	Table 4	Figure 16
PLL Slave Mode 2 (PLL Reference Clock: BICK pin)	1	0	Table 4	Figure 17
EXT Slave Mode	0	0	x	Figure 18
EXT Master Mode	0	1	x	Figure 19

Note 25. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from the MCKO pin.

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BICK pin	LRCK pin
PLL Master Mode	0	"L"	Selected by PLL3-0 bits	Output (Selected by BCKO1-0 bits)	Output (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	0	"L"	Selected by PLL3-0 bits	Input (≥ 32fs)	Input (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode 2 (PLL Reference Clock: BICK pin)	0	"L"	GND	Input (Selected by PLL3-0 bits)	Input (1fs)
	1	Selected by PS1-0 bits			
EXT Slave Mode	0	"L"	Selected by CM1-0 bits	Input (≥ 32fs)	Input (1fs)
	1	N/A			
EXT Master Mode	0	"L"	Selected by CM1-0 bits	Output (Selected by BCKO1-0 bits)	Output (1fs)
	1	N/A			

Table 2. Clock pins state in Clock Mode (N/A: Not Available)

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK5703 is in power-down mode (PDN pin = "L") and when exits reset state, the AK5703 is in slave mode. After exiting reset state, the AK5703 goes to master mode by changing M/S bit = "1".

When the AK5703 is in master mode, the LRCK and BICK pins are a Hi-Z state until M/S bit becomes "1". The LRCK and BICK pins of the AK5703 must be pulled-down or pulled-up by a resistor (about 100kΩ) externally to avoid the floating state.

M/S bit	Mode	
0	Slave Mode	(default)
1	Master Mode	

Table 3. Select Master/Slave Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) circuit generates a clock that is selected by the PLL2-0 and FS3-0 bits. The PLL lock times, when the AK5703 is supplied stable clocks or the sampling frequency is changed after PLL is powered-up (PMPLL bit = "0" → "1"), are shown in Table 4.

1) PLL Mode Setting

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	PLL Lock Time (max)	
1	0	0	0	1	BICK pin	128fs	2ms	
2	0	0	1	0	BICK pin	32fs	2ms	
3	0	0	1	1	BICK pin	64fs	2ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10ms	
5	0	1	0	1	MCKI pin	12.288MHz	10ms	
6	0	1	1	0	MCKI pin	12MHz	10ms	(default)
7	0	1	1	1	MCKI pin	24MHz	10ms	
8	1	0	0	0	MCKI pin	19.2MHz	10ms	
10	1	0	1	0	MCKI pin	13MHz	10ms	
11	1	0	1	1	MCKI pin	26MHz	10ms	
12	1	1	0	0	MCKI pin	13.5MHz	10ms	
13	1	1	0	1	MCKI pin	27MHz	10ms	
Others	Others				N/A			

Table 4. Setting of PLL Mode (fs: Sampling Frequency), (N/A: Not Available)

2) Setting of sampling frequency in PLL Mode

When the PLL reference clock input is the MCKI pin or the BICK pin, the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency (Note 26)	
0	0	0	0	0	8kHz mode	
1	0	0	0	1	12kHz mode	
2	0	0	1	0	16kHz mode	
3	0	0	1	1	24kHz mode	
5	0	1	0	1	11.025kHz mode	
7	0	1	1	1	22.05kHz mode	
10	1	0	1	0	32kHz mode	
11	1	0	1	1	48kHz mode	
15	1	1	1	1	44.1kHz mode	(default)
Others	Others				N/A	

Table 5. Setting of Sampling Frequency at PMPLL bit = "1" (N/A: Not Available)

Note 26. When the MCKI pin is the PLL reference clock input, the sampling frequency generated by PLL differs from the sampling frequency of mode name in some combinations of MCKI frequency(PLL3-0 bits) and sampling frequency (FS3-0 bits). Refer to Table 6 for the details of sampling frequency. In master mode, LRCK and BICK output frequency correspond to sampling frequencies shown in Table 6. When the BICK pin is the PLL reference clock input, the sampling frequency generated by PLL is the same sampling frequency of mode name.

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz](Note 27)
11.2896	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
12.288	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
12	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
24	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
	Sampling frequency that differs from sampling frequency of mode name	

Note 27. These are rounded off to six decimal places.

Table 6. Sampling Frequency at PLL mode (Reference clock is MCKI)

Input Frequency MCKI[MHz]	Sampling Frequency Mode	Sampling Frequency generated by PLL [kHz](Note 27)
19.2	8kHz mode	8.000000
	12kHz mode	12.000000
	16kHz mode	16.000000
	24kHz mode	24.000000
	32kHz mode	32.000000
	48kHz mode	48.000000
	11.025kHz mode	11.025000
	22.05kHz mode	22.050000
	44.1kHz mode	44.100000
13	8kHz mode	7.999786
	12kHz mode	11.999679
	16kHz mode	15.999572
	24kHz mode	23.999358
	32kHz mode	31.999144
	48kHz mode	47.998716
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
26	8kHz mode	7.999786
	12kHz mode	11.999679
	16kHz mode	15.999572
	24kHz mode	23.999358
	32kHz mode	31.999144
	48kHz mode	47.998716
	11.025kHz mode	11.024877
	22.05kHz mode	22.049753
	44.1kHz mode	44.099507
13.5	8kHz mode	8.000300
	12kHz mode	12.000451
	16kHz mode	16.000601
	24kHz mode	24.000901
	32kHz mode	32.001202
	48kHz mode	48.001803
	11.025kHz mode	11.025218
	22.05kHz mode	22.050436
	44.1kHz mode	44.100871
27	8kHz mode	8.000300
	12kHz mode	12.000451
	16kHz mode	16.000601
	24kHz mode	24.000901
	32kHz mode	32.001202
	48kHz mode	48.001803
	11.025kHz mode	11.025218
	22.05kHz mode	22.050436
	44.1kHz mode	44.100871
	Sampling frequency that differs from sampling frequency of mode name	

Note 27. These are rounded off to six decimal places.

Table 6. Sampling Frequency at PLL mode (Reference clock is MCKI)

■PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, the LRCK and BICK pin go to "L", and an irregular frequency clock is output from the MCKO pin when MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin outputs "L" (Table 7).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, BICK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit "0".

PLL State	MCKO pin		BICK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After that PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except above case)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	Table 9	Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". Then, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC output invalid data when the PLL is unlocked.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock (except above case)	"L" Output	Invalid
PLL Lock	"L" Output	Table 9

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to the MCKI pin, the internal PLL circuit generates MCKO, BICK and LRCK clocks. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs, 64fs or 128fs, by BCKO1-0 bits (Table 10).

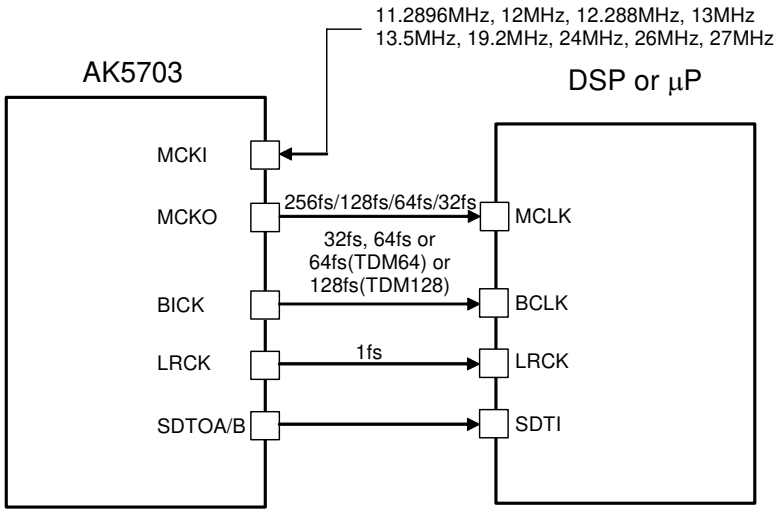


Figure 15. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	(default)
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

Mode	BCKO1 bit	BCKO0 bit	BICK Output Frequency	
0	0	0	32fs	(default)
1	0	1	64fs	
2	1	0	128fs (TDM128 Mode)	
3	1	1	N/A	

Note 28. 128fs is only available in TDM mode.

Table 10. BICK Output Frequency at Master Mode (N/A: Not Available)

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to MCKI or BICK pin. The required clock to the AK5703 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

a) PLL Slave Mode 1 (PLL reference clock: MCKI pin)

The BICK and LRCK inputs must be synchronized with MCKO output. The phase between MCKO and LRCK is not important. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).

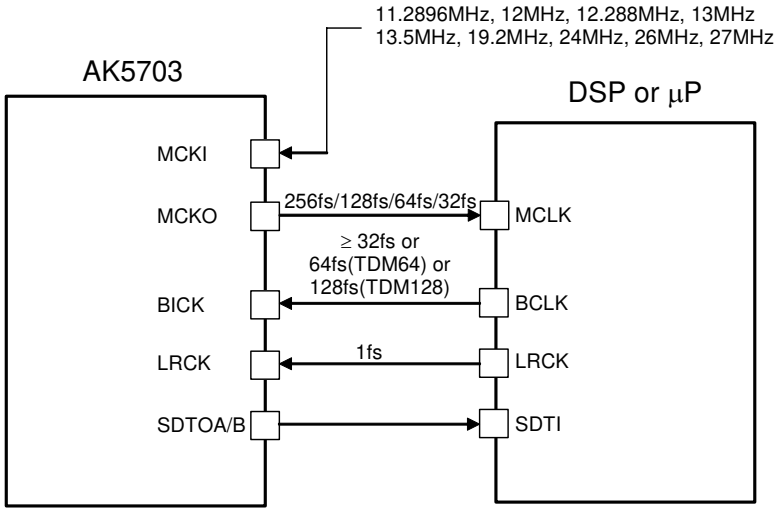


Figure 16. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL Slave Mode 2 (PLL reference clock: BICK pin)

The sampling frequency corresponds to a range from 8kHz to 48kHz by changing FS3-0 bits (Table 5). The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit.

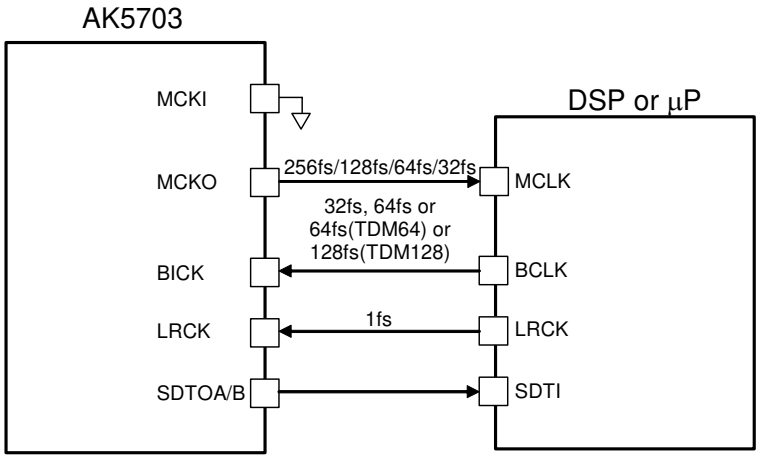


Figure 17. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)