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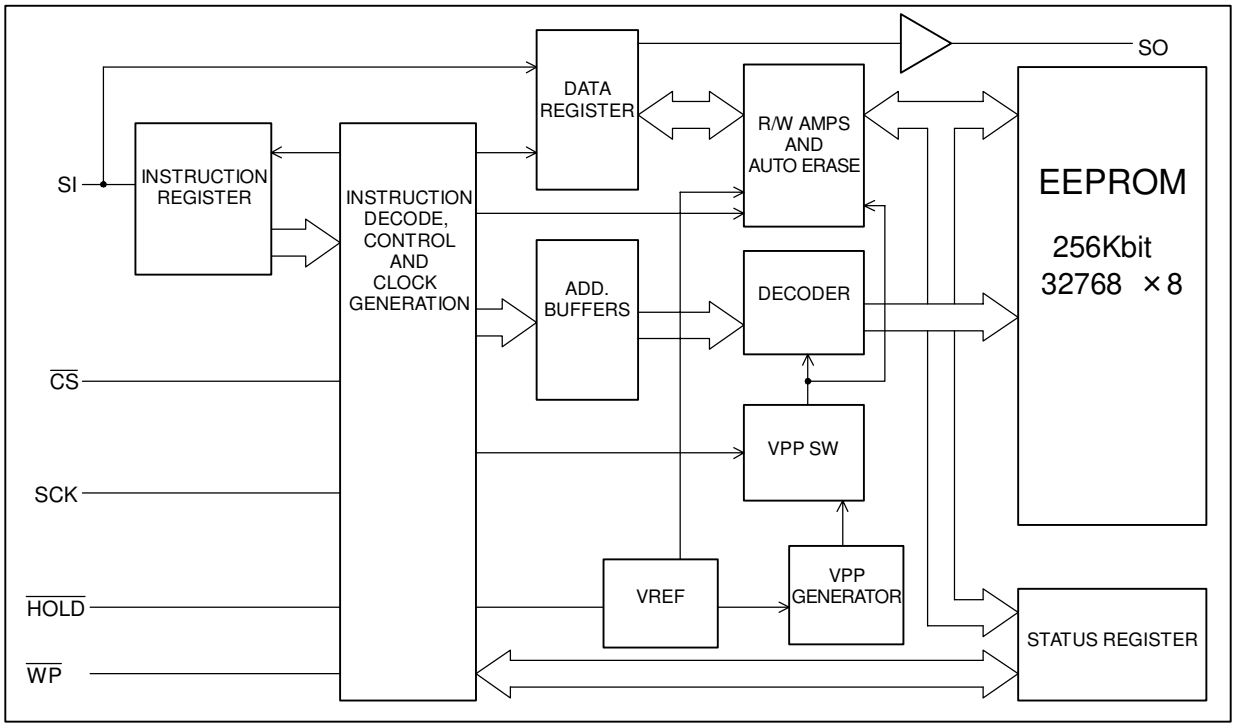
AK6516C

SPI bus 256Kbit Serial CMOS EEPROM

Features

- ☐ Advanced CMOS EEPROM Technology
- ☐ Single Voltage Supply: 1.6V to 5.5V
- ☐ 256Kbits; 32768 x 8 organization
- ☐ SPI Serial Interface Compatible
- ☐ Low Power Consumption
  - 0.8μA Max. (Standby mode)
- ☐ High Reliability
  - Endurance: 100K E/W cycles / Address
  - Data Retention: 10 Years
- ☐ Special Features
  - 64 byte Page Write Mode
  - Block Write Protection (Protect 1/4,1/2 or Entire Array)
  - Automatic write cycle time-out with auto-ERASE
- ☐ Software and Hardware controlled Write Protection
- ☐ Self timed Programming Cycle: 5msec. Max.
- ☐ Ideal for Low Density Data Storage
  - Low cost, space saving, 8-pin SOP package

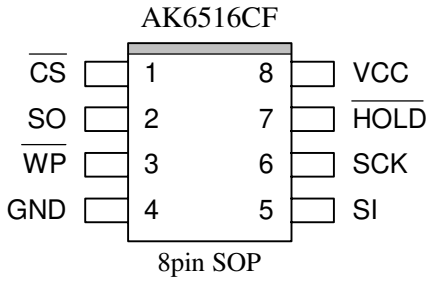


Block Diagram

General Description

The AK6516C is a 262144-bit, serial, read/write, non-volatile memory device fabricated using an advanced CMOS EEPROM technology. The AK6516C has 262144-bits of memory organized as 32768 registers of 8 bits each. The AK6516C can operate all function under wide operating voltage range: 1.6V to 5.5V. The charge up circuit for high voltage generation needed for write operations is integrated.
The AK6516C serial interface is compatible to a SPI bus. The AK6516C has 6 instructions: READ, WRITE, WREN (write enable), WRDI (write disable), RDSR (read status register), and WRSR (write status register).
Each instruction is organized by an op-code (8bits), address (16bits), and data (8bits). When input level of $\overline{CS}$ pin changed from high level to low level, AK6516C can receive instructions.

■ Pin Configurations



Pin name	Functions
$\overline{CS}$	Chip Select input
SCK	Serial Clock input
SI	Serial Data input
SO	Serial Data output
$\overline{WP}$	Write Protect input
$\overline{HOLD}$	Hold input
VCC	Power Supply
GND	Ground

■ Type of Products

Model	Memory size	Temp. Range	VCC	Package
AK6516CF	256K bits	-40°C to +85°C	1.6V to 5.5V	8pin Plastic SOP

■ Data Transfer

An IC that outputs the clock is called "MASTER", an IC that receives the clock is called "SLAVE". The AK6516C operates as a SLAVE. Data is written to the SI pin and read from SO pin. The MSB is transmitted first.

After $\overline{CS}$ pin changes high level to low level, AK6516C receives the first data bit on the SI pin synchronously with the rising edge of the input pulse of serial clock. While $\overline{CS}$ pin is high level, the data input to the SI pin is don't care and SO pin indicates Hi-Z.

All the functions are organized 8 bits of op-code, address, and data. If there is an invalid op-code, the AK6516C ignores the address and data information and SO pin indicates Hi-Z. In order to input new op-code, $\overline{CS}$ pin should be toggled.

■ Hold

AK6516C has a $\overline{HOLD}$ pin that can hold the data transfer. When $\overline{HOLD}$ changes high to low while SCK is low, the data transfer stops. After the $\overline{HOLD}$ pin changes low to high while SCK is low, the data transfer starts again. While the data transfer is paused, AK6516C ignores the clock on the SCK line.

■ Write Protect

AK6516C has status registers. When the WPEN bit in the status registers is "1", Write Protect function is enabled. When WPEN bit is "1" and $\overline{WP}$ pin is low level, the status register is protected from write function. When $\overline{WP}$ pin becomes low level while the WRITE to the status register instruction is written, the AK6516C doesn't accept the instruction. When the $\overline{WP}$ pin changes low level while the internal programming, the programming function continues.

When the WPEN bit is "0", $\overline{WP}$ pin function is disabled. Even if $\overline{WP}$ pin is fixed to low level, the WRITE function to the status register can be done. When the $\overline{WP}$ pin is high level, AK6516C can accept all of READ and WRITE functions.

Pin Description

$\overline{CS}$ (Chip Select Input)

When $\overline{CS}$ changes high level to low level, the AK6516C can receive the instructions.
$\overline{CS}$ should be kept low level while receiving op-code, address and data, and while outputting data.
When $\overline{CS}$ is high level, SO indicate Hi-Z.

SCK (Serial Clock Input)

The SCK clock pin is the synchronous clock input for input/output data.

SI (Serial Data Input)

The op-code, address, and data are written to the SI pin.

SO (Serial Data Output)

The SO pin outputs the data from memory array and status register.

$\overline{WP}$ (Write Protect Input)

The $\overline{WP}$ pin controls the write function to the status register.

When the WPEN bit in the status register is "0", the function of $\overline{WP}$ pin becomes disable. Then the status register can be programmable when the WEN bit in the status register is "1". And it does not depend on the status of $\overline{WP}$ pin.

When the WPEN bit is "1", the function of $\overline{WP}$ is enabled. Then the status register can not be programmable when the WEN bit is "1" and the status of $\overline{WP}$ pin is low.
When the WPEN bit is "1", $\overline{WP}$ pin is high and WEN bit is "1", AK6516C can accept the WRITE instruction to the status registers.

During the instruction input, $\overline{WP}$ pin should keep high or low level.

$\overline{HOLD}$ (Hold Input)

The $\overline{HOLD}$ pin can hold the data transfer. When the $\overline{HOLD}$ pin changes hi to low while the SCK is low, the data transfer is held. And the transfer starts when the $\overline{HOLD}$ pin changes low to high while the SCK is low. While the holding the data transfer, AK6516C ignores the clock signal on SCK pin.

Function Description

AK6516C has six instructions. The instruction can be input after the $\overline{CS}$ pin changes high to low. All the instructions are MSB first.

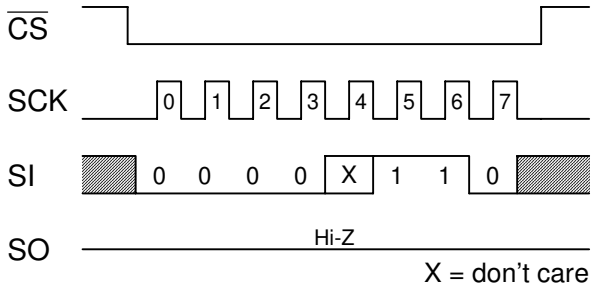
Instruction	Op-code	Address		Data	Description
READ	0000 X011	X A14-A8	A7-A0	D7-D0 (out)	Read from Memory Array
WRITE	0000 X010	X A14-A8	A7-A0	D7-D0 (in)	Write to Memory Array
WREN	0000 X110	------		------	Write Enable
WRDI	0000 X100	------		------	Write Disable
RDSR	0000 X101	Bit7-Bit0 (out)	------	------	Read Status Register
WRSR	0000 X001	Bit7-Bit0 (in)	------	------	Write Status Register

X: don't care

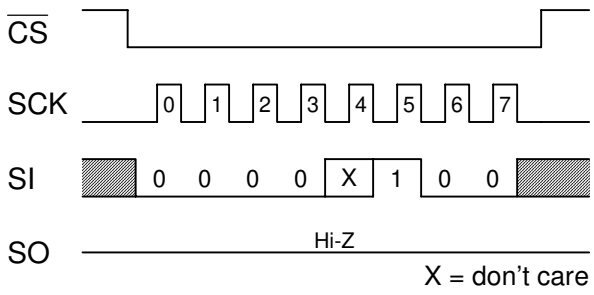
Table 1. Instruction set for AK6516C

WREN (WRITE ENABLE) / WRDI (WRITE DISABLE)

The WRITE function can be accepted only in the status of Write Enable. After VCC is applied, AK6516C is in the status of Write Disable. After the function of WRDI, AK6516C cannot accept any programming function.



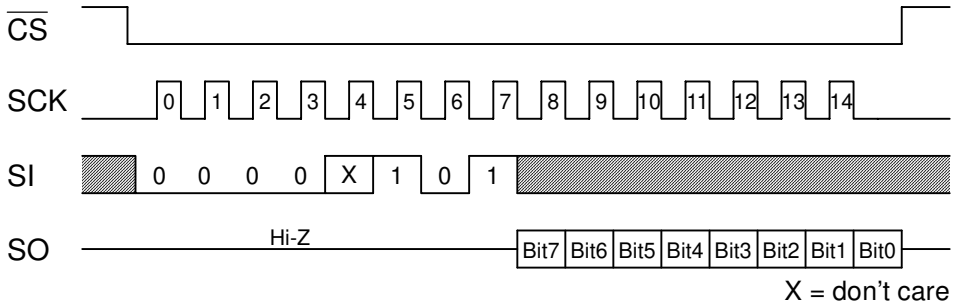
WREN



WRDI

RDSR (READ STATUS REGISTER)

The RDSR function is used to read the data in the STATUS register. The STATUS register has RDY bit, WEN bit, BP0/BP1 bit and WPEN bit. RDSR function can be used to read READY/BUSY status bit, WRITE ENABLE/DISABLE bit, and BLOCK PROTECT bit.
These bits can be set by WRSR function.



RDSR

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

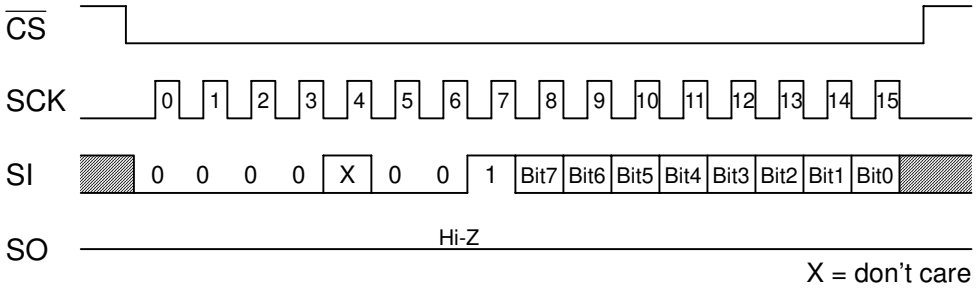
Register	Definition
WPEN	$\overline{WP}$ pin set bit (programmable) See Table 3.
BP0 / BP1	Block Protect bit for EEPROM memory array (programmable) See Table 4.
WEN	WRITE ENABLE / DISABLE bit (READ only) This is set by WREN/WRDI function. WEN=0 : WRITE DISABLE WEN=1 : WRITE ENABLE
$\overline{RDY}$	READY/BUSY status bit (READ only) $\overline{RDY}$=0 : READY $\overline{RDY}$=1 : BUSY

Table 2. Status Register Configuration

WRSR (WRITE STATUS REGISTER)

The WRSR instruction can set the Write Protect Block size of the memory array.
AK6516C has 4 Blocks of memory arrays. Write Protect Block size can be selected from 1/4, 1/2 and whole memory array. The block, which is set by Write Protect, is Read only.
BP0 bit, BP1 bit, and WPEN bit are programmable with EEPROM memory cell bits. The characteristics of those bits (WREN, tE/W, RDSR) are same as the EEPROM memory array.

$\overline{WP}$ pin function can be set by WPEN (WRITE PROTECT ENABLE) bit which is defined by WRSR function. When $\overline{WP}$ pin is low level and WPEN bit is "1", the WRITE function to Status register, which has WPEN bit and BP0/BP1 bit, and to Write Disable Block is not performed. Then WRITE function is performed only to the Write enable block.
When $\overline{WP}$ pin is "1" or WPEN bit is "0", then the function of $\overline{WP}$ pin is disabled and WRITE function to the Status Register is performed.
WREN function should be done before WRSR function. And after the Programming function, AK6516C becomes Write Disable status automatically.



WRSR

WPEN Bit	$\overline{WP}$ Pin	WEN Bit	Write Protected Block	Not Protected Block	Status Register
0	X	0	WRITE Disable	WRITE Disable	WRITE Disable
0	X	1	WRITE Disable	WRITE Enable	WRITE Enable
1	Low	0	WRITE Disable	WRITE Disable	WRITE Disable
1	Low	1	WRITE Disable	WRITE Enable	WRITE Disable
X	High	0	WRITE Disable	WRITE Disable	WRITE Disable
X	High	1	WRITE Disable	WRITE Enable	WRITE Enable

Table 3. WPEN function

Status Register bits		Write Protected Block
BP1	BP0	
0	0	none
0	1	6000h - 7FFFh
1	0	4000h - 7FFFh
1	1	0000h - 7FFFh

Table 4. Write Protected Block Size

WRITE (WRITE SEQUENCE)

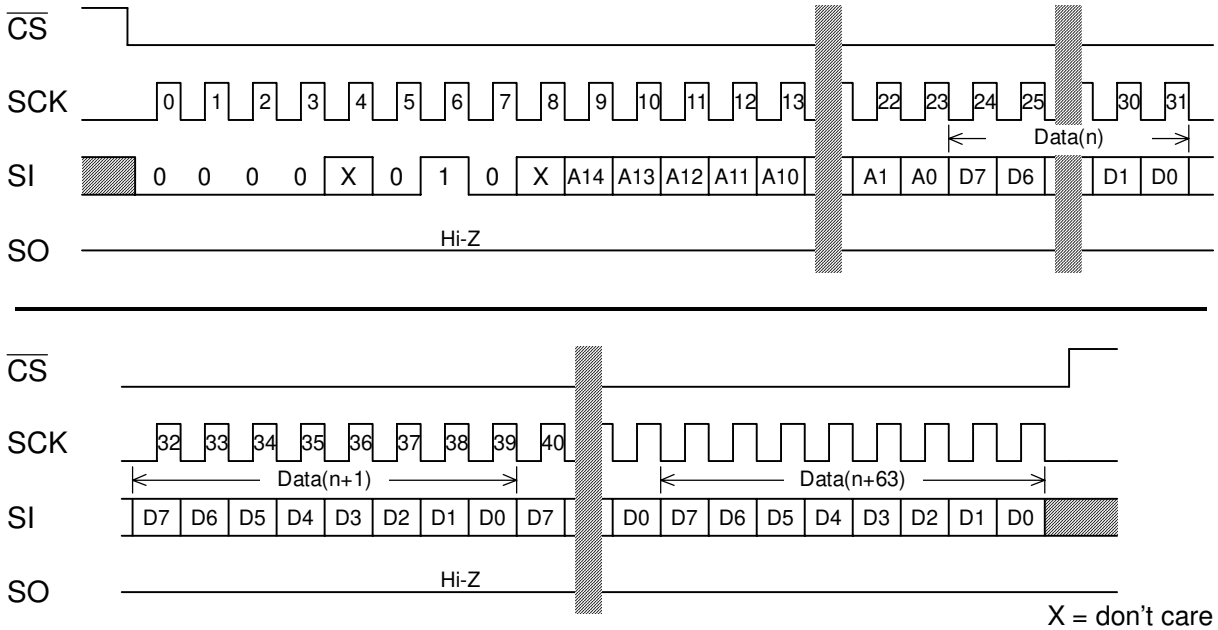
WRITE instruction can start the WRITE function to the memory cell array.
After $\overline{CS}$ pin changes high to low, op-code, address and data are input from SI pin. After the instruction input, the internal programming cycle starts when $\overline{CS}$ pin changes low to high. After the instructions are inputted, $\overline{CS}$ pin should change low to high after the last data bit (D0) inputs and before next SCK clock rises. Write function can start only at this timing.

AK6516C can indicate the BUSY status by using RDSR instruction and READ the $\overline{RDY}$ bit (Bit0) in the status register. $\overline{RDY}$ is "1" indicates AK6516C is in the programming cycle, and $\overline{RDY}$ is "0" indicates AK6516C is in the READY status. AK6516C outputs the "FF" when RDSR instruction executes during the programming cycle. Only RDSR instruction can be accepted during programming cycle.

AK6516C has Page Write mode, which can write the data within 64 bytes with one programming cycle. The input data sent to the shift register within 64 bytes. If the number of bytes exceeded 64, the address counter rolls over to the first address of the page.
Internal programming cycle starts after $\overline{CS}$ pin changes low to high.

After WRITE instruction, AK6516C changes to Write Disable status automatically. AK6516C needs WREN instruction before every WRITE instruction. When WRITE instruction is done while AK6516C is in Write Disable status, WRITE instructions are ignored and AK6516C becomes standby status after $\overline{CS}$ changes to high. AK6516C can accept the next instruction after $\overline{CS}$ becomes low.

WRITE instruction cannot write the data into the address of the protected block.

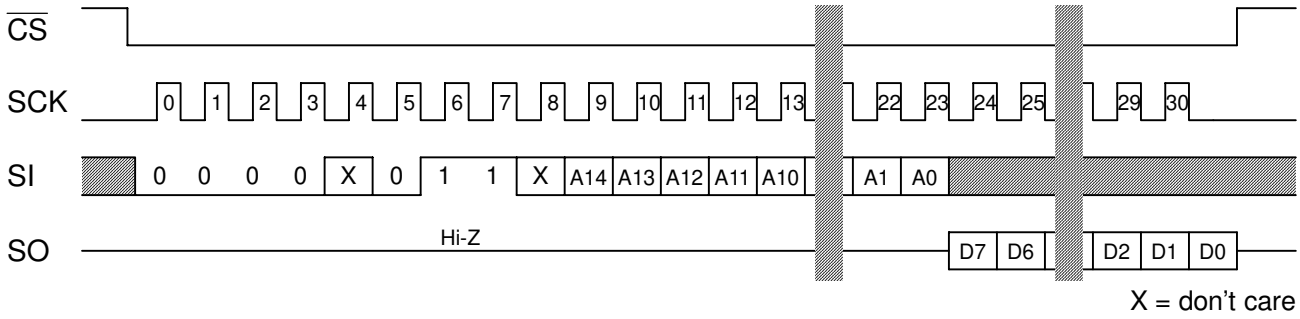


WRITE

READ (READ SEQUENCE)

After $\overline{CS}$ changes high to low, the op-code and address are sent on SI pin and the data (D7-D0) read from SO pin.

After 1 byte of data output, internal address register is incremented, and the next byte of data is outputted. After READ the data in the highest address, the address register rolls over to the lowest address. After the last bit of the address shift into the register, the input data on SI pin is ignored.



READ

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	-0.6	+6.5	V
All Input Voltages with Respect to Ground	VIO	-0.6	VCC+0.6	V
Ambient Storage Temperature	Tst	-65	+150	°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	1.6	5.5	V
Ambient Operating Temperature	Ta	-40	+85	°C

Electrical Characteristics

(1) D.C. ELECTRICAL CHARACTERISTICS

(1.6V≤VCC≤5.5V, -40°C≤Ta≤85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
Current Dissipation (WRITE)	ICC1	VCC=5.5V,fSCK=10.0MHz, *1		2.5	mA
	ICC2	VCC=2.5V,fSCK=5.0MHz, *1		2.0	mA
	ICC3	VCC=1.6V,fSCK=2.0MHz, *1		1.5	mA
Current Dissipation (READ)	ICC4	VCC=5.5V,fSCK=10.0MHz, *1		2.0	mA
	ICC5	VCC=2.5V,fSCK=5.0MHz, *1		0.4	mA
	ICC6	VCC=1.6V,fSCK=2.0MHz, *1		0.2	mA
Current Dissipation (Standby)	ICCS	VCC=5.5V *2		0.8	μA
Input High Voltage	VIH1	2.5V≤VCC≤5.5V	0.7xVCC	VCC+0.5	V
	VIH2	1.6V≤VCC<2.5V	0.8xVCC	VCC+0.5	V
Input Low Voltage	VIL1	2.5V≤VCC≤5.5V	-0.3	0.3xVCC	V
	VIL2	1.6V≤VCC<2.5V	-0.3	0.2xVCC	V
Output High Voltage	VOH1	4.5V≤VCC≤5.5V IOH=-2mA	VCC-0.5		V
	VOH2	2.5V≤VCC<4.5V IOH=-0.4mA	VCC-0.2		V
	VOH3	1.6V≤VCC<2.5V IOH=-0.1mA	VCC-0.2		V
Output Low Voltage	VOL1	4.5V≤VCC≤5.5V IOL=3.0mA		0.4	V
	VOL2	2.5V≤VCC<4.5V IOL=1.6mA		0.4	V
	VOL3	2.5V≤VCC<4.5V IOL=1.0mA		0.2	V
	VOL4	1.6V≤VCC<2.5V IOL=1.0mA		0.2	V
Input Leakage $\overline{CS}$, SCK, DI pins $\overline{WP}$, $\overline{HOLD}$ pins	ILI	VCC=5.5V, VIN=VCC/GND		±1.0	μA
Output Leakage SO pin	ILO	VCC=5.5V, VOUT=VCC/GND		±1.0	μA

*1: VIN=VIH/VIL, SO=open

*2: $\overline{CS}$=VCC, VIN=VCC/GND, $\overline{WP}$,$\overline{HOLD}$=VCC, SO=open

(2) CAPACITANCE

(Ta=25°C, fSCK=1MHz, VCC=5.0V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Output Capacitance SO pin	CO	VO=0V		8.0	pF
Input Capacitance $\overline{CS}$, SCK, SI pins	CIN	VIN=0V		6.0	pF

Note: These parameters are not 100% tested. These are the sample value.

(3) A.C. ELECTRICAL CHARACTERISTICS 1

(1.6V≤VCC≤5.5V, -40°C≤Ta≤85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
SCK Frequency	fSCK1	4.5V≤VCC≤5.5V		10.0	MHz
	fSCK2	2.5V≤VCC<4.5V		5.0	MHz
	fSCK3	1.6V≤VCC<2.5V		2.0	MHz
SCK Setup Time	tSKSH1	4.5V≤VCC≤5.5V	20		ns
	tSKSH2	2.5V≤VCC<4.5V	50		ns
	tSKSH3	1.6V≤VCC<2.5V	50		ns
$\overline{CS}$ Setup Time	tCSS1	4.5V≤VCC≤5.5V	40		ns
	tCSS2	2.5V≤VCC<4.5V	80		ns
	tCSS3	1.6V≤VCC<2.5V	200		ns
SCK Pulse Width	tSKW1	4.5V≤VCC≤5.5V	40		ns
	tSKW2	2.5V≤VCC<4.5V	80		ns
	tSKW3	1.6V≤VCC<2.5V	200		ns
SCK Rise Time *3	tRC			2	μs
SCK Fall Time *3	tFC			2	μs
Data Setup Time	tDIS1	4.5V≤VCC≤5.5V	15		ns
	tDIS2	2.5V≤VCC<4.5V	20		ns
	tDIS3	1.6V≤VCC<2.5V	50		ns
Data Hold Time	tDIH1	4.5V≤VCC≤5.5V	15		ns
	tDIH2	2.5V≤VCC<4.5V	30		ns
	tDIH3	1.6V≤VCC<2.5V	60		ns
Data Rise Time *3	tRD			2	μs
Data Fall Time *3	tFD			2	μs
SO pin Output Delay	tPD1	4.5V≤VCC≤5.5V		25	ns
	tPD2	2.5V≤VCC<4.5V		60	ns
	tPD3	1.6V≤VCC<2.5V		100	ns
SO pin Hi-Z Time	tOZ1	4.5V≤VCC≤5.5V		40	ns
	tOZ2	2.5V≤VCC<4.5V		100	ns
	tOZ3	1.6V≤VCC<2.5V		200	ns
SO pin Output Hold Time	tOHD		0		ns
$\overline{CS}$ Hold Time	tCSH1	4.5V≤VCC≤5.5V	40		ns
	tCSH2	2.5V≤VCC<4.5V	80		ns
	tCSH3	1.6V≤VCC<2.5V	200		ns
SCK Hold Time	tSKH1	4.5V≤VCC≤5.5V	20		ns
	tSKH2	2.5V≤VCC<4.5V	50		ns
	tSKH3	1.6V≤VCC<2.5V	50		ns
$\overline{CS}$ High Time	tCS1	4.5V≤VCC≤5.5V	40		ns
	tCS2	2.5V≤VCC<4.5V	100		ns
	tCS3	1.6V≤VCC<2.5V	200		ns

*3: These parameters are not 100% tested. These are the sample value.

(4) A.C. ELECTRICAL CHARACTERISTICS 2

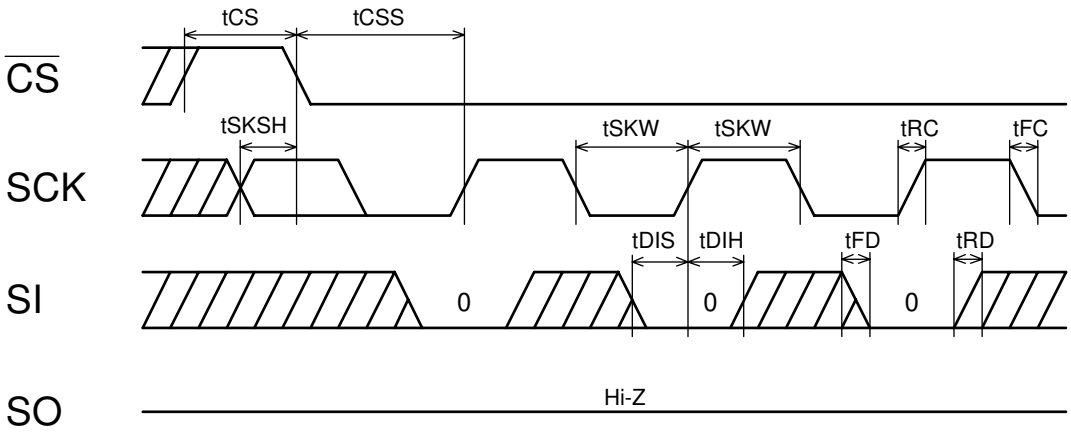
(1.6V≤VCC≤5.5V, -40°C≤Ta≤85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{\text{HOLD}}$ Setup Time 1	tHFS1	4.5V≤VCC≤5.5V	15		ns
	tHFS2	2.5V≤VCC<4.5V	30		ns
	tHFS3	1.6V≤VCC<2.5V	90		ns
$\overline{\text{HOLD}}$ Hold Time 1	tHFH1	4.5V≤VCC≤5.5V	15		ns
	tHFH2	2.5V≤VCC<4.5V	30		ns
	tHFH3	1.6V≤VCC<2.5V	90		ns
$\overline{\text{HOLD}}$ Setup Time 2	tHRS1	4.5V≤VCC≤5.5V	15		ns
	tHRS2	2.5V≤VCC<4.5V	30		ns
	tHRS3	1.6V≤VCC<2.5V	90		ns
$\overline{\text{HOLD}}$ Hold Time 2	tHRH1	4.5V≤VCC≤5.5V	15		ns
	tHRH2	2.5V≤VCC<4.5V	30		ns
	tHRH3	1.6V≤VCC<2.5V	90		ns
$\overline{\text{HOLD}}$ Low to Output Hi-Z	tHOZ1	4.5V≤VCC≤5.5V		25	ns
	tHOZ2	2.5V≤VCC<4.5V		100	ns
	tHOZ3	1.6V≤VCC<2.5V		150	ns
$\overline{\text{HOLD}}$ High to Output Low-Z	tHPD1	4.5V≤VCC≤5.5V		25	ns
	tHPD2	2.5V≤VCC<4.5V		50	ns
	tHPD3	1.6V≤VCC<2.5V		100	ns
Selftimed Programming Time	tWR			5	ms

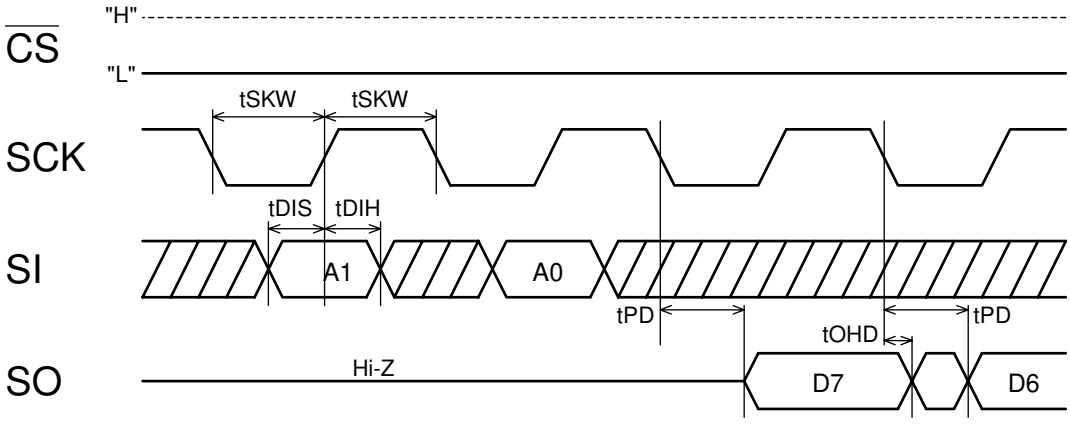
■ AC Measurement Condition

Load Capacitance	CL=100pF

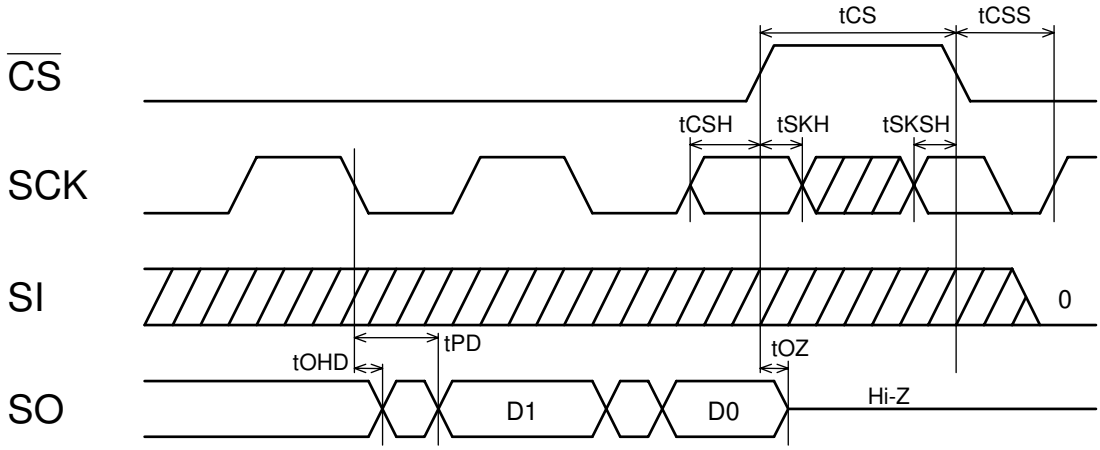
Synchronous Data Timing



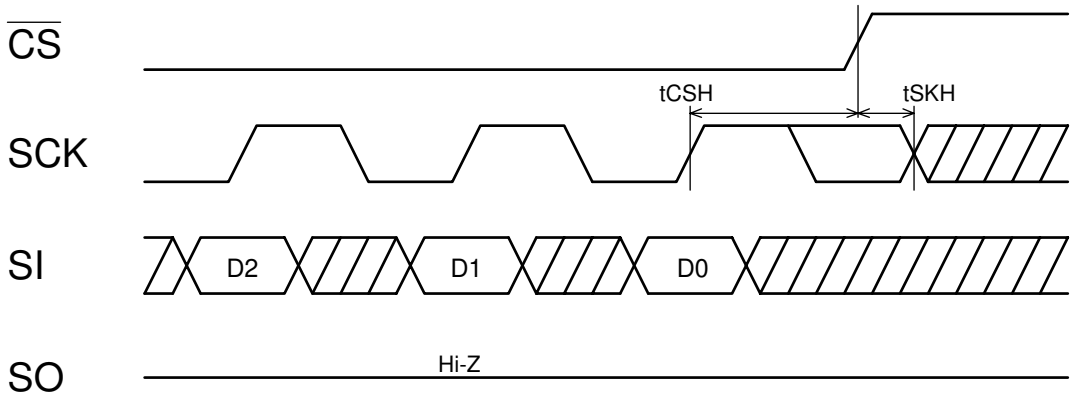
Instruction Input



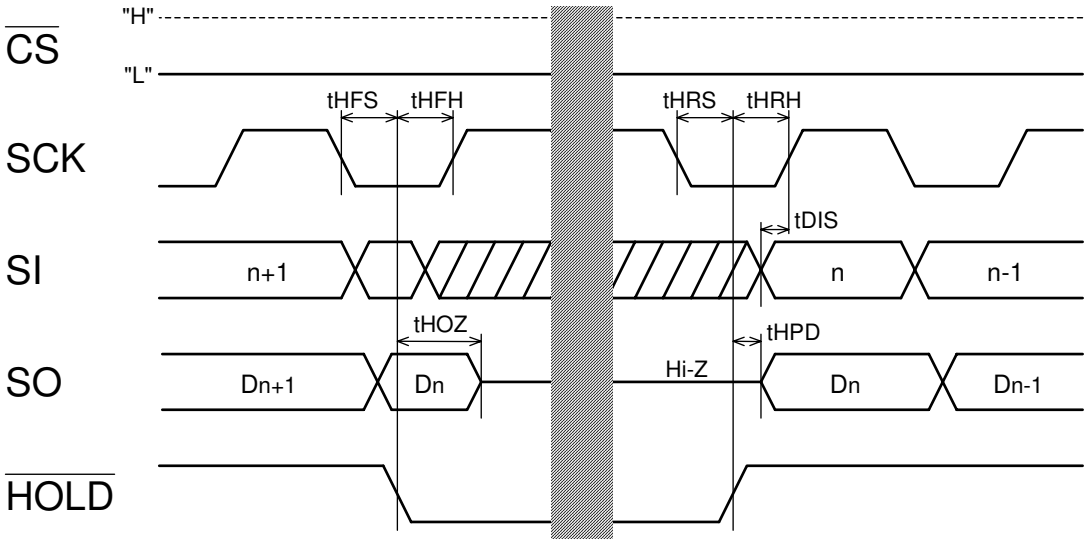
Data Output (READ)



Data Output (READ)



Data Input (WRITE)


"H"
"L"
CS
SCK
SI
SO
HOLD
tHFS
tHFH
tHRS
tHRH
tDIS
tHOZ
tHPD
n+1
n
n-1
Dn+1
Dn
Hi-Z
Dn
Dn-1

Hold

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