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AK7742

24bit 2ch ADC + 24bit 4ch DAC with Audio DSP

GENERAL DESCRIPTION

The AK7742 is a highly integrated audio digital processor, including two stereo 24bit DAC's and one stereo ADC with input selector. The stereo DAC and ADC feature high performance, archiving 106dB and 96dB dynamic range respectively, 8kHz to 96kHz sampling rate are supported. The audio DSP has 1536step/fs parallel processing power, and 74k-bit delay memory allows surround processing, acoustic effect and parametric equalizers. As the AK7742 is a RAM based DSP, it is programmable for user requirements. The AK7742 is available in a space saving small 48pin LQFP package.

FEATURES

■ **DSP:**
- **Word length: 24bit (Data RAM 24bit floating point)**
- **Instruction cycle: 13.6 ns (1536step/fs fs=48kHz; 9216step/fs fs=8kHz)**
- **Multiplier 20 x 16 → 36bit (double precision available)**
- **Divider 20 / 20 → 20bit**
- **ALU: 40bit arithmetic operation (overflow margin 4bit) 24bit floating point arithmetic and logic operation**
- **Program RAM: 1536 x 36bit**
- **Coefficient RAM: 1536 x 16bit**
- **Data RAM: 1536 x 24-bit (24bit floating point)**
- **Delay RAM: 74kbit (3072 x 24bit)**
- **Sampling frequency: 8kHz ~ 96kHz**
- **Master / Slave operation**
- **Serial signal input port (4ch) MSB justified 24bit / LSB justified 24 / 20 / 16bit and I^2S**
- **Serial signal output port (6ch) MSB justified 24bit / LSB justified 24 / 16bit and I^2S**

■ **ADC: 2ch (stereo)**
- **24bit 64 x Over-sampling delta sigma (fs=8kHz~48kHz)**
- **DR, S/N: 96dB (fs=48kHz, fully differential input)**
- **S/(N+D): 84dB (fs=48kHz)**
- **Differential, Single-end Inputs**
- **Digital HPF (fc=1Hz)**
- **3:1 Analog input selector**
- **Digital Volume (24dB~-103dB, 0.5dB Step, Mute)**

■ **DAC: 4ch (two stereo pairs)**
- **24bit 128 x Over-sampling advanced multi-bit (fs=8kHz~96kHz)**
- **DR, S/N: 106dB**
- **S/(N+D): 92dB**
- **Differential output**
- **Digital Volume (12dB~-115dB, 0.5dB Step, Mute)**

■ **DSP Through Mode**

■ **I^2C BUS interface for micro-controller**

■ **Power supply: +3.3V ±0.3V, internal regulator for 1.8V**

■ **Operating temperature range: -20°C~70°C (AK7742EQ), -20°C~85°C (AK7742EN)**

■ **Package: 48pin LQFP, 0.5mm pitch (AK7742EQ)**
48pin QFN, 0.4mm pitch (AK7742EN)

■ Block Diagram

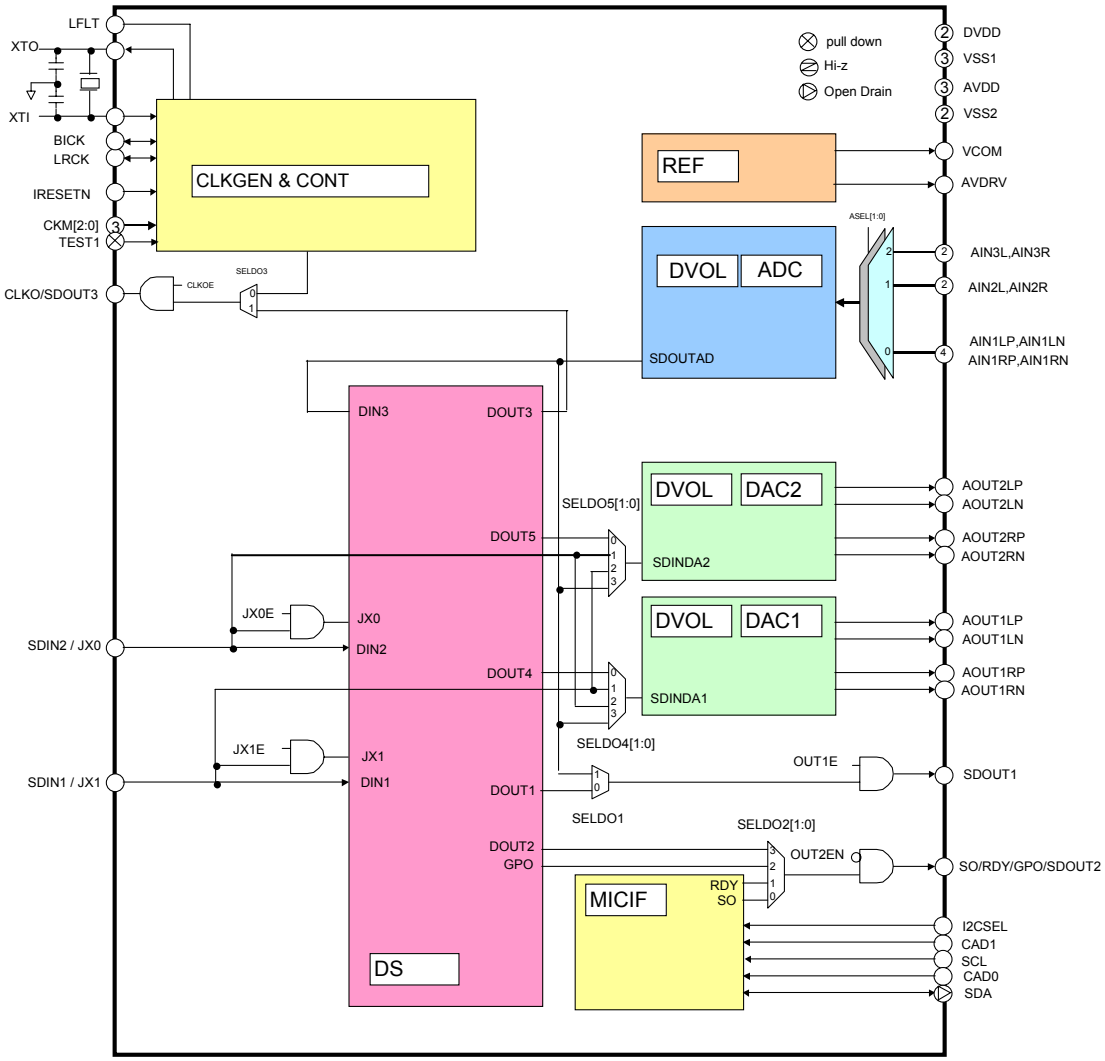


Figure 1. Block Diagram

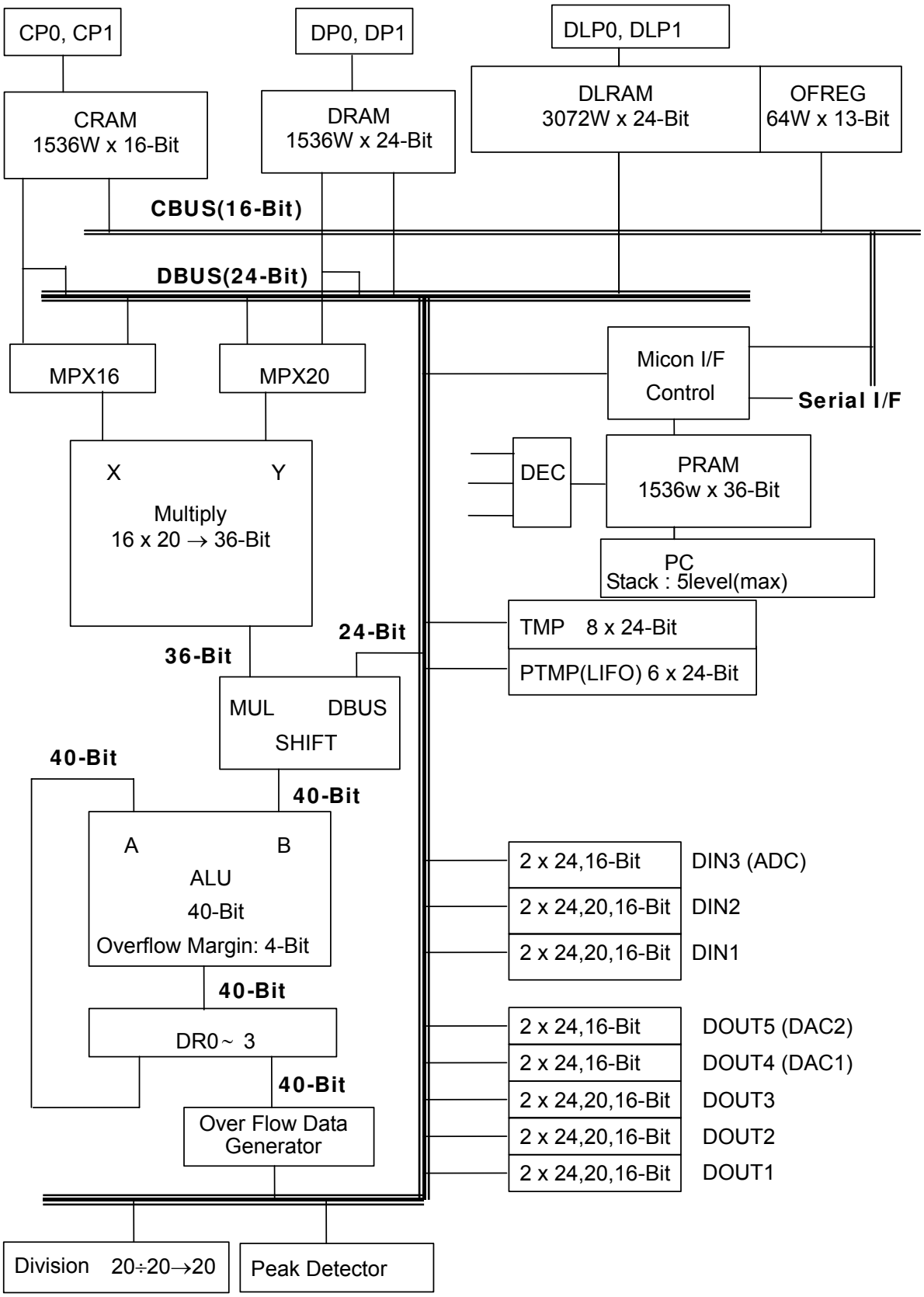


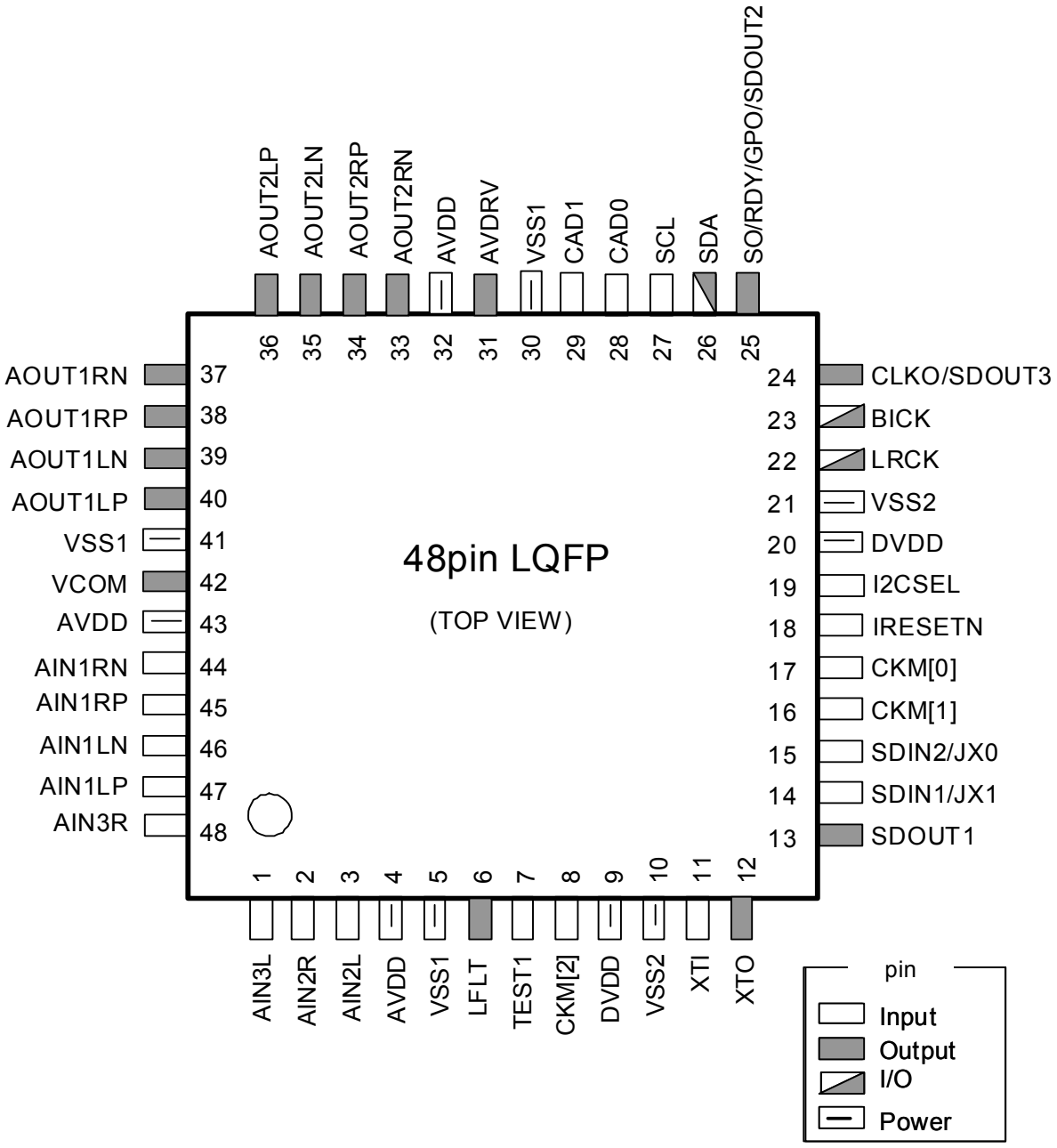
Figure 2. AK7742 DSP Block

■ Ordering Guide

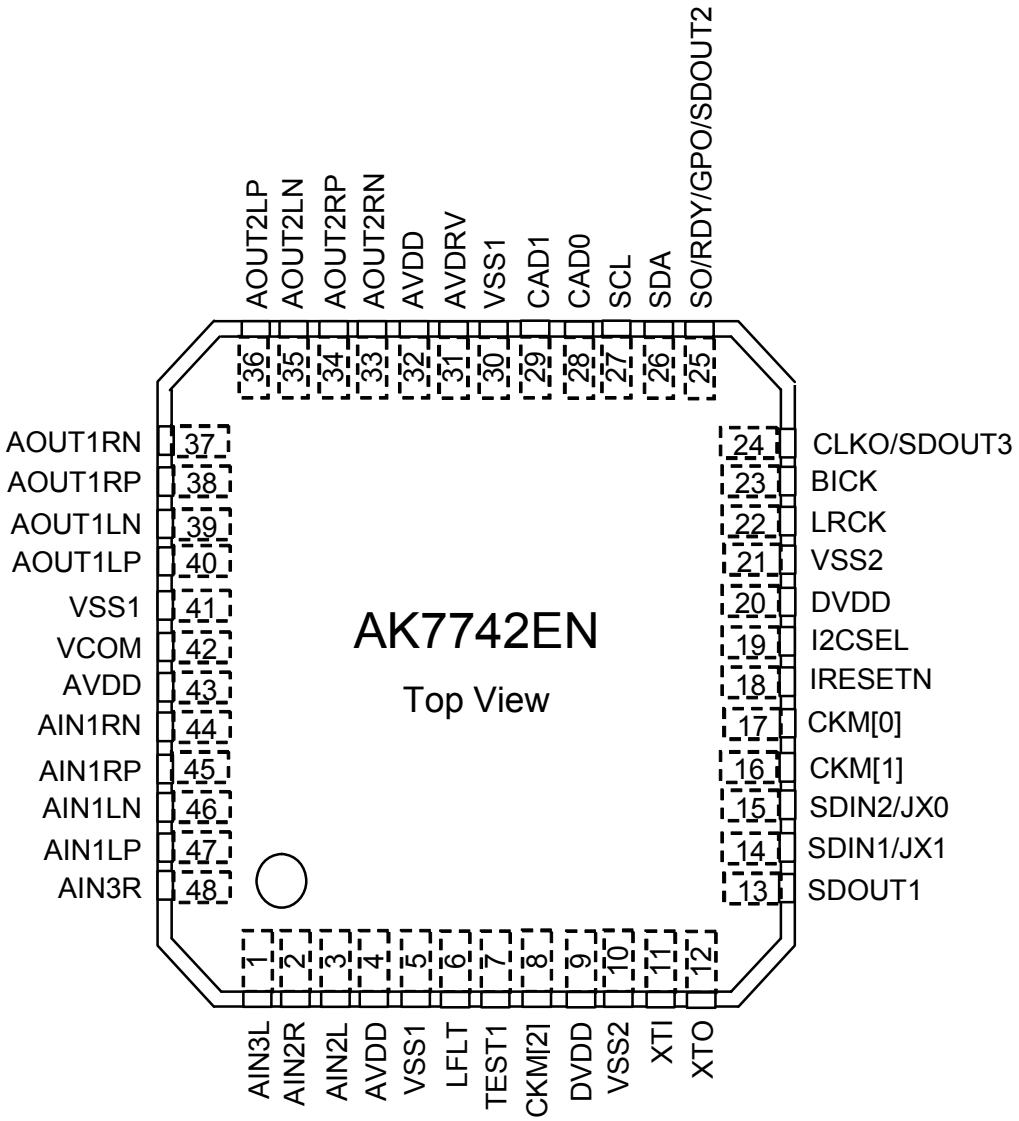
AK7742EQ	-20 ~ +70°C	48pin LQFP (0.5mm pitch)
AK7742EN	-20 ~ +85°C	48pin QFN (0.4mm pitch)
AKD7742	Evaluation board for the AK7742	

■ Pin Layout

AK7742EQ



AK7742EN


AK7742EN
Top View
1 AIN3L
2 AIN2R
3 AIN2L
4 AVDD
5 VSS1
6 LFLT
7 TEST1
8 CKM[2]
9 DVDD
10 VSS2
11 XTI
12 XTO
13 SDOUT1
14 SDIN1/JX1
15 SDIN2/JX0
16 CKM[1]
17 CKM[0]
18 IRESETN
19 I2CSEL
20 DVDD
21 VSS2
22 LRCK
23 BICK
24 CLKO/SDOUT3
25 SO/RDY/GPO/SDOUT2
26 SDA
27 SCL
28 CAD0
29 CAD1
30 VSS1
31 AVDRV
32 AVDD
33 AOUT2RN
34 AOUT2RP
35 AOUT2LN
36 AOUT2LP
37 AOUT1RN
38 AOUT1RP
39 AOUT1LN
40 AOUT1LP
41 VSS1
42 VCOM
43 AVDD
44 AIN1RN
45 AIN1RP
46 AIN1LN
47 AIN1LP
48 AIN3R

PIN FUNCTION

No.	Pin name	I/O	Function	Classification
1	AIN3L	I	ADC Lch Single-end input 3 pin	Analog input
2	AIN2R	I	ADC Rch Single-end input 2 pin	Analog input
3	AIN2L	I	ADC Lch Single-end input 2 pin	Analog input
4	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
5	VSS1		Analog ground 0V	Analog power supply
6	LFLT	O	Filter connection pin for PLL Connect C=12nF to VSS1. "L" output during initial reset.	Analog output
7	TEST1	I	Test pin (internal pull-down resistor) Connect to VSS2	Test
8	CKM[2]	I	Clock mode select pin 2	Mode select
9	DVDD		Power supply pin for digital section 3.0V ~ 3.6V	Digital power supply
10	VSS2		Digital ground 0V	Digital power supply
11	XTI	I	Master clock input pin When using a crystal oscillator, connect it between this pin and XTO. When using external main clock, input to this pin with CMOS level.	Clock
12	XTO	O	Crystal oscillator output pin When using a crystal oscillator, connect it between this pin and XTI. When not using crystal oscillator, leave open. Output during initial reset is not determined.	Clock
13	SDOUT1	O	DSP serial data output pin "L" output during initial reset	Data interface
14	SDIN1/JX1	I	Serial data input pin 1 / JX1	Data interface
15	SDIN2/JX0	I	Serial data input pin 2 / JX0	Data interface
16	CKM[1]	I	Clock mode select pin 1	Mode select
17	CKM[0]	I	Clock mode select pin 0	Mode select
18	IRESETN	I	Reset pin (for initialization)	Reset
19	I2CSEL	I	I^2CBUS select pin Connect to DVDD	Microcomputer I/F
20	DVDD		Power supply pin for digital section 3.0V ~ 3.6V	Digital power supply
21	VSS2		Digital ground 0V	Digital power supply
22	LRCK	I/O	LR channel select clock pin "L" output during initial reset with master mode.	Data interface
23	BICK	I/O	Serial bit clock pin "L" output during initial reset with master mode.	Data interface
24	CLKO/SDOUT3	O	Clock output / DSP serial data output pin "L" output during initial reset	Clock
25	SO/RDY/GPO/ SDOUT2	O	Serial data output pin / Data write ready output pin / General purpose output / DSP serial data output pin "L" output during initial reset	Microcomputer I/F
26	SDA	I/O	SDA I^2C bus interface	Microcomputer I/F
27	SCL	I	SCL I^2C bus interface	Microcomputer I/F
28	CAD0	I	I^2C bus address pin 0	Microcomputer I/F
29	CAD1	I	I^2C bus address pin 1	Microcomputer I/F
30	VSS1		Analog ground 0V	Analog power supply

31	AVDRV	O	AVDRV Pin Connect 1μF to VSS1. Never to use for external circuit. “L” output during initial reset	Analog power supply
32	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
33	AOUT2RN	O	DAC2 Rch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
34	AOUT2RP	O	DAC2 Rch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
35	AOUT2LN	O	DAC2 Lch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
36	AOUT2LP	O	DAC2 Lch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
37	AOUT1RN	O	DAC1 Rch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
38	AOUT1RP	O	DAC1 Rch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
39	AOUT1LN	O	DAC1 Lch differential inverted analog output pin “Hi-Z” output during initial reset	Analog output
40	AOUT1LP	O	DAC1 Lch differential non-inverted analog output pin “Hi-Z” output during initial reset	Analog output
41	VSS1		Analog ground 0V	Analog power supply
42	VCOM	O	Analog common voltage Connect 0.1μF and 2.2μF in parallel to VSS1. Never to use for external circuit. “L” output during initial reset	Analog output
43	AVDD		Power supply pin for analog section 3.0V ~ 3.6V	Analog power supply
44	AIN1RN	I	ADC Rch differential inverted analog input pin	Analog input
45	AIN1RP	I	ADC Rch differential non-inverted analog input pin	Analog input
46	AIN1LN	I	ADC Lch differential inverted analog input pin	Analog input
47	AIN1LP	I	ADC Lch differential non-inverted analog input pin	Analog input
48	AIN3R	I	ADC Rch Single-end input 3 pin	Analog input

Note:

Digital input pins are never to be left open.

If analog input pins (AIN1LP, AIN1LN, AIN1RP, AIN1RN, AIN2L, AIN2R, AIN3L, AIN3R) are not used, leave them open.

ABSOLUTE MAXMUM RATING

(VSS1=VSS2=0V: Note 1)

Item		Symbol	min	max	Unit
Power supply voltage (AVDD= DVDD)					
Analog		AVDD	-0.3	4.3	V
Digital		DVDD	-0.3	4.3	V
Input current (except for power supply pin)		IIN	-	±10	mA
Analog input voltage (Note 2) AIN1LP, AINL1N, AIN1RP, AINR1N, AIN2L, AIN2R, AIN3L, AIN3R		VINA	-0.3	(AVDD+0.3) or 4.3	V
Digital input voltage (Note 3)		VIND	-0.3	(DVDD+0.3) or 4.3	V
Operating ambient temperature	AK7742EQ	Ta	-20	70	ºC
	AK7742EN	Ta	-20	70	ºC
Storage temperature		Tstg	-65	150	ºC

Note 1. All indicated voltages are with respect to ground. VSS1 and VSS2 must be the same voltage.
Note 2. The maximum value of analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
Note 3. The maximum value of digital input voltage is smaller value between (DVDD+ 0.3)V and 4.3V.

WARNING: Operating at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these critical conditions.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V: Note 1)

Item	Symbol	min	typ	max	Unit
Power supply voltage					
Analog	AVDD	3.0	3.3	3.6	V
Digital	DVDD	3.0	3.3	3.6	V

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in the datasheet.

Note) Do not turn off the power of the AK7742 during the power supplies of surrounding devices are turned on. DVDD must not exceed the pull-up of SDA and SCL of I^2C BUS. (The diode exists for DVDD in the SDA and SCL pins.)

ANALOG CHARACTERISTICS

■ ADC Characteristics

(Ta=25ºC; AVDD=DVDD=3.3V; BICK=64fs; signal frequency 1kHz; Measurement bandwidth=20Hz~20kHz, fs=48kHz, ADC differential input, CKM mode 0 (CKM[2:0]=000), unless otherwise specified)

	Parameter	min	typ	max	Unit
Stereo ADC	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) (-1dBFS) (Note 4)	76	84		dB
	Dynamic range (A-weighted) (Note 4)	88	96		dB
	S/N (A-weighted) (Note 4)	88	96		dB
	Inter-channel isolation (f=1kHz) (Note 5)	90	105		dB
	DC accuracy				
	Channel gain mismatch		0.1	0.3	dB
	Analog input				
	Input voltage (differential input) (Note 6)	±1.85	±2.00	±2.15	Vp-p
	Input voltage (single-end input) (Note 7)	1.85	2.00	2.15	Vp-p
	Input impedance (Note 8)	41	62		kΩ

Note 4. This value is not guaranteed for single-ended inputs.
Note 5. Indicates isolation between L and R when -1dBFS signal is applied.
Note 6. Target input pins are AIN1LP, AIN1LN, AIN1RP, AIN1RN.
Note 7. Target input pins are AIN2L, AIN2R, AIN3L, AIN3R.
Note 8. Target input pins are AIN1LP, AIN1LN, AIN1RP, AIN1RN, AIN2L, AIN2R, AIN3L, AIN3R.

■ DAC Characteristics

(Ta=25ºC; AVDD=DVDD=3.3V; BICK=64fs; signal frequency 1kHz; Measurement bandwidth=20Hz~20kHz, fs=48kHz, R_L=5KΩ, C_L= 15pF; CKM mode 0 (CKM[2:0]=000), unless otherwise specified)

	Parameter	min	typ	max	Unit
Stereo DAC	Resolution			24	Bits
	Dynamic characteristics				
	S/(N+D) (0dBFS)	80	92		dB
	Dynamic range (A-weighted)	90	106		dB
	S/N (A-weighted)	90	106		dB
	Inter-channel isolation (f=1kHz)(Note 9)	90	100		dB
	DC accuracy				
	Channel gain mismatch		0.2	0.5	dB
	Analog output				
	Output voltage (Note 10)	3.36	3.66	3.96	Vp-p
	Load resistance	5			kΩ
	Load capacitance			30	pF

Note 9. Indicates isolation between each DAC's of Lch and Rch when -1dBFS signal is applied.
Note 10. Full scale output voltage. The output voltage scales with AVDD.

DC CHARACTERISTICS

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Unit
High level input voltage (Note 11)	VIH	80%DVDD			V
Low level input voltage (Note 11)	VIL			20%DVDD	V
SCL, SDA High level input voltage	VIH	70%DVDD			V
SCL, SDA Low level input voltage	VIL			30%DVDD	V
High level output voltage Iout=-100μA	VOH	DVDD-0.5			V
Low level output voltage Iout=100μA (Note 12)	VOL			0.5	V
SDA Low level output voltage Iout=3mA	VOL			0.4	V
Input leak current (Note 13)	Iin			±10	μA
Input leak current (pull-down) (Note 14)	Iid		22		μA
Input leak current XTI pin	Iix		26		μA

Note 11. Except for the SCL, SDA pin.
Note 12. Except for the SDA pin.
Note 13. Except for the TEST1 pin, XTI pin.
Note 14. The TEST1 pin has an internal pull-down device, nominally 150kΩ.

POWER CONSUMPTION

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V(typ=3.3V, max=3.6V))

Parameter	min	typ	max	Unit
Power supply current (Note 15)				
Normal Operation AVDD+DVDD		75	122	mA
Reset (IRESETN= "L" reference data) AVDD+DVDD (Note 16)		2		mA

Note 15. Depends on the system frequency and contents of DSP program.
Note 16. This is a reference value when using a crystal oscillator. Since most of the supply current at the initial reset state is in the oscillator section, the value may vary according to the crystal type and the external circuit. This value is just reference.

DIGITAL FILTER CHARACTERISTICS

■ ADC

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN), AVDD=DVDD=3.0~3.6V, fs=48kHz; Note 17)

Parameter	Symbol	min	typ	max	Unit
Pass band (±0.005dB) (Note 18)	PB	0		21.5	kHz
(-0.02dB)			21.768		kHz
(-6.0dB)			24.00		kHz
Stop band	SB	26.5			kHz
Pass band ripple (Note 18)	PR			±0.005	dB
Stop band attenuation (Note 19, Note 20)	SA	80			dB
Group delay distortion	ΔGD			0	μs
Group delay (Ts=1/fs)	GD		30		Ts
Digital filter + Analog filter characteristics					
Amplitude characteristic 20Hz~20.0kHz			±0.01		dB

Note 17. Each parameter is related to the sampling frequency (fs). HPF response is not included.
Note 18. Pass band is from DC to 21.5kHz when fs=48kHz.
Note 19. Stop band is from 26.5kHz to 3.0455MHz when fs=48kHz.
Note 20. When fs=48kHz, the analog modulator samples the analog input at 3.072MHz. Therefore the input signal is not attenuated by the digital filter in multiple bands (n x 3.072MHz ±21.99kHz; n=0, 1, 2, 3 …) of the sampling frequency.

■ DAC

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN), AVDD=DVDD=3.0~3.6V, fs=48kHz; Note 17)

Parameter	Symbol	min	typ	max	Unit
Digital filter					
Pass band ±0.07dB (Note 21)	PB	0		21.7	kHz
(-6.0dB)		-	24.0	-	kHz
Stop band (Note 21)	SB	26.2			kHz
Pass band ripple	PR			±0.01	dB
Stop band attenuation	SA	64			dB
Group delay (Ts=1/fs) (Note 22)	GD	-	24		Ts
Digital filter + Analog filter					
Amplitude characteristic 0~20.0kHz			±0.5		dB

Note 21. Pass band and Stop band parameter is related to sampling frequency(fs). PB=0.4535fs (at-0.05dB), SB=0.5465fs.
Note 22. The digital filter's delay is calculated as the time from setting 24-bit data into the input register until an analog signal is output.

SWITCHING CHARACTERISTICS

■ System Clock

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V)

Parameter		Symbol	min	typ	max	Unit
XTI						
a)with a crystal oscillator						
Frequency(256fs) CKM[2:0]= 000	fs=44.1KHz fs=48KHz	fXTI	-	11.2896 12.288	-	MHz
b)with an external clock						
Duty cycle		Duty	40	50	60	%
Frequency(256fs) CKM[2:0]= 000, 010	fs=44.1KHz fs=48KHz	fXTI	11.0	11.2896 12.288	12.4	MHz
Frequency (384fs) CKM[2:0]= 001	fs=44.1KHz fs=48KHz	fXTI	16.5	16.9344 18.432	18.6	MHz
LRCK frequency (Note 23)		Fs	7.35	48	96	kHz
BICK frequency						
a) CKM[2:0]= 001, 010			32	64		fs
High level width		tBCLKH	64			ns
Low level width		tBCLKL	64			ns
Frequency		fBCLK	0.46	3.072	6.144	MHz
b) CKM[2:0]= 011 (Note 25)				64		fs
Duty cycle		Duty	40	50	60	%
Frequency		fBCLK	2.75	3.072	3.1	MHz
c) CKM[2:0]= 100 (Note 26)				32		fs
Duty cycle		Duty	40	50	60	%
Frequency		fBCLK	230	256	258	kHz
d) CKM[2:0]= 101 (Note 27)				64		fs
Duty cycle		Duty	40	50	60	%
Frequency		fBCLK	460	512	516	kHz

Note 23. LRCK frequency and sampling rate (fs) should be the same.
Note 24. The BICK must be divided 32, 48 or 64 clocks correctly. (BICK can be selected from 32fs, 48fs or 64fs)
Note 25. When BICK is resource of internal MCLK. The BICK must be divided 64 clocks correctly. 64fs fixed.
Note 26. When BICK is resource of internal MCLK. The BICK must be divided 32 clocks correctly. 32fs fixed.
Note 27. When BICK is resource of internal MCLK. The BICK must be divided 64 clocks correctly. 64fs fixed.

■ Reset

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Unit
IRESET (Note 28)	tRST	600			ns

Note 28. It is necessity that the power is supplied and master clock is input when the IRESET pin goes to "H".

■ Audio Interface

1) SDIN1, SDIN2, SDOUT1, SDOUT2, SDOUT3

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave mode					
BICK frequency	fBCLK	32	64		fs
BICK low level width	tBCLKL	150			ns
BICK high level width	tBCLKH	150			ns
Delay time from BICK "↑" to LRCK (Note 29)	tBLRD	40			ns
Delay time from LRCK to BICK "↑" (Note 29)	tLRBD	40			ns
Serial data input latch setup time	tBSIDS	40			ns
Serial data input latch hold time	tBSIDH	40			ns
Delay time from LRCK to serial data output	tLRD	-10		40	ns
Delay time from BICK "↓" to serial data output (Note 30)	tBSOD	-10		40	ns
Master mode					
BICK frequency	fBCLK		64		fs
BICK duty cycle			50		%
Delay time from BICK "↑" to LRCK	tBLRD	40			ns
Delay time from LRCK to BICK "↑"	tLRBD	40			ns
Serial data input latch setup time	tBSIDS	40			ns
Serial data input latch hold time	tBSIDH	40			ns
Delay time from BICK "↓" to serial data output (Note 30)	tBSOD	-30		40	ns

Note 29. BICK rising edge must not occur at the same time as LRCK edge.

Note 30. The serial data output is synchronized to BICK falling edge, and held until next BICK falling (spec -10ns) in Slave mode. In case of the LRCK edge comes before BICK edge, data will be held until LRCK edge (spec -10ns). In Master mode, serial data is held until 30ns before falling edge of BICK. Therefore, please use BICK rising edge in both slave and master modes for a safety latch.

■ I²CBUS Interface

(Ta=-20°C ~70°C (AK7742EQ), Ta=-20°C ~85°C (AK7742EN); AVDD=DVDD=3.0~3.6V)

Parameter	Symbol	min	typ	max	Unit
I²C Timing					
SCL clock frequency	fSCL			400	KHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

Note 31. I²C is a registered trademark of Philips Semiconductors.

■ Timing Diagram

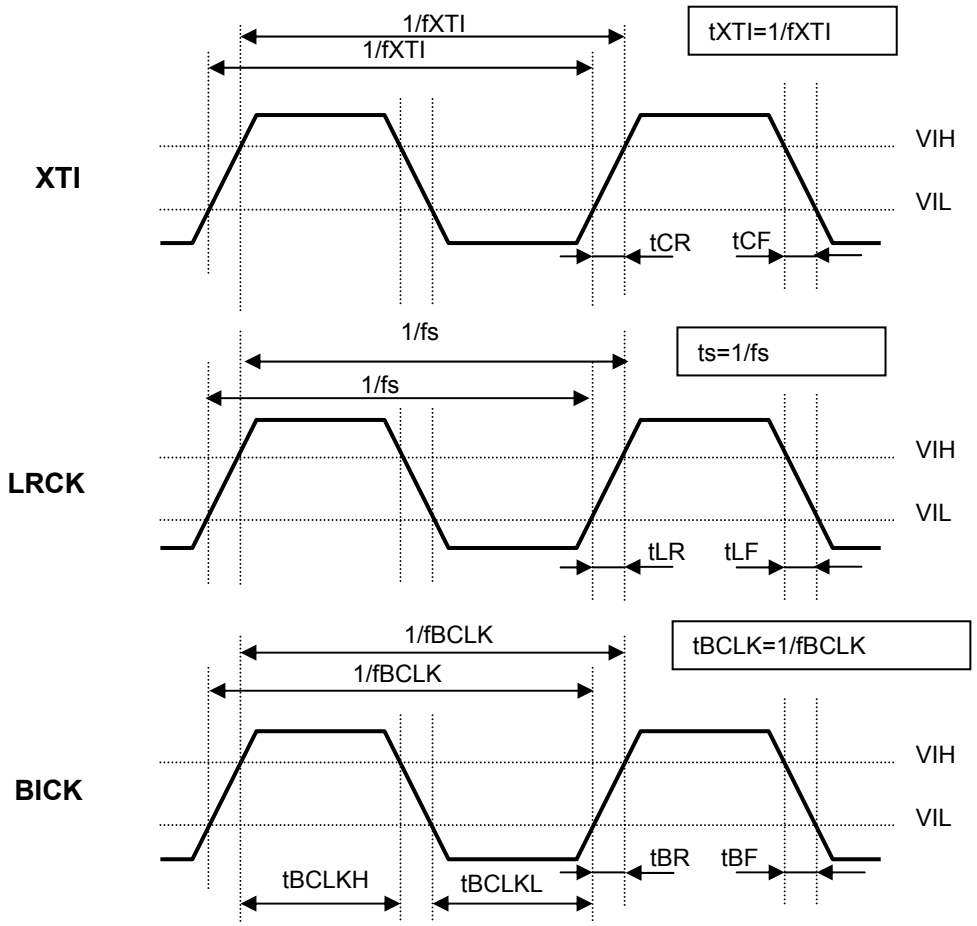


Figure 3. System Clock

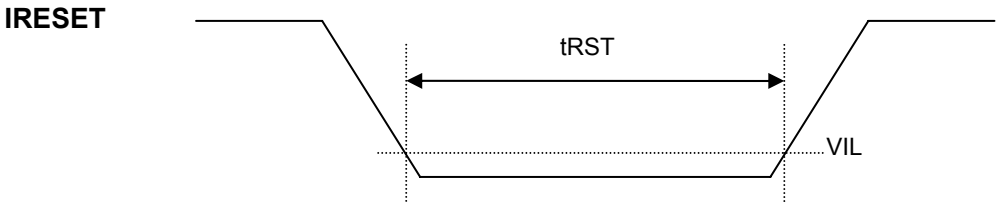


Figure 4. Reset

Audio Interface

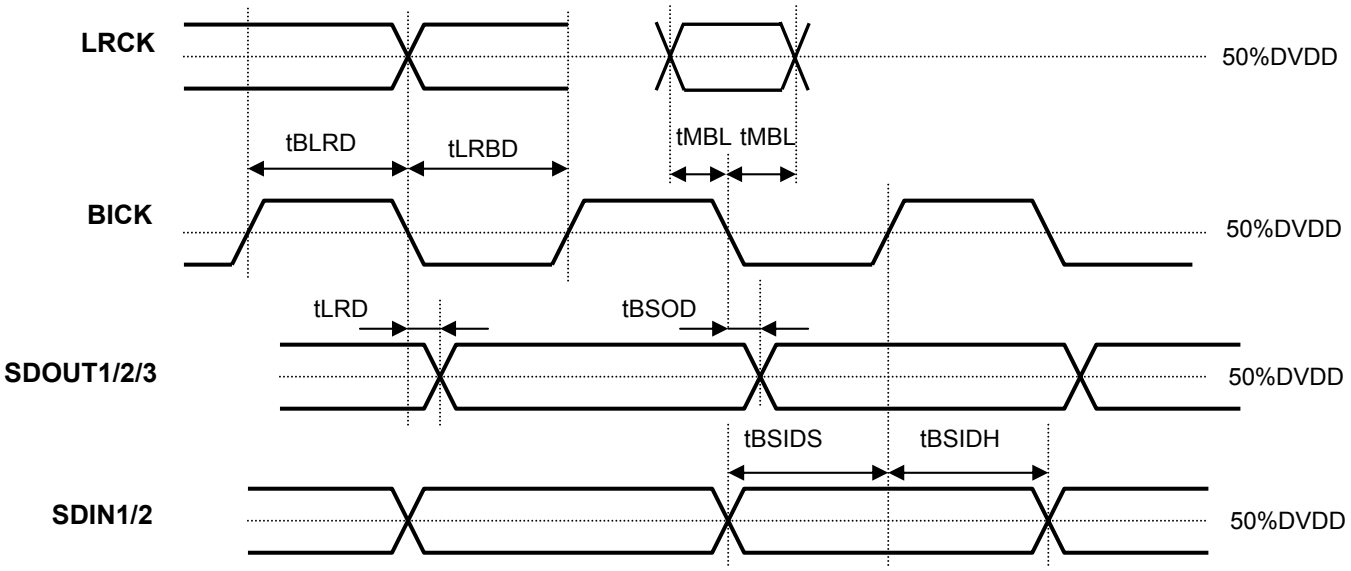


Figure 5. Audio Interface

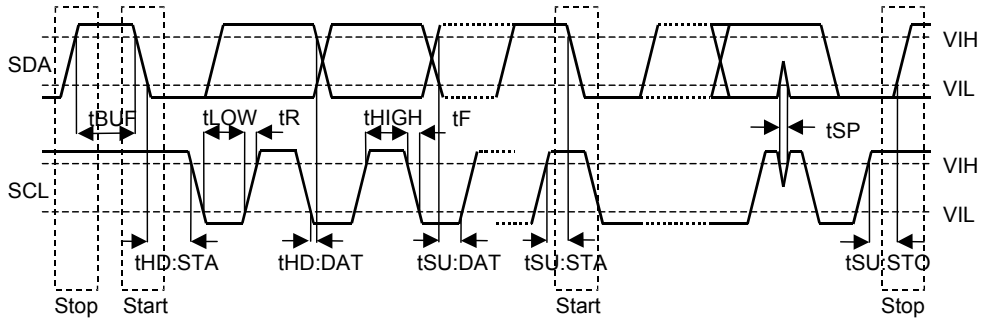


Figure 6. I^2C Bus Interface

OPERATION OVERVIEW

■ CKM[2:0] Clock Mode Select Pin

Master/Slave mode switching, MCLK/ICLK (internal master clock/generating clock) clock source pin select, and ICLK frequency change are controlled by CKM [2:0] clock mode select pins. CKM[2:0] pins can only be set during initial reset.

CKM Mode	CKM [2:0]	Master Slave	MCLK source	Input frequency for MCLK	Input pin(s) required for system clock	use the oscillator permitted
0	000	Master	XTI	12.288MHz (Note 32)	XTI (256fs)	YES
1	001	Slave	XTI	18.432MHz (Note 32)	XTI (384fs), BICK (32fs, 48fs, 64fs) LRCK (fs)	-
2	010	Slave	XTI	12.288MHz (Note 32, Note 35)	XTI(256fs), BICK (32fs, 48fs, 64fs), LRCK (fs)	-
3	011	Slave	BICK	64fs (fs=48kHz fixed)	BICK, LRCK	-
4	100	Slave	BICK	32fs (fs=8kHz fixed)	BICK, LRCK	-
5	101	Slave	BICK	64fs (fs=8kHz fixed)	BICK, LRCK	-
6	110	TEST	N/A	N/A	N/A	-
7	111	TEST	N/A	N/A	N/A	-

(N/A: Not available)

Note 32. On operating fs=44.1kHz series, multiply 44.1/48.
Note 33. CKM mode 6/7 are for testing purpose only. Cannot be used.
Note 34. The sampling frequency is set by control register CONT0 in CKM mode 0.
Note 35. In case of CKM mode 1/2, XTI and LRCK must be synchronized. The phase is not critical.
Note 36. The sampling frequency on CKM mode 3-5 is fixed. The setting of control register CONT0 is ignored.
Note 37. In case of CKM mode 3-5, BICK must be divided exactly from LRCK. BICK and LRCK must be synchronized.

[Description rule]
Regarding the input / output levels in this Datasheet, the low level is represented as "L" and the high level is represented as "H". The registers or bus pins (such as CKM[2:0] is represented "0" and "1".
##h means hexadecimal code. (# = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F)

■ Relationship of Clock Source (ICLK) and MCLK

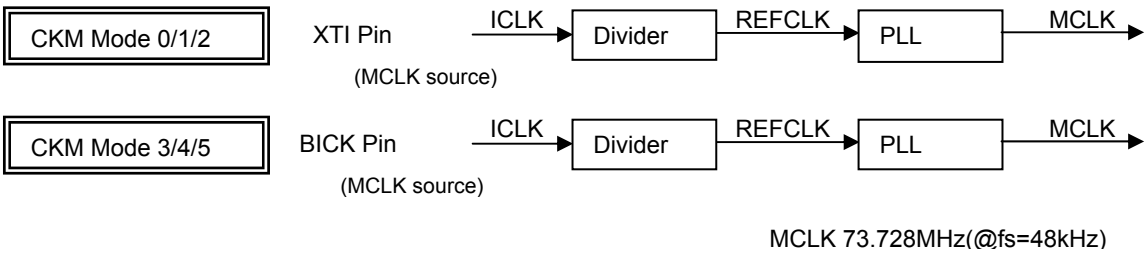


Figure 7. The Relationship of Clock Source (ICLK) and MCLK

1. Master Mode (CKM Mode 0)

fs: Sampling frequency

CKM Mode	CKM [2:0]	XTI		Input frequency range (MHz)	Use of crystal permitted
		fs:48kHz series	fs:44.1kHz series		
0	000	12.288MHz	11.2896MHz	11.0~12.4	YES

Input system clock to the XTI pin. The internal counter which is synchronized to XTI generates LRCK (1fs) and BICK (64fs). LRCK and BICK is not output during initial reset state (IRESETN pin= "L") and system reset state. (Refer to ■ Reset)

The system clock for the AK7742 can be supplied to the XTI pin by the following way. In case of CKM mode 0, connect proper crystal oscillator XTI and XTO pin, or supply appropriate system clock to the XTI pin.

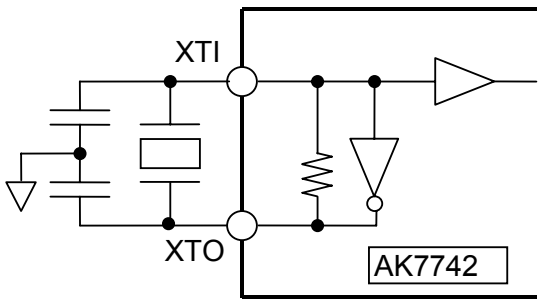


Figure 8. Using Crystal Oscillator (CKM Mode 0)

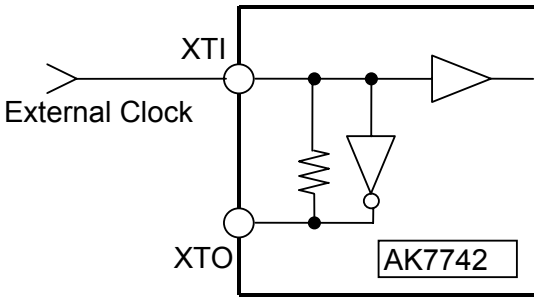


Figure 9. Using External System Clock(CKM Mode 0)

The sampling frequency is determined by control register CONT0 DFS[2:0] (D3, D2, D1).

2. Slave Mode (XTI Input Clock) (CKM Mode 1/2)

fs: sampling frequency

CKM Mode	CKM [2:0]	XTI		Input frequency range (MHz)	Use of crystal permitted
		fs:48kHz series	fs:44.1kHz series		
1	001	18.432MHz	16.9344MHz	16.5~18.6	Not Permitted
2	010	12.288MHz	11.2896MHz	11.0~12.4	Not Permitted

The required system clocks are XTI, LRCK and BICK. XTI and LRCK must be synchronized but the phase is not critical.

3. Slave Mode (BICK input) (CKM Mode 3/4/5)

In the CKM mode 3/4/5, BICK is used for clock source. This clock is multiplied by a PLL directly, therefore burst clock or the clock with two different frequencies can not be used.

fs: sampling frequency

CKM Mode	CKM [2:0]	BICK			Input frequency range
		BICK	fs:48kHz series	fs:44.1kHz series	
3	011	64fs(fs=48,44.1kHz)	3.072MHz	2.8224MHz	2.75~3.1MHz
4	100	32fs(fs=8kHz)	256kHz		230~258kHz
5	101	64fs(fs=8kHz)	512kHz	-	460~516kHz

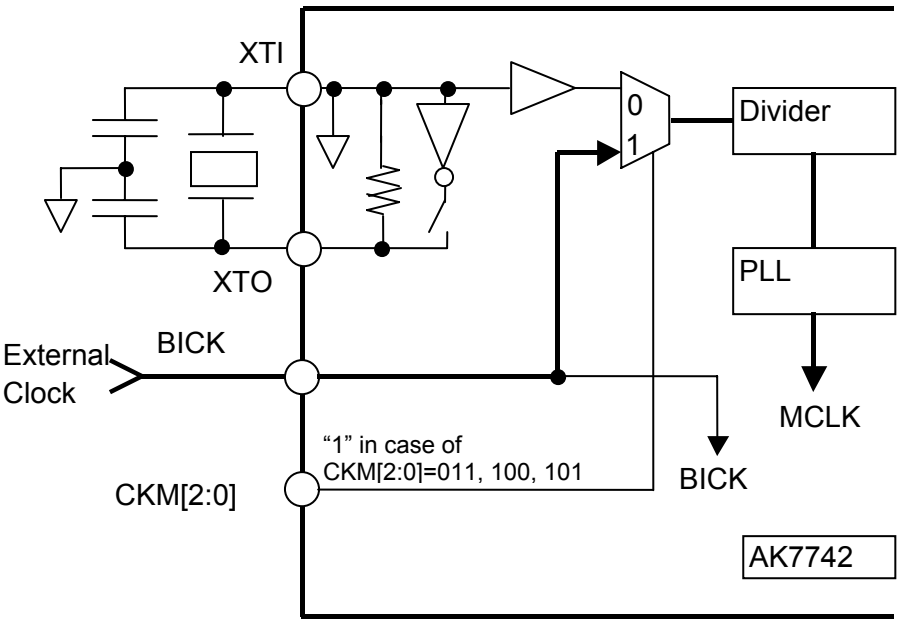


Figure 10. Internal Connection Image

Sampling rate is fixed by CKM[2:0] pin setting. The control register CONT0 DFS mode setting is ignored. In applications which do not need the XTI pin of the AK7742, set the XTI pin= "L"(VSS2).

4. CKM[2:0] Pin Setting Changing

CKM[2:0] pin setting must be made during initial reset after the AK7742 is powered-up or clock reset.

5. CKM[2:0] Pin Setting / IO Interface

Slave/ Master	CKM Mode	CKM [2:0]	DFS Mode	DFS [2:0]	fs(kHz)	BICK	
						MSB/LSB justified	I^2S compatible
M	0	000	0	000(default)	48/44.1	64fs	64fs
M	0	000	1	001	32/29.4	64fs	64fs
M	0	000	2	010	16/14.7	64fs	64fs
M	0	000	3	011	8	64fs	64fs
M	0	000	4	100	96/88.2	64fs	64fs
S	1	001	0	000(default)	48/44.1	64fs,48fs,32fs	64fs,48fs
S	1	001	1	001	32/29.4	64fs,48fs,32fs	64fs,48fs
S	1	001	2	010	16/14.7	64fs,48fs,32fs	64fs,48fs
S	1	001	3	011	8	64fs,48fs,32fs	64fs,48fs
S	1	001	4	100	96/88.2	64fs,48fs,32fs	64fs,48fs
S	2	010	0	000(default)	48/44.1	64fs,48fs,32fs	64fs,48fs
S	2	010	1	001	32/29.4	64fs,48fs,32fs	64fs,48fs
S	2	010	2	010	16/14.7	64fs,48fs,32fs	64fs,48fs
S	2	010	3	011	8	64fs,48fs,32fs	64fs,48fs
S	2	010	4	100	96/88.2	64fs,48fs,32fs	64fs,48fs
S	3	011	-	-	48/44.1	64fs	64fs
S	4	100	-	-	8	32fs	32fs
S	5	101	-	-	8	64fs	64fs

Note 38. DFS mode is assigned to control register CONT0 DFS[2:0] (D3, D2, D1).

■ Control Register Setting

The AK7742 control register settings are executed through a microcontroller interface. The AK7742 has 15 control registers, and each register has 8bit length. The LSB bit is always "0". Register configuration is shown below. The value of each control register becomes valid when LSB "0" is written.
All registers are initialized by IRESETN pin = "L". The system reset does not initialize the registers.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C0h	40h	CONT0	DIFPCM	DIFI2S	PCM[1]	PCM[0]	DFS[2]	DFS[1]	DFS[0]	0	00h
C1h	41h	CONT1	ATSPAD	ATSPDA	BANK[1]	BANK[0]	TEST	SS[1]	SS[0]	0	00h
C2h	42h	CONT2	POMODE	DATARAM	BIT32FS	WAVM	WAVP[1]	WAVP[0]	EEFN	0	00h
C3h	43h	CONT3	DIF[1]	DIF[0]	DOF[1]	DOF[0]	CLKS[2]	CLKS[1]	CLKS[0]	0	00h
C4h	44h	CONT4	CLKOE	BITCLKEN	LRCLKEN	OUT2EN	OUT1EN	JX1E	JX0E	0	00h
C5h	45h	CONT5	SELDO5 [0]	SELDO4 [0]	SELDO3	SELDO2[1]	SELDO2[0]	SELDO1	SELDO4 [1]	0	00h
C6h	46h	CONT6	ADMUTE	Reserved	ASEL[1]	ASEL[0]	SELDO5[1]	DA2MUTE	DA1MUTE	0	00h
C7h	47h	CONT7	DEM1[1]	DEM1[0]	DEM2[1]	DEM2[0]	TEST	TEST	TEST	0	00h
C8h	48h	CONT8	SRESETN	ADRST	DA2RST	DA1RST	DSPRST	TEST	CKRST	0	00h
D0h	50h	CONT10	VOLADL[7]	VOLADL[6]	VOLADL[5]	VOLADL[4]	VOLADL[3]	VOLADL[2]	VOLADL[1]	VOLADL[0]	30h
D1h	51h	CONT11	VOLADR[7]	VOLADR[6]	VOLADR[5]	VOLADR[4]	VOLADR[3]	VOLADR[2]	VOLADR[1]	VOLADR[0]	30h
D2h	52h	CONT12	VOLDA1L[7]	VOLDA1L[6]	VOLDA1L[5]	VOLDA1L[4]	VOLDA1L[3]	VOLDA1L[2]	VOLDA1L[1]	VOLDA1L[0]	18h
D3h	53h	CONT13	VOLDA1R[7]	VOLDA1R[6]	VOLDA1R[5]	VOLDA1R[4]	VOLDA1R[3]	VOLDA1R[2]	VOLDA1R[1]	VOLDA1R[0]	18h
D4h	54h	CONT14	VOLDA2L[7]	VOLDA2L[6]	VOLDA2L[5]	VOLDA2L[4]	VOLDA2L[3]	VOLDA2L[2]	VOLDA2L[1]	VOLDA2L[0]	18h
D5h	55h	CONT15	VOLDA2R[7]	VOLDA2R[6]	VOLDA2R[5]	VOLDA2R[4]	VOLDA2R[3]	VOLDA2R[2]	VOLDA2R[1]	VOLDA2R[0]	18h

Note 39. Do not access to not specified command codes or registers.
Note 40. "TEST" bit is for test purpose, "0" should be written.
Note 41. The default is initial value of when the IRESETN pin= "L".

1) CONT0: Sampling rate, I/O interface

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C0h	40h	CONT0	DIFPCM	DIFI2S	PCM[1]	PCM[0]	DFS[2]	DFS[1]	DFS[0]	0	00h

DIFPCM: Audio interface select

0: MSB justified, LSB justified, I²S (default)
1: PCM format

Note 42. When using PCM format, D6: DIFI2S must be set "0".

DIFI2S: Audio interface I²S select

0: Except I²S mode (default)
1: I²S mode

When using I2S mode for SDIN1-2, SDOUT1-3, set to DIFI2S bit = "1". All interface setting of DIF[1:0], DOF[1:0] should be set MSB justified (24bit). DIFI2S bit should be set to "0" when using DSP through mode, and all interface setting of DIF[1:0], DOF[1:0] should be set MSB justified (24bit).

Note 43. When using I²S format, D7: DIFPCM must be set "0".

PCM[1:0]: PCM format select (only slave mode available)

Select PCM interface at DIFPCM bit = "1".
PCM format is available for CKM mode 3/4/5.

PCM Mode	PCM[1:0]	LRCK (FRAME)	LRCK edge referenced to BICK edge	BIT32FS bit 0	BIT32FS bit 1	
0	00	short (SF)	rising (RE)	Figure 21	Figure 22	(default)
1	01	short (SF)	falling (FE)	Figure 23	Figure 24	
2	10	long (LF)	rising (RE)	Figure 25	Figure 26	
3	11	long (LF)	falling (FE)	Figure 27	Figure 28	

Please refer to "Audio Data Interface" section.

DFS[2:0]: Sampling frequency setting (CKM Mode 0/1/2)

fs: sampling frequency

CKM Mode	CKM [2:0]	DFS Mode	DFS [2:0]	fs(kHz) 48kHz series	fs(kHz) 44.1kHz series	
0-2	0XX	0	000	48	44.1	(default)
0-2	0XX	1	001	32	29.4	
0-2	0XX	2	010	16	14.7	
0-2	0XX	3	011	8	-	
0-2	0XX	4	100	96	88.2	
3	011	-	-	48	44.1	
4	100	-	-	8	-	
5	101	-	-	8	-	
6	110	-	-	N/A	N/A	
7	111	-	-	N/A	N/A	

(N/A: Not available)

Note 44. DFS mode is available for CKM mode 0/1/2.
No permission to set DFS mode 5-7.

Write "0" into the "0" register.

2) CONT1: RAM control

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C1h	41h	CONT1	ATSPAD	ATSPDA	BANK[1]	BANK[0]	TEST	SS[1]	SS[0]	0	00h

ATSPAD: ADC soft mute transition

0: 912LRCK(max) (19ms at fs=48kHz) (default)
1: 912LRCK x 4(max) (76ms at fs=48kHz)

ATSPDA: DAC1/2 Volume Transition Time Setting

0: 1/fs (default)
1: 4/fs

BANK[1:0]: DLRAM Mode setting

DLRAM Mode	BANK[1:0]	Ring 24bit limited range floating point	Ring 8.4f	Linear 24bit limited range floating point	
0	00	3072word			(default)
1	01	2048word	2048word		
2	10	1024word	2048word	1024word	
3	11	N/A	N/A	N/A	

(N/A: Not available)

SS[1:0]: DLRAM sampling setting

SS Mode	SS[1]	SS[0]	Sampling set time	
0	0	0	address is updated every sampling	(default)
1	0	1	address is updated every 2 samplings	
2	1	0	address is updated every 4 samplings	
3	1	1	address is updated every 8 samplings	

Note 45. When SS mode 1/2/3 is selected, aliasing noise may be generated.
Note 46. DLRAM mode 1/2 affects to the Ring 8.4f buffer only. DLRAM mode 0 affects to the Ring 20.4f buffer.

Write "0" into the TEST bits and "0" registers.

3) CONT2: RAM control

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C2h	42h	CONT2	POMODE	DATARAM	BIT32FS	WAVM	WAVP[1]	WAVP[0]	EEFN	0	00h

POMODE: DLRAM pointer0 select

0: OFREG (default)
1: DBUS direct

DATARAM: DATARAM addressing select

DATARAM Mode	A(000h-3FFh) 1024word	B(400h-5FFh) 512word	
0	Ring addressing	Ring addressing	(default)
1	Ring addressing	Linear addressing	
Pointer	DP0	DP1	

BIT32FS: BICK32fs setting (only slave mode available)

0: BICK64fs (default)
1: BICK32fs
Normally BICK is 64fs. At CKM mode 4, set BIT32FS bit = "1".

WAVM: CRAM WAV Mode select

0: 1/4 mode (default)
1: 1/2 mode
1/4 mode has an advantage of CRAM memory size but calculation precision drops down.

WAVP[1:0]: CRAM memory assignment

WAVP Mode	WAVP[1]	WAVP[0]	WAVM=0	WAVM=1	number of point	
0	0	0	33word	65word	128	(default)
1	0	1	65word	129word	256	
2	1	0	129word	257word	512	
3	1	1	257word	513word	1024	

EFEN: Extended Instruction enable

0: disable (default)
1: enable

Write "0" into the "0" registers.

4) CONT3: I/O interface / Clock select

Write during system reset state.

Command Code		Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write	Read										
C3h	43h	CONT3	DIF[1]	DIF[0]	DOF[1]	DOF[0]	CLKS[2]	CLKS[1]	CLKS[0]	0	00h

DIF[1:0]: DSP DIN1, DIN2 input format select

DIF Mode	DIF[1]	DIF[0]	input format	
0	0	0	MSB justified (24bit)	(default)
1	0	1	LSB justified 24bit	
2	1	0	LSB justified 20bit	
3	1	1	LSB justified 16bit	

Note 47. In case of I^2S format (DIFI2S bit = "1"), set DIF mode 0.

DOF[1:0]: DSP DOUT1, DOUT2, DOUT3 output format select

DOF Mode	DOF[1]	DOF[0]	output format	
0	0	0	MSB justified (24bit)	(default)
1	0	1	LSB justified 24bit	
2	1	0	LSB justified 20bit	
3	1	1	LSB justified 16bit	

Note 48. In case of I^2S format (DIFI2S bit = "1") or BIT32FS bit = "1", set DOF mode 0.

CLKS[2:0]:CLKO clock select

CLKS Mode	CLKS[2:0]	fs=48kHz series	fs=44.1kHz series	
0	000	12.288MHz	11.2896MHz	(default)
1	001	6.144MHz	5.6448MHz	
2	010	3.072MHz	2.8224MHz	
3	011	8.192MHz	7.5264MHz	
4	100	4.096MHz	3.7632MHz	
5	101	2.048MHz	1.8816MHz	
6	110	18.432MHz	16.9344MHz	
7	111	N/A	N/A	

(N/A: Not available)

Write "0" into the "0" registers.