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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AK7755

DSP with Mono ADC Stereo CODEC + Mic/Lineout Amp

1. General Description

The AK7755 is a highly integrated digital signal processor, including a mono ADC, a stereo audio CODEC, a MIC pre-amplifier, a line-out amplifier and digital audio I/F. The audio DSP has 2560step at fs = 48kHz parallel processing power. As the AK7755 is a RAM based DSP, it is programmable for user requirements such as high performance hands free function and acoustic effects. The AK7755 is available in a space saving small 36-pin QFN package.

2. Features

☐ **DSP**
- **Word length: 24-bit (Data RAM 24-bit floating point)**
- **Instruction cycle: 8.1ns (2560fs at fs=48kHz)**
- **Multiplier 24 x 24 → 48-bit (double precision available)**
- **Divider 20 / 20 → 20-bit (with floating point normalization function)**
- **ALU: 52-bit arithmetic operation (with overflow margin 4-bit)**
- **Program RAM: 4096 × 36-bit**
- **Coefficient RAM: 2048 × 24-bit**
- **Data RAM: 2048 × 24-bit (24-bit floating point)**
- **Offset Register: 32 × 13-bit**
- **Delay RAM: 8192 × 24-bit**
- **Accelerator Coefficient RAM: 2048 × 20-bit**
- **Accelerator Data RAM: 2048 × 16-bit**
- **JX pins (Interrupt)**
- **Master/Slave Operation**
- **Master Clock: 2560fs**
  (Internally Generated by PLL from 32, 48, 64, 128, 256 and 384fs clock)

☐ **Two Digital Interfaces (I/F1, I/F2)**
- **Digital Signal Input Port (4ch): MSB justified 24-bit, LSB justified 24/20/16-bit, I^2S**
- **Digital Signal Input Port (6ch): MSB justified 24-bit, LSB justified 24/20/16-bit, I^2S**
- **Short / Long Frame**
- **24-bit linear, 8-bit A-law, 8-bit μ-law**
- **TDM 256fs (8ch) MSB justified and I^2S formats**

☐ **Stereo 24-bit ADC:**
- **Sampling Frequency: fs=8kHz ~ 96kHz**
- **ADC Characteristics S/(N+D): 91dB, DR, S/N: 102dB**
- **Two-Channel Analog Input Selector (Differential, Single-ended Input)**
- **Channel Independent Mic Analog Gain Amplifier**
  (0~18dB (2dB Step), 18~36dB (3dB Step))
- **Analog DRC (Dynamic Range Control)**
- **Channel Independent Digital Volume (24~-103dB, 0.5dB Step Mute)**
- **Digital HPF for DC Offset Cancelling**

☐ **Mono 24-bit ADC**
- **Sampling Frequency: 8kHz ~ 96kHz**
- **ADC Characteristics S/(N+D): 90dB; DR, S/N: 100dB**
- **Line Amplifier: 21dB ~ -21dB, 3dB Step**
- **Digital Volume (24dB ~ -103dB, 0.5dB step, Mute)**
- **Digital HPF for DC Offset Cancelling**

- ☐ **Stereo 24-bit DAC**
  - **Sampling Frequency: fs=8kHz ~ 96kHz**
  - **Digital Volume (12dB ~ -115dB, 0.5step, Mute)**
  - **Digital De-emphasis Filter (tc=50/15us, fs=32kHz, 44.1kHz, 48kHz)**
- ☐ **Line Output**
  - **Single-ended Output**
  - **S/(N+D): 91dB, DR, S/N: 106dB**
  - **Stereo Analog Volume (+0dB ~ -28dB, 2.0dB step, Mute)**
- ☐ **Analog Mixer**
- ☐ **Digital Mixer**
- ☐ **4ch Digital Microphone Interface**
- ☐ **I^2C Bootloader**
  - **EEPROM Mat Selectable**
- ☐ **µP Interface: SPI, I^2C-bus (400kHz Fast Mode)**
- ☐ **Power supply**

  Analog (AVDD): 3.0V ~ 3.6V (typ. 3.3V)
  Digital1 (DVDD): 1.14V ~ 1.3V (typ. 1.2V)
  (External Power Supply or Internal Regulator is selectable)
  I/F (TVDD): 1.7V ~ 3.6V (typ. 3.3V)
- ☐ **Operating Temperature Range: -40°C ~ 85°C**
- ☐ **Package: 36-pin QFN (0.5mm pitch)**

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4. Block Diagram and Functions

■ Block Diagram

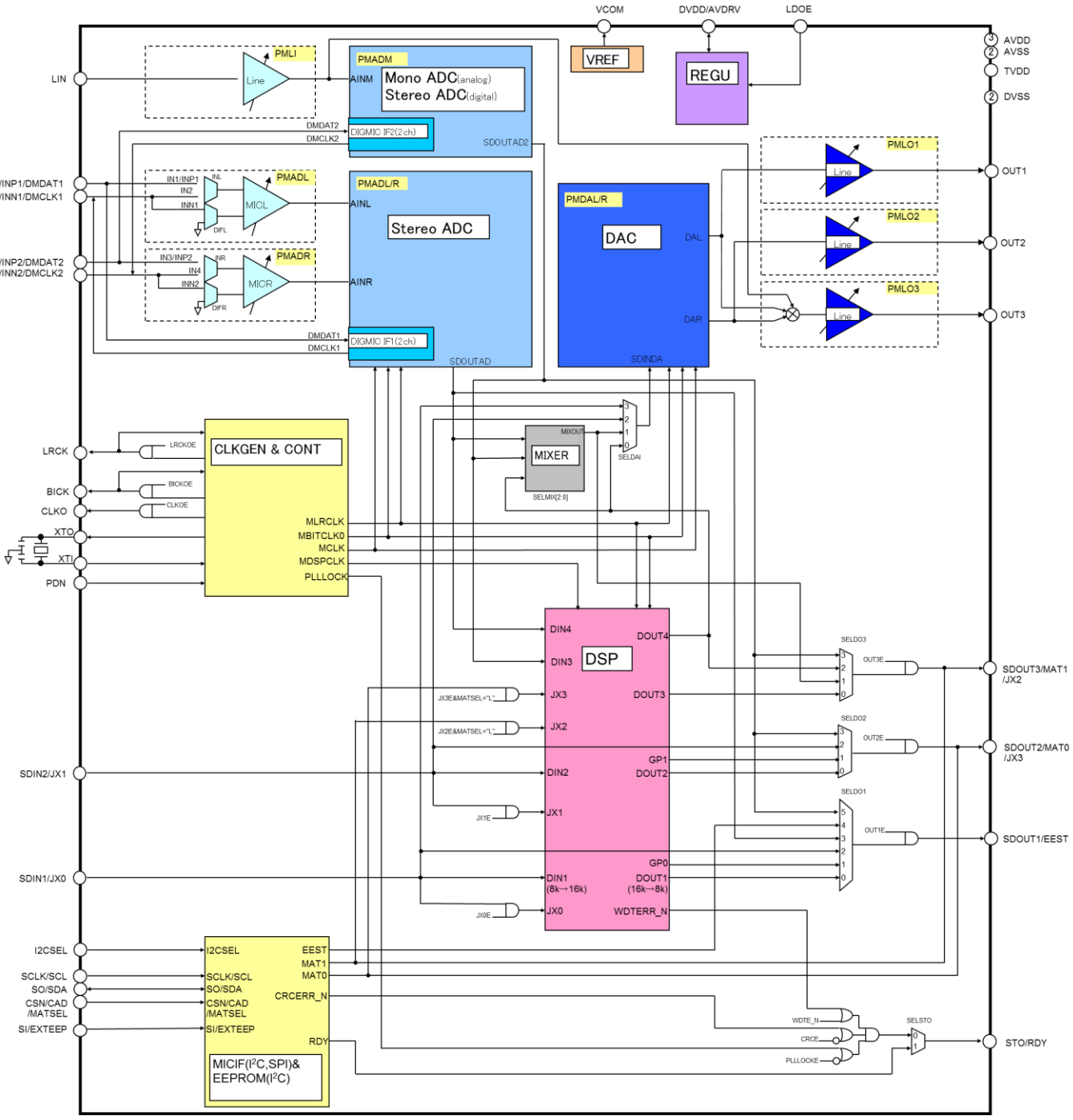


Figure 1. Block Diagram

■ DSP Block Diagram

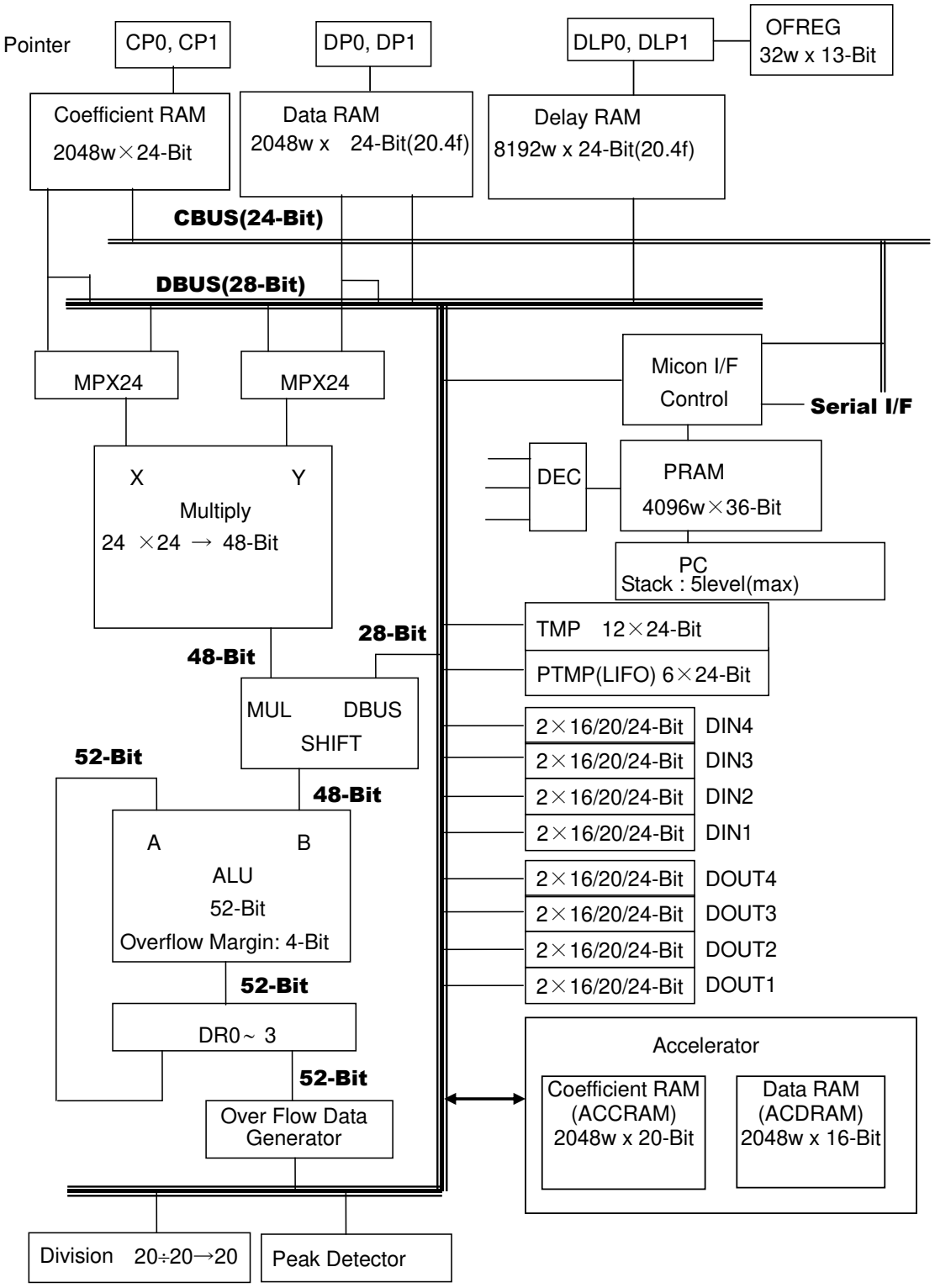


Figure 2. DSP Block Diagram

5. Pin Configurations and Functions

■ Ordering Guide

AK7755EN/VN	-40 ~ +85°C	36-pin QFN (0.5mm pitch)
AKD7755	Evaluation Board for AK7755	

■ Pin Layout

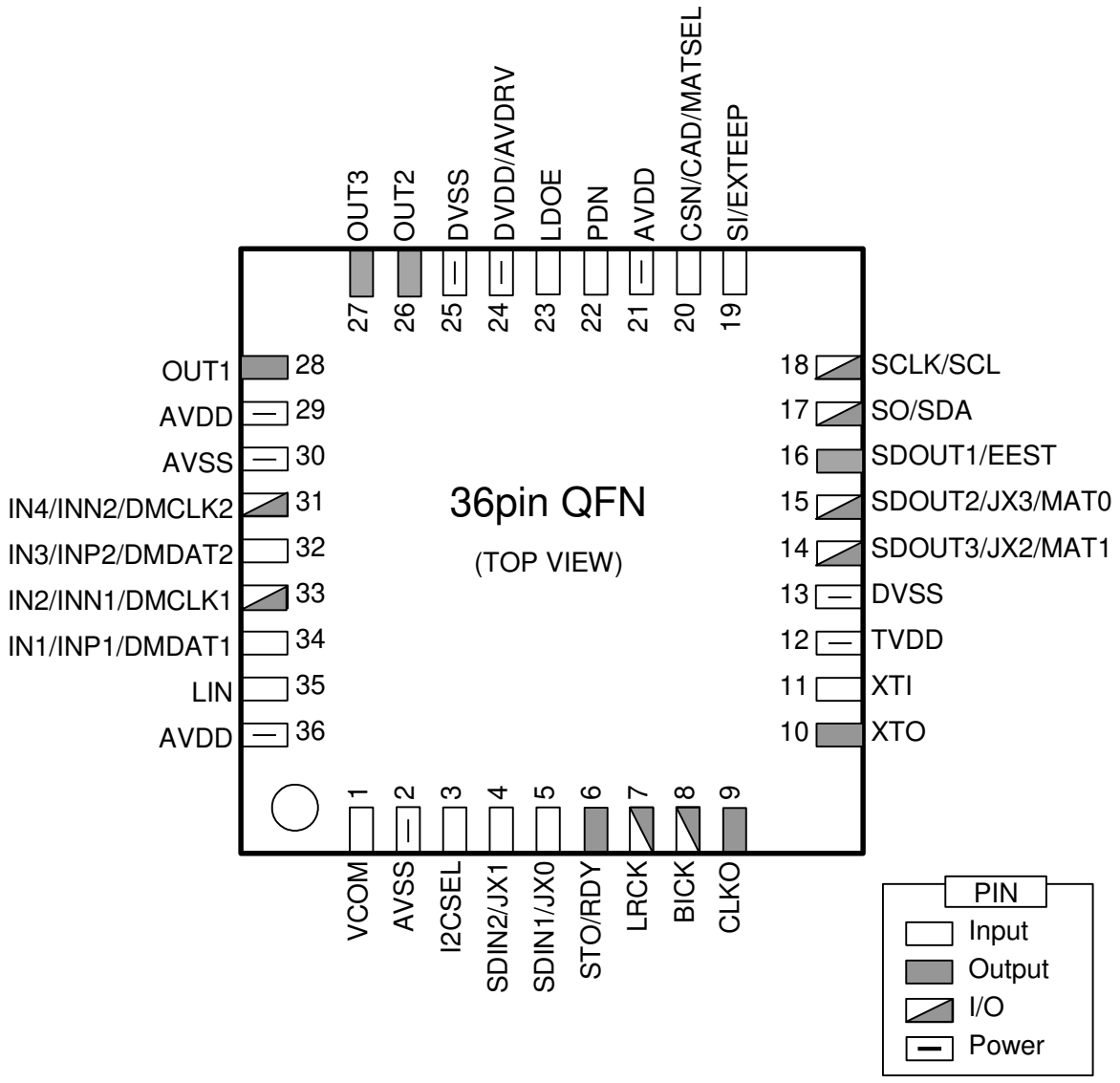
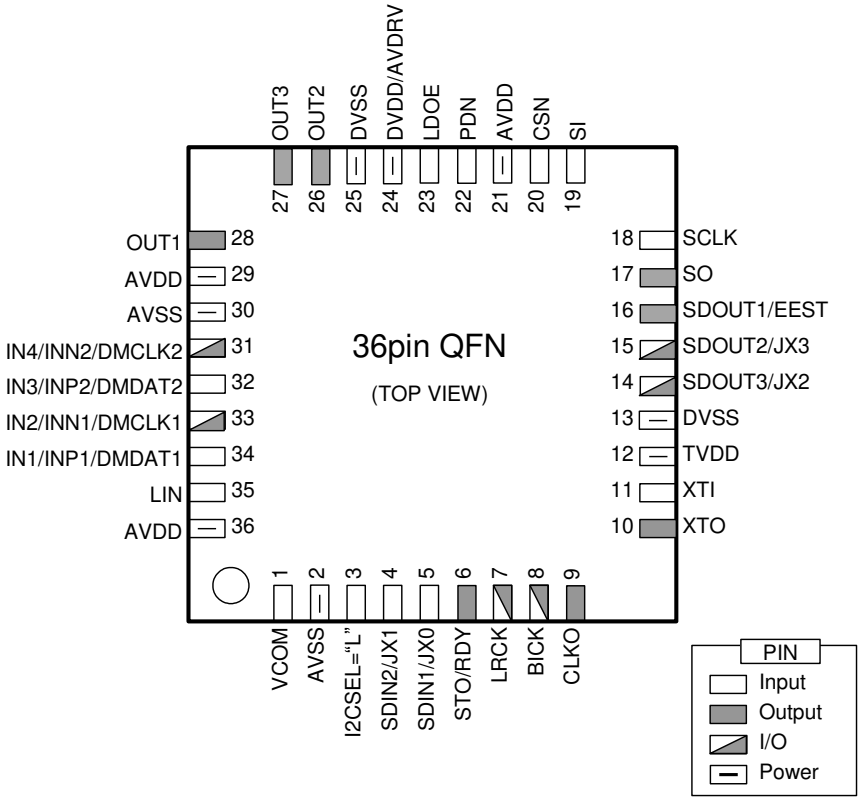
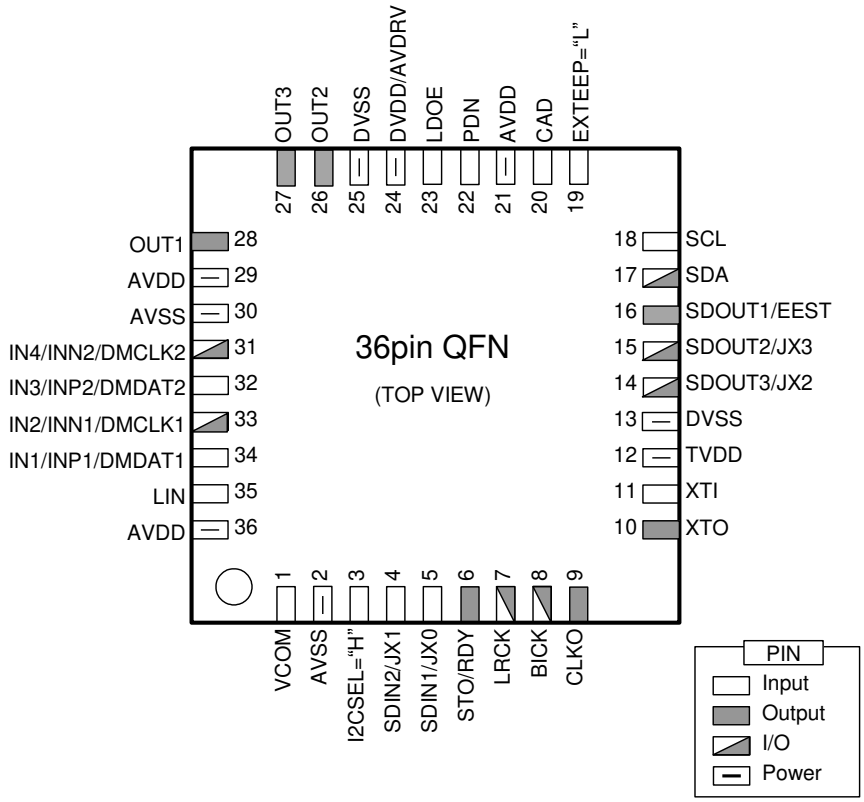


Figure 3. Pin Layout

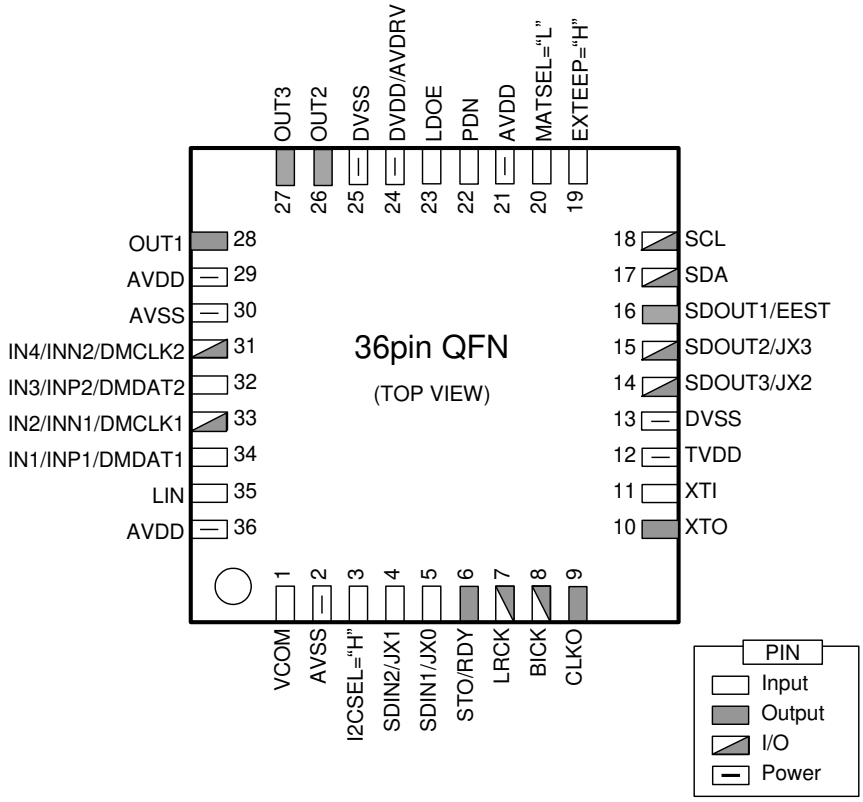
I2CSEL pin = “L”



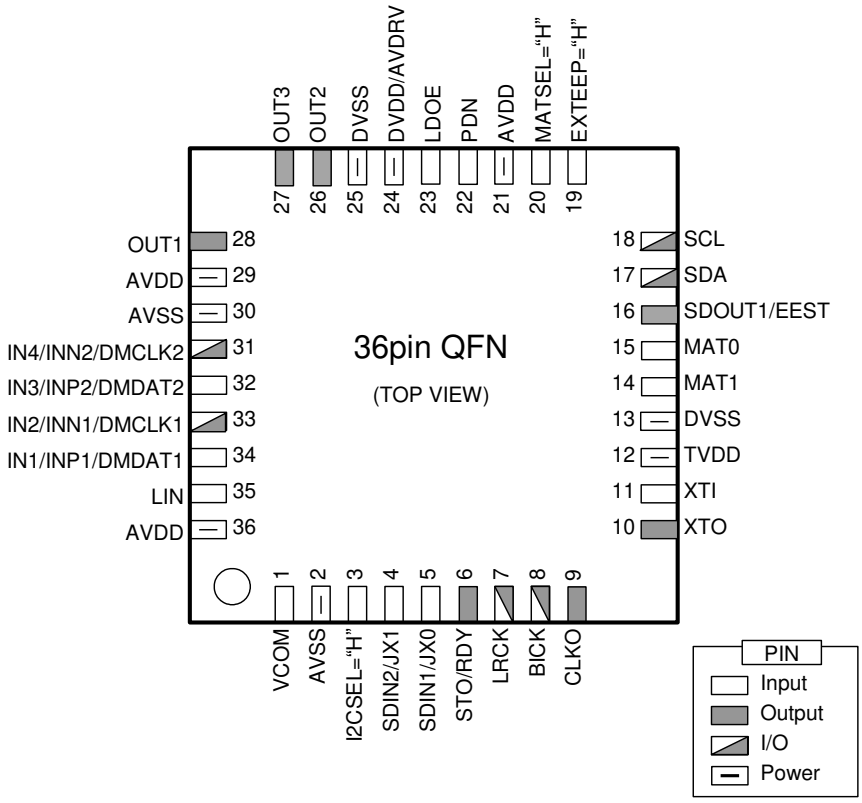
I2CSEL pin = “H”, EXTEEP pin = “L”



I2CSEL pin = “H”, EXTEEP pin = “H”, MATSEL pin = “L”



I2CSEL pin = “H”, EXTEEP pin = “H”, MATSEL pin = “H”



■ Pin Functions

No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin of Analog Block ▪ Connect a 2.2μF capacitor between AVSS. ▪ Do not connect to an external circuit.
2	AVSS	-	Analog Ground Pin 0V
3	I2CSEL	I	I^2C-BUS Select Pin ▪ I2CSEL pin = "L": SPI Interface ▪ I2CSEL pin = "H": I^2C-bus Interface The I2CSEL pin must be fixed to "L" (DVSS) or "H" (TVDD).
4	SDIN2	I	Serial Data Input2 Pin
	JX1	I	External Conditional Jump1 Pin (JX1E bit = "1")
5	SDIN1	I	Serial Data Input1 Pin
	JX0	I	External Conditional Jump0 Pin (JX0E bit = "1")
6	STO	O	Status Output Pin
	RDY	O	RDY Pin
7	LRCK	I/O	LR Channel Select Pin (Internal pull-down)
8	BICK	I/O	Serial Bit Clock Output Pin (Internal pull-down)
9	CLKO	O	Clock Output Pin
10	XTO	O	Crystal oscillator output pin ▪ When a crystal oscillator is used, connect it between XTI and XTO. ▪ When a crystal oscillator is not used, leave this pin as open.
11	XTI	I	Crystal oscillator input pin ▪ When a crystal oscillator is used, connect it between XTI and XTO. ▪ When a crystal oscillator is not used, connect this pin to the external clock or leave open.
12	TVDD	-	Digital IO Power Supply Pin: 1.7~3.6V (typ. 3.3V)
13	DVSS	I	Ground Pin 0V
14	SDOUT3	O	Serial Data Output3 Pin
	JX2	I	External Conditional Jump2 Pin (JX2E bit = "1")
	MAT1	I	I2CSEL pin = EXTEEP pin = MATSEL pin = "H" EEPROM Download Mat Select Address1
15	SDOUT2	O	Serial Data Output2 Pin
	JX3	I	External Conditional Jump3 Pin (JX3E bit = "1")
	MAT0	I	I2CSEL pin = EXTEEP pin = MATSEL pin = "H" EEPROM Download Mat Select Address0
16	SDOUT1	O	Serial Data Output1 Pin
	EEST	O	EEPROM Interface Status
17	SO	O	SO Pin (I2CSEL pin = "L")
	SDA	I/O	I^2CBUS Interface (I2CSEL pin = "H")
18	SCLK	I	Serial Data Clock Pin for SPI Interface (I2CSEL pin = "L") ▪ Set this pin to "H" when there is no clock input.
	SCL	I/O	I^2CBUS Interface Pin (I2CSEL pin = "H") EEPROM Download This becomes an output pin when EXTEEP pin = "H".
19	SI	I	Serial Data Input Pin for SPI Interface (I2CSEL pin = "L") ▪ Set this pin to "L" when not used.
	EXTEEP	I	EEPROM Download Control Pin (I2CSEL pin = "H")

20	CSN	I	ChipSelectN Pin for SPI Interface (I2CSEL pin = "L") ▪ Set this pin to "H" when the AK7755 is in power-down mode or when the microprocessor I/F is not used.
	CAD	I	I2CBUS Address Pin (I2CSEL pin = "H")
	MATSEL	I	EEPROM Mat Select Pin (I2CSEL pin = EXTEEP pin = "H")
21	AVDD	-	Analog Power Supply Pin: (typ. 3.3V)
22	PDN	I	Power-down N Pin ▪ The AK7755 can be powered-down by this pin. ▪ Set this pin to "L" upon power-up the AK7755.
23	LDOE	I	LDO Select Pin LDOE pin = "L": 24 pin External 1.2V Power Supply LDOE pin = "H": 24 pin LDO Output (LDO Drive) The LDOE pin must be fixed to "L(DVSS)" or "H(TVDD)".
24	DVDD	I	Power Supply Pin for Digital Core: (typ. 1.2V)
	AVDRV	O	LDO Output (LDOE pin = "H") Connect a 1uF capacitor between this pin and DVSS. This pin must not be connected to an external circuit.
25	DVSS	-	Ground Pin 0V
26	OUT2	O	Line Output 2 Pin
27	OUT3	O	Line Output 3 Pin
28	OUT1	O	Line Output 1 Pin
29	AVDD	-	Analog Power Supply Pin: 3.3V (typ)
30	AVSS	-	Analog Ground Pin 0V
31	IN4/INN2	I	ADC Input Pin (AINE bit = "1")
	DMCLK2	O	Digital MIC Clock Output 2 Pin (DMIC2 bit = "1")
32	IN3/INP2	I	ADC Input Pin (AINE bit = "1")
	DMDAT2	I	Digital MIC Clock Input 2 Pin (DMIC2 bit = "1")
33	IN2/INN1	I	ADC Input Pin (AINE bit = "1")
	DMCLK1	O	Digital MIC Clock Output 1 Pin (DMIC1 bit = "1")
34	IN1/INP1	I	ADC Input Pin (AINE bit = "1")
	DMDAT1	I	Digital MIC Clock Input 1 Pin (DMIC1 bit = "1")
35	LIN	I	Mono ADC Input Pin
36	AVDD	-	Analog Power Supply Pin: 3.3V (typ)

Note 1. All digital input pins must not be allowed to float. If analog input pins are not used, leave them open. The I2CSEL pin, LDOE pin and CAD/MATSEL pin should be fixed to "L" (DVSS) or "H" (TVDD).

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LIN, IN1/INP1/DMDAT1, IN2/INN1/DMCLK1, IN3/INP2/DMDAT2, IN4/INN2/DMCLK2, OUT1, OUT2, OUT3	These pins must be open.
Digital	STO/RDY, CLKO, XTI, XTO, SDOUT3/ JX2/MAT1, SDOUT2/JX3/MAT0, SDOUT1/EEST, SO/SDA, LRCK, BICK	These pins must be open.
	I2CSEL, SDIN2/JX1, SDIN1/JX0, SCLK/SCL, SI/EXTEEP, CSN/CAD/MATSEL, LDOE	These pins must be connected to DVSS.

6. Absolute Maximum Ratings

(AVSS=DVSS=0V; Note 2)

Parameter	Symbol	min	max	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital1(I/F)	TVDD	-0.3	4.3	V
Digital2(Core)	DVDD	-0.3	1.6	V
DVSS-AVSS (Note 2)	ΔGND	-0.3	0.3	V
Input Current, Any Pin Except Supplies	IIN	—	±10	mA
Analog Input Voltage (Note 3)	VINA	-0.3	(AVDD+0.3)≤4.3	V
Digital Input Voltage (Note 4)	VIND	-0.3	(TVDD+0.3)≤4.3	V
Ambient Temperature	Ta	-40	85	℃
Storage Temperature	Tstg	-65	150	℃

Note 2. All voltages with respect to ground. AVSS and DVSS must be the same voltage.
Note 3. The maximum analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
Note 4. The maximum digital input voltage is smaller value between (DVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS=0V; Note 2)

Parameter	Symbol	min	typ	max	Unit
Power Supplies					
Analog	AVDD	3.0	3.3	3.6	V
Digital1(I/F)	TVDD	1.7	3.3	3.6	V
Digital2(Core)	DVDD	1.14	1.2	1.3	V

Note 5. AVDD and TVDD must be powered up first before DVDD when DVDD is supplied externally (LDOE pin = "L"). In this case, the power-up sequence between AVDD and TVDD is not critical. When using the internal regulator (LDOE pin = "H"), the power-up sequence between AVDD and TVDD is not critical. But all power supplies must be ON before starting operation of the AK7755 by PDN pin = "H".
Note 6. Do not turn off the power supply of the AK7755 with the power supply of the surrounding device turned on. Pull-up of SDA and SCL pins must not exceed TVDD.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Electrical Characteristics

■ Analog Characteristics

1. MIC Amplifier Gain

(Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V)

	Parameter		min	typ	max	Unit
MIC AMP	Input Impedance		14	20		kΩ
	Gain	MGNL[3:0]bits=0h, MGNR[3:0]bits=0h		0		dB
		MGNL[3:0]bits=1h, MGNR[3:0]bits=1h		2		dB
		MGNL[3:0]bits=2h, MGNR[3:0]bits=2h		4		dB
		MGNL[3:0]bits=3h, MGNR[3:0]bits=3h		6		dB
		MGNL[3:0]bits=4h, MGNR[3:0]bits=4h		8		dB
		MGNL[3:0]bits=5h, MGNR[3:0]bits=5h		10		dB
		MGNL[3:0]bits=6h, MGNR[3:0]bits=6h		12		dB
		MGNL[3:0]bits=7h, MGNR[3:0]bits=7h		14		dB
		MGNL[3:0]bits=8h, MGNR[3:0]bits=8h		16		dB
		MGNL[3:0]bits=9h, MGNR[3:0]bits=9h		18		dB
		MGNL[3:0]bits=Ah, MGNR[3:0]bits=Ah		21		dB
		MGNL[3:0]bits=Bh, MGNR[3:0]bits=Bh		24		dB
		MGNL[3:0]bits=Ch, MGNR[3:0]bits=Ch		27		dB
		MGNL[3:0]bits=Dh, MGNR[3:0]bits=Dh		30		dB
		MGNL[3:0]bits=Eh, MGNR[3:0]bits=Eh		33		dB
		MGNL[3:0]bits=Fh, MGNR[3:0]bits=Fh		36		dB

2. Line-in Amplifier Gain

(Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V)

	Parameter		min	typ	max	Unit
Line-in AMP	Input Impedance		14	20		kΩ
	Gain (Note 7)	LIGN[3:0]bits=0h		0		dB
		LIGN[3:0]bits=1h		-3		dB
		LIGN[3:0]bits=2h		-6		dB
		LIGN[3:0]bits=3h		-9		dB
		LIGN[3:0]bits=4h		-12		dB
		LIGN[3:0]bits=5h		-15		dB
		LIGN[3:0]bits=6h		-18		dB
		LIGN[3:0]bits=7h		-21		dB
		LIGN[3:0]bits=8h		N/A		dB
		LIGN[3:0]bits=9h		+3		dB
		LIGN[3:0]bits=Ah		+6		dB
		LIGN[3:0]bits=Bh		+9		dB
		LIGN[3:0]bits=Ch		+12		dB
		LIGN[3:0]bits=Dh		+15		dB
		LIGN[3:0]bits=Eh		+18		dB
		LIGN[3:0]bits=Fh		+21		dB

Note 7. If the output signal of line-in amplifier is input to the analog mixer, +18dB gain is added to the signal at the mixer.

3. MIC Amp + ADC

Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V;
Signal Frequency 1kHz; Sampling Rate fs=48kHz; Measurement Frequency =20Hz to 20kHz
Sampling Rate fs=96kHz; Measurement Frequency =20Hz to 40kHz
CKM mode0(CKM[2:0]= "000"); BITFS[1:0]= "00" (64fs); Differential Input Mode

	Parameter		min	typ	max	Unit
MIC Amp + ADC	Resolution				24	Bit
	Dynamic Characteristics (Differential Input mode)					
	S/(N+D) (-1dBFS)	Fs=48kHz (Note 12)	80	91		dB
		Fs=48kHz (Note 13)		88		
		Fs=96kHz (Note 12)		89		
		Fs=96kHz (Note 13)		85		
	Dynamic Range (Note 8)	Fs=48kHz (A-weighted) (Note 12)	94	102		dB
		Fs=48kHz (A-weighted) (Note 13)		93		
		Fs=96kHz (Note 12)		95		
		Fs=96kHz (Note 13)		89		
	S/N	Fs=48kHz (A-weighted) (Note 12)	94	102		dB
		Fs=48kHz (A-weighted) (Note 13)		93		
		Fs=96kHz (Note 12)		95		
		Fs=96kHz (Note 13)		89		
	Inter-Channel Isolation (Note 9)		90	105		dB
	DC accuracy (Differential Input)					
	Channel Gain Mismatch			0.0	0.3	dB
	Analog Input					
	Input Voltage (Differential Input) (Note 10)	(Note 12)	±2.0	±2.2	±2.4	Vp-p
		(Note 13)		±0.277		
	Input Voltage (Single-ended Input) (Note 11)	(Note 12)	2.0	2.2	2.4	Vp-p
		(Note 13)		0.277		

Note 8. S/(N+D) when -60dB FS signal is applied.
Note 9. Indicates inter-channel isolation between Lch and Rch when –1dBFS signal is input.
Note 10. INP1/INN1 and INP2/INN2 pins.
Note 11. IN1, IN2, IN3 and IN4 pins.
Note 12. MGNL/R[3:0] bits = 0h (0dB)
Note 13. MGNL/R[3:0] bits = 9h (18dB)

4. Line-in Amp + ADC

Ta=25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V;
Signal Frequency 1kHz; Sampling Rate fs=48kHz; Measurement Frequency =20Hz to 20kHz
Sampling Rate fs=96kHz; Measurement Frequency =20Hz to 40kHz
CKM mode0(CKM[2:0]= "000"); BITFS[1:0]= "00" (64fs);

	Parameter		min	typ	max	Unit
Line-in Amp + ADC	Resolution				24	Bit
	Dynamic Characteristics					
	S/(N+D) (-1dBFS)	Fs=48kHz (Note 16)	77	90		dB
		Fs=48kHz (Note 17)		86		
		Fs=96kHz (Note 16)		88		
		Fs=96kHz (Note 17)		85		
	Dynamic Range (Note 14)	Fs=48kHz (A-weighted) (Note 16)	92	100		dB
		Fs=48kHz (A-weighted) (Note 17)		90		
		Fs=96kHz (Note 16)		95		
		Fs=96kHz (Note 17)		86		
	S/N	Fs=48kHz (A-weighted) (Note 16)	92	100		dB
		Fs=48kHz (A-weighted) (Note 17)		90		
		Fs=96kHz (Note 16)		95		
		Fs=96kHz (Note 17)		86		
	Analog Input					
	Input Voltage (Note 15)	(Note 16)	2.00	2.20	2.40	Vp-p
		(Note 17)		0.277		

Note 14. S/(N+D) when -60dB FS signal is applied.
Note 15. The Lin pin.
Note 16. LIGN[3:0] bits = 0h (0dB)
Note 17. LIGN[3:0] bits = Eh (+18 dB)

5. Line-out AMP Gain

Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V

	Parameter		min	typ	max	Unit
Line -out AMP	Gain	LOVOL1[3:0]bits=0h, LOVOL2[3:0]bits=0h, LOVOL3[3:0]bits=0h		mute		dB
		LOVOL1[3:0]bits=1h, LOVOL2[3:0]bits=1h, LOVOL3[3:0]bits=1h		-28		dB
		LOVOL1[3:0]bits=2h, LOVOL2[3:0]bits=2h, LOVOL3[3:0]bits=2h		-26		dB
		LOVOL1[3:0]bits=3h, LOVOL2[3:0]bits=3h, LOVOL3[3:0]bits=3h		-24		dB
		LOVOL1[3:0]bits=4h, LOVOL2[3:0]bits=4h, LOVOL3[3:0]bits=4h		-22		dB
		LOVOL1[3:0]bits=5h, LOVOL2[3:0]bits=5h, LOVOL3[3:0]bits=5h		-20		dB
		LOVOL1[3:0]bits=6h, LOVOL2[3:0]bits=6h, LOVOL3[3:0]bits=6h		-18		dB
		LOVOL1[3:0]bits=7h, LOVOL2[3:0]bits=7h, LOVOL3[3:0]bits=7h		-16		dB
		LOVOL1[3:0]bits=8h, LOVOL2[3:0]bits=8h, LOVOL3[3:0]bits=8h		-14		dB
		LOVOL1[3:0]bits=9h, LOVOL2[3:0]bits=9h, LOVOL3[3:0]bits=9h		-12		dB
		LOVOL1[3:0]bits=Ah, LOVOL2[3:0]bits=Ah, LOVOL3[3:0]bits=Ah		-10		dB
		LOVOL1[3:0]bits=Bh, LOVOL2[3:0]bits=Bh, LOVOL3[3:0]bits=Bh		-8		dB
		LOVOL1[3:0]bits=Ch, LOVOL2[3:0]bits=Ch, LOVOL3[3:0]bits=Ch		-6		dB
		LOVOL1[3:0]bits=Dh, LOVOL2[3:0]bits=Dh, LOVOL3[3:0]bits=Dh		-4		dB
		LOVOL1[3:0]bits=Eh, LOVOL2[3:0]bits=Eh, LOVOL3[3:0]bits=Eh		-2		dB
		LOVOL1[3:0]bits=Fh, LOVOL2[3:0]bits=Fh, LOVOL3[3:0]bits=Fh		0		dB

6. DAC+Line-out Amp

Ta= 25°C; AVDD=TVDD=3.3V; DVDD=1.2V; AVSS=DVSS=0V;
Signal Frequency 1kHz; Sampling Rate fs=48kHz; Measurement Frequency =20Hz to 20kHz
Sampling Rate fs=96kHz; Measurement Frequency =20Hz to 40kHz
CKM mode0(CKM[2:0]=000); BITFS[1:0] bits = "00"; LOVOL1/2/3[3:0] bits = Fh(0dB);

	Parameter		min	typ	max	Unit
DAC	Resolution				24	Bit
	Dynamic Characteristics 1 (OUT1, OUT2, OUT3)					
	S/(N+D) (0 dBFS)	fs=48kHz	80	91		dB
		fs=96kHz		89		
	Dynamic Range (Note 18)	fs=48kHz (A-weighted)	100	106		dB
		fs=96kHz		101		
	S/N	fs=48kHz (A-weighted)	100	106		dB
		fs=96kHz		101		
	Inter-Channel Isolation (f=1kHz) (Note 19)		90	110		dB
	DC accuracy					
	Channel Gain Mismatch			0.0	0.5	dB
	Analog Output					
	Output Voltage (Note 20)		2.28	2.51	2.74	Vp-p
	Load Resistance		10			kΩ
	Load Capacitance				30	pF

Note 18. S/(N+D) when -60dB FS signal is applied.
Note 19. Indicates inter-channel isolation between Lch and Rch of DAC when –1dBFS signal is input.
Note 20. Full-scale output voltage. The output voltage is proportional to AVDD (AVDD x 0.76).

■ DC Characteristics

(Ta= -40 to 85°C, AVDD=3.3V, DVDD=1.2V, TVDD=1.7 to 3.6V, AVSS=DVSS=0V)

Parameter		Symbol	min	typ	max	Unit
High Level Input Voltage		VIH	80%TVDD			V
Low Level Input Voltage		VIL			20%TVDD	V
SCL, SDA High Level Input Voltage		VIH	70%TVDD			V
SCL, SDA Low Level Input Voltage		VIL			30%TVDD	V
DMDAT1, DMDAT2 High Level Input Voltage (DMIC1, DMIC2 bit = "1")		VIH2	65%AVDD			V
DMDAT1, DMDAT2 Low Level Input Voltage (DMIC1, DMIC2 bit = "1")		VIL2			35%AVDD	V
High Level Output Voltage Iout= -100µA (Note 21)		VOH	TVDD-0.3			V
Low Level Output Voltage Iout=100µA (Note 22)		VOL			0.3	V
SDA Low Level Output Voltage Iout=3mA	TVDD≥2.0V	VOL			0.4	V
	TVDD<2.0V	VOL			20%TVDD	
DMCLK1, DMCLK2 High Level Output Voltage Iout = -80µA (DMIC1, DMIC2 bit = "1")		VOH2	AVDD-0.4			V
DMCLK1, DMCLK2 Low Level Output Voltage Iout = 80µA (DMIC1, DMIC2 bit = "1")		VOL2			0.4	V
Input Leak Current (Note 23)		Iin			±10	µA
Input Leak Current at Pulled-down Pins (Note 24)		Iid		77		µA
Input Leak Current at XTI pin		Iix		17		µA

Note 21. Except XTO pin
Note 22. Except SDA and XTO pins.
Note 23. Internal Pulled-down pins, except the XTI pin
Note 24. The LRCK, BICK, SDOUT2/JX3/MAT0 and SDOUT3/JX2/MAT1 pins are internal pulled-down pins (typ. 43 kΩ@3.3V).

■ Power Consumptions

(Ta=25°C, AVDD=3.0 to 3.6V (typ=3.3V, max=3.6V), TVDD=1.7 to 3.6V (typ=3.3V, max=3.6V), DVDD=1.14 to 1.3V (typ=1.2V, max=1.3V), AVSS=DVSS=0V)

	Parameter	min	typ	max	Unit
Power consumptions in operation 1 (Note 25) (LDOE pin = "L")	AVDD		16	24	mA
	TVDD		3	4.5	mA
	DVDD		25	40	mA
Power consumptions in operation 2 (Note 25) (LDOE pin = "H")	AVDD		48	72	mA
	TVDD		3	4.5	mA
Power consumptions in power-down (PDN pin= "L", LDOE pin = "L")	AVDD		10		uA
	TVDD		10		uA
	DVDD		200		uA
Power consumptions in power-down (PDN pin= "L", LDOE pin = "H")	AVDD		1		uA
	TVDD		1		uA

Note 25. DVDD power consumption will be changed depending on DSP programs.
(e.g. It will be 6mA when using AKM's Hands Free program.)

■ Digital Filter Characteritics

1. ADC

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, fs=48kHz (Note 26))

Parameter		Symbol	min	typ	max	Unit
Passband (Note 27)	+0.14dB ~ –0.12dB	PB	0		20.7	kHz
	-0.87dB			21.6		kHz
	-3.0dB			22.8		kHz
Stoppband		SB	28.4			kHz
Passband Ripple (Note 27)		PR			±0.14	dB
Stopband Ripple (Note 28, Note 29)		SA	65			dB
Group Delay Distorsion		ΔGD		0		μs
Group Daley (Ts=1/fs)		GD		12.5		Ts

Note 26. The passband and stopband frequencies scale with "fs" (system sampling rate). The characteristic of the high pass filter is not included.

Note 27. The passband is from DC to 18.9kHz when fs=48kHz.

Note 28. The stopband is 28kHz to 3.044MHz when fs=48kHz.

Note 29. When fs = 48kHz, the analog modulator samples the input signal at 3.072MHz. There is no attenuation of an input signal in band (n x 3.072MHz ±21.99kHz; n=0, 1, 2, 3…) of integer times of the sampling frequency by the digital filter.

2. DAC

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, fs=48kHz)

Parameter		Symbol	min	Typ	max	Unit
Passband (Note 30)	(±0.05dB)	PB	0		21.7	kHz
	(-6.0dB)			24		kHz
Stopband (Note 30)		SB	26.2			kHz
Passband Ripple		PR			±0.05	dB
Stopband Attenuation		SA	64			dB
Group Delay (Ts=1/fs) (Note 31)		GD		24		Ts
Digital Filter + Analog Filter						
Amplitude Characteristics	20Hz to 20.0kHz			±0.5		dB

Note 30. The passband and stopband frequencies are proportional to "fs" (system sampling rate), and represents PB=0.4535 × fs(@±0.05dB) and SB=0.5465 × fs, respectively.

Note 31. The digital filter delay is calculated as the time from setting data into the input register until an analog signal is output.

■ Switching Characteristics

1. System Clock

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter		Symbol	min	typ	max	Unit
a) with a Crystal Oscillator:						
CKM[2:0]bits=0h		fXTI		11.2896 12.288		MHz
CKM[2:0]bits=1h		fXTI		16.9344 18.432		MHz
b) with an External Clock						
Duty Cycle			40	50	60	%
CKM[2:0]bits=0h,2h		fXTI	11.0	11.2896 12.288	12.4	MHz
CKM[2:0]bits=1h		fXTI	16.5	16.9344 18.432	18.6	MHz
LRCK Frequency (Note 32)		fs	8	48	96	kHz
BICK Frequency (Note 33)						
TDM256 bit = "0" (Normal Interface)	High Level Width	tBCLKH	64			ns
	Low Level Width	tBCLKL	64			ns
	Frequency	fBCLK	0.23	3.072	6.2	MHz
TDM256 bit = "1" (TDM Interface)	High Level Width	tBCLKH	32			ns
	Low Level Width	tBCLKL	32			ns
	Frequency	fBCLK	1.8	12.288	12.3	MHz

Note 32. RCK frequency and sampling rate (fs) should be the same.

Note 33. When BICK is the source of the master clock, it should be synchronized to LRCK and have stable frequency.

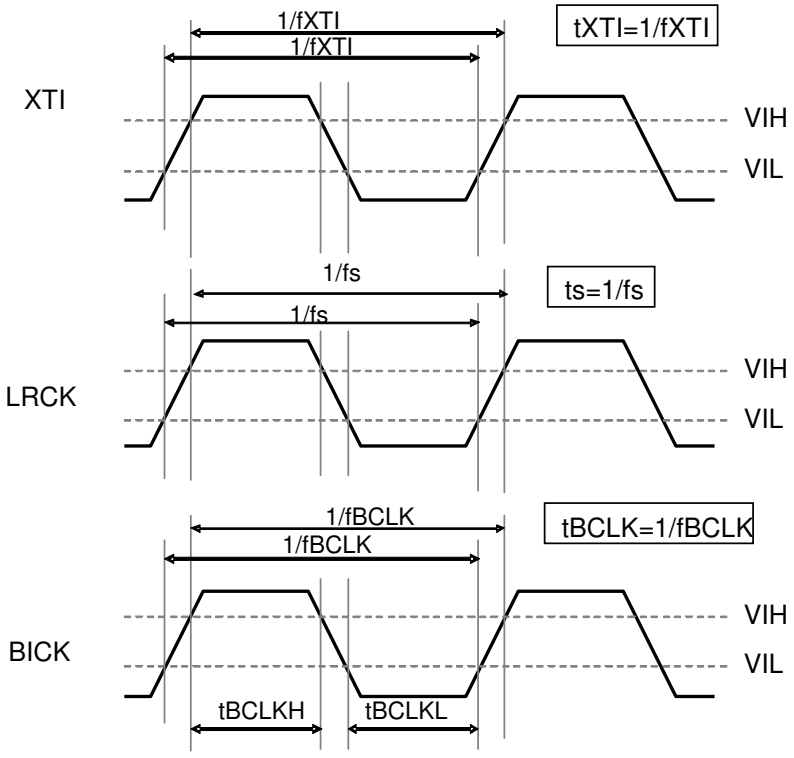


Figure 4. System Clock Timing

2. Power Down

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V)

Parameter	Symbol	min	typ	max	Unit
PDN Pulse Width (Note 34)	tRST	600			ns

Note 34. The PDN pin must be set "L" when power up the AK7755.

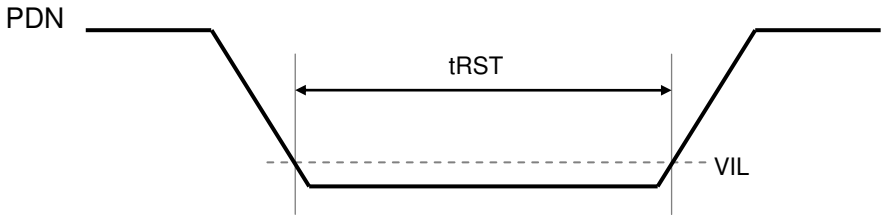


Figure 5. Reset Timing

3. Serial Data Interface

SDIN1, SDIN2, SDOUT1, SDOUT2, SDOUT3

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK (Note 35)	tBLRD	20			ns
Delay Time from LRCK to BICK "↑" (Note 35)	tLRBD	20			ns
Serial Data Input Latch Setup Time	tBSIDS	20			ns
Serial Data Input Latch Hold Time	tBSIDH	20			ns
Delay Time from LRCK to Serial Data Output (Note 36)	tLRD			20	ns
Delay Time from BICK "↓" to LRCK Output (Note 37)	tBSOD			20	ns
Master Mode					
BICK Frequency	fBCLK		32, 48 64, 256		fs
BICK Duty Cycle			50		%
Delay Time from BICK "↓" to LRCK (Note 37)	tMBL	-12		12	ns
Serial Data Input Latch Setup Time	tBSIDS	20			ns
Serial Data Input Latch Hold Time	tBSIDH	20			ns
Delay Time from LRCK to Serial Data Output (Note 36)	tLRD			20	ns
Delay Time from BICK "↓" or "↑"to LRCK Output (Note 37)	tBSOD			20	ns
SDINn → SDOUTn (n=1, 2)					
Delay Time from SDINn to SDOUTn Output	tIOD			60	ns

Note 35. BICK edge must not occur at the same time as LRCK edge.
If BICK polarity was inverted, the counting edge of BICK will be "↓".

Note 36. Except I^2S.

Note 37. When the polarity of BICK1 is inverted, delay time is from BICK1 "↑".

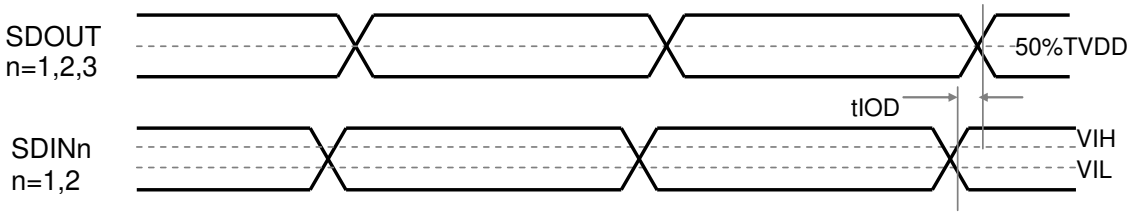


Figure 6. Serial Interface Delay Time from SDINn to SDOUTn Output

3-1. Slave Mode

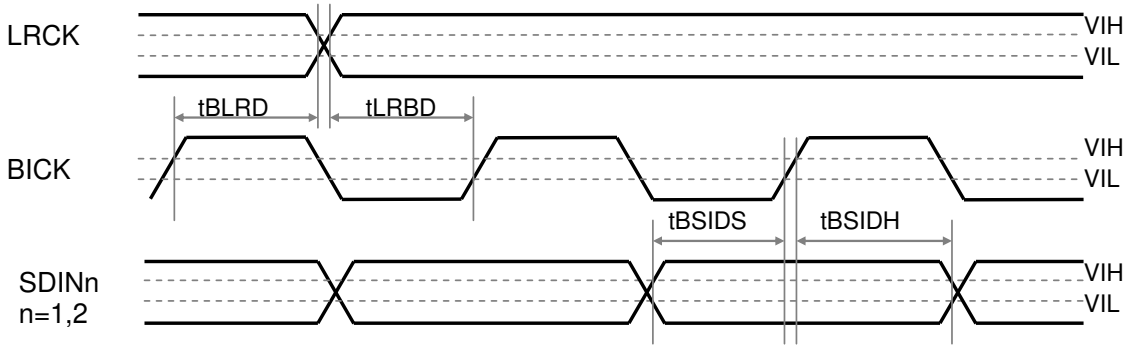


Figure 7. Serial Interface Input Timing in Slave Mode

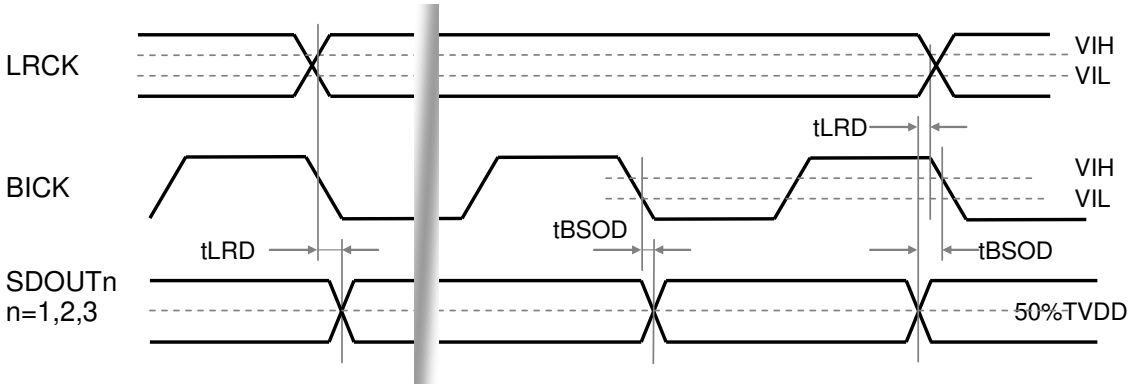


Figure 8. Serial Interface Output Timing in Slave Mode

3-2. Master Mode

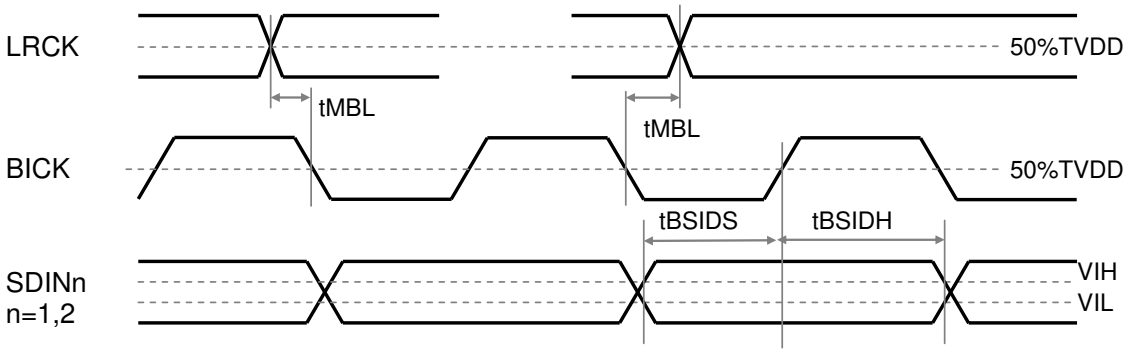


Figure 9. Serial Interface Input Timing in Master Mode

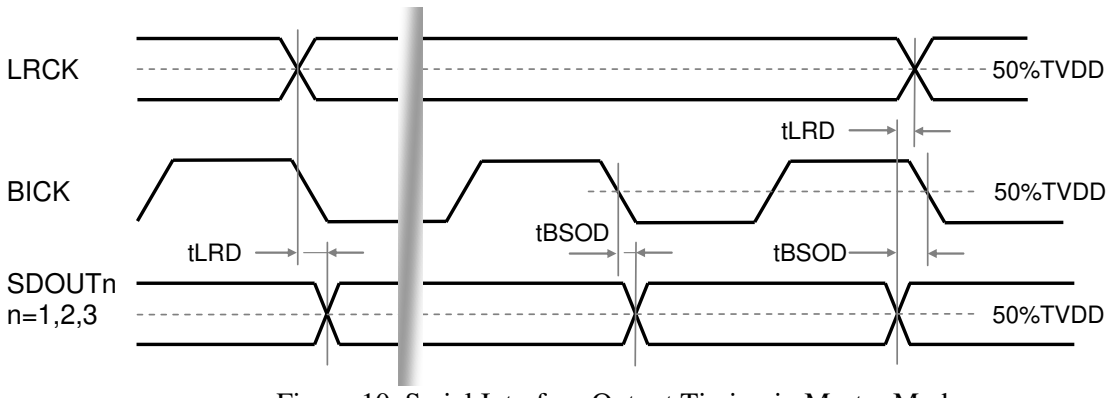


Figure 10. Serial Interface Output Timing in Master Mode

4. SPI Interface

4-1. Clock Reset (CKRESTN bit = "0")

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcontroller Interface Signal					
SCLK Frequency	fSCLK			3.5	MHz
SCLK Low Level Width	tSCLKL	120			ns
SCLK High Level Width	tSCLKH	120			ns
Microcontroller → AK7755					
CSN High Level Width	tWRQH	300			ns
Time from CSN "↑" to PDN "↑"	tRST	360			ns
Time from PDN"↑" to CSN "↓"	tIRRQ	1			ms
Time from RQN"↓" to SCLK"↓"	tWSC	360			ns
Time from SCLK"↑" to CSN"↑"	tSCW	480			ns
SI Latch Setup Time	tSIS	120			ns
SI Latch Hold Time	tSIH	120			ns
AK7755 → Microcontroller					
SO Output Delay Time from SCLK "↓"	tSOS			120	ns
SO Output Hold Time from SCLK "↑" (Note 38)	tSOH	120			ns

Note 38. Except when input the eighth bit of the command code.

4-2. PLL Clock (CKRESTN bit = "1")

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
Microcontroller Interface Signal					
SCLK Frequency	fSCLK			7	MHz
SCLK Low Level Width	tSCLKL	60			ns
SCLK High Level Width	tSCLKH	60			ns
Microcontroller → AK7755					
CSN High Level Width	tWRQH	150			ns
Time from CSN "↑" to PDN "↑"	tRST	180			ns
Time from PDN"↑" to CSN "↓"	tIRRQ	1			ms
Time from RQN"↓" to SCLK"↓"	tWSC	150			ns
Time from SCLK"↑" to CSN"↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	60			ns
SI Latch Hold Time	tSIH	60			ns
AK7755 → Microcontroller					
SO Output Delay Time from SCLK "↓"	tSOS			60	ns
SO Output Hold Time from SCLK "↑" (Note 38)	tSOH	60			ns

Note 39. It takes 10ms at maximum until PLL is locked, after setting CKRESTN bit to "1" from "0".

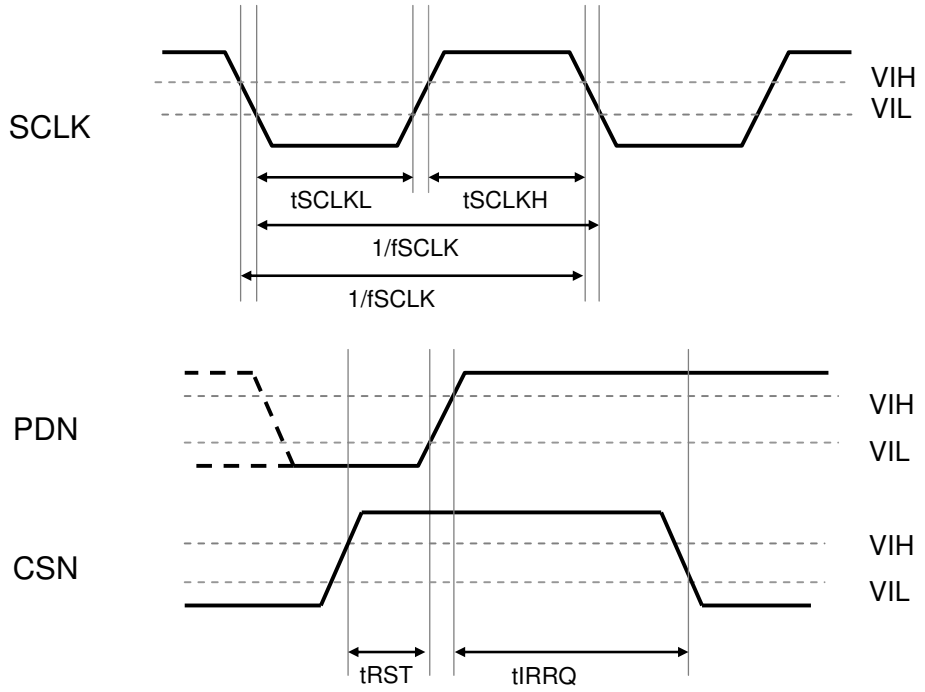


Figure 11. SPI Interface Timing 1

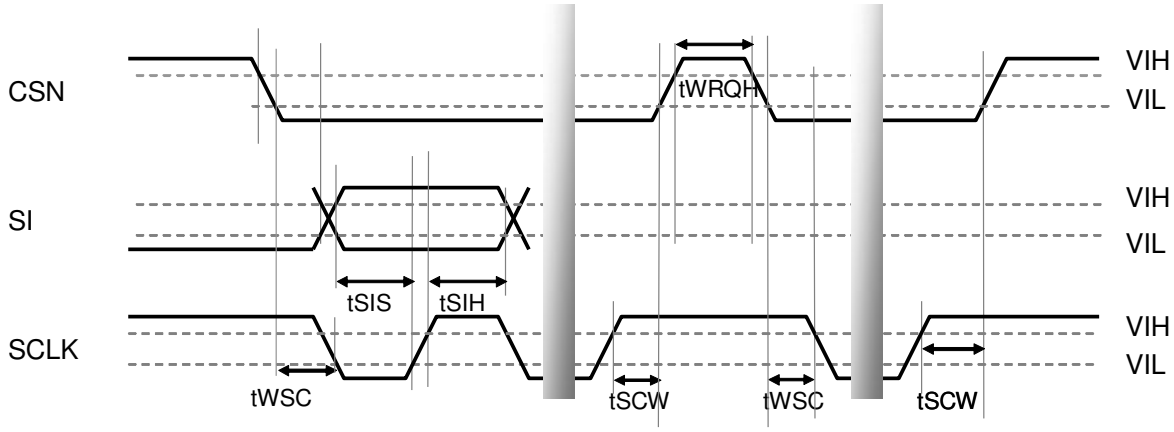


Figure 12. SPI Interface Timing 2 (Microcontroller → AK7755)

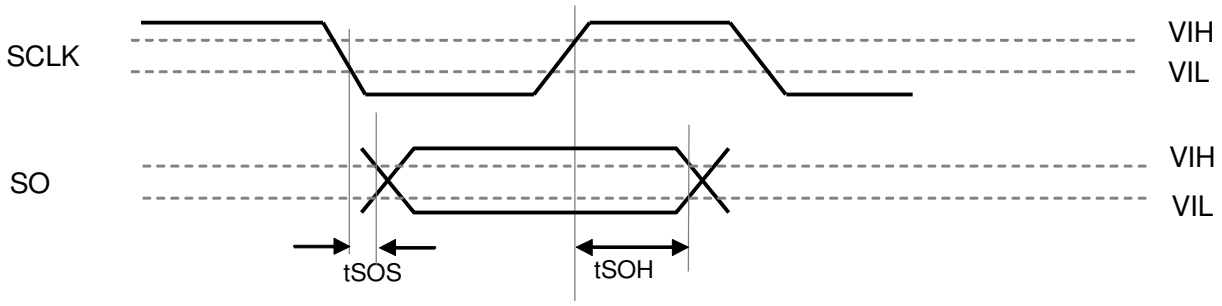


Figure 13. SPI Interface Timing 3 (AK7755 → Microcontroller)

5. I²C-BUS Interface

(Ta= -40 to 85°C; AVDD=3.0 to 3.6V, TVDD=1.7 to 3.6V, DVDD=1.14 to 1.3V, AVSS=DVSS=0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
I2C Timing					
SCL clock frequency	fSCL			400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

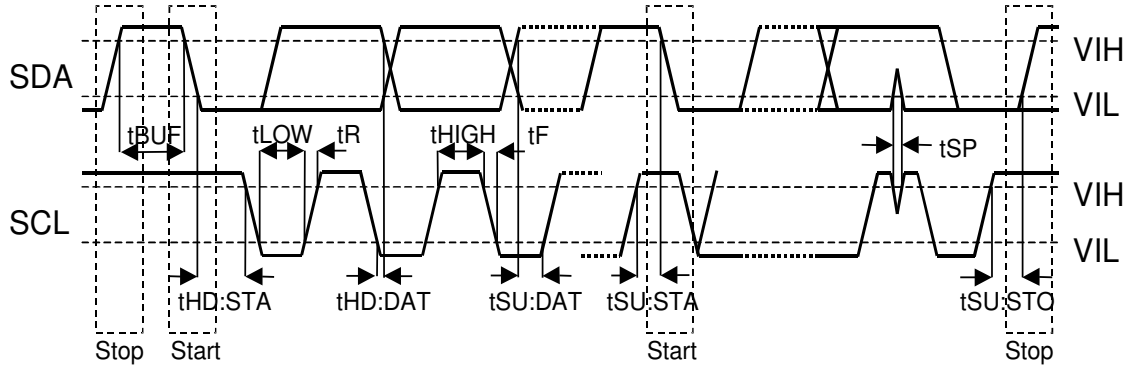


Figure 14. I²C BUS Interface Timing

6. Digital Microphone Interface

(AVDD=3.0~3.6V, TVDD=1.7~3.6V, DVDD=1.14~1.3V, AVSS=DVSS=0V, Ta= -40°C~85°C; CL=100pF)

Parameter	Symbol	min	typ	max	Unit
DMDAT1, DMDAT2					
Serial Data Input Latch Setup Time	tDMDS	50			ns
Serial Data Input Latch Hold Time	tDMDH	0			ns
DMCLK1, DMCLK2					
Clock Frequency (Note 40)	fDMCK	0.5	64fs	6.2	MHz
Duty Cycle	dDMCK	40	50	60	%
Rise Time	tDMCKR			10	ns
Fall Time	tDMCKF			10	ns

Note 40. Clock frequency is determined by the sampling rate (fs) selected by DFS[2:0] bits.

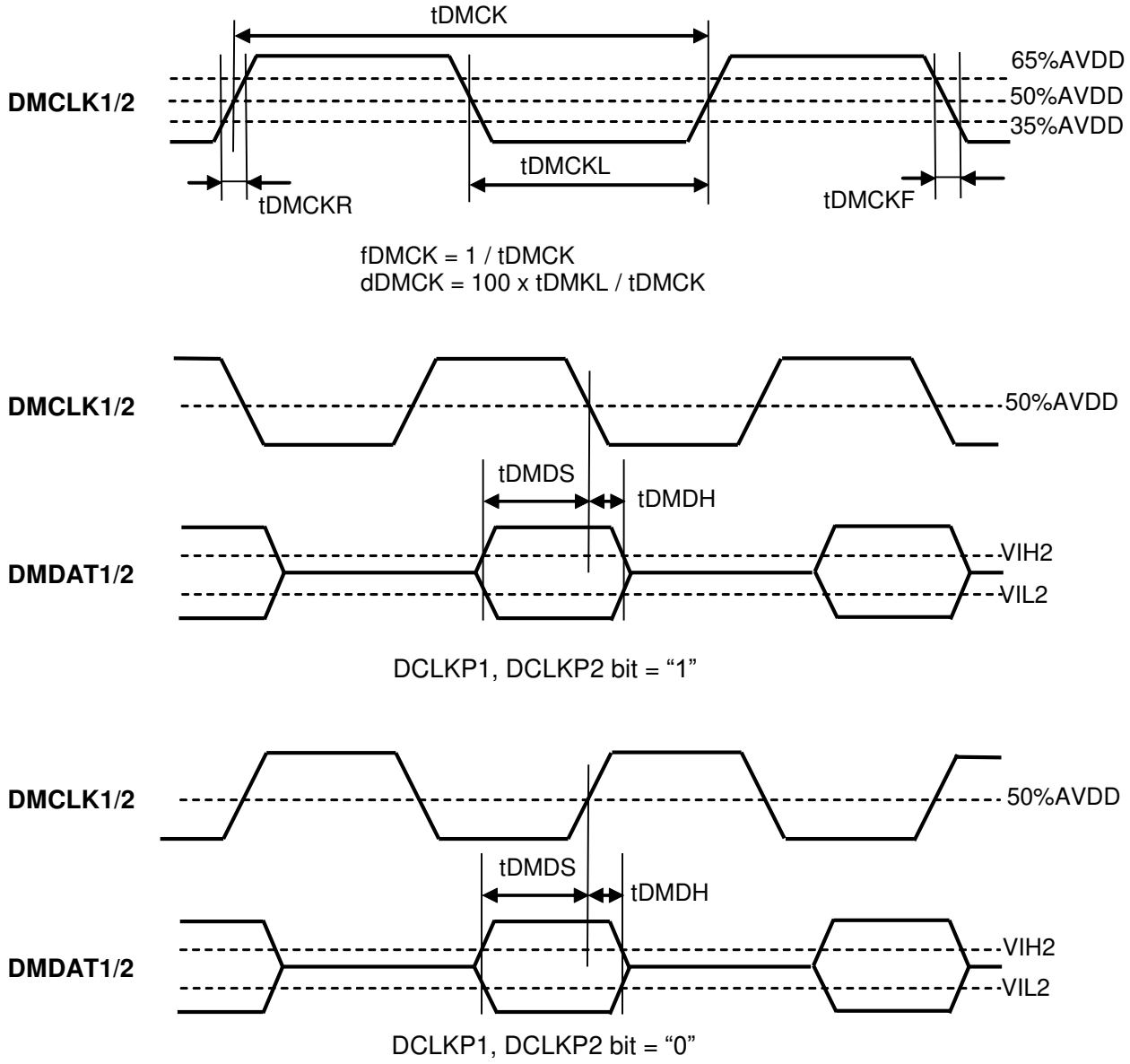


Figure 15. Digital Microphone Interface Timing Wave Form