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Preliminary

3.3V LVDS 1:4 Clock Fanout Buffer AK8181F

Features

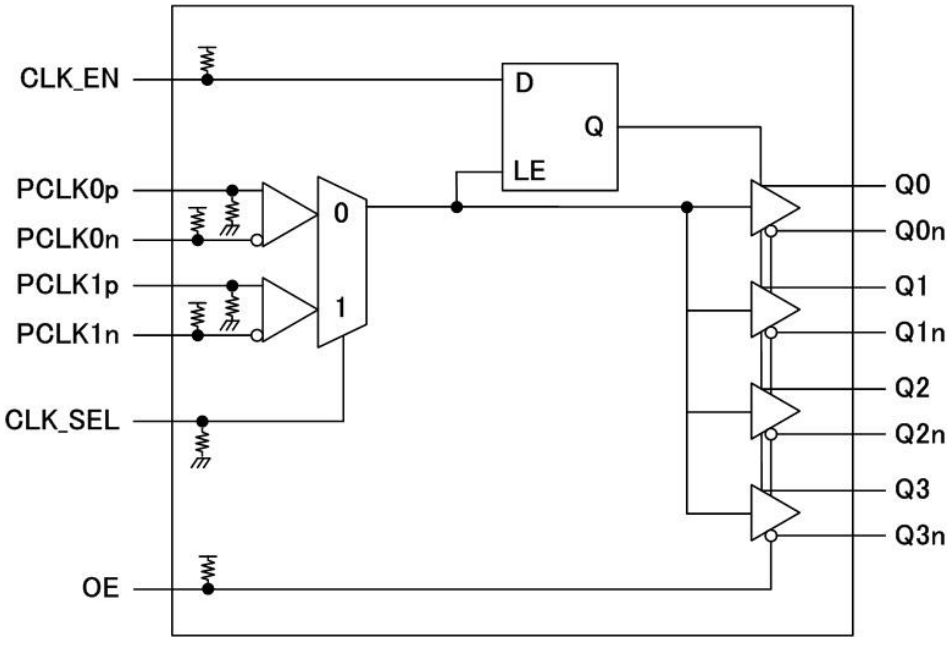
- Four differential 3.3V LVDS outputs
- Selectable differential PCLK0p/n or LVPECL clock inputs
- PCLK0p/n pair can accept the following differential input levels; LVDS, LVPECL, LVHSTL, SSTL, HCSL
- PCLK1p/n supports the following input types; LVPECL, CML, SSTL
- Clock output frequency up to 650MHz
- Translates any single-ended input signal to 3.3V LVDS levels with resistor bias on PCLK0n input
- Output skew : 30ps (maximum)
- Part-to-part skew : 600ps (maximum)
- Propagation delay : 2.5ns (maximum)
- Operating Temperature Range: -40 to +85℃
- Package: 20-pin TSSOP (Pb free)
- Pin compatible with ICS8543I

Description

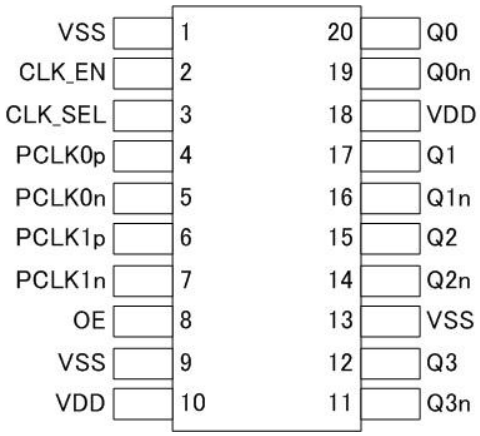
The AK8181F is a member of AKM's LVDS clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew. The AK8181F distributes 4 buffered clocks.

AK8181F are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low skew. The AK8181F is available in a 20-pin TSSOP package.

Block Diagram



Pin Descriptions



Package: 20-Pin TSSOP(Top View)

Pin No.	Pin Name	Pin Type	Pullup down	Description
1	VSS	PWR	---	Negative power supply
2	CLK_EN	IN	Pull up	Synchronizing clock output enable (LVCMOS/LVTTL) Pin is connected to VDD by internal resistor. (typ. 51kΩ) High (Open): clock outputs follow clock input. Low: Q outputs are forced low, Qn outputs are forced high.
3	CLK_SEL	IN	Pull down	CLK Select Input (LVCMOS/LVTTL) Pin is connected to VSS by internal resistor. (typ. 51kΩ) High: selects PCLK1p/n inputs Low (Open): selects PCLK0p/n inputs
4	PCLK0p	IN	Pull down	Non-inverting differential clock input Pin is connected to VSS by internal resistor. (typ. 51kΩ) *When using PCLK1 input (CLK_SEL=High), it should be connected to VSS or opened.
5	PCLK0n	IN	Pull up	Inverting differential clock input Pin is connected to VDD by internal resistor. (typ. 51kΩ) *When using PCLK1 input (CLK_SEL=High), it should be connected to VDD or opened.
6	PCLK1p	IN	Pull down	Non-inverting differential LVPECL clock input Pin is connected to VSS by internal resistor. (typ. 51kΩ) *When using PCLK0 input (CLK_SEL=Low), it should be connected to VSS or opened.
7	PCLK1n	IN	Pull up	Inverting differential LVPECL clock input Pin is connected to VDD by internal resistor. (typ. 51kΩ) *When using PCLK0 input (CLK_SEL=Low), it should be connected to VDD or opened.
8	OE	IN	Pull up	Output enable. Controls enabling and disabling of outputs Q0, Q0n through Q3, Q3n Pin is connected to VDD by internal resistor. (typ. 51kΩ)
9	VSS	PWR	---	Negative power supply
10	VDD	PWR	---	Positive power supply

Pin No.	Pin Name	Pin Type	Pullup down	Description
11, 12	Q3n, Q3	OUT	---	Differential clock output (LVDS)
13	VSS	PWR	---	Negative power supply
14, 15	Q2n, Q2	OUT	---	Differential clock output (LVDS)
16, 17	Q1n, Q1	OUT	---	Differential clock output (LVDS)
18	VDD	PWR	---	Positive power supply
19, 20	Q0n, Q0	OUT	---	Differential clock output (LVDS)

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8181F	AK8181F	Tape and Reel	20-pin TSSOP	-40 to 85 °C

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.5 to VDD+0.5	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 150	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

(2) VSS=0V

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage (1)	VDD	VDD±5%	3.135	3.3	3.465	V

(1) Power of 3.3V requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be located close to each VDD pin.

Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}			4		pF
Input Pullup Resistor	R_{PU}			51		kΩ
Input Pulldown Resistor	R_{PD}			51		kΩ

Power Supply Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Current	I_{DD}	PCLK0p/n = input 650MHz PCLK1p/n = open			45	mA
		PCLK0p/n = open PCLK1p/n = input 650MHz			45	mA

DC Characteristics (LVCMOS/LVTTL)

All specifications at VDD=3.3V±5%, VSS=0V, Ta: -40 to +85℃, unless otherwise noted

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage		V_{IH}		2.0		VDD+0.3	V
Input Low Voltage		V_{IL}		-0.3		0.8	V
Input High Current	CLK_SEL	I_H	Vin=VDD=3.465V			150	µA
	CLK_EN, OE		Vin=VDD=3.465V			5	µA
Input Low Current	CLK_SEL	I_L	Vin=VSS, VDD=3.465V	-5			µA
	CLK_EN, OE		Vin=VSS, VDD=3.465V	-150			µA

DC Characteristics (Differential)

All specifications at VDD=3.3V±5%, VSS=0V, Ta: -40 to +85℃, unless otherwise noted

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Current	PCLK0p	I_H	Vin=VDD=3.465V			150	µA
	PCLK0n		Vin=VDD=3.465V			5	µA
Input Low Current	PCLK0p	I_L	Vin=VSS, VDD=3.465V	-5			µA
	PCLK0n		Vin=VSS, VDD=3.465V	-150			µA
Peak-to-Peak Input Voltage		V_{PP}		0.15		1.3	V
Common Mode Input Voltage (1) (2)		V_{CMR}		VSS+0.5		VDD-0.85	V

(1) For single ended applications, the maximum input voltage for PCLK0p and PCLK0n is VDD+0.3V.

(2) Common mode voltage is defined as V_{IH}.

DC Characteristics (LVPECL)

All specifications at VDD=3.3V±5%, VSS=0V, Ta: -40 to +85℃, unless otherwise noted

Parameter		Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Current	PCLK1p	I_H	Vin=VDD=3.465V			150	µA
	PCLK1n		Vin=VDD=3.465V			5	µA
Input Low Current	PCLK1p	I_L	Vin=VSS, VDD=3.465V	-5			µA
	PCLK1n		Vin=VSS, VDD=3.465V	-150			µA
Peak-to-Peak Input Voltage		V_{PP}		0.3		1.0	V
Common Mode Input Voltage (1) (2)		V_{CMR}		VSS+1.5		VDD	V

(1) For single ended applications, the maximum input voltage for PCLK1p and PCLK1n is VDD+0.3V.

(2) Common mode voltage is defined as V_{IH}.

DC Characteristics (LVDS)

All specifications at VDD=3.3V±5%, VSS=0V, Ta: -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Differential Output Voltage	V_{OD}		200	280	360	mV
V_{OD} Magnitude Change	ΔV_{OD}			0	40	mV
Offset Voltage	V_{OS}		1.125	1.25	1.375	V
V_{OS} Magnitude Change	ΔV_{OS}			5	25	mV
High Impedance Leakage Current	I_{OZ}	OE=L	-10		+10	µA
Differential Output Short Circuit Current	I_{OSD}			-3.5	-5	mA
Output Voltage High	V_{OH}			1.34	1.6	V
Output Voltage Low	V_{OL}		0.9	1.06		V

AC Characteristics

All specifications at VDD=3.3V±5%, VSS=0V, Ta: -40 to +85°C, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Frequency	f_{OUT}				650	MHz
Propagation Delay (1)	t_{PD}		0.9		2.5	ns
Output Skew (2) (3)	$t_{sk(O)}$				30	ps
Part-to-Part Skew (3) (4)	t_{skPP}				600	ps
Output Rise/Fall Time (5)	t_r, t_f	20% to 80% @50MHz	100		300	ps
Output Duty Cycle	DC_{OUT}		45	50	55	%

All parameters measured at f ≤ 650MHz unless noted otherwise.

The cycle to cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

(1) Measured from the differential input crossing point to the differential output crossing point.

(2) Defined as skew between outputs at the same supply voltage and with equal load conditions.

(3) This parameter is defined in accordance with JEDEC Standard 65.

(4) Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

(5) Design value.

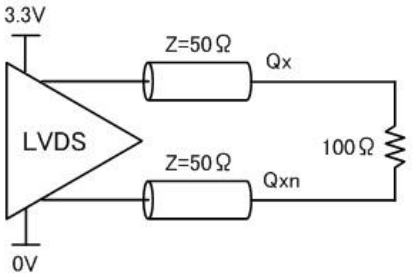


Figure 1 3.3V Output Load AC Test Circuit

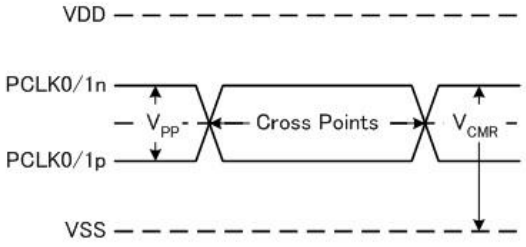


Figure 2 Differential Input Level

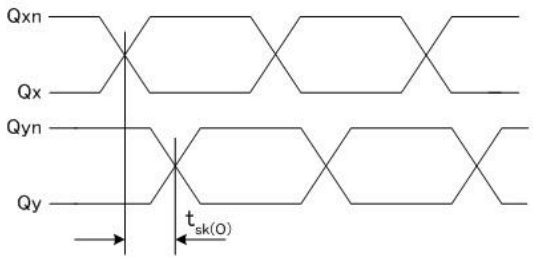


Figure 3 Output Skew

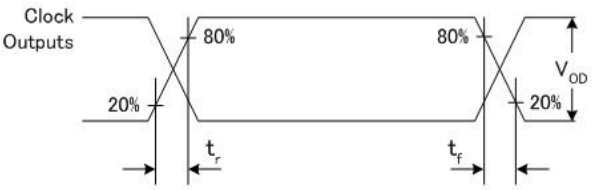


Figure 4 Output Rise/Fall Time

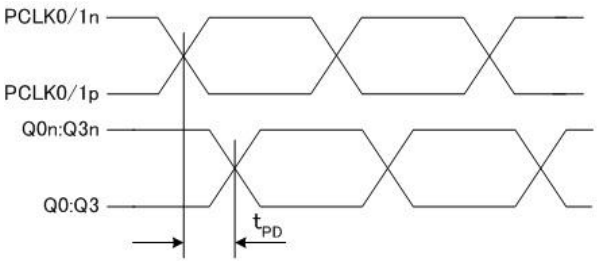


Figure 5 Propagation Delay

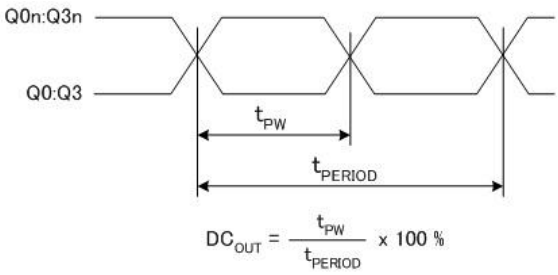


Figure 6 Output Duty/ Pulse Width/ Period

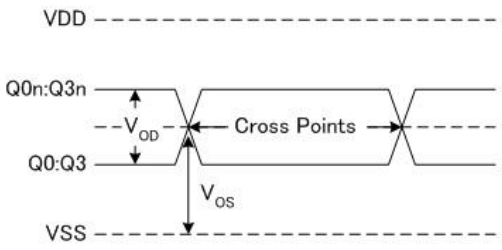


Figure 7 Differential Output Level

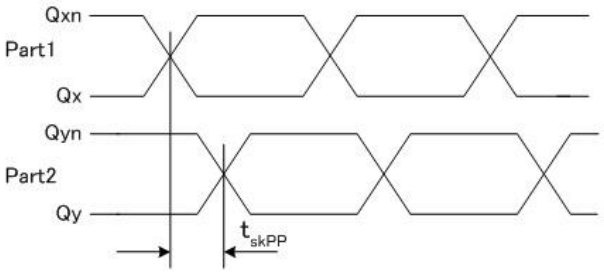


Figure 8 Part-to-Part Skew

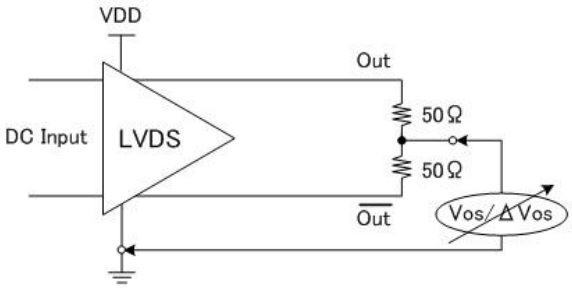


Figure 9 Offset Voltage Setup

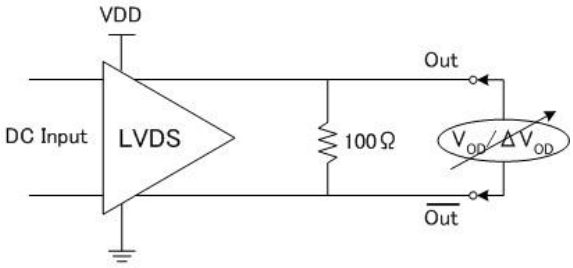


Figure 10 Differential Output Voltage Setup

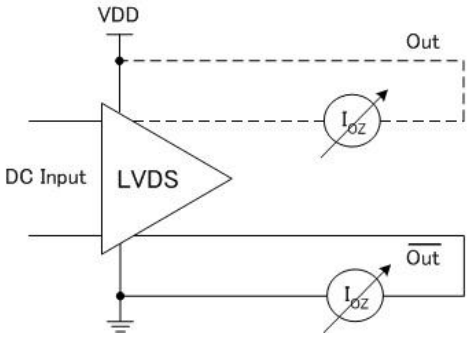


Figure 11 High Impedance Leakage Current Setup

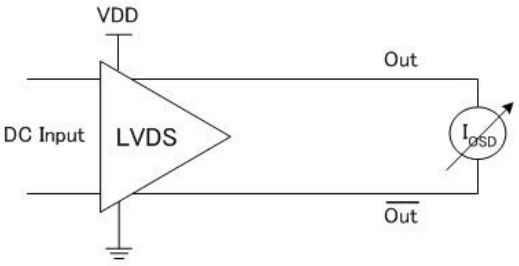


Figure 12 Differential Output Short Circuit Setup

Function Table

The following table shows the inputs/outputs clock state configured through the control pins.

Table 1: Control Input Function Table

Inputs				Outputs	
OE	**CLK_EN**	**CLK_SEL**	**Selected Source**	**Q0:Q3**	**Q0n:Q3n**
1	0	0 (Open)	PCLK0p/n	Disabled: Low	Disabled: High
1	0	1	PCLK1p/n	Disabled: Low	Disabled: High
1	1 (Open)	0 (Open)	PCLK0p/n	Enabled	Enabled
1	1 (Open)	1	PCLK1p/n	Enabled	Enabled
0	X	X	---	Hi-Z	Hi-Z

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 13. In the active mode, the state of the outputs are a function of the PCLK0p/n and PCLK1p/n as described in Table 2.

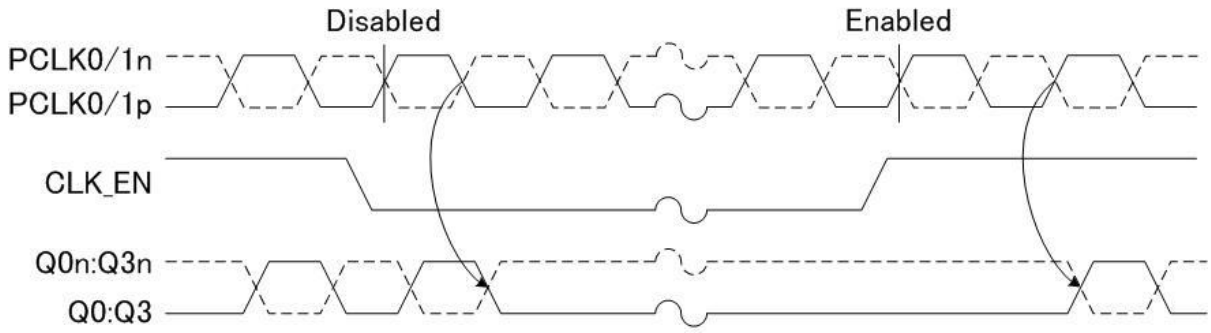


Figure 13 CLK_EN Timing Diagram

Table 2 Clock Input Function Table

Inputs		Outputs		Input to Output	Polarity
PCLK0/1p	**PCLK0/1n**	**Q0:Q3**	**Q0n:Q3n**		
0	1	Low	High	Differential to Differential	Non Inverting
1	0	High	Low	Differential to Differential	Non Inverting
0	Biased (1)	Low	High	Single Ended to Differential	Non Inverting
1	Biased (1)	High	Low	Single Ended to Differential	Non Inverting
Biased (1)	0	High	Low	Single Ended to Differential	Inverting
Biased (1)	1	Low	High	Single Ended to Differential	Inverting

(1) Please refer to the application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure.8 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = VDD/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and VDD = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

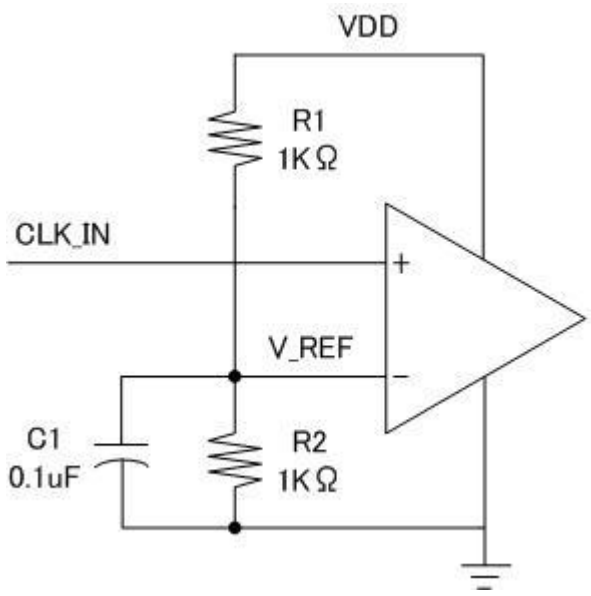
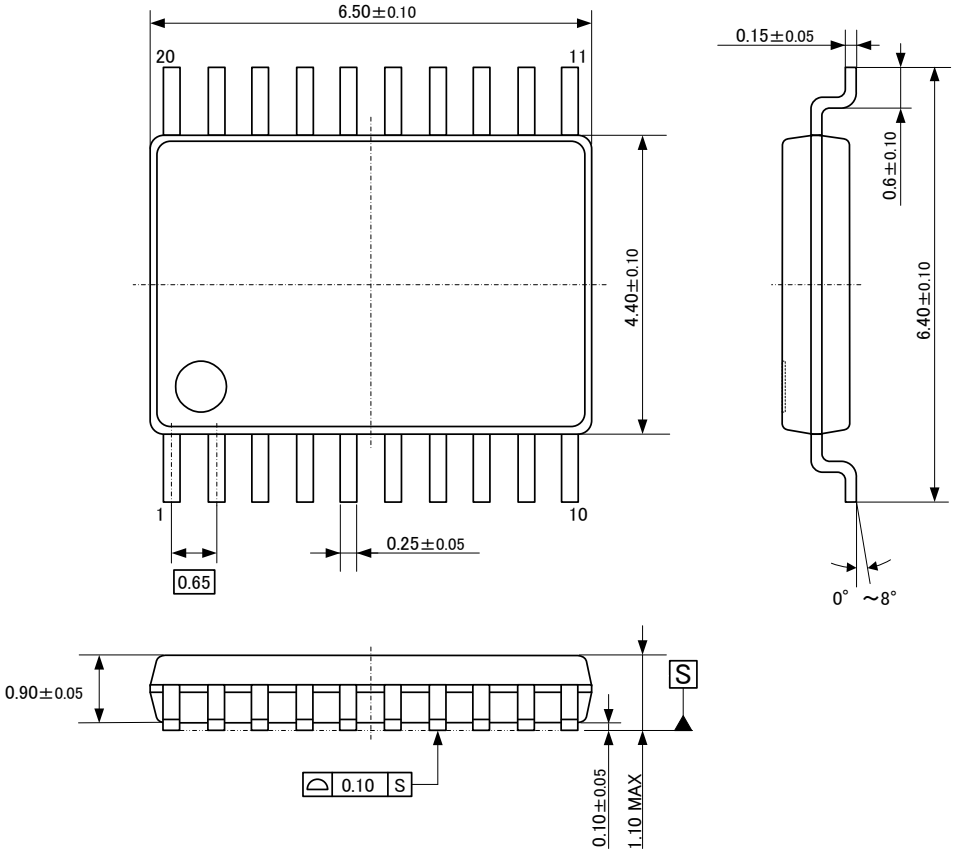


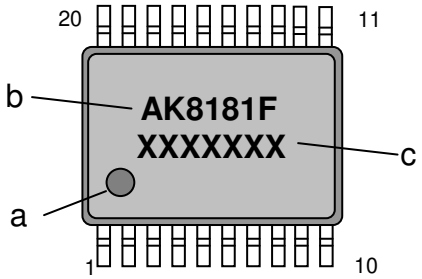
Figure 14 Single Ended Signal Driving Differential Input

Package Information

- **Mechanical data : 20pin TSSOP**

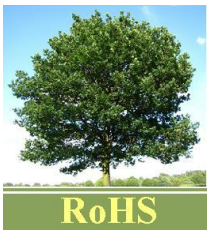


- **Marking**



a: #1 Pin Index
b: Part number
c: Date code (7 digits)

- **RoHS Compliance**



All integrated circuits form Asahi Kasei Microdevices Corporation (AKM) assembled in “lead-free” packages* are fully compliant with RoHS.

(*) RoHS compliant products from AKM are identified with “Pb free” letter indication on product label posted on the anti-shield bag and boxes.

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  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
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