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AK8411

Single Channel Input, 16 Bit 5 MSPS Video ADC

Device Outline

The AK8411 is a +3.3 V CMOS, Single Channel 16 Bit 5 MSPS ADC which integrates on-chip Offset Adjust DAC, Gain Adjust PGA and CDS circuit.

Features

- ☐ CCD I/F
  - Number of Channels 1 channel
  - Range 1.98 Vpp (typ.)
  - Signal Input Range 0~3.3V @ DC Direct Coupled input mode at AVDD = 3.3 V
  - Integrated On-chip CDS circuit
  - Compatible with both Positive and Negative signal polarities
- ☐ ADC
  - Maximum Conversion Rate 5 MSPS
  - Resolution 16 Bit (Straight Binary Code)
- ☐ Black Level Correction DAC
  - Correctable Range ± 240 mV (typ.)
  - Resolution 8 Bit
- ☐ Gain Adjust
  - Adjustable Range 0 dB ~ +13.9 dB (typ.) (1.0× ~ 4.9×)
  - Resolution 6 Bit
- ☐ Total Performance (Input ~ Video ADC)
  - Output Noise 5 LSBs rms (typ.) @ PGA Gain = 0 dB setting
- ☐ Data Output
  - 2 bit wide × 8 cycles
- ☐ Power Supplies
  - Analog part: +3.3V ±5 % / Digital Output part: +3.3V ±0.3V
- ☐ CPU I/F
  - 3-Wire Serial Interface (Write Only)
  - Clock, Data are commonly shared with A/D Data Output pins
- ☐ Power Dissipation
  - 71 mW (typ.) with DC Direct Coupled input mode at AVDD= 3.3V
- ☐ Operating Temperature Range 0 °C ~ +70 °C
- ☐ Package 16 Pin TSSOP
  - Pin pitch: 0.65 mm, (Pin edge to edge: 6.4) × 5 mm, Mold size: 4.4 mm × 5 mm

Circuit Block Description

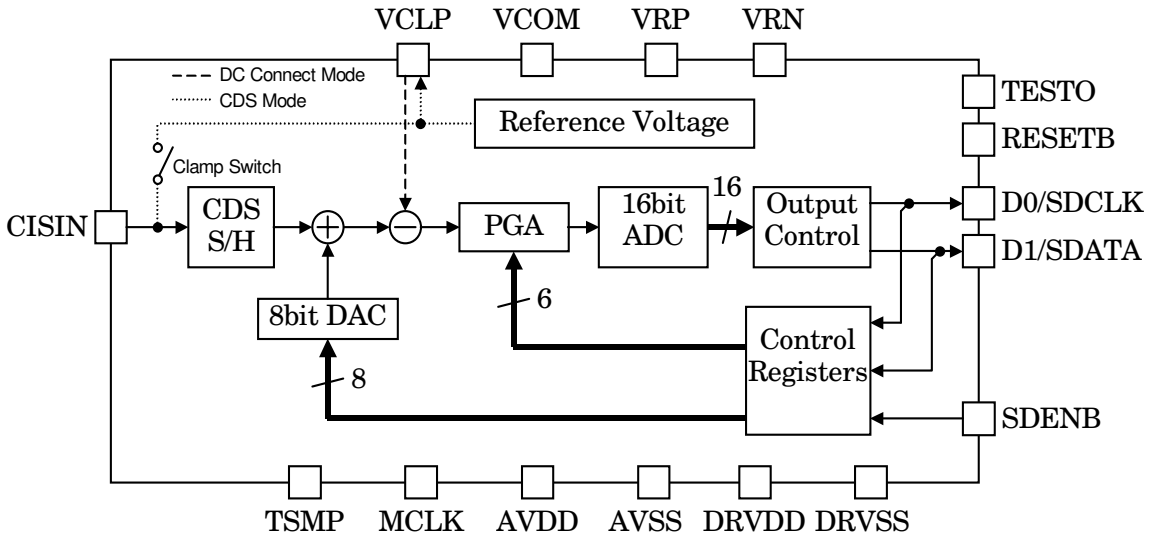

Fig. 1 Block Diagram

■ Sensor Interface Part

Circuit to sample & hold input signal which is fed on CISIN pin. Signal input range is 1.98V (typ.). There are two input modes, DC Direct Coupled Mode and CDS Mode. In DC Direct Coupled Mode, Positive polarity signal is handled. In CDS Mode, Negative polarity signal is handled. Signal Reference Voltage should be input on VCLP pin in DC Direct Coupled mode. In CDS mode, Voltage level to clamp signal is internally generated and it is output on VCLP pin.

■ Black Level Correction Circuit

Circuit to add an Offset voltage to the sampled signal level. Voltage range of DAC which generates Offset is ±240 mV (typ.) and its resolution is 8 Bit.

■ PGA Part

Circuit to adjust signal amplitude, prior to AD conversion. Adjustable gain range is from 0dB to 13.9dB (typ.) (1.0× ~ 4.9×) and its resolution is 6 Bit.

■ ADC Part

AD conversion circuit to convert into Digital data an Analog signal after both Black level correction and Gain adjustment are made. Its resolution is 16 Bit with its maximum conversion rate of 5MSPS. Data output is in a straight Binary code. 0000h is output at Black level input (0Vpp input) and FFFFh is output at White level input (maximum input).

■ Output Control Part

A 16 Bit-wide ADC output data is re-arranged into 2 Bit ×8 cycle stream at this part. In Single Edge Mode operation, Data is output at the rising edge of MCLK. In Double Edge Mode operation, it is output at both rising and falling edges of MCLK.

■ Reference Voltage Generator

Circuit to generate internal reference voltages. Clamp Reference Voltage VCLP, internal

common voltage VCOM and ADC reference voltages VRP and VRN are generated. Each reference voltage is output on respective device pins. For voltage stabilization, capacitors should be connected between respective pins and AVSS.

■ Serial Interface Part

A 3-Wire Interface circuit to access setting-registers. SDCLK (clock) and SDATA (data) pins are shared with D0 and D1 pins of ADC Data Output. When SDENB pin is at low, D0 and D1pins function as SDCLK and SDATA input pins. In order to avoid both SDCLK and SDATA pins to become floating condition, proper pull-down resistors should be connected between D0 / SDCLK pin, D1 / SDATA pin and AVSS respectively.

Pin Functions

No.	Name	IO	Description
1	TSMP	I	Sampling Timing
2	MCLK	I	Main Clock Single edge mode : 8 × Sampling frequency Double edge mode : 4 × Sampling frequency
3	RESETB	I	Reset pin : Active Low, on chip pull-up resister : 100kΩ (typ.)
4	D1/SDATA	O I	SDENB=High ; A/D Data output : Upper Bit SDENB=Low ; Serial Interface Data input
5	DRVDD	PWR	A/D Output buffer power supply
6	DRVSS	PWR	A/D Output buffer ground
7	D0/SDCLK	O I	SDENB=High ; A/D Data output : Lower Bit SDENB=Low ; Serial Interface Clock input
8	SDENB	I	Serial Interface Enable
9	VCOM	O	Internal Reference Voltage
10	VRN	O	ADC Negative Reference Voltage
11	VRP	O	ADC Positive Reference Voltage
12	VCLP	I O	Sensor Reference Level input at DC Direct Coupled mode Clamp Level output at CDS mode
13	CISIN	I	Sensor Signal input
14	AVSS	PWR	Analog ground
15	AVDD	PWR	Analog power supply
16	TESTO	O	Test Output pin. Should be left open

I: Input , O: Output , PWR: Power Supply

Pin Allocation

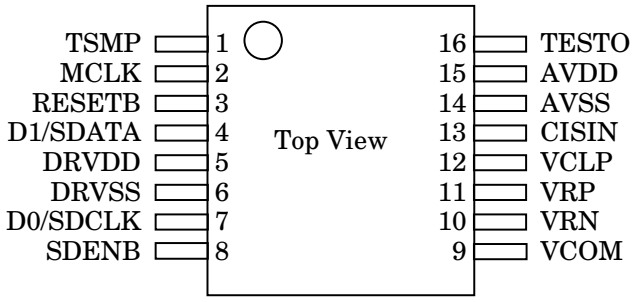

Fig. 2 Pin Allocation

Functional Description

■ Main Clock (MCLK)

The AK8411 has two clock modes, Single Edge Mode and Double Edge Mode. A required clock frequency differs in each mode. In the Single Edge mode, the required MCLK frequency is 8 times of the Pixel clock rate and in the Double Edge mode, it is 4 times of the Pixel clock rate. When to change MCLK frequency, a time required from frequency change to valid data output is 10 ms maximum.

■ Sampling Timing Pulse (TSMP)

TSMP is a pixel-period-equivalent input pulse to decide sampling timing of input signal. As MCLK and TSMP are also used to generate internal common voltage, it takes 10 ms maximum to output valid data upon stabilization of internal common voltage after re-start of MCLK and TSMP when MCLK or TSMP is stopped longer than 2000 ns. When the stopped time of MCLK or TSMP is equal to or shorter than 2000 ns, a valid data is output right after the recovery of MCLK or TSMP application.

■ Clamp Circuit

Circuit to pull-in the feed-through level of CCD signal to VCLP voltage so that CCD signal to be input is set within the input range of Sample & Hold circuit. This circuit is enabled at CDS mode operation.

■ Sampling Pulses SHD, SHR (internal pulses)

SHD is an internal pulse to sample data level of CIS signal. CIS signal is sampled at the falling edge of SHD. There are two types of sampling modes. One is MCLK Synchronous Sampling Mode where SHD is internally generated from MCLK and TSMP, and the other is TSMP Sampling Mode where TSMP is directly used as SHD as is. SHR is a pulse to sample feed-through level of CIS signal in CDS mode operation. CIS signal is sampled at the falling edge of SHR. SHR is also used to control clamp switch. Clamp switch is ON (Close) at SHR = High and Clamp switch is OFF (Open) at SHR = Low.

■ Input Circuit

DC Direct Coupled Mode

A mode to capture a difference between the sampled signal level at the Sample & Hold circuit and the reference level to be input on VCLP. It is effective when the Pixel signal level is output at higher than the reference level.

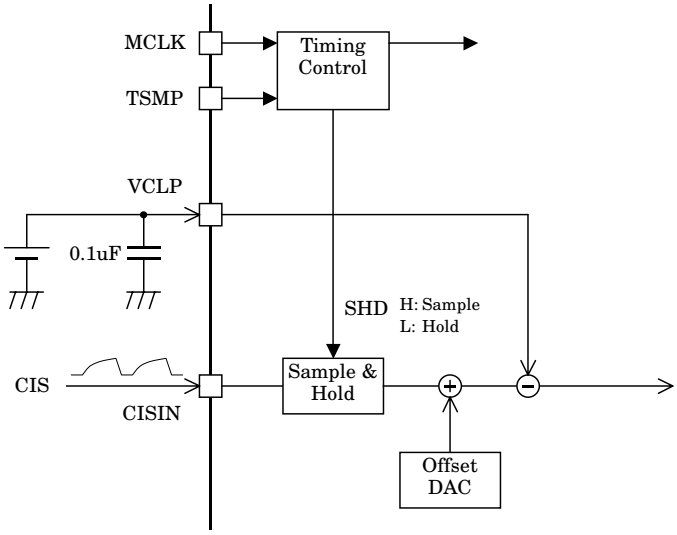

Fig. 3 in DC Direct Coupled Mode

CDS Mode

A mode to sample feed-through level of CIS signal (CCD type) and data level, and its difference is captured. In this scheme, thermal noise overlapped with CIS signal and shift of Clamp level is cancelled out. It is effective when the pixel signal level is output at lower than the reference level.

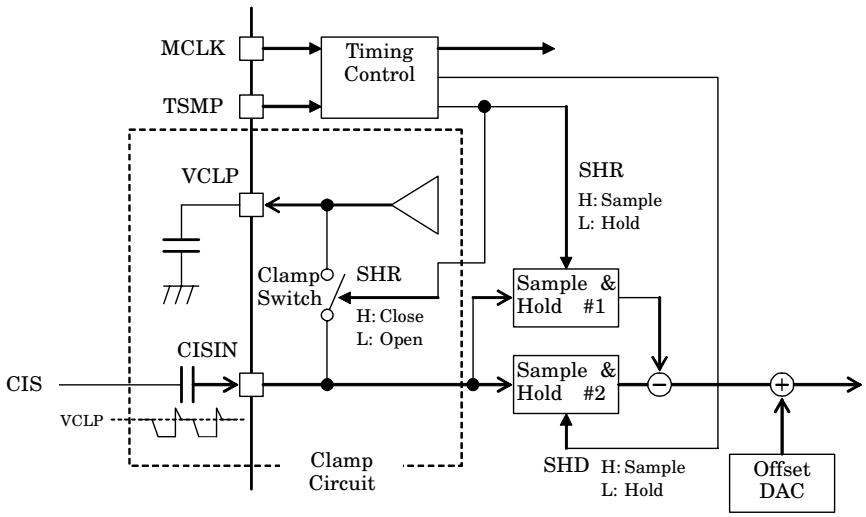

Fig. 4 in CDS Mode

■ D0, D1 A/D Data output

A/D data is output in 2 Bit wide x 8 cycles. In Single Edge Mode operation, A/D data D0 & D1 are output in sync with the rising edges of MCLK. In Double Edge Mode operation, D0 & D1 are output in sync with both rising and falling edges of MCLK.

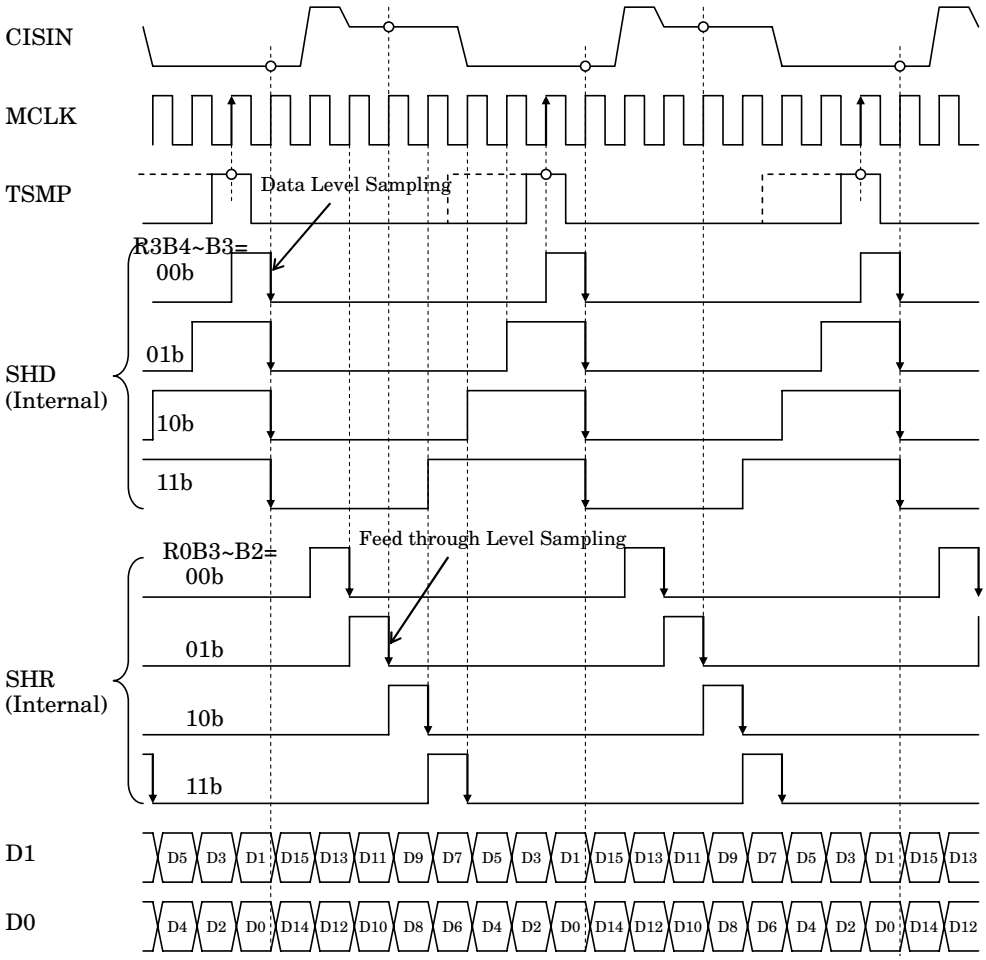

Fig. 5 Sampling Timing and ADC Output
(in Single Edge, MCLK Sync Sampling Mode)

In Single Edge Mode operation, it is required that 1 ~ 3 rising edges of MCLK occur during the TSMP High duration time. When MCLK rises twice or more during the TSMP High duration time, the last MCLK rising edge becomes effective. When rising edges of MCLK during TSMP High duration time occur 4 times and more, correct operation is not made. When the Data Level Sampling Mode is MCLK Sync sampling, SHD falls at the next MCLK rise after the last MCLK rise which detected TSMP = High condition. High duration time of SHD can be set by register. When the clock mode is in Single Edge Mode, it can be set from one to four MCLK periods in a single period unit. When the clock mode is in Double Edge Mode, it can be set from a half to 2 MCLK periods in a half period unit.

In Single Edge Mode operation, pulse width of SHR is equal to a single MCLK period. Falling edge position of SHR is pre-settable in MCLK-period resolution in the range from 2 clock MCLK delay to 5 clock MCLK delay , counting from the next MCLK rising edge after the

rising edge of MCLK where the last TSMP = High condition is detected.

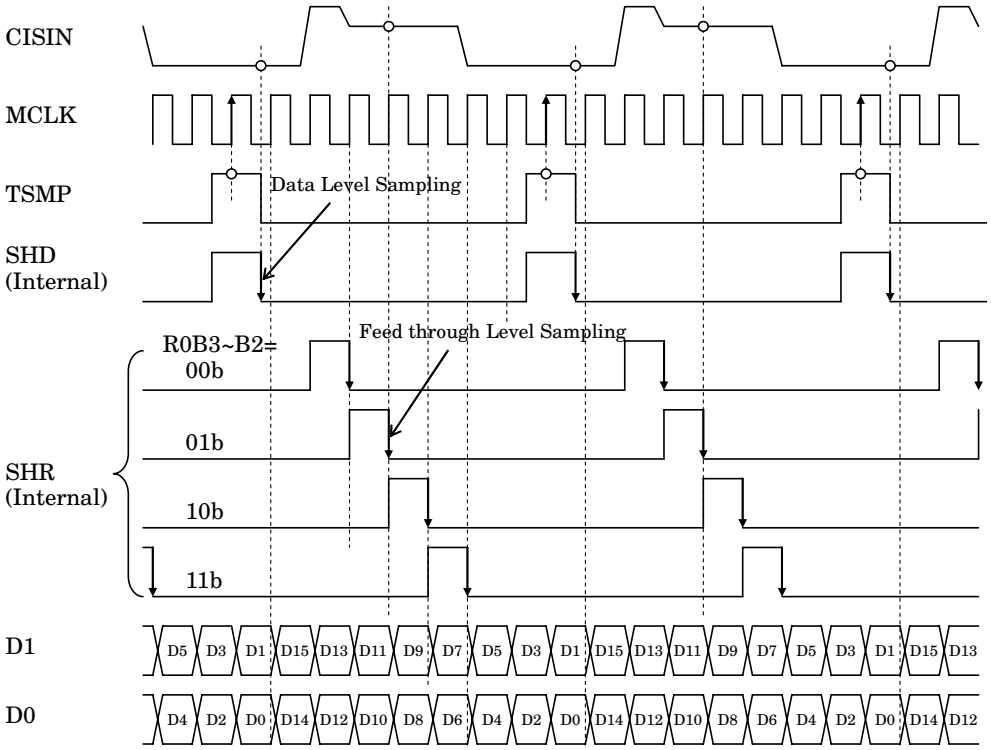

Fig. 6 Sampling Timing and ADC Output
(in Single Edge, TSMP Sampling Mode)

When the data level sampling pulse mode is TSMP sampling, TSMP pulse is directly used as internal SHD as is. SHD Pulse Width Setting Register becomes invalid in TSMP sampling mode.

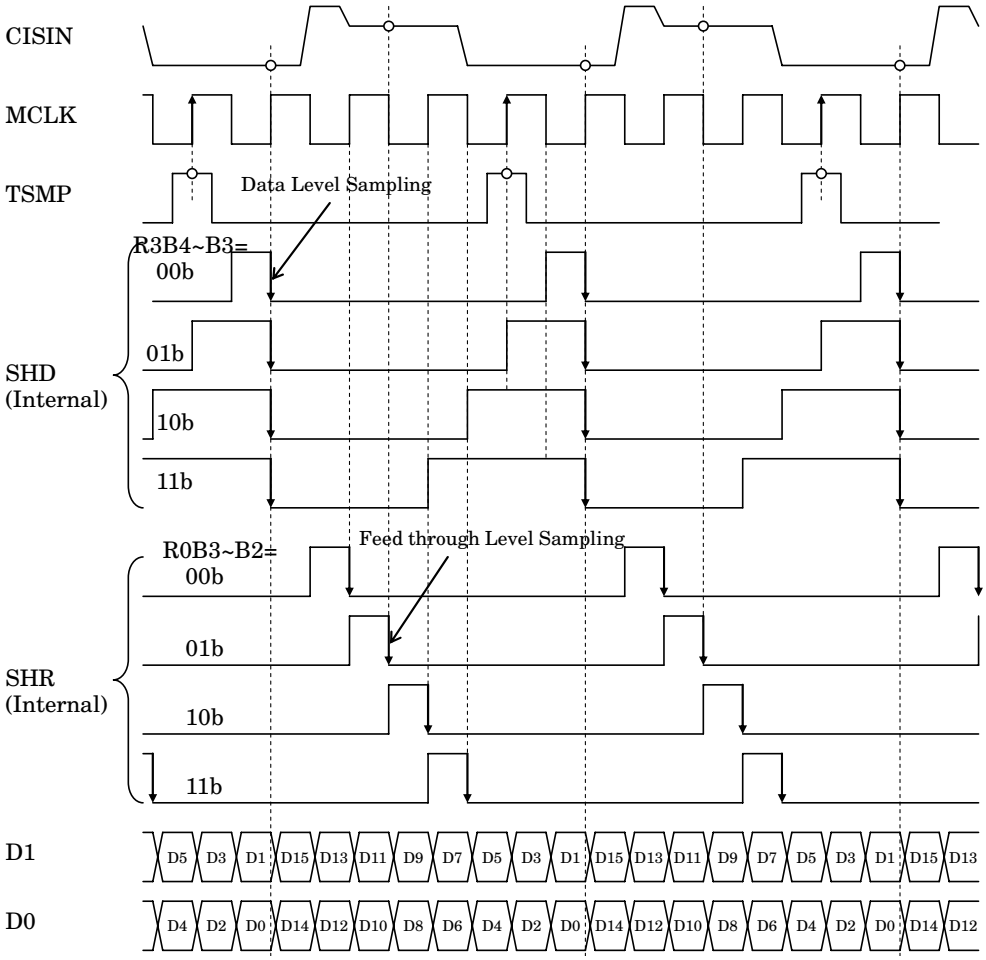

Fig. 7 Sampling Timing and ADC Output
(in Double Edge, MCLK Sync Sampling Mode)

In Double Edge Mode operation, it is required that a single rising edge of MCLK occurs during TSMP High duration. When rising edge of MCLK during TSMP High duration occurs twice and more, proper operation is not made.

SHR pulse width in Double Edge Mode is equal to a half of MCLK period. Falling edge position of SHR is pre-settable in 1/2 MCLK-period resolution in the range from a single MCLK clock delay to 2.5 clock delay, counting from the next MCLK rising edge after the rising edge of MCLK where TSMP = High condition is detected.

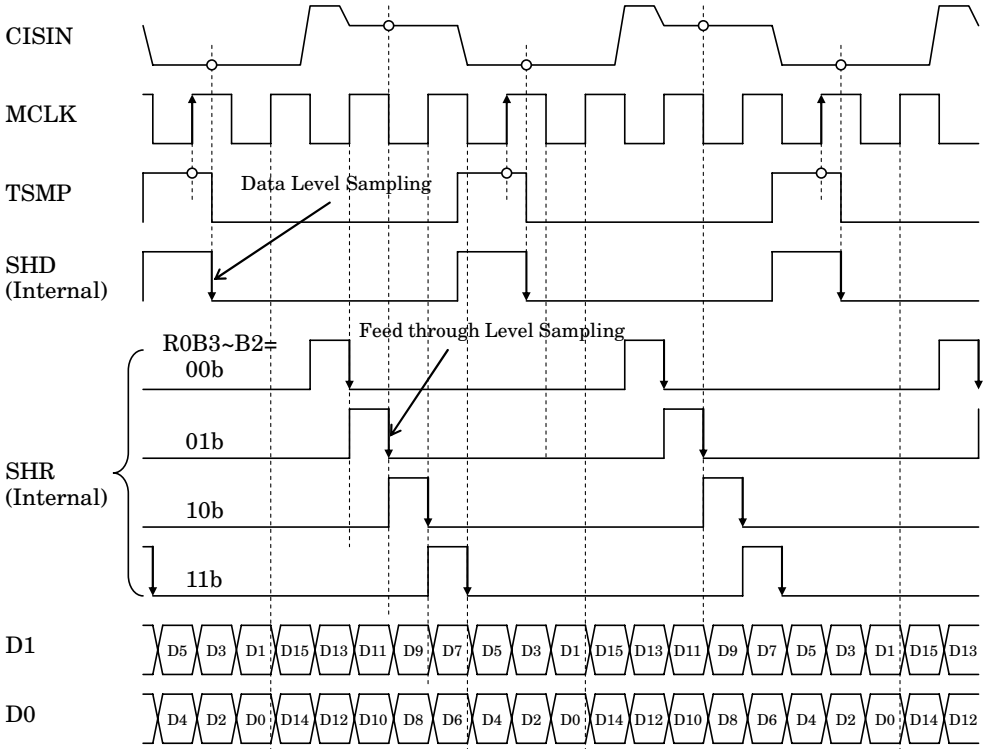

Fig. 8 Sampling Timing and ADC Output
(in Double Edge, TSMP Sampling Mode)

■ Power-On-Reset

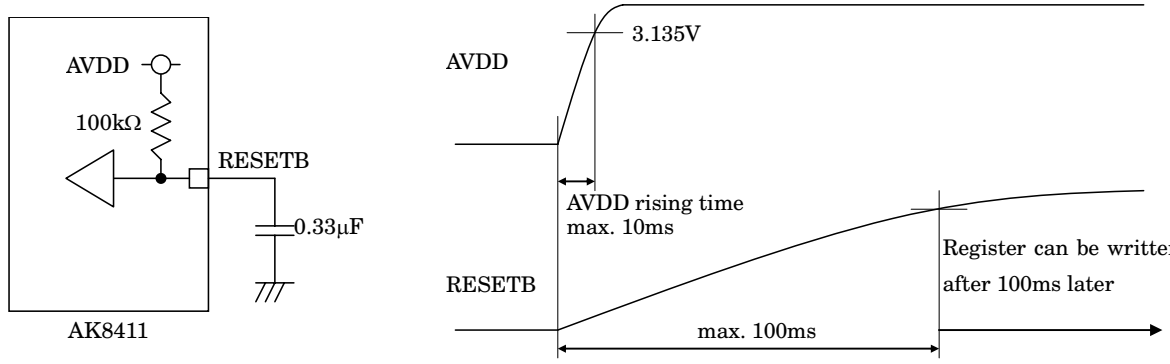

Fig. 9 Power-On-Reset

At the power-on, Power-On-Reset must be executed by using RESETB pin. When a 0.33 uF external capacitor on RESETB pin is used, the rise time of AVDD must be shorter than 10 ms in order to assure proper Power-On-Reset operation. Maximum time from AVDD power-on to the release from Power-On-Reset is 100 ms. Registers should be written after waiting for longer than 100 ms after AVDD power-on.

As electric charge is retained in the external capacitor even after AVDD is made to 0V, voltage on RESETB pin does not go to 0V immediately. If AVDD is powered-up again before RESETB pin returns to 0V, a proper Power-On-Reset operation is not made. In order to assure proper Power-On-Reset operation when to power-up AVDD again, it is required that AVDD time to be kept at 0V is longer than 300 ms. If the 300 ms AVDD time to be kept at 0V, is not obtainable, the device must be reset by applying a low pulse externally on RESETB pin.

Absolute Maximum Ratings

Voltages are referenced to corresponding ground level. AVSS = DVSS = 0V

Item	Symbol	Min.	Max.	Unit	Note
Power supplies					
Analog power supply	AVDD	–0.3	4.5	V	
Output Buffer power supply	DRVDD	–0.3	4.5	V	
Digital Input Voltage	VTD	–0.3	AVDD+0.3	V	
Analog Input Voltage	VTA	–0.3	AVDD+0.3	V	
Storage temperature	Tstg	–65	150	°C	

Operation under a condition exceeding above limits may cause permanent damage to the device. Normal operation is not guaranteed under the above extreme conditions.

Recommended Operating Conditions

Voltages are referenced to corresponding ground level. AVSS=DRVSS= 0V

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power supplies						
Analog power supply	AVDD	3.135	3.3	3.465	V	
Output buffer power supply	DRVDD	3.0	3.3	3.6	V	
Operating temperature	Ta	0		70	°C	

Electrical Characteristics

■ DC Characteristics

(AVDD=3.135~3.465V, DRVDD=3.0~3.6V, Ta=0~70°C, unless otherwise specified)

Item	Symbol	Pin	Min.	Typ.	Max.	Unit	Note
H level input voltage	VIH	Note 1, 2, 4	0.7× AVDD			V	
L level input voltage	VIL	Note 1, 2, 4			0.3× AVDD	V	
H level output voltage	VOH	Note 3	0.7× DRVDD			V	IOH= –2mA
L level output voltage	VOL	Note 3			0.3× DRVDD	V	IOL=2mA
Input leakage current 1	IL1	Note 1	–10		10	μA	
Input leakage current 2	IL2	Note 2	–69.3		10	μA	apply 0V ~ AVDD
High-Z leakage current	ILZ	Note 4	–10		10	μA	
Pull-up resistor	RPU	Note 2	50	100	150	kΩ	

(Note 1) TSMP, MCLK, SDENB
(Note 2) RESETB
(Note 3) D0, D1 (at SDENB=High)
(Note 4) SDATA, SDCLK (at SDENB=Low)

■ Analog Characteristics

(AVDD=3.3V, DRVDD=3.3V, MCLK=40MHz, Single Edge Mode, Ta=25°C, unless otherwise specified)

Item	Min.	Typ.	Max.	Unit	Note
Reference Voltage					
VCOM voltage	1.4	1.5	1.6	V	
VRP voltage	1.9	2.0	2.1	V	
VRN voltage	0.9	1.0	1.1	V	
Analog Input					
Maximum signal input level		1.98		V_{p-p}	
Absolute gain	–0.7	0	0.7	dB	At DC mode (Note 1)
	–1.45	–0.45	0.55	dB	At CDS mode (Note 1)
Sampling rate	1		5	MSPS	
Input reference level	0	1.1	1.5	V	At DC mode
VCLP Input resistance	10	60		kΩ	At DC mode
Signal input range	0		AVDD	V	At DC mode (Note 2)
Clamp level (VCLP voltage)	1.95	2.05	2.15	V	At CDS mode
Clamp resister		7	10	kΩ	At CDS mode
Black level correction DAC					
Resolution		8		bit	(Note 3)
Correctable range	±215	±240	±265	mV	(Note 4)
Internal offset voltage	–50		50	mV	(Note 5)
PGA (Programmable Gain Amp.) circuit					
Resolution		6		bit	
Minimum gain		0		dB	
Maximum gain	12.9	13.9	14.9	dB	(Note 6)
Video ADC					
Resolution		16		bit	
Differential Non-linearity	–16		+16	LSB	
Integral Non-linearity		±32		LSB	
Noise					
Output noise		5		LSB_{rms}	PGA min.
		15		LSB_{rms}	PGA max.
Power Consumption					
Analog part power dissipations		21.5	31.5	mA	At DC mode (Note 7)
		24.5	34.5	mA	At CDS mode (Note 7)
			0.1	mA	At Power down (Note 8)
Digital output driver power dissipation		3	10	mA	(Note 9)

(Note 1) 0dB is defined at the gain where ADC output reaches its full-scale when 1.98Vpp signal is input with PGA setting at 00h.

(Note 2) CISIN input signal must be in this range which is referenced to AVSS.

(Note 3) Monotonicity guaranteed.

(Note 4) ±50 mV of the total correctable range is used for internal offset adjustment.

(Note 5) It defines that a boundary point of ADC output codes between 0000h and 0001h exists within ±50mV range of the offset adjustment DAC setting when 1.1V is fed on CISIN & VCLP pins in DC Direct Coupled mode, and when PGA gain is set to 0dB.

(Note 6) Relative value to the gain at PGA setting is 00h.

(Note 7) A full-scale minus 2 dB, 1 MHz sine-wave signal is input.

(Note 8) A clock supply to MCLK is stopped.

(Note 9) At the capacitive load is 20pF.

■ Switching Characteristics

(AVDD=3.135~3.465V, DRVDD=3.0~3.6V, Ta=0~70°C, unless otherwise specified)

#.	Item	Pin	Min.	Typ.	max.	Unit	Conditions
1	MCLK cycle time (T)	MCLK	25		125	ns	Single edge
			50		250	ns	Double edge
2	MCLK 'H' , 'L' width	MCLK	10			ns	Single edge
			25			ns	Double edge
3	TSMP set-up time (referenced to MCLK↑)	TSMP	5			ns	(Note 1)
4	TSMP hold time (referenced from MCLK↑)	TSMP	5			ns	(Note 1)
5	Aperture delay (referenced from MCLK↑)	CISIN		2		ns	Data level
6	Aperture delay (referenced from MCLK↑)	CISIN		2		ns	Reference level
7	TSMP period (MCLK period-unit)	TSMP		8T			Single edge
				4T			Double edge
8	Data output delay (referenced from MCLK↑)	D0, D1	2		25	ns	Single edge At load:20pF, (Note 2)
			2		20	ns	Single edge At load:20pF, (Note 3)
	Data output delay (referenced from MCLK↑↓)	D0, D1	2		25	ns	Double edge At load :20pF, (Note 2)
			2		20	ns	Double edge At load :20pF, (Note 3)
9	Pipeline delay	D0, D1		4			TSMP period-unit
10	Reset pulse width	RESETB	50			ns	

(Note 1) Number of MCLK rising edges during TSMP = H duration is allowed to be 1 to 3 times in Single Edge Mode operation, and only a single edge is allowed in Double Edge mode operation.

(Note 2) when output buffer drivability is set at normal setting

(Note 3) when output buffer drivability is set at 2× setting

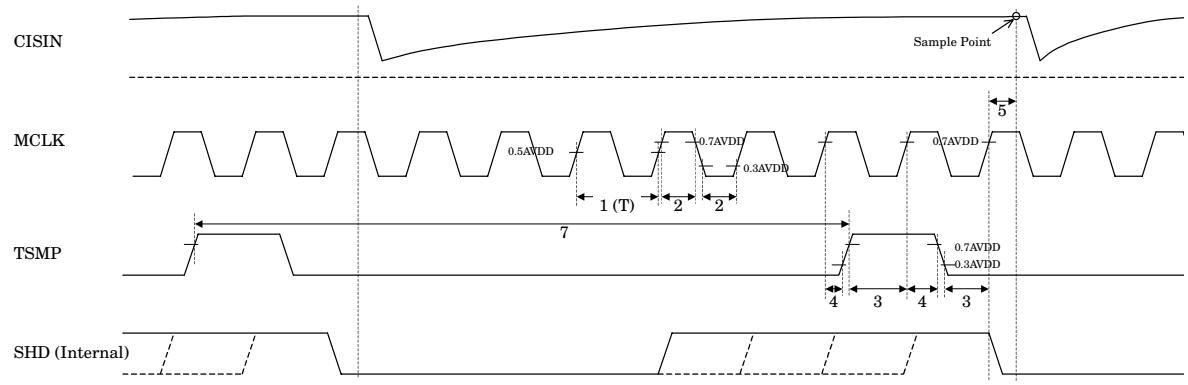

Fig. 10 Sampling Timing (in DC Direct Coupled, Single Edge Mode)

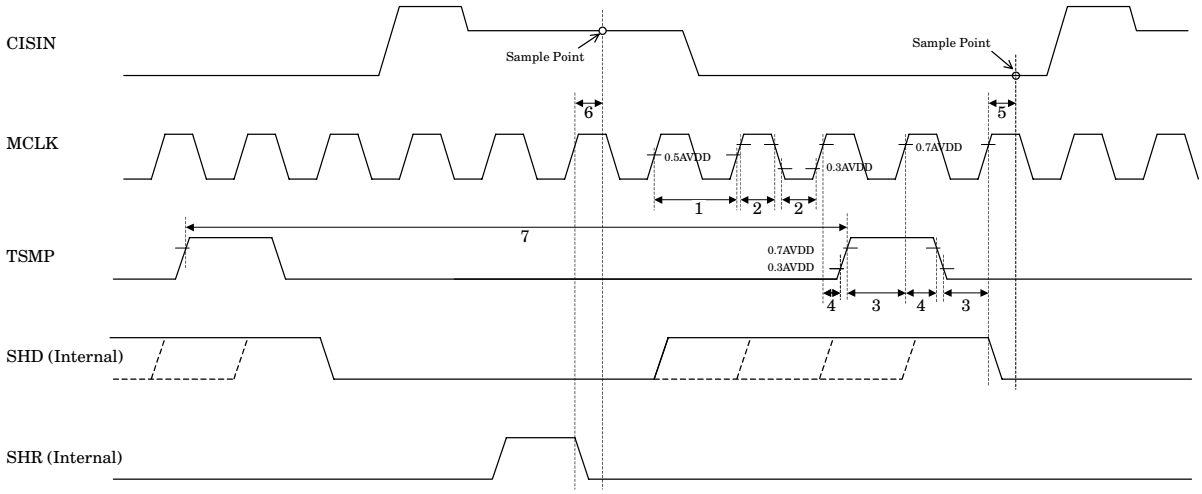

Fig. 11 Sampling Timing (in CDS, Single Edge Mode)

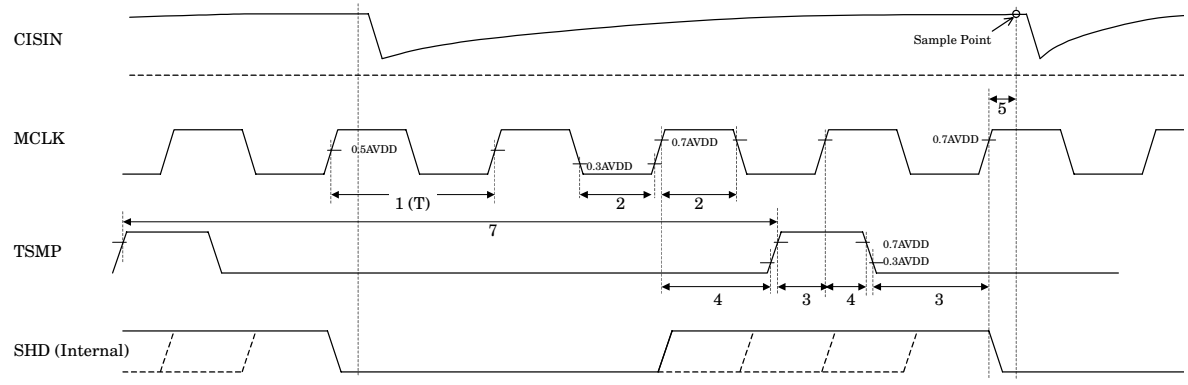

Fig. 12 Sampling Timing (in DC Direct Coupled, Double Edge Mode)

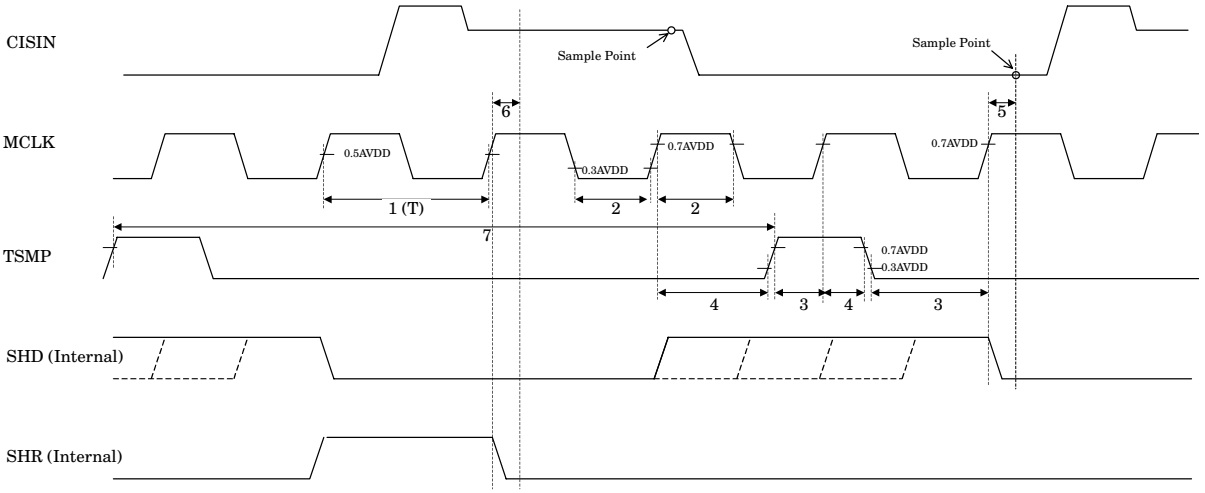

Fig. 13 Sampling Timing (in CDS, Double Edge Mode)

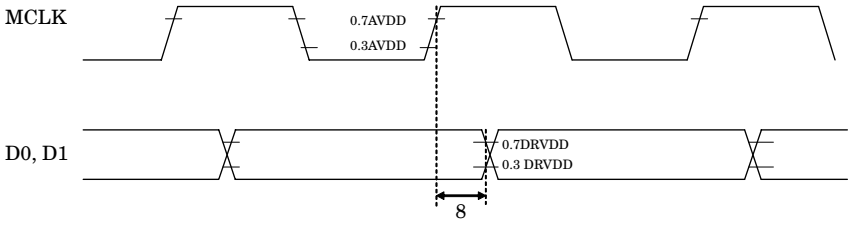

Fig. 14 Data Output Timing (Single Edge Mode)

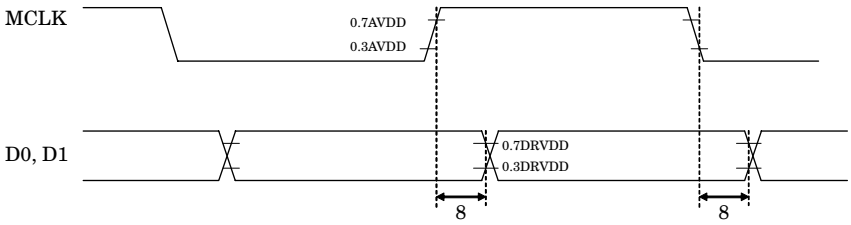

Fig. 15 Data Output Timing (Double Edge Mode)

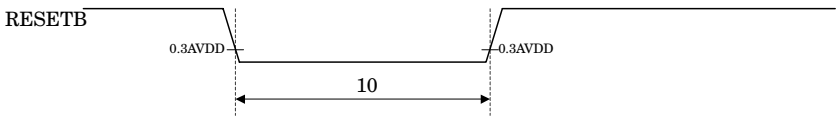

Fig. 16 Reset Pulse Width

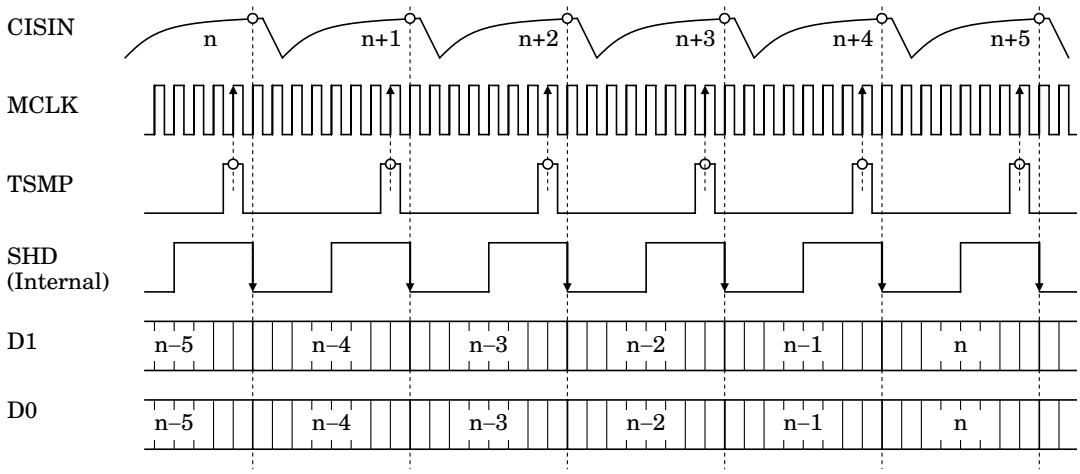

Fig. 17 Pipeline Delay (in Single Edge Mode)

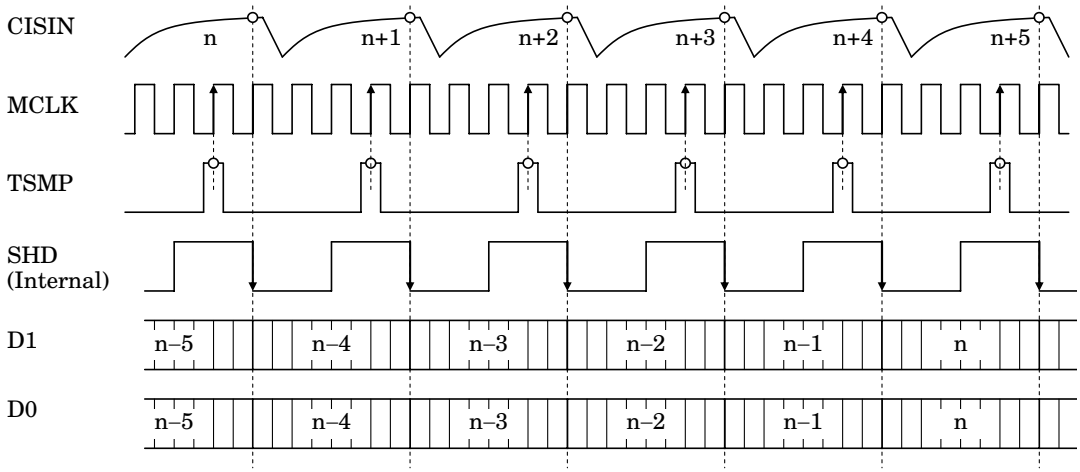

Fig. 18 Pipeline Delay (in Double Edge Mode)

Data are output in the same Pipeline Delay time both in DC Direct Coupled Mode and CDS Mode which is referenced to TSMP.

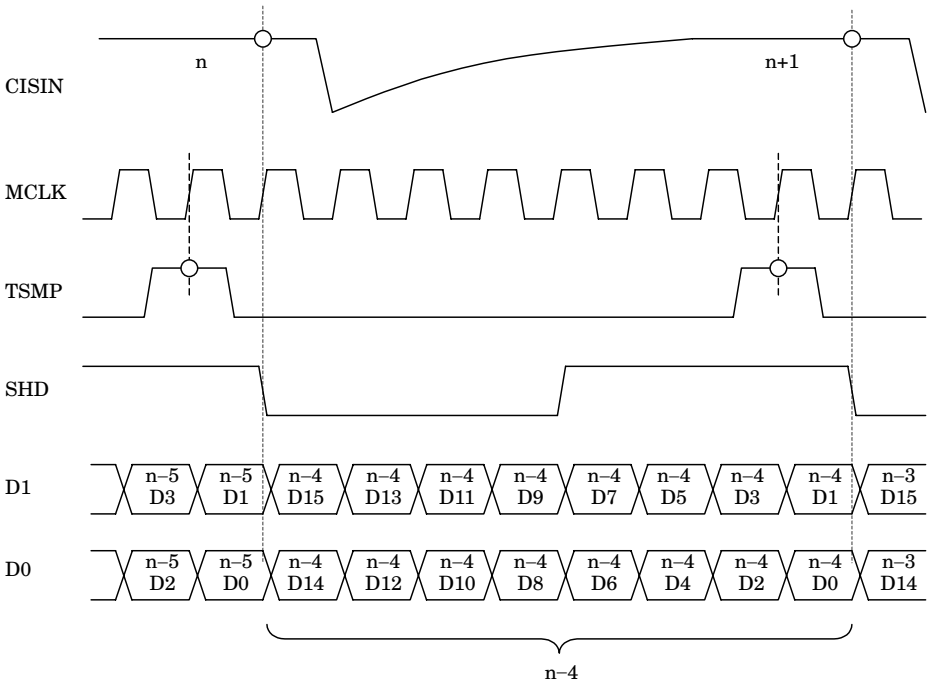

Fig. 19 Pipeline Delay (scaled-up diagrams in Single Edge Mode)

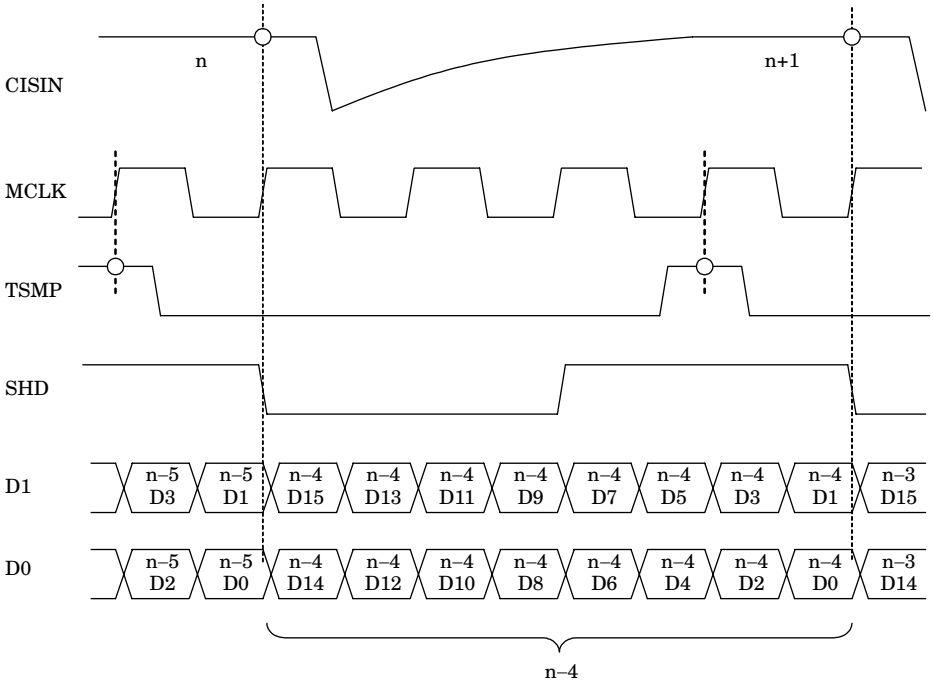

Fig. 20 Pipeline Delay (scaled-up diagrams in Double Edge Mode)

Data are output in the same Pipeline Delay time both in DC Direct Coupled Mode and CDS Mode which is referenced to TSMP.

■ Switching Characteristics : Serial Interface

(AVDD = 3.135 ~3.465V, DRVDD = 3.0 ~3.6V, Ta = 0 ~70°C , unless otherwise specified)

#	Item	Pins	Min.	Typ.	Max.	Unit	Conditions
1	Clock Period	SDCLK	0.1		10	MHz	
2	Clock Pulse Width (H duration)	SDCLK	40			ns	
3	Clock Pulse Width (L duration)	SDCLK	40			ns	
4	SDENB setup time (to SDCLK rising edge↑)	SDENB	80			ns	
5	SDENB hold time (from SDCLK rising edge↑)	SDENB	80			ns	
6	Data High-Z delay (from SDENB falling edge↓)	D0, D1	0		40	ns	
7	Data Enable delay (from SDENB rising edge↑)	D0, D1	0		40	ns	
8	SDATA setup time (to SDCLK rising edge↑)	SDATA	40			ns	
9	SDATA hold time (from SDCLK rising edge↑)	SDATA SDENB	40			ns	
10	SDCLK,SDENB Rise time	SDCLK SDENB			6	ns	
11	SDCLK,SDENB Fall time	SDCLK SDENB			6	ns	
12	SDENB High level pulse width	SDENB	40			ns	

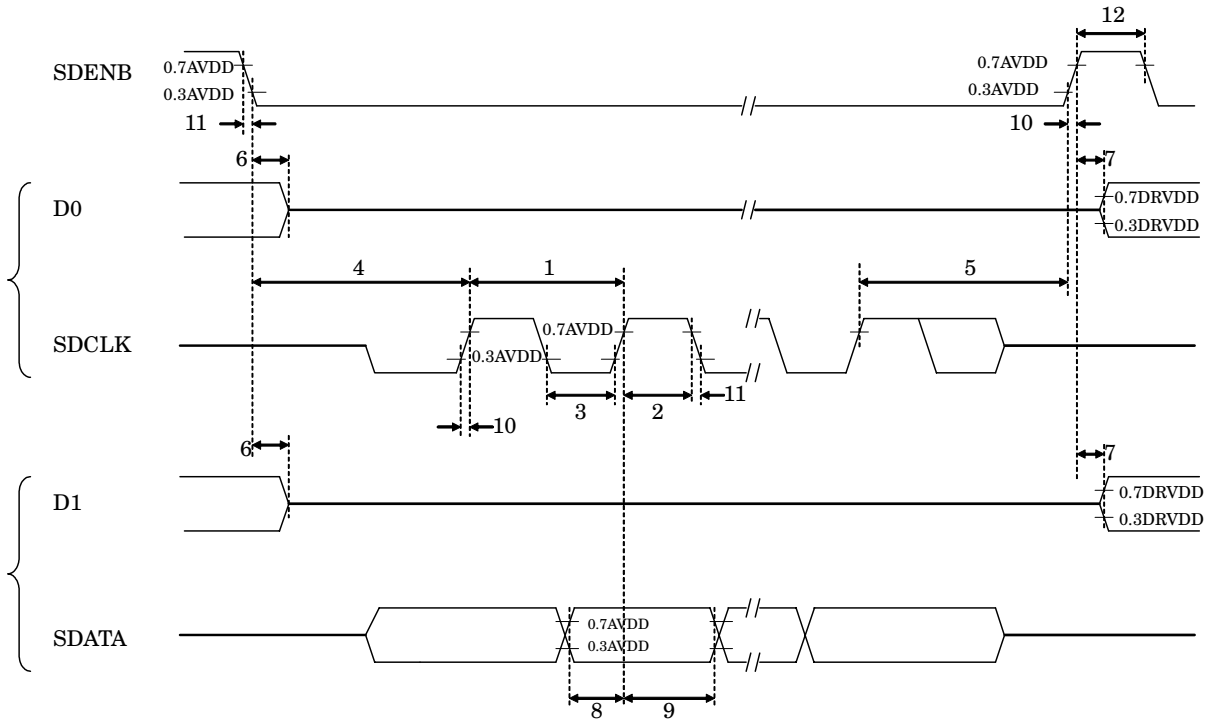

Fig. 21 Serial Interface Timing

Serial Interface

Clock Input pin SDCLK and Data Input pin SDATA for Serial Interface are shared with A/D Data Output pins, D0 and D1 respectively. When SDENB becomes low, D0 and D1 are put into High-Z conditions and it is enabled to input SDCLK and SDATA. SDATA is captured at the rising edge of SDCLK. SDATA is 16 Bit long. Write "zeros" from the 1st Bit to the 5th Bit. 6th~8th Bits are assigned for Register Address where the 6th Bit is MSB and the 8th Bit is LSB. 9th~ 16th Bits are assigned for Data where the 9th Bit is MSB and the 16th Bit is LSB.
16 and more rising edges of SDCLK are required while SDENB is low, from the time to fall to the time to rise. When it is less than 16 rises, registers will not be written properly.
If it is more than 16 rises while SDENB is low, from falling to rising, the last 16 edges become effective. There is a possibility that an erroneous data will be written into registers if noises occur on D0 Output / SDCLK input pin and D1 Output / SDATA input pin when these pins are at High-Z conditions. To avoid this, resistors should be connected between D0 / SDCLK pin, D1 / SDATA pin and AVSS respectively to pull-down these pins.

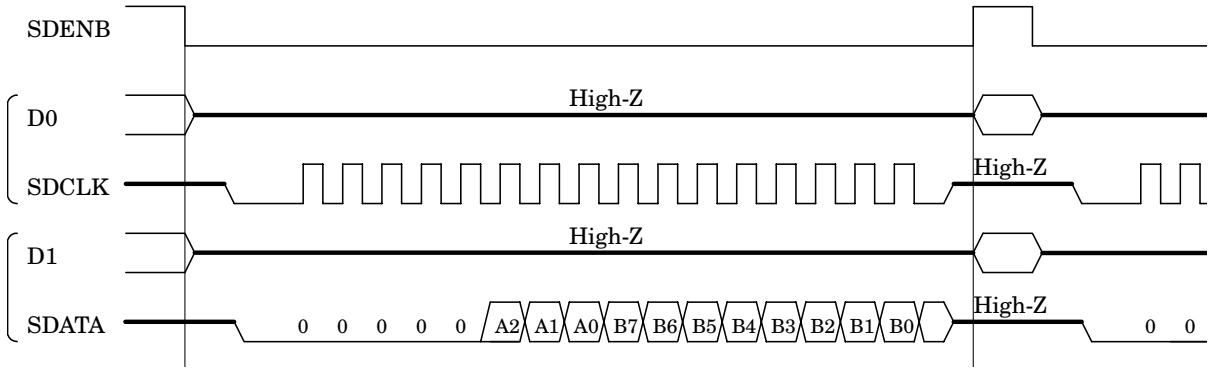

Fig. 22 Register Write Operation

Control Registers

It takes 10 ms maximum from register contents to be modified till valid data to be output on D0 & D1 pins. When to modify register contents when R0 B7 is set to "zero" (Reset condition), set R0 B7 to "one" (release from Reset) first, then modify other registers, including B6 ~B0 Bits at Address Zero. Un-used bits can be written with either "zeros" or "ones".

Address	Init.	B7	B6	B5	B4	B3	B2	B1	B0
0	00h	Reset	0	Output buffer drivability	Input mode	Reference level sampling position		Clock mode	Power down
1	80h	Offset DAC Data (8bit)							
2	00h	Un-used		PGA Gain data (6bit)					
3	00h	Un-used		SHD mode	SHD width		0	0	Output order
4	00h	for testing purpose							
5	00h	for testing purpose							

■ R0 B7 Register reset

B7	Operation
0	Reset (at reset)
1	release from Reset

When this bit is set to "0", all other registers are set to initial values, except for this bit. When this bit is "0", write operation into all other registers except for this bit is ignored.

■ R0 B6 Reserved

write " 0 ".

■ R0 B5 Output Buffer Drivability

B5	Output mode
0	Normal (at reset)
1	2× (Double)

When Output Buffer Drivability is set to "2×", maximum output current of the output buffers increases. This selection is used when the Data Output Delay which is referenced to Data Capture clock becomes too large, due to capacitive loading.

■ R0 B4 Input mode

B4	Input mode
0	DC Direct-Coupled mode (at Reset)
1	CDS mode

Signal Polarity which can be processed by the AK8411 is determined by the type of Input Modes. In DC Direct-Coupled Mode, it handles Positive polarity (signal is output toward higher voltage than reference level) and in CDS Mode, it handles Negative polarity (signal is output toward lower voltage than reference level).

■ R0 B3~B2 Feed-Through Level Sampling Pulse (SHR) Position

B3	B2	SHR Position at Single edge mode	SHR Position at Double edge mode
0	0	2×MCLK delay (at reset) from the Data Level Sampling position	1×MCLK delay (at reset) from the Data Level Sampling position
0	1	3×MCLK delay	1.5×MCLK delay
1	0	4×MCLK delay	2×MCLK delay
1	1	5×MCLK delay	2.5×MCLK delay

This register is to set fall position of internal pulse SHR, at which feed-through level is sampled. Pulse width of SHR is fixed. SHR is enabled only when the device is in CDS Mode operation. SHR stops while it is in DC Direct-Coupled Mode operation.

■ R0 B1 Clock Mode

B1	Clock mode
0	Single edge (at reset)
1	Double edge

In Single Edge Mode operation, D0 & D1 data of ADC are output in sync with rising edge of MCLK. Required MCLK frequency is 8 x Pixel rate. In Double Edge Mode operation, data are output in sync with both rising and falling edges of MCLK. Required MCLK frequency is 4 x Pixel rate.

■ R0 B0 Operation mode select

B0	Operation mode
0	Power down (at reset)
1	Normal operation

When this bit is set to ”0“, logic circuit excluding Serial Interface stops its operation while analog part is powered-down. Register contents just before being put into power-down operation are retained even during Power-Down operation.

■ R1 Offset DAC setting

B7~B0	Offset level
00000000	–240mV
:	:
01111111	–1.88mV
10000000 (at reset)	0mV
10000001	+1.88mV
:	:
11111111	+238mV

$Offset(x) = -240 + 480/256 \times x[\mathrm{mV}]$ (x=0~255) where x is a register set value.

at reset : x=128, Offset(128)=0mV

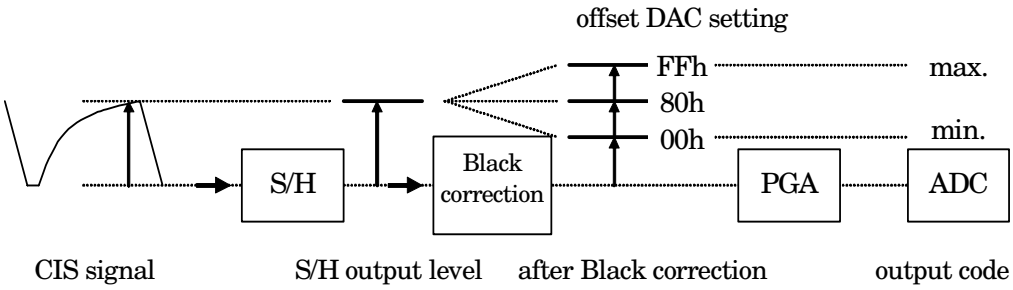

Fig. 23 Level Changes by Offset Setting

(in DC Direct-Coupled Mode operation = Positive polarity operation)

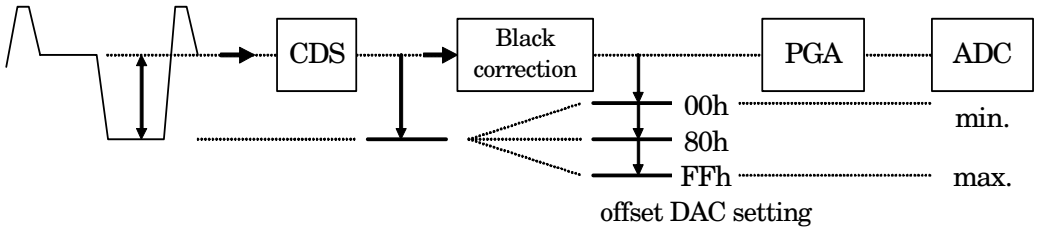

Fig. 24 Level Changes by Offset Setting

(in CDS Mode operation = Negative Polarity operation)

Offset DAC Output is added to the sampled & held signal level. Both in DC Direct-Coupled Mode operation (Positive Polarity) and in CDS Mode operation (Negative Polarity), when setting code to the Offset DAC is smaller, the ADC Output code becomes smaller, and when it is larger, the ADC Output code becomes larger.

■ R2h PGA Gain setting

$$Gain(x) = \frac{1.98}{2.0} \times \frac{80}{16 + (63 - x)} [times] \quad (x=0\sim63)$$ where x is a register setting value.

At reset, x=0 then Gain (0) = 1.0 time.

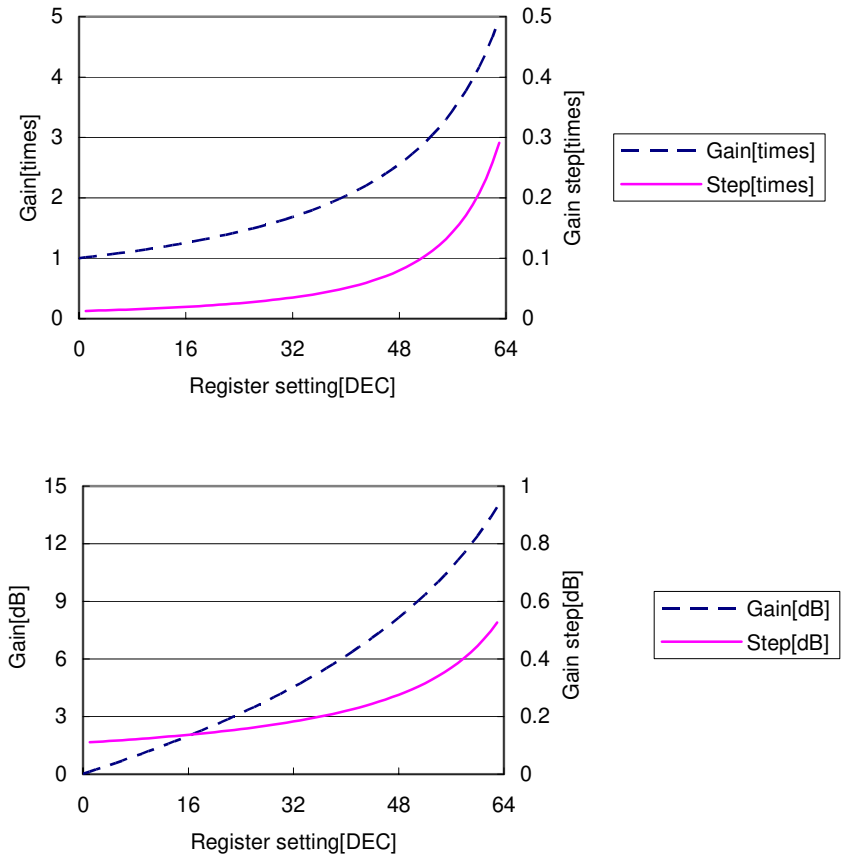

Fig. 25 Gain curves (theoretical values)

■ R3 B5 Data Level Sampling Pulse (SHD) Mode Select

B5	Data level sampling pulse (SHD)
0	MCLK synchronous sampling (at reset)
1	TSMP sampling

■ R3 B4~B3 Data Level Sampling Pulse Width (SHD) Select

B4	B3	SHD pulse width in Single edge mode	SHD pulse width in Double edge mode
0	0	1×MCLK period (at reset)	0.5×MCLK period(at reset)
0	1	2×MCLK period	1×MCLK period
1	0	3×MCLK period	1.5×MCLK period
1	1	4×MCLK period	2×MCLK period

Falling edge position of SHD, namely Data Level Sampling point is fixed. Only the Rising edge of SHD changes by register setting. This register becomes invalid when the Sampling Pulse Mode is at TSMP.

■ R3 B2-B1 Reserved

write 00b to these bits.

■ R3 B0 Output Order Select

B0	Output order
0	Normal (at reset)
1	MSB 8bit / LBS 8bit split

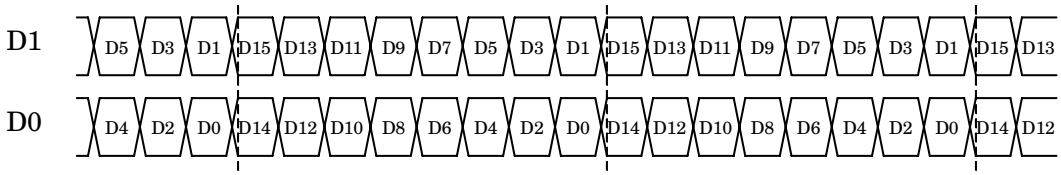

Fig. 26 Normal

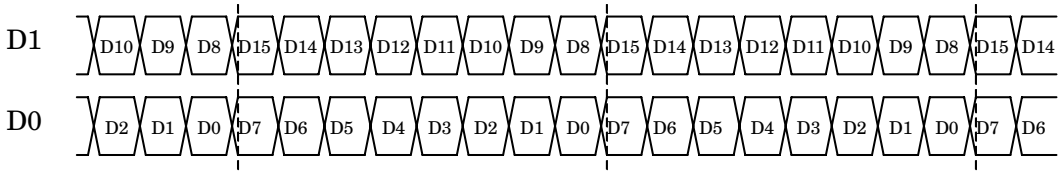

Fig. 27 MSB 8bit / LSB 8bit split mode

Timing diagrams shown in this data sheet are a case of Normal Order of Output Data, unless otherwise noted.

External Circuit Examples

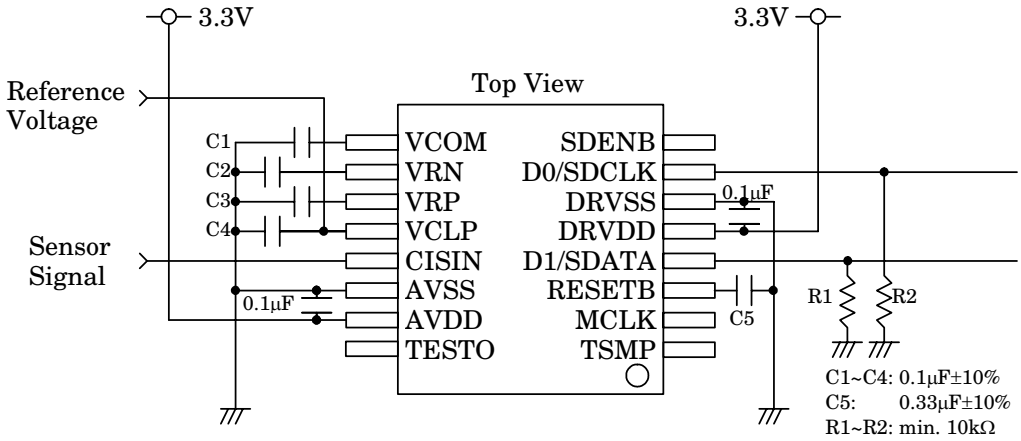

Fig. 28 in DC Direct-Coupled Mode operation

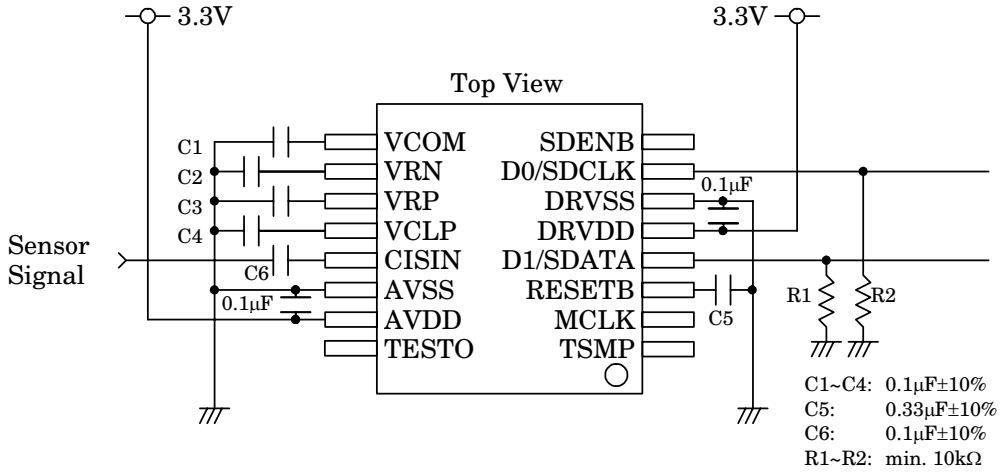

Fig. 29 in CDS Mode operation

Package

■ Package Dimensions

Unit: mm

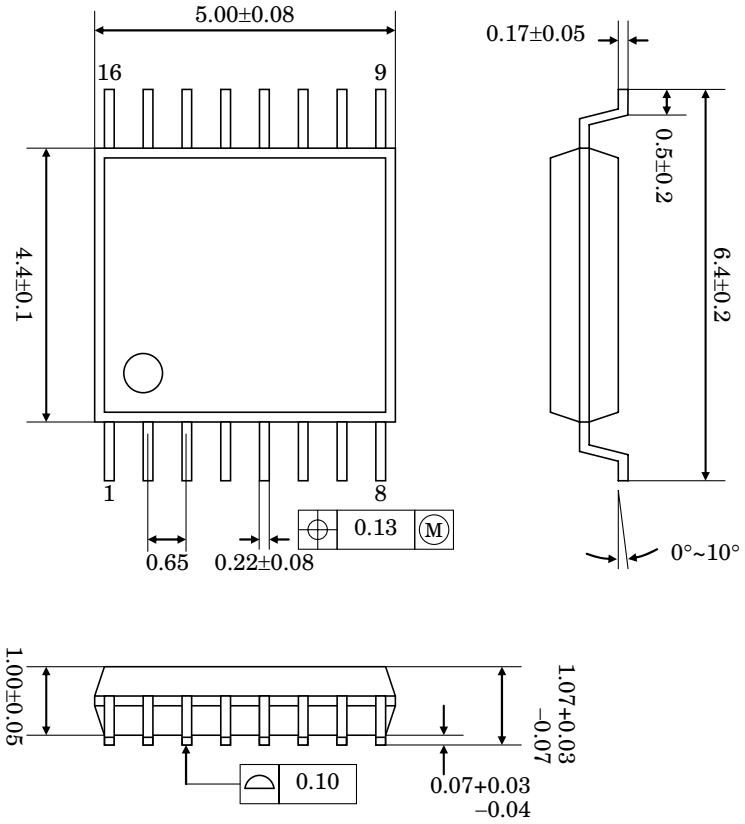

Fig. 30 Package dimensions

■ Package Markings

1. AKM logo : AKM
2. Marketing code : 8411VT
3. Date code : XXX week code
   : YY AKM's factory control code

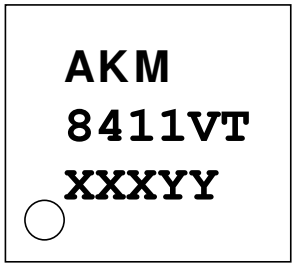

Fig. 31 Package Marking

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