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AK8817VQ
NTSC/PAL Digital Video Encoder

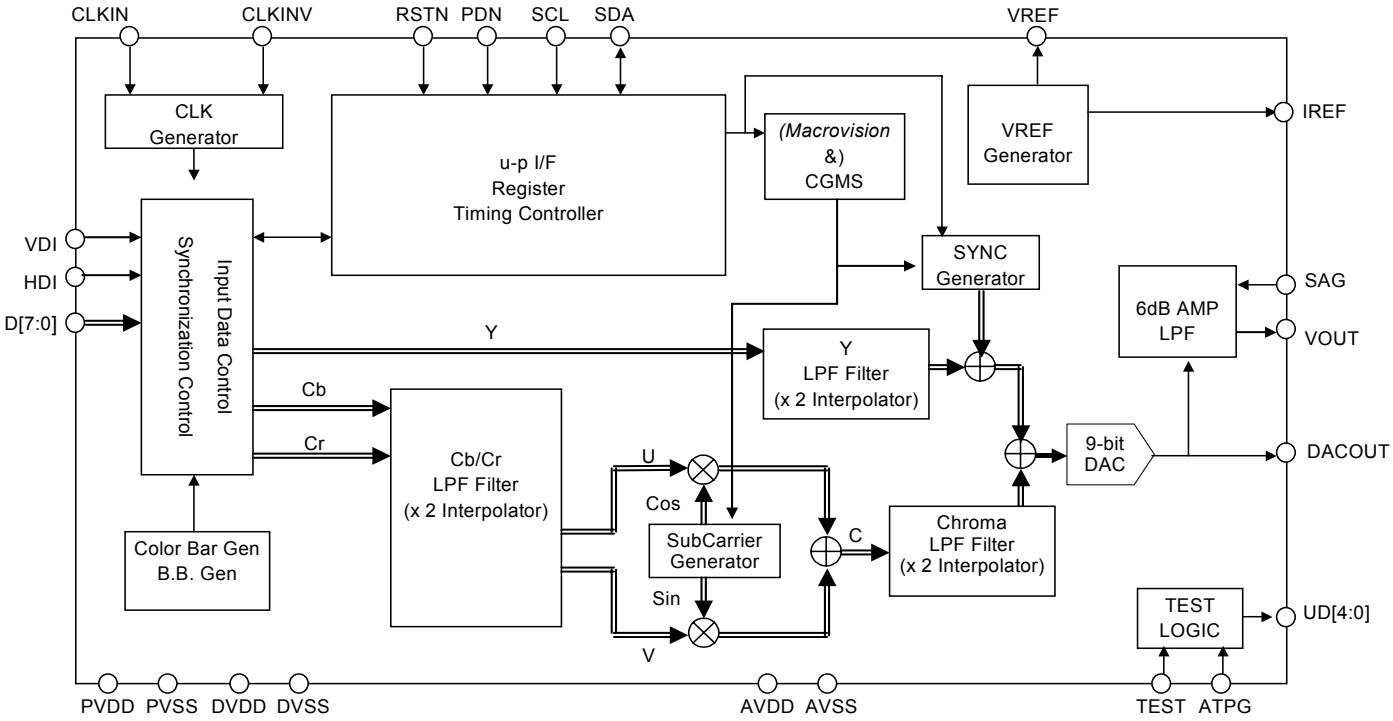
General Description

The AK8817VQ is a Digital Video Encoder for Portable and Mobile application. ITU-R BT.601 level compatible Y, Cb,and Cr signals which correspond to 27MHz or square pixel are encoded into either NTSC or PAL compatible composite video signal. Interface is made in HSYNC-, VSYNC- synchronized slave-mode operation or ITU-R.Bt656. AK8817VQ has 75ohm driver with LPF. It is possible to encode the VBID(CGMS-A) and WSS signal on the output video signal. Host Control interface is I2C Bus I/F.

Features

- NTSC-M, PAL-B, D, G, H, I Composite Video encoding
- Y:Cb:Cr 4:2:2
- H/V Slave Operation / ITU-R.BT656 Interface
- Y filtering: 2 x over-sampling
- C filtering: 4 x over-sampling
- 9bit DAC
- Setup
- VBID (CGMS-A) Compatible
- WSS Compatible
- Operation Clock rate : 27MHz or Square-pixel Clock rate(NTSC:24.5454MHz/PAL29.50MHz)
- Video Amp with LPF
- On-chip Color Bar Output
- Black Burst Output
- Power Supply (AVDD, DVDD) 2.7V - 3.6V
- I/F Power Supply (PVDD) 1.6V - DVDD
- Power Down mode
- Monolithic CMOS
- 48pin LQFP (Pb Free)
- Temperature Range: -40 ~ 105°C

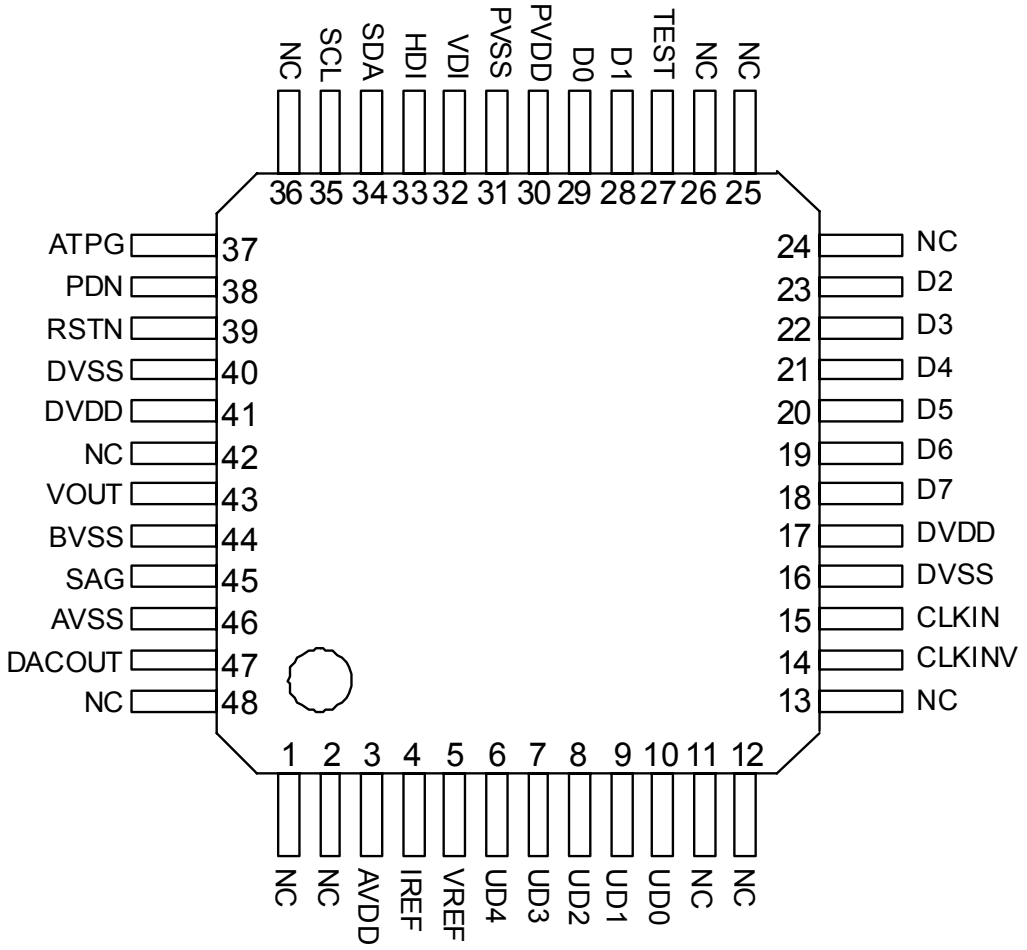
Block Diagram



Ordering Guide

AK8817VQ 48pin LQFP

Pin Assignment



Pin Functional Description

Pin#	Pin Name	I/O	Functional Outline
1	N.C.	-	For normal operation, left open.
2	N.C.	-	For normal operation, left open.
3	AVDD	P	Analog power supply pin.
4	IREF	O	IREF output pin. Connect this pin to Analog ground via a 12k ohm resistor (better than +/- 1% accuracy).
5	VREF	O	On-chip VREF output pin. AVSS level is output on this pin at PDN = L. Connect this pin to Analog Ground via a 0.1 uF or larger capacitor.
6	UD4	O	Test output pin. For normal operation, left open.
7	UD3	O	Test output pin. For normal operation, left open.
8	UD2	O	Test output pin. For normal operation, left open.
9	UD1	O	Test output pin. For normal operation, left open.
10	UD0	O	Test output pin. For normal operation, left open.
11	N.C.	-	For normal operation, left open.
12	N.C.	-	For normal operation, left open.
13	N.C.	-	For normal operation, left open.
14	CLKINV	I	Internal clock is inverted (internal operation timing edge is inverted.) Connect to either DVDD or DGND.
15	CLKIN	I	Clock input pin. Input a clock which is synchronized with data. When to input 601 data : 27 MHz. When to input square pixel data : 24.5454 MHz (NTSC)/ 29.50 MHz (PAL)
16	DVSS	G	Digital ground pin (digital core ground).
17	DVDD	P	Digital power supply pin (digital core power supply).
18	D7	I	Data Video Signal input pin (MSB). Hi-Z input is acceptable to this pin at PDN = L.
19	D6	I	Data Video Signal input pin. Hi-Z input is acceptable to this pin at PDN = L.
20	D5	I	Data Video Signal input pin. Hi-Z input is acceptable to this pin at PDN = L.
21	D4	I	Data Video Signal input pin. Hi-Z input is acceptable to this pin at PDN = L.
22	D3	I	Data Video Signal input pin. Hi-Z input is acceptable to this pin at PDN = L.
23	D2	I	Data Video Signal input pin. Hi-Z input is acceptable to this pin at PDN = L.
24	N.C.	-	For normal operation, left open.
25	N.C.	-	For normal operation, left open.
26	N.C.	-	For normal operation, left open.
27	TEST	I	For normal operation, connect to ground.
28	D1	I	Data Video Signal input pin. Hi-Z input is acceptable to this pin at PDN = L.
29	D0	I	Data Video Signal input pin (LSB). Hi-Z input is acceptable to this pin at PDN = L.
30	PVDD	P	Power supply pin for chip pad.

Pin#	Pin Name	I/O	Functional Outline
31	PVSS	G	Ground pin for PVDD.
32	VDI	I	Vertical SYNC signal input pin. Hi-Z input is acceptable to this pin at PDN = L.
33	HDI	I	Horizontal SYNC signal input pin. Hi-Z input is acceptable to this pin at PDN = L.
34	SDA	I/O	I2C data pin. This pin is pulled-up to PVDD. Hi-Z input is possible when PDN is at low. SDA input is not accepted during the reset sequence operation.
35	SCL	I	I2C clock input pin An input level of lower-than-PVDD should be input. Hi-Z input is possible when PDN is at low. SCL input is not accepted during the reset sequence operation.
36	N.C.	-	For normal operation, left open.
37	ATPG	I	For normal operation, connect to ground.
38	PDN	I	Power Down Pin. After returning from PD mode to normal operation, RESET Sequence should be done to AK8817VQ. “L “(GND level): Power-down “H “: normal operation
39	RSTN	I	Reset input pin. In order to initialize the device , an initialization must be made in accordance with the reset sequence. “L “ : reset “H “ : normal operation Hi-Z input is acceptable to this pin at PDN = L.
40	DVSS	G	Digital ground pin (digital core ground).
41	DVDD	P	Digital power supply pin (digital core power supply).
42	N.C.	-	For normal operation, left open.
43	VOUT	O	Video output pin.
44	BVSS	G	Substrate ground pin. Connect this pin to Analog ground
45	SAG	O	SAG Compensation Input pin
46	AVSS	G	Analog ground pin.
47	DACOUT	O	DAC output pin. Connect this pin to Analog ground via a 390 ohm resistor (better than +/- 1% accuracy).
48	N.C.	-	For normal operation, left open.

Analog Output pin status

MODE / PIN name	IREF	VREF	DACOUT	VOUT
PDN＝L	Hi-Z	Hi-Z	Hi-Z	Hi-Z
PDN=H、DAC=L VIDEOAMP=L	Output	Outpu	Hi-Z DAC Power Down	Hi-Z VIDEOAMP Power Down
PDN=H、DAC=H VIDEOAMP=L	Output	Output	Output	VIDEOAMP Power Down(1)
PDN=H、DAC=H VIDEOAMP=H	Output	Output	Output	Output

DAC: Sub Address 0x00 bit7 0: L->DACOFF 1: H->DACON
VIDEOAMP: Sub Address 0x01 bit3,4 00: L->VIDEOAMP_OFF 01,10: H-> VIDEOAMP_ON

Note1) Video Amp becomes power down. Since DACOUT pin and VOUT pin are connected with RESISTOR in the LSI, DACOUT pin are not Hi-Z. In case of using only DAC, VOUT pin and SAG pin should be open states.

Electrical Characteristics

(1) Absolute Maximum Ratings

Parameter	Min	Max	Units	Note
Supply voltage DVDD, AVDD, PVDD	-0.3	4.5	V	
Digital Input pin voltage (VinP)	-0.3	PVDD +0.3	V	D[7:0], HDI, VDI, RSTN, PDN, CLKIN, CLKINV,SCL, SDA
Input pin current (Iin)	-10	10	mA	Exclude Power supply pin.
Storage temperature	-40	125	°C	

(Note1)
Power supply voltages are values where each ground pin (DVSS = AVSS = PVSS) is at 0 V(voltage reference).
All power supply ground pins DVSS, AVSS and PVSS should be at same potential.

(2) Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units	Conditions
Supply voltage * AVDD,DVDD	2.7	3.3	3.6	V	AVDD = DVDD
Interface power supply PVDD	1.6	1.8	DVDD	V	
Operating temperature (Ta)	-40		105	°C	

* Power supply voltages are values where each ground pin (PVSS = AVSS = PVSS) is at 0 V(voltage reference).
All power supply ground pins DVSS, AVSS and PVSS should be at same potential.

(3) DC Characteristics

< Operating voltage: DVDD 2.7V~3.6V / PVDD 1.6 V~DVDD, loading condition 15 pF, temperature -40~+105°C >

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Digital input H voltage (VIH)	0.7PVDD 0.8PVDD			V	2.7V≦PVDD≦DVDD 1.6V≦PVDD＜2.7V	0.7PVDD 0.8PVDD
Digital input L voltage (VIL)			0.3PVDD 0.2PVDD	V	2.7V≦PVDD≦DVDD 1.6V≦PVDD＜2.7V	
Digital input leak current	IL			+/-10	uA	
I2C (SDA) L output	VOLC			0.4	V	IOLC = 3mA

(Note)
Digital output pins refer to D[7:0], HDI, VDI, PDN, RSTN, SCL, SDA,CLKIN and CLKINV pin outputs in general term.

(4) Analog Characteristics

< AVDD = 3.3 V, temperature 25 °C >

Parameter	Symbol	Min	Typ	Max	Units
DAC resolution		9		bit	
DAC integral non-linearity (error)		+/- 0.6	+/- 2.0	LSB	
DAC differential non-linearity (error)		+/- 0.4	+/- 1.0	LSB	
DAC output full scale voltage	1.18	1.28	1.38	V	Note1)
DAC output offset voltage			5.0	mV	Note2)
Video Amp Output Gain	5.0	6.0	7.0	dB	Amp Input Level 1Vpp
Video Amp Full scale Level		2.0		Vpp	Note3)
Video Amp THD	-45	-51		dB	100kHz - 5.5MHz Note4)
Video Amp S/N		54		dB	100kHz - 5.5MHz Note4)
LPF Ripple	-1	+/- 0.5	+1	dB	100kHz - 5.5MHz 0dB = 100kHz input
LPF Stop Band Level	20	30		dB	27MHz 0dB = 100kHz input
LPF Group Delay		10	100	ns	|GD3MHz - GD6MHz|
On-chip reference voltage (VREF)	1.17	1.23	1.30	V	
Reference voltage drift		-50		ppm/°C	

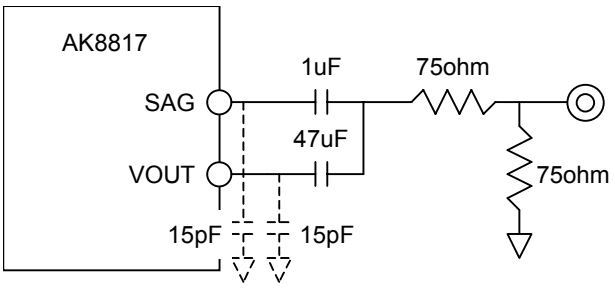
Note1) Values are when a 390 ohm output load, a 12k ohm IREF pin resistor and on-chip VREF are used.
Full scale output current is calculated as Iout = full scale output voltage (typ. 1.28 V) / 390 ohm = typ. 3.28 mA.
Note2) A voltage referenced to VSS when a decimal zero voltage is input to DAC.
Note3) VOUT Output Level Output Load Resistor: 150ohm, Load Capacitor: 15pF Internal Color Bar output
Note4) Output signal from DAC to which Input data corresponded 1Vpp. This signal is input to AMP.
Load resistor is 150ohm and Load capacitor is 15pF as shown bellow figure at (5) Current Consumption.

(5) Current consumption

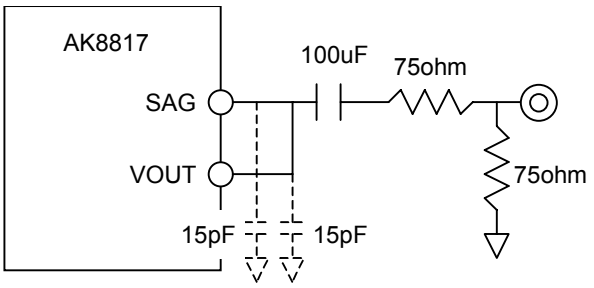
< Operating voltage : DVDD = AVDD = PVDD = 3.3 V, Ta = +25 °C >

Parameter	Symbol	Min	Typ	Max	Units
Total power consumption		29	38	mA	Note1)
Power-down current 1		10	30	uA	Note2)
Digital part operating current 1		15		mA	Note3)
Analog part operating current 1		14		mA	Note4)
Analog part operating current 2		5.5		mA	Note5)
Analog part operating current 3		0.8		mA	Note6)

Note1) operation at 27 MHz, NTSC mode on-chip 75% color bar output is enabled and Video Amp output is " on " (no external output loads are connected , other than those recommended, connecting-components).



SAG Compensation ON



SAG Compensation OFF

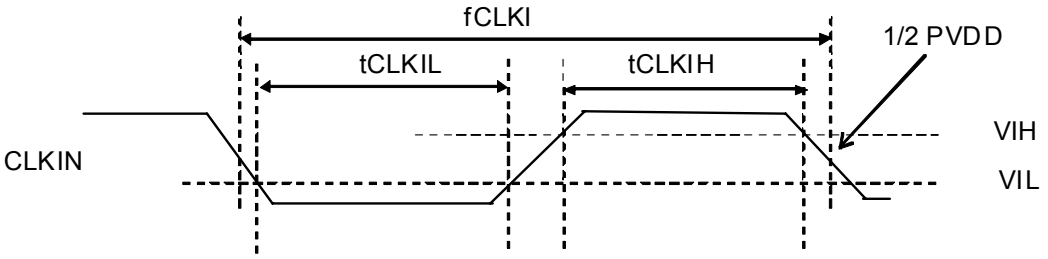
Note2) measuring conditions :
input / output settings after power-down sequence are, PDN pin is at GND level, CLKOUT and SDO output are at high level (power supply voltage) with no external connection, input voltage on those input pins is 1/2 level of power supply which are set to accept Hi-Z input at power-down, and TEST = ATPG = GND (or left open).
Power supplies are AVDD = DVSS = PVDD.
Each ground pin (DVSS, AVSS, PVSS) is always 0 V (voltage reference).

Note3) Operation at 27 MHz, NTSC mode on-chip 75% color bar output is enabled.
Note4) DAC ON, Video Amp On SAG Compensation On
Note5) DAC ON, Video Amp Off (SAG Compensation Off)
Note6) DAC Off, Video Amp Off (SAG Compensation Off)

AC Timing

< DVDD 2.7 V ~ 3.6 V / PVDD 1.6 V ~ DVDD, Ta at -40 ~ +105 °C > loading condition : CL = 15 pF

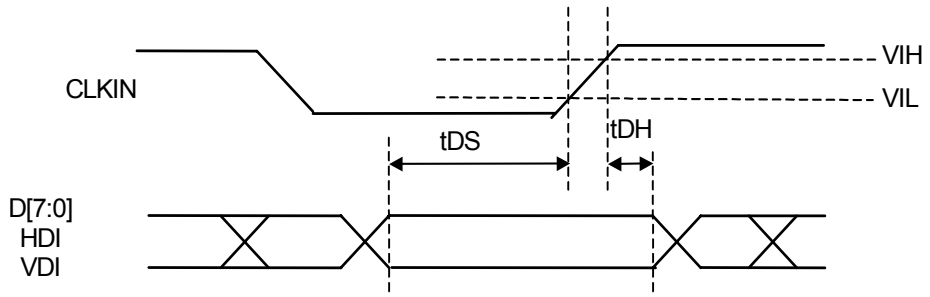
(1) CLK



Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions
CLKIN	fCLKI		24.5454		MHz	PIXRT=1 NTSC
			27			PIXRT=0 NTSC/PA
			29.50			PIXRT=1 PAL
CLK duty ratio	pCLKID	40		60	%	
CLK Accuracy				100	ppm	

tCLKIL, tCLKIH : minimum pulse width 12 nS (tr/tf10%-90%Level Rising/Falling time ≤ 2nS)

(2) Pixel Data Input Timing

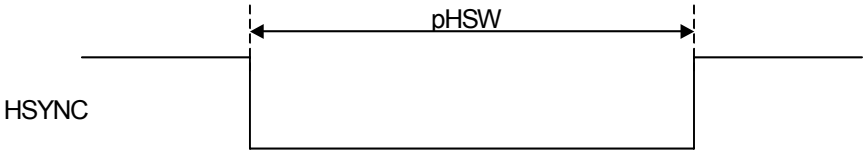


CLKINV = Low

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions
Data Setup Time	tDS	5			nsec	
Data Hold Time	tDH	8			nsec	

When CLKINV = High, similar tDS and tDH are specified at the falling edge of CLKOUT.

(3) HSYNC pulse width

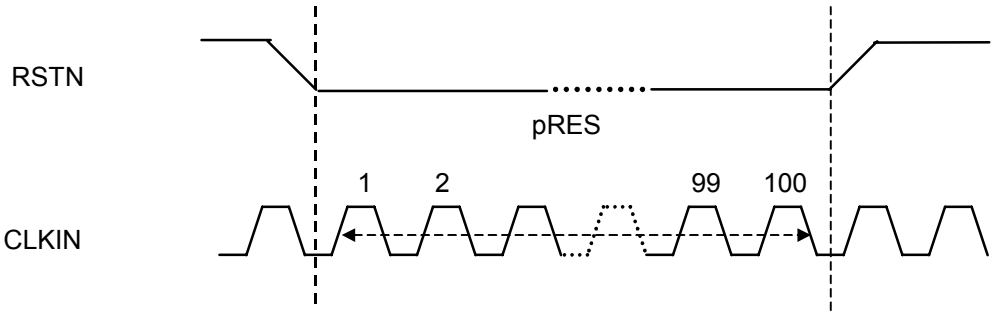


Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions
HDI Pulse Width	pHSW	15	116		CLKs	NTSC (24.5454MHz)
		15	128			27MHz
		15	139			PAL (29.50MHz)

* typical values are calculated by converting the HSYNC pulse width of Analog Video specification into number of system clock pulses.

(4) Reset

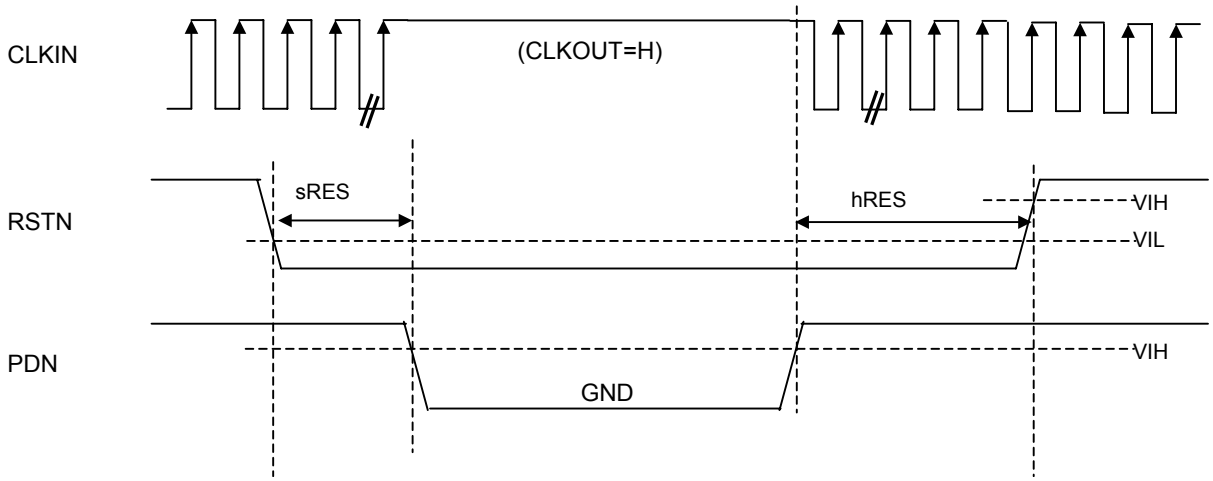
(4-1) Reset Timing



Parameter	Symbol	Min.	Typ.	Max	Unit
RSTN Pulse Width	pRES	100			CLKs

(4-2) Power Down Sequence / Reset Sequence

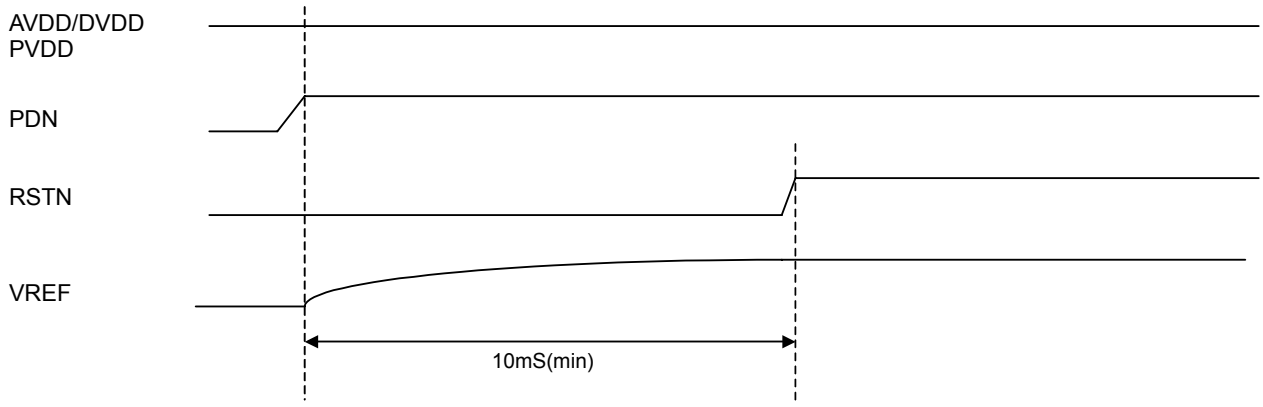
Before PDN setting (PDN to low), Reset must be enabled for a duration of longer-than-100 clock time.
After PDN release (PDN to high), Reset must be enabled for 10 mS or longer till analog part reference voltage & current are stabilized.



Parameter	Symbol	Min.	Typ.	Max	Unit
RSTN Pulse Width	sRES	100			CLKs
Time from PDN to high to RSTN to high	hRES	10			msec

At power-down, all control signals must be surely connected to either the selected power supply or ground level, and not to VIH / VIL levels.

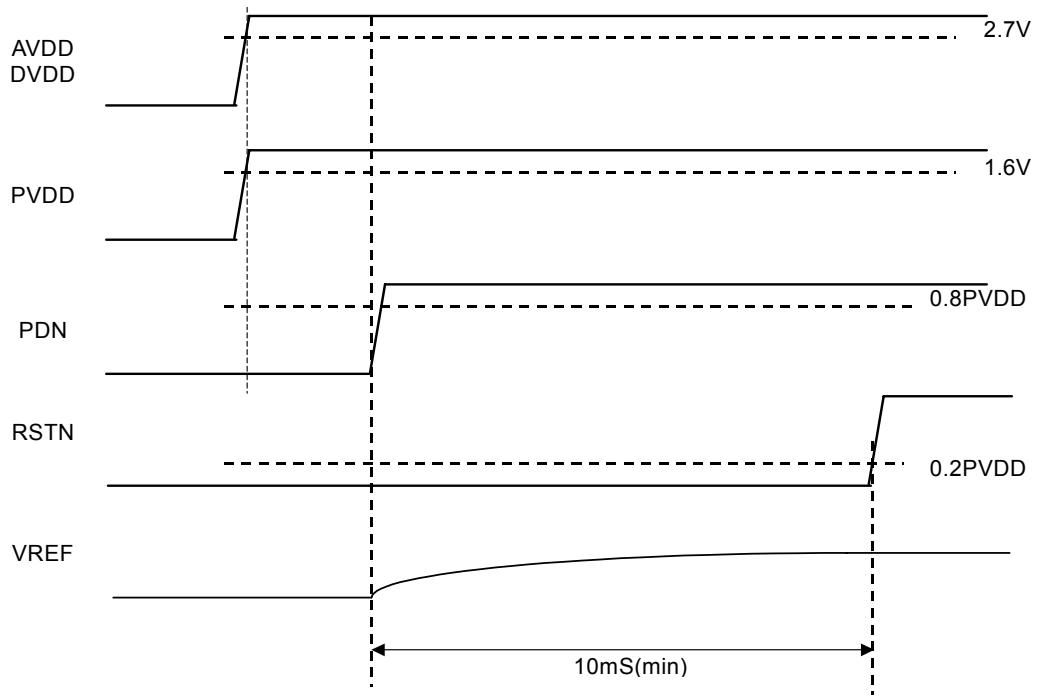
(4-3) Power Down Sequence/Power up sequence



Recover from Power Down state

(4-4) Power On Reset

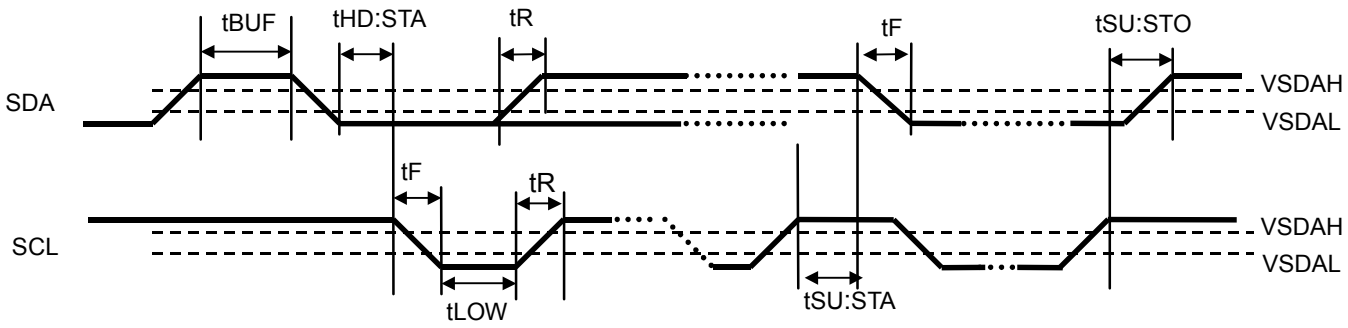
After Power up, It is necessary to make reset sequence until Analog Reference voltage(VREF) becomes stable.
PVDD/DVDD/AVDD should be power up at same time or 1st PVDD power up and AVDD/DVDD makes up.



item	Symbol	Min	Typ	Max	Unit	Note
RESETN Pulse width	pRES_PON	10			msec	

Remark: Reset sequence requires clock input.

(5) I2C Bus Input/Output Timing < Ta = -40 ~ +105 °C >

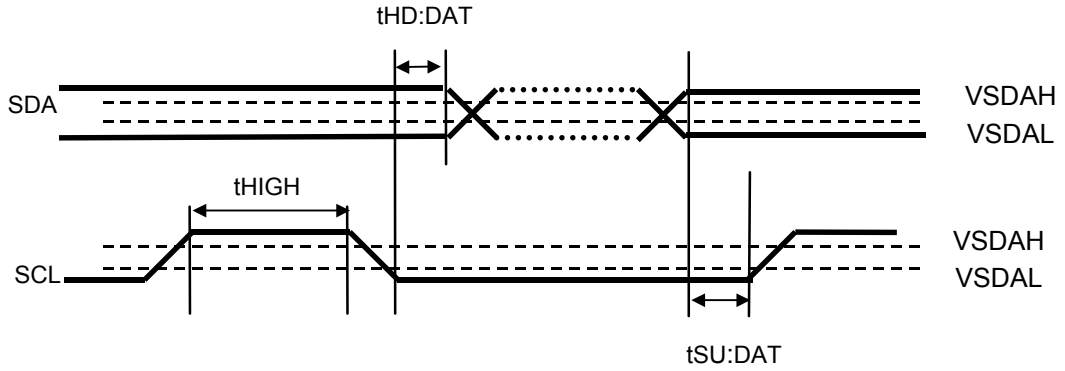


(5-1) Timing 1
VSDAH: 0.8PVDD
VSDAL : 0.2PVDD

Parameter	Symbol	Min.	Max.	Unit
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

The above I2C bus related timing is specified by the I2C Bus Specification, and it is not limited by the device performance. For details, please refer to the I2C Bus Specification.

(5-2) Timing 2



VSDAH: 0.8PVDD
VSDAL : 0.2PVDD

Parameter	Symbol	Min.	Max.	Unit
Data Setup Time	tSU:DAT	100 (note1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9 (note2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

note 1 : when to use I2C Bus Standard mode, tSU:DAT >- 250 ns must be met.
note 2 : when the AK8817VQ is used in such bus interface where tLOW is not extended (at minimum specification of tLOW), this condition must be met.

Device Control Interface

The AK8817VQ is controlled via I2C Bus Control Interface.

[I2C SLAVE Address]

2C Slave Address is **0x40**

[I2C Control Sequence]

(1) Write Sequence

When the Slave Address of the AK8817VQ Write mode is received at the first byte, Sub Address at the second byte and Data at the third and succeeding bytes are received.

There are 2 operations in Write Sequence - a sequence to write at every single byte, and a sequential write operation to write multiple bytes successively.

(a) 1 Byte Write Sequence

S	Slave Address	w	A	Sub Address	A	Data	A	Stp
	8-bits		1bit	8-bits	1bit	8-bits	1bit	

(b) Multiple Bytes (m-bytes) Write Sequence *(Sequential Write Operation)*

S	Slave Address	w	A	Sub Address (n)	A	Data(n)	A	Data(n+1)	A	….	Data(n+m)	A	stp
	8-bits		1bit	8-bits	1bit	8-bits	1bit	8-bits	1bit		8-bits	1bit	

(2) Read Sequence

When the Slave Address of the AK8817VQ Read mode is received, Data at the second and succeeding bytes are transmitted.

S	Slave Address	w	A	Sub Address (n)	A	rS	Slave Address	R	A	Data1	A	Data2	A	Data3	A	…	Data n	Ā	stp
	8-bits		1	8-bits	1		8-bits		1	8-bits	1	8-bits	1	8-bits	1		8-bits	1	

Abbreviated terms listed above mean :

S, rS : Start Condition
A : Acknowledge (SDA Low)
A- : Not Acknowledge (SDA High)
stp : Stop Condition
R/W 1 : Read 0 : Write

: to be controlled by the Master Device. Micro-computer interface is output normally .
: to be controlled by the Slave Device. To be output by the AK8817VQ.

Video Encoder Functional Outline

(1) Reset

(1-1) Reset of Serial Interface part (asynchronous reset)

Reset is made by setting RSTN pin to low.

(1-2) Reset of other than Serial Interface blocks

Reset is made by keeping RSTN pin low for a longer than 100 clock time, in normal operation.

(1-3) at Power-On-Reset (including power-down release case)

Follow the power-on-reset sequence.

At the completion of each initialization, all internal registers are set to default values (refer to Register Map). Right after the reset, Video output of the AK8817VQ is put into Hi-Z condition.

(2) Power-Down

It is possible to put the device into power-down mode by setting the AK8817VQ power-down pin to GND.

Transition to power-down mode should be followed by the power-down sequence. As for the recover from the power-down mode, it should be followed by the power-down release sequence.

(3) Master Clock

A following clock should be input as a Master clock.

In Encoder Mode operation (a synchronized clock with input data is required)

	When ITU-R BT.601 data is input (PIXRT-bit = 0)	When Square Pixel data is input (PIXRT-bit = 1)
NTSC Encoder	27MHz	24.5454MHz
PAL Encoder	27MHz	29.50MHz

(4) Video Signal Interface

Video input signal (data) should be synchronized in either of the following methods :

* Slave mode operation where synchronization is made with HSYNC (HDI) / VSYNC (VDI).
* ITU-R BT. 656 I / F (EAV decode) (only 27MHz operation)

(5) Pixel Data

Input data to the AK8817VQ is YCbCr (4:2:2).

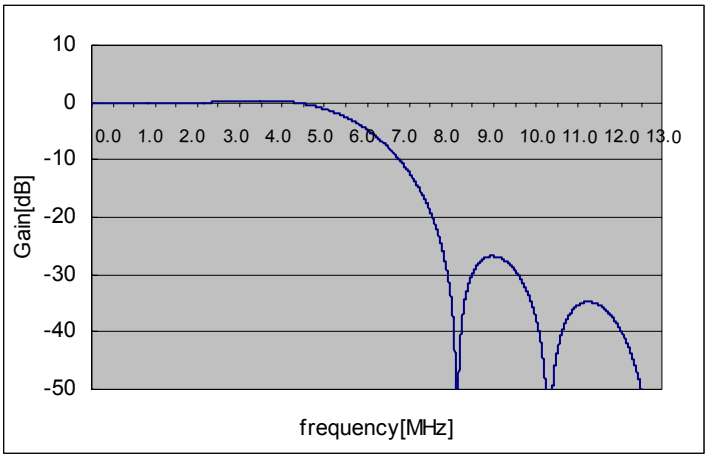
Data with Y : 16 ~ 235 and CbCr : 16 ~ 240 should be input.

(6) Video Signal Conversion

Video Re-Composition module converts the multiplexed data (ITU-R BT.601 Level Y, Cb, Cr) into interlaced NTSC-M and PAL-B, D, G, H, I data. Video encoding setting is done by “Control 1 Register “.

(7) Luminance Signal Filter (Luma Filter)

Luminance signal is output via LPF (see x2 Luma Filter in the block diagram).



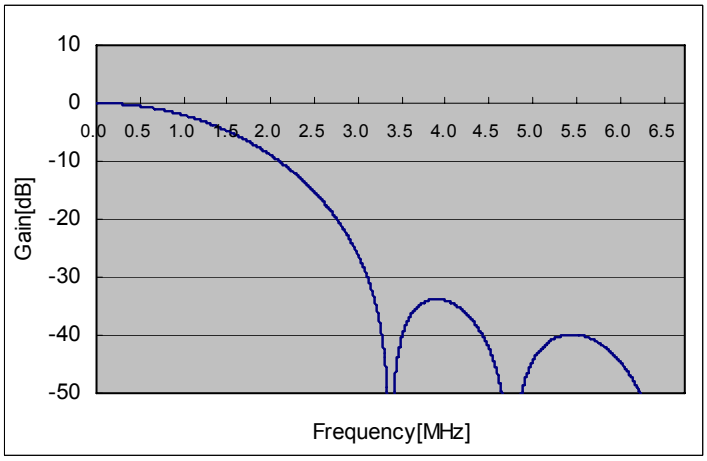
(8) Chroma Signal Filter (Chroma Filter)

Chroma input signal components (Cb, Cr) prior to the modulation go through a 1.3 MHz Band Limiting Filter (see 4:2:2 to 4:4:4 x2 interpolator in the block diagram).

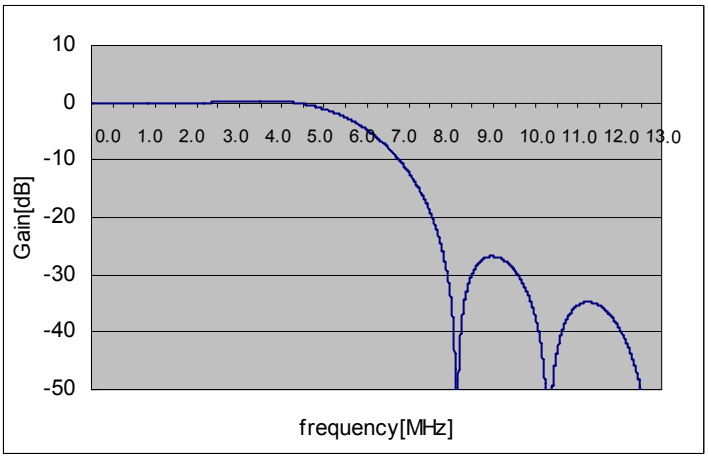
Chroma signal which is modulated by the sub-carrier is output via a low pass filter (Chroma LPF in the block diagram).

Frequency response of each filter is shown below.

4:2:2 to 4:4:4 Interpolator Filter



x 2 Interpolator Filter



(9) Color Burst Signal

Burst signal is generated by a 32 bit digital frequency synthesizer.
Color Burst Frequency is selected by mode setting of NTSC / PAL.

Standerd	Subcarrier Freq (MHz)	Video Process 1 VMOD-bit
NTSC-M	3.57954545	0
PAL-B,D,G,H,I	4.43361875	1

Burst Signal Table

(10) Sub - Carrier Reset

A function to reset sub-carrier by Color Frame sequence.
Reset function can be turned “OFF “ by setting SCR-bit of Control 1 Register.
Default value is set to enable Sub-carrier reset.

SCR	0	1
NTSC	Sub-carrier phase is reset in every 2 Frames (4 Fields)	Sub-carrier reset is not done
PAL	Sub-carrier phase is reset inevery 4 Frames (8 Fields)	Sub-carrier reset is not done

(11) Setup processing

Setup processing can be performed on Video signal by Control 2 Register Setup-bit.
Following processing is made on Luminance signal (Y signal) and Chroma signal (C signal) by the Setup processing.

Y Setup = Y x 0.925 + 7.5 IRE where Y setup is the Luminance signal after Setup processing.
C Setup = C x 0.925 where C Setup is the Chroma signal after Setup processing.

(12) Video DAC

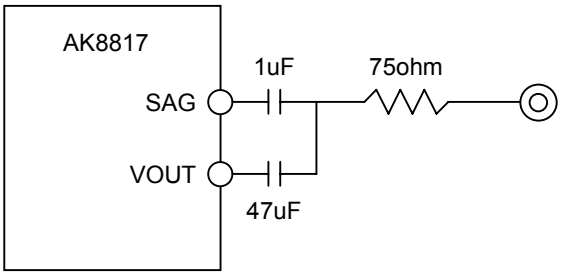
The AK8817VQ has a 9 Bit resolution, current-drive DAC as a video DAC which runs at 29.5 / 24.5454 MHz or 27.00MHz clock frequency.
This DAC is designed to output 1.28 V o-p at full scale under the following conditions loading resistance of 390 ohms, VREF at 1.23 V and IREF pin resistor of 12k ohms.
[VREF] pin should be connected to ground via a 0.1 uF or larger capacitor.
DAC output can be turned “ON” or “OFF” by register setting and current consumption can be lowered.
When the output is turned off, it is put into high impedance condition.

(13) Video Amp

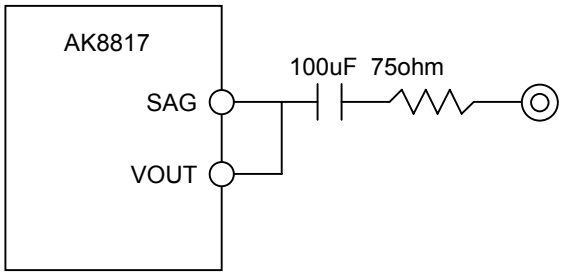
AK8817VQ has Video amp that can drive 150ohm with Low pass filter. It can also possible to compensate SAG distortion. To compensate SAG external capacitor is 47uF and 1uF as shown following figure. Recommendation voltage when SAG compensation circuit is used is 3V or more.

VOUT pin and SAG pin should be shorten when SAG Compensation is not used. Output pin should make AC coupling. SAG Compensation circuit can be set on or off with setting register.

In case of not using internal Video amp (Only DAC use case), Video Amp becomes power down. In this case SAG and VOUT should be Open.



SAG Compensation ON

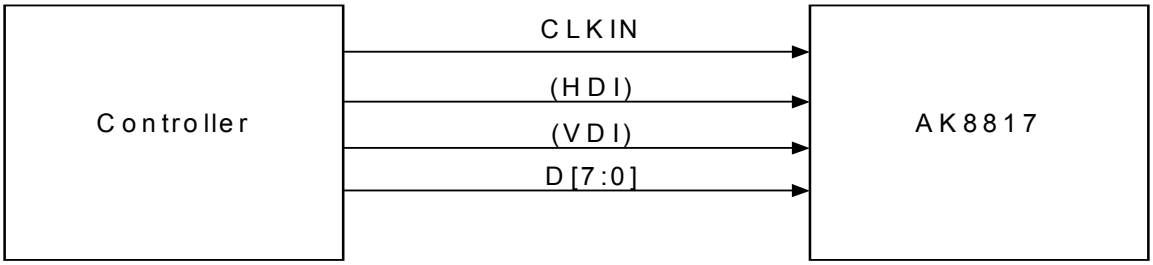


SAG Compensation Off

VAMPMD[1:0]	Operation	Conditions
00	Video Amp OFF + SAG Compensation OFF	Only DAC output
01	Video AMP ON + SAG Compensation ON	Recommendation Voltage of DVDD/AVDD is 3v or more.
10	Video Amp ON + No SAG Compensation	SAG pin and VOUT should be shorten.
11	Reserved	

(14) Video Data Interface Timing

Data is captured by a clock which is fed on CLKIN pin.
The Video Encoder receives a clock from a controller (refer to the following diagram).
In Slave mode operation, Synchronization is made with HDI / VDI.
In ITU-R BT.656 mode operation, HDI / VDI are not required.



(14-2) Video Interface mode

The AK8817VQ synchronizes with input signal by the following, 2 interface modes.

(a) Slave-mode interface where synchronization is made with externally-fed synchronization signals HDI / VDI (HDI / VDI interface)

(b) ITU-R BT.656 Interface mode (656 interface)

interface mode setting is controlled by [REC656]-bit of Control 2 Register.

REC656-bit	Operation
0	HDI / VDI Slave mode
1	ITU-R BT.656 Interface mode

(a-1) Timing signal (HDI / VDI) VS Data input relation

Horizontal Synchronization (in-line Pixel Sync) is made with HDI synchronization timing signal.

Vertical Synchronization (in-line Frame Line Sync) is made with VDI synchronization timing signal.

Recognition of Video Field (Odd Field or Even Field) is made by VDI input signal which is referenced with HDI.

In normal operation, the AK8817VQ checks changes of HDI and VDI at the clock edge (CLK synchronization) which becomes a data capture reference position.

At a pixel position where HDI is judged to become " Low ", it is recognized as 0_H (zero th position).

Cb0 data position depends on input data rate (ITU-R BT.601 or Square Pixel data).

Cb0 Data

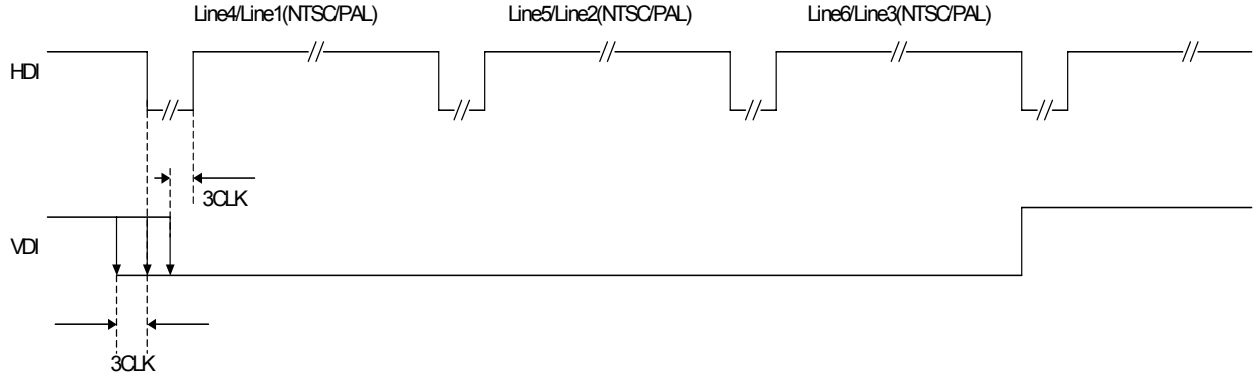
	At ITU-R BT.601 Data input	At Square Pixel data input
NTSC Encoder	244^{th} data	236^{th} data
PAL Encoder	264^{th} data	310^{th} data

Video Field is recognized by the VDI relation with HDI.

Field recognition is made as follows :

The AK8817VQ distinguishes at every Field if it is Odd Field (1^{st} Field) or not. Even Field Sync signal is not usually input.

1) Recognition timing of Odd Field is decided by those timing signal relations which are fed on HDI and VDI pins. When the VDI falling pulse is input on VDI input pin during the time from 3 clocks prior to the falling edge of HDI timing pulse which is fed on HDI input till 3 clocks prior to the rising edge of HDI timing pulse, the Line is recognized to be Line 4.



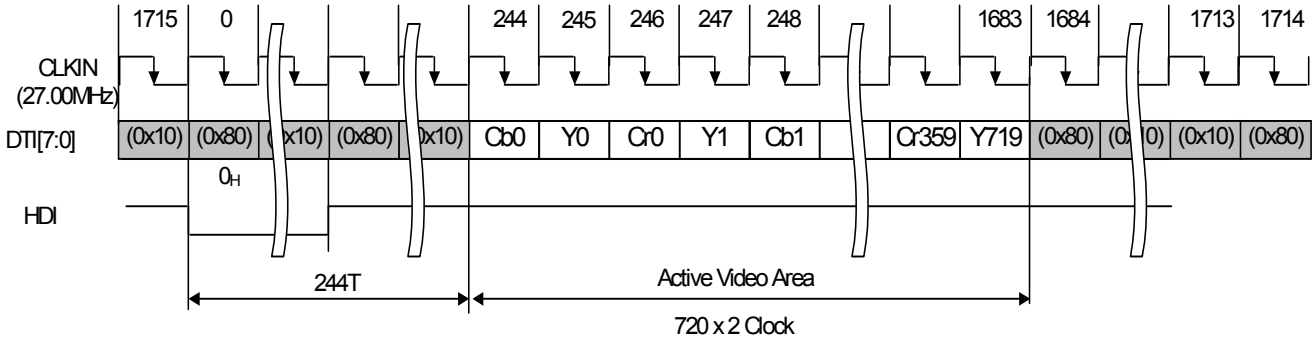
2) Whenever Horizontal / Vertical SYNC signal inputs are not fed as expected in the Video Specifications, in term of timing and # of pulses (kept at " High " level), the AK8817VQ continues to self-run the operation which is based on the Sync signals, fed just before.

But it is recommended to feed Sync signals as specified every time in order to prevent erroneous operation.

3) VD pulse input at other than Odd Field synchronization is ignored (Synchronization is made with Odd Field only).

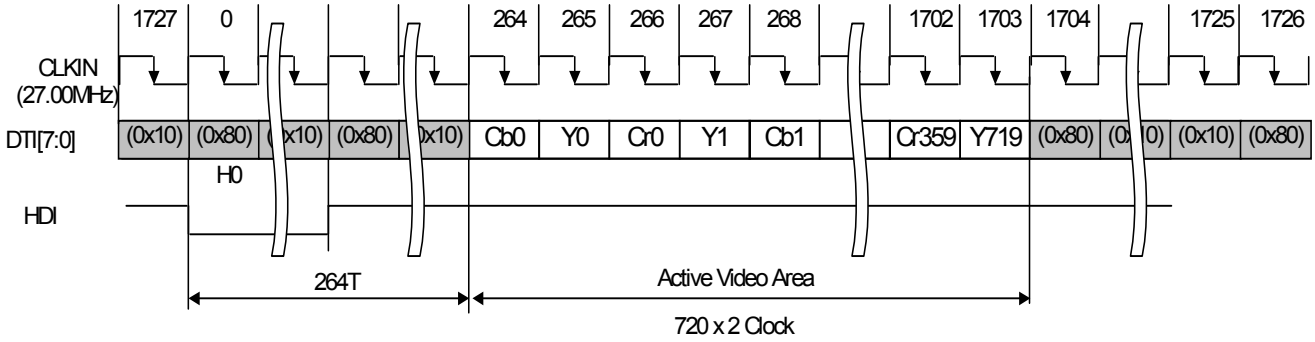
(a-2) Horizontal Synchronization (Pixel Data synchronization within a Line)

(a-2-1) at ITU-R BT. 601 data input case
(a-2-1-1) NTSC



*) when D [7:0], HDI and CLKIN are in same phase relation as a timing example above, the AK8817VQ takes input data at
the falling edge of each CLKIN if CLKEDGE-bit = 1.(CLKINV = 1.)
*) as an input data other than during active video period, Black level (C / Y = 0x80 / 0x10) or other than 0x00 / 0xFF codes in non Hi-Z state should be input.

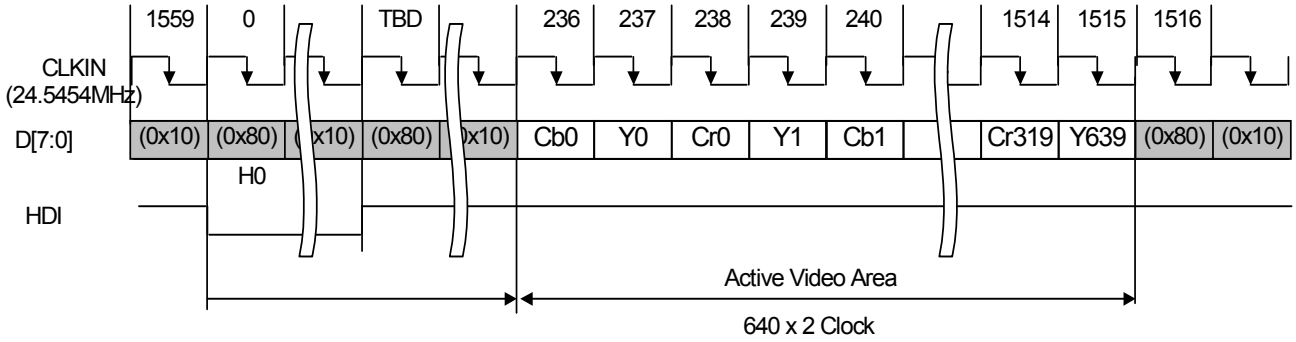
(a-2-1-2) PAL



*) when D [7:0], HDI and CLKIN are in same phase relation as a timing example above, the AK8817VQ takes input data at the falling edge of each CLKIN if CLKEDGE-bit = 1. .(CLKINV = 1.)
*) as an input data other than during active video period, Black level (C / Y = 0x80 / 0x10) or other than 0x00 / 0xFF codes in non Hi-Z state should be input.

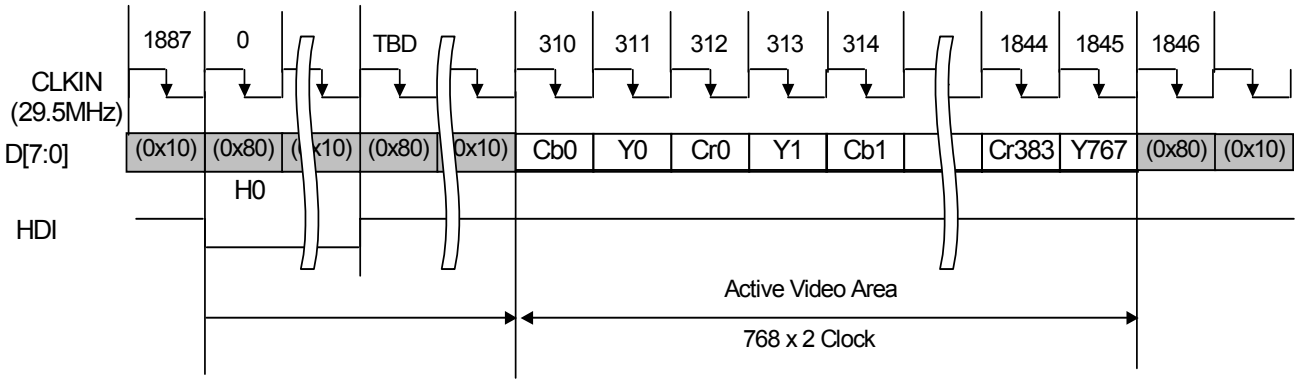
(a-2-2) at Square Pixel Rate input case

(a-2-2-1) NTSC



*) when D [7:0], HDI and CLKIN are in same phase relation as a timing example above, the AK8817VQ takes input data at
the falling edge of each CLKIN if CLKINV = 1.
*) as an input data other than during active video period, Black level (C / Y = 0x80 / 0x10) or other than 0x00 / 0xFF codes in non Hi-Z state should be input.

(a-2-2-2) PAL

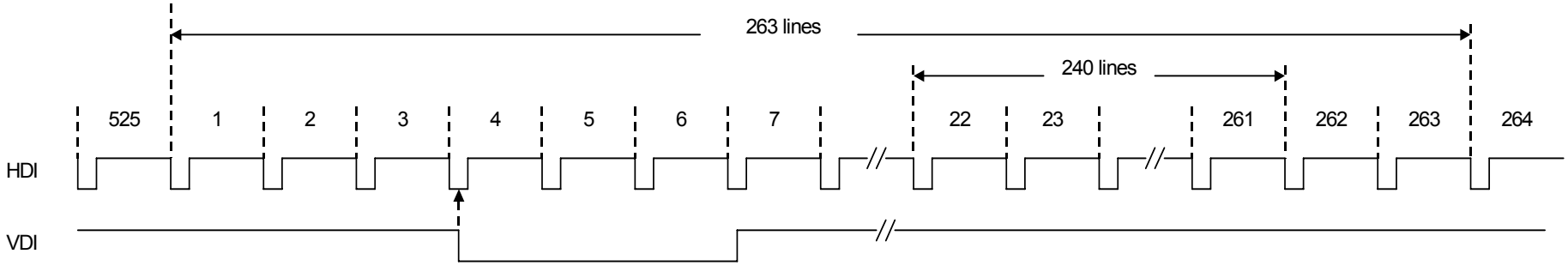


*) when D [7:0], HDI and CLKIN are in same phase relation as a timing example above, the AK8817VQ takes input data at
the falling edge of each CLKIN if CLKINV-bit = 1. .(CLKINV = 1.)
*) as an input data other than during active video period, Black level (C / Y = 0x80 / 0x10) or other than 0x00 / 0xFF codes in non Hi-Z state should be input.

(a-3) HDI and VDI relation in each Frame

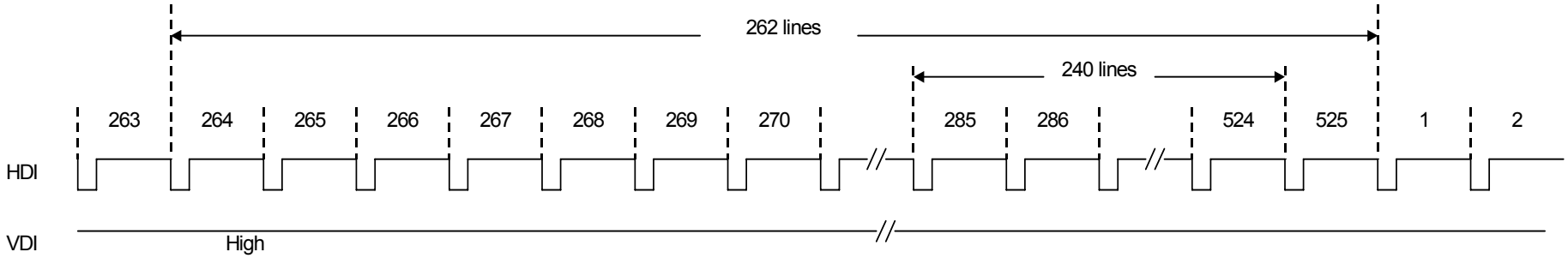
(a-3-1) NTSC (Frame) 525 Line 480 active lines

The First Field (ODD)



*)VDI negative-going should be fed during the time from 3 clocks prior to negative-going of HDI at L4 till 3 clocks prior to positive-going of HDI.
VDI positive-going can occurs at arbitrary location, but keep VDI low for 3 line duration time as a rough idea.

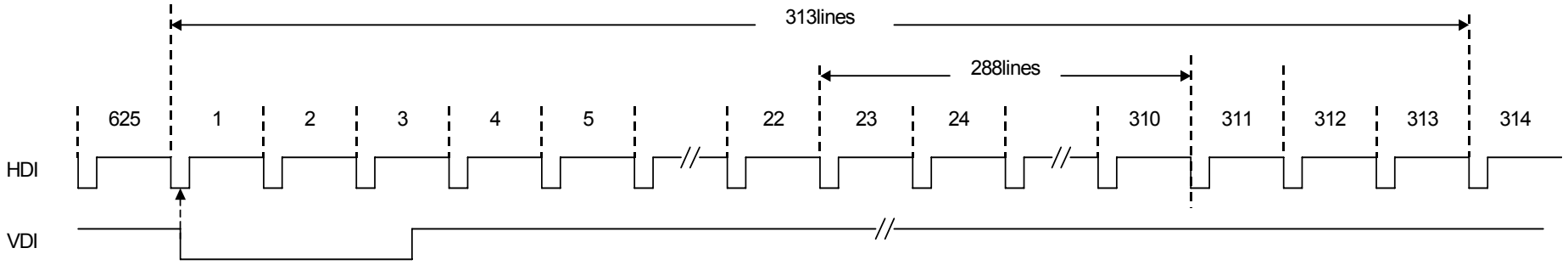
The Second Field (EVEN)



*) VDI negative-going is not required for the Second Field. It is required for the First Field only (VDI fed during the Second Field is ignored).

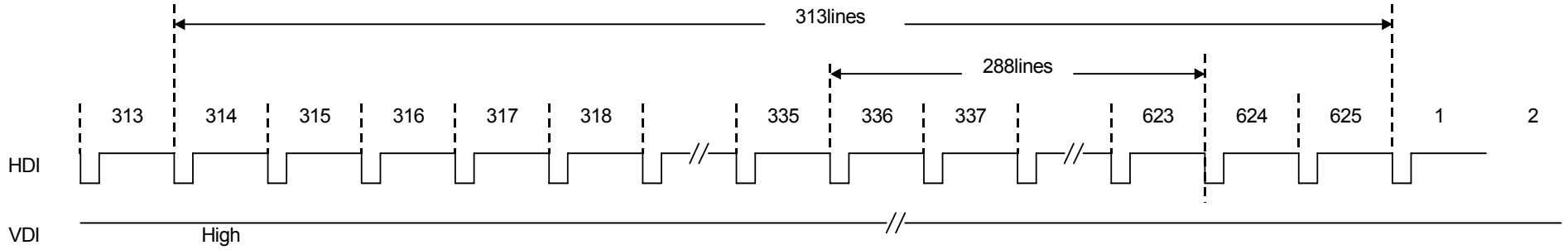
(a-3-2) PAL (Frame) 625 Line 576 active lines

The First Field (ODD)



*) VDI negative-going should be fed during the time from 3 clocks prior to negative-going of HDI at L1 till 3 clocks prior to positive-going of HDI.
VDI positive-going can occur at arbitrary location, but as a rough idea, keep VDI low for 2.5, or 2 or 3 line- duration time.
Data fed at Line 23 is not output on Video output

The Second Field (EVEN)



*) VDI negative-going is not required for the Second Field. It is required for the First Field only (VDI fed during the Second Field is ignored).
Data fed at Line 623 is not output.

(b-1) ITU-R BT.656 Interface mode

The AK8817VQ makes a synchronization with an incoming signal by decoding EAV in the signal when ITU-R BT.656 encoded signal is input.

EAV code is located at the following position in the Video stream (this mode of operation is not supported in the Square Pixel clock operation).

	EAV										SAV													
Y/Cb/Cr	Cb	Y	Cr	Y	Cb	Y	Cr	Y			Cb	Y	Cr			Y	Cb	Y	Cr	Y	Cb	Y	Cr	Y	Cb
Data# 525system	360	720	360	721	361	722	361	723			368	736	368			855	428	856	428	857	0	0	0	1	1
Data# 625system	360	720	360	721	361	722	361	723			366	732	366			861	431	862	431	863	0	0	0	1	1