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AsahiKASEI
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AK8826VN

HD/SD Multi Format Video Encoder with 3ch DAC

General Description

The AK8826 is a HD/SD TV Video Encoder with onchip 3-channel 10bit DAC.

As input data, in SDTV encoder mode, SMTE-125M / ITUR-R.BT601, 656 compatible Y/Cb/Cr 4:2:2 formats (8bit) are accepted and in HDTV encoder mode, SMPTE-274M (1080i), SMPTE296M (720p) compatible Y/Cb/Cr 4:2:2 formats (8bit x 2) are accepted.

As input data capture method, either a Synchronous mode to be made by detecting encoded EAV signal or a mode to synchronize with externally-fed H/V SYNC signal is selectable.

Outputs of CVBS / SDY / SDC and HDY / HDPB / HDPR and R / G / B analog signal can be output exclusively.

VBI signal can be also superimposed on output in addition to Video signals by register setting.

AK8826 supports I2C compatible interface as Micro-Processor interface.

Features

Component Video Encoder

- Compatible Input Data
  - SMPTE125M-1995 / ITU-R BT601 (525i/625i)
  - SMPTE293M-1996 / ITU-R BT1358 (525p/625p)
  - SMPTE274M-1998 (1080i)
  - SMPTE296M-2001 (720p)
- Input Signal Format (525i / 625i, 525p / 625p, 1080i, 720P)
  - Y/Cb/Cr 4:2:2 (8bit x 1: 525i/625i)
  - Y/Cb/Cr 4:2:2 (8bit x 2: 525p/625p/1080i/720p)
  - RGB 6:6:6
  - RGB 5:6:5
- Input Clock
  - 27MHz (525i / 625i / 525p / 625p) / 74.25MHz (1080i/720p)
- Output Signals
  - Y/Pb/Pr Interlace
  - Y/Pb/Pr Progressive
  - (EIA 770.2, EAI 770.3)
- Input Signal Synchronization
  - ITU-R.BT 656 I/F (EAV Decode)
  - Slave operation by HSYNC / VSYNC
    - (525i: ITU-R. BT601 Compatible 625i / 525p / 625p / 1080i / 720p; CEA-861-D Compatible)
- VBID (CGMS-A), CC/XDS, WSS, CEA-805-B (Type A/B)
- Internal Color bar Generator
- Internal Black Burst Generator
- Adjustable Y / Pb / Pr Delay Function

NTSC / PAL Composite Video Encoder

- NTSC-M, PAL-B, D, G, H, I. M, N Encoding
- Composite Video Output / S-Video Output
- Compatible Input Data
  - SMPTE125M-1995 / ITU-R BT601(525i/625i) Y/Cb/Cr 4:2:2 (8bit x 1)
  - RGB 6:6:6
  - RGB 5:6:5
- Input Signal Synchronization
  - ITU-R.BT 656 I/F (EAV Decode)
  - Slave operation by HSYNC / VSYNC
    - (525i / 625i: ITU-R. BT601 Compatible)
- Input Clock
  - 27MHz
- VBID(CGMS-A), CC/XDS, WSS

RGB Video DAC
- RGB output
- Input Data Format
  RGB 6:6:6
  RGB 5:6:5
- Input Clock
  54MHz (max)

Common Specification
- 10bit DAC x 3ch (max operating speed 150MHz)
- I^2C BUS I/F (400kHz) compatible
- Power Down mode
- Internal VREF Circuit
- 3.0V / 1.8V VCC
- 48pin QFN (7.2mm x 7.2mm)

1. Block Diagram

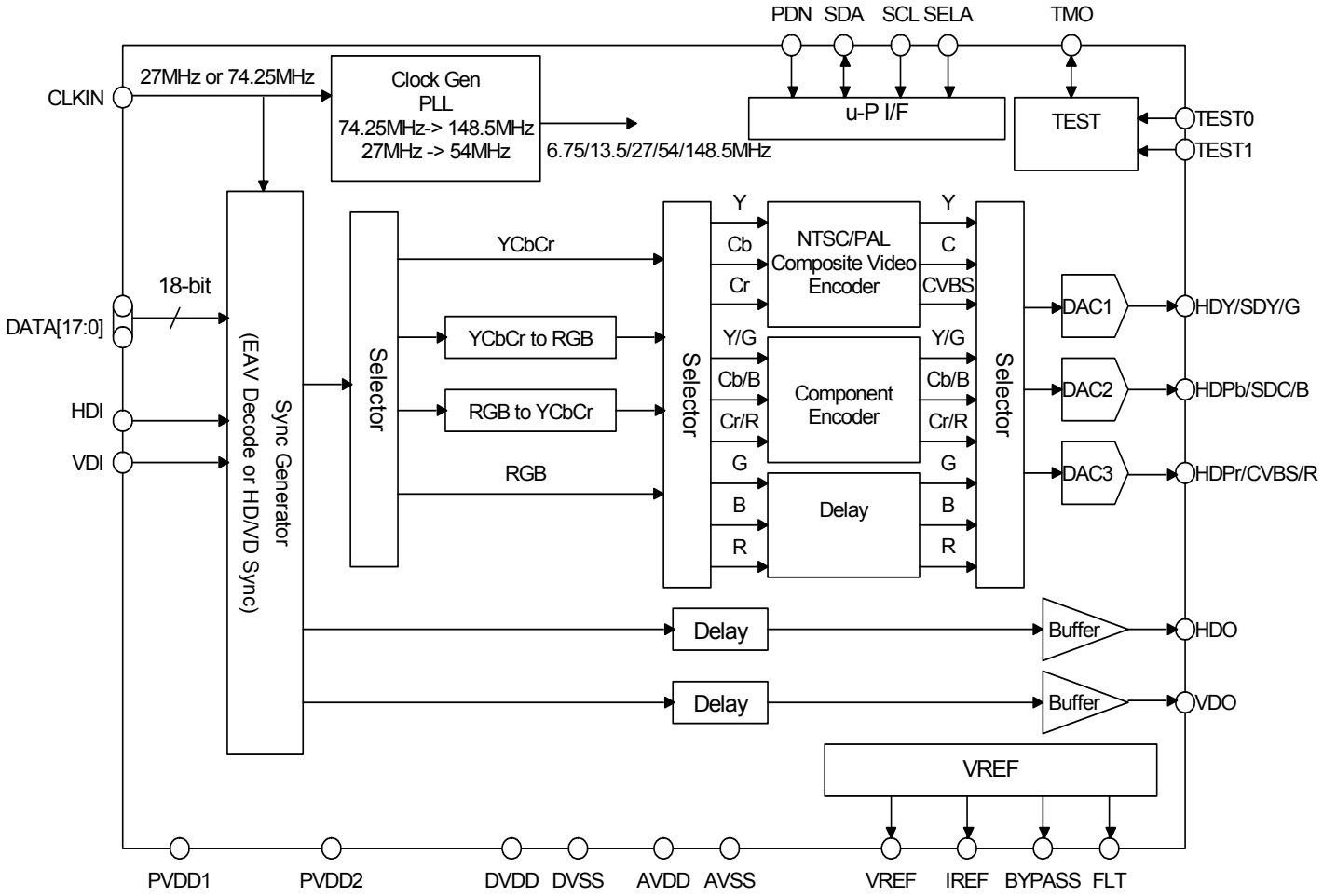

Fig. 1 Block Diagram

With Register setting, AK8826 works as
- Multi-Format Component Video Encoder (Component Video Encoder)
- NTSC/PAL Composite Video Encoder (Composite Video Encoder)
- High Speed Video DAC

1-1. Component Video Encoder Block

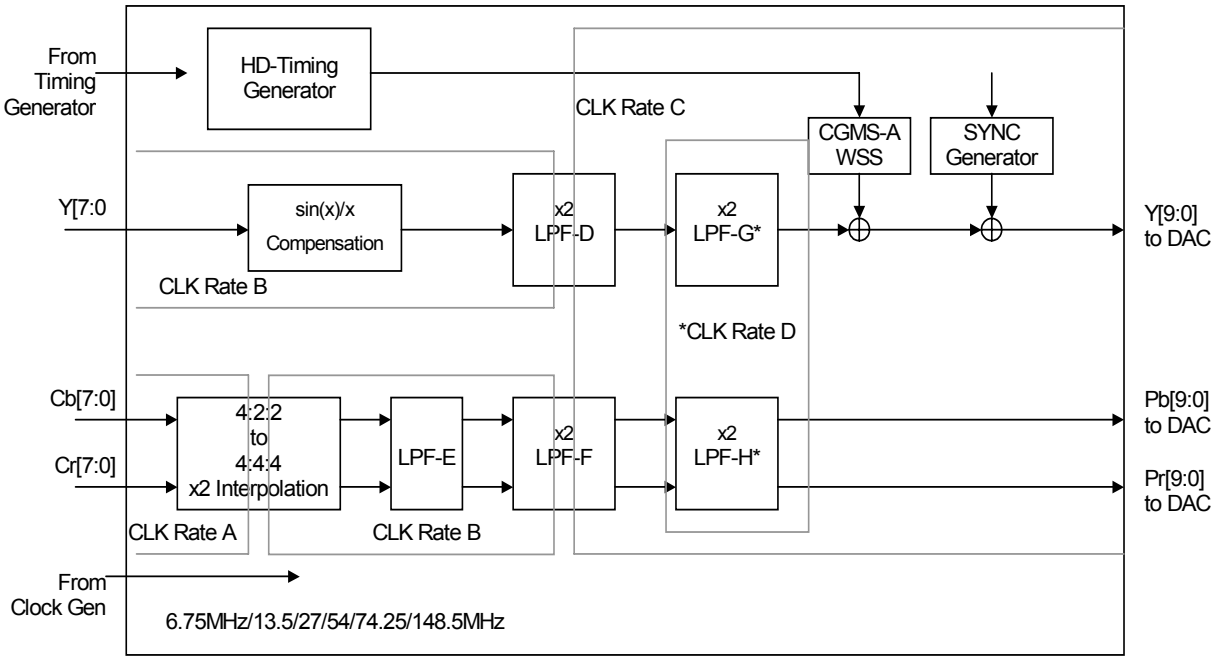

Fig. 2 Component Video Encoder Block

This Block described as Component Video Encoder Block in this datasheet.
CLK Rate D is only a case of D1(525i/625i) mode.

Clock Rate

	D1(525i /625i)	D2(525P / 625P)	D3/D4(1080i/720P)
CLK Rate A	6.75MHz	13.5MHz	37.125MHz
CLK Rate B	13.5MHz	27MHz	74.25MHz
CLK Rate C	27MHz	54MHz	148.5MHz
CLK Rate D	54MHz	-	-

1-2. NTSC/PAL Composite Video Encoder Block

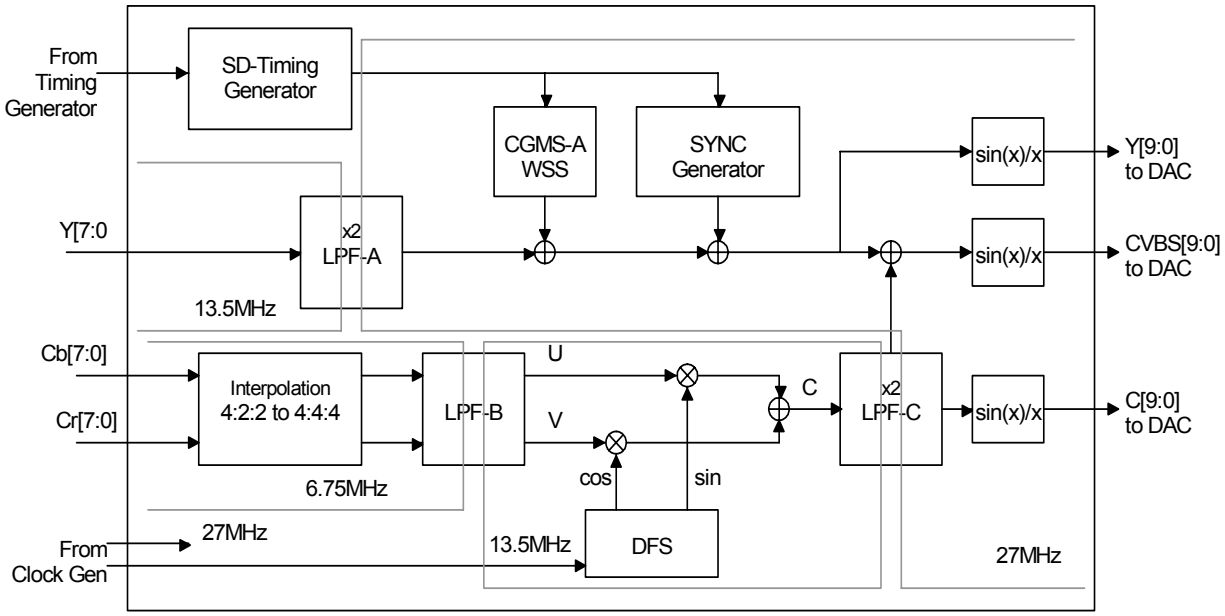

Fig. 3 Composite Video Encoder Block

This Block described as Composite Video Encoder Block in this datasheet.

1-3 High Speed Video DAC mode

AK8826 can be used as High Speed Video DAC. This mode is described as Video DAC mode in this datasheet.

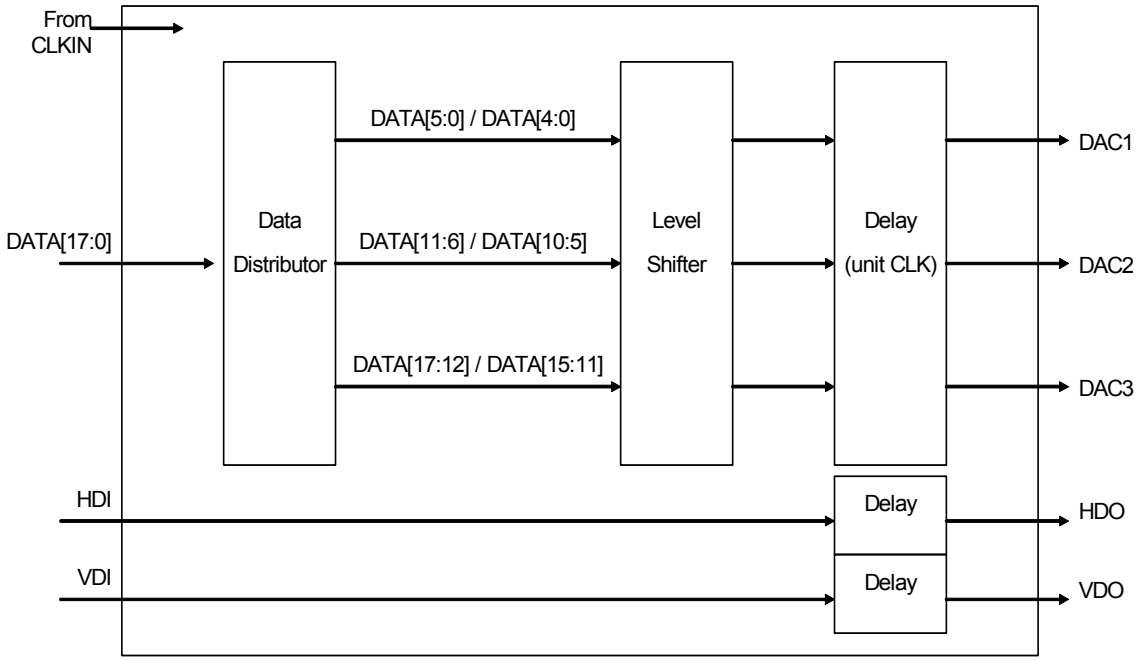

Fig. 4 High Speed Video ADC Block

1-4. CLK Gen Block

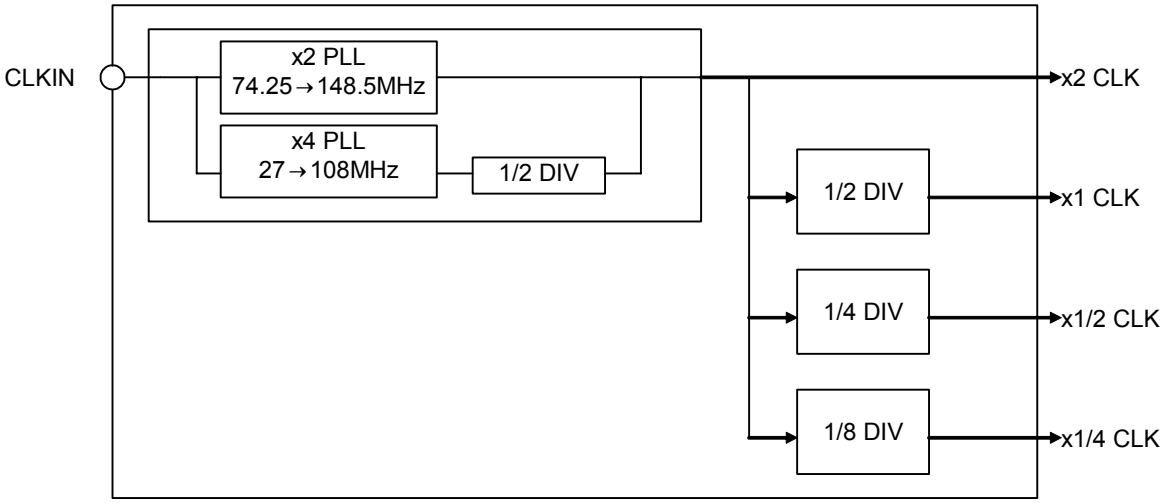

Fig. 5 CLK Gen Block

Clock Rate

	D1(525i /625i)	D2(525P / 625P)	D3/D4(1080i/720P)
x1/4 CLK	6.75MHz	-	-
x1/2 CLK	13.5MHz	13.5MHz	37.125MHz
x1 CLK	27MHz	27MHz	74.25MHz
x2 CLK	54MHz	54MHz	148.5MHz

Notice Information
In this document, relations of the word are shown as following table

Number of Lines in Frame	Description in this datasheet
525 Interlace	525i or 480i or D1
625 Interlace	625i or 576i or D1
525 Progressive	525p or 480p or D2
625 Progressive	625p or 576p or D2
1125 Interlace	1125i or 1080i or D3
750 Progressive	750p or 720p or D4

2. Ordering Guide

AK8826VN 48 pin QFN

3. Pin Assignment

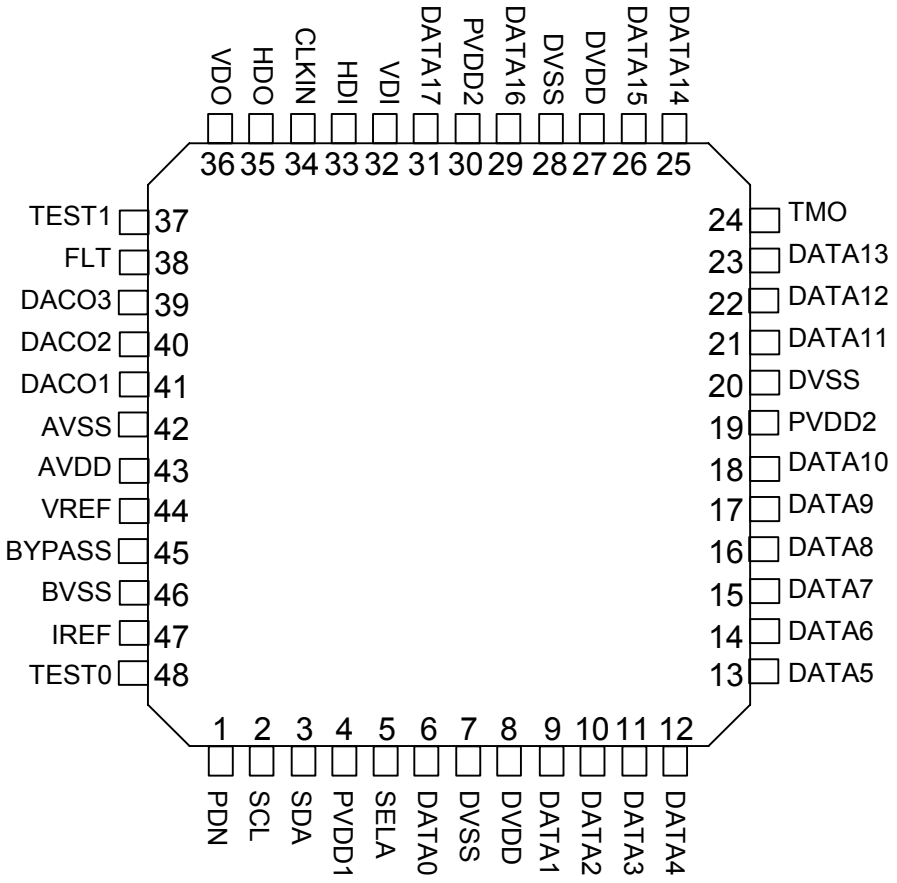

Fig. 6 Pin Layout (TopView)

4. Function of Pins

pin#	Pin Name	power	I/O	Function
1	PDN	P1	I	Control Pin for Power Down and Reset. AK8826 is initialized with PDN = Low. AK8826 becomes Power down states during PDN=Low Normal operation mode, PDN pin should be High. This pin is Prohibited to be Hi-z States
2	SCL	P1	I	I2C BUS clock input pin. Pulled up externally.
3	SDA	P1	I/O	I2C Bus Data Input Pin. Pulled up externally.
4	PVDD1	P1	P	Power supply pin for I/O(PDN, SDA, SCL, SELA)
5	SELA	P1	I	I2C BUS Address select pin. Fixed to PVSS1 or PVDD1.
6	DATA0	P2	I	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
7	DVSS	D	G	Ground pins for Digital.
8	DVDD	D	P	Power supply pins for Digital.
9	DATA1	P2	I	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
10	DATA2	P2	I	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
11	DATA3	P2	I	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
12	DATA4	P2	I	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
13	DATA5	P2	I	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
14	DATA6	P2	I	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
15	DATA7	P2	I	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
16	DATA8	P2	I/O	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
17	DATA9	P2	I/O	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
18	DATA10	P2	I/O	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
19	PVDD2	P2	P	Power supply pins for I/O(CLKIN, DATA[17:0], HDI, VDI)
20	DVSS	D	G	Ground pins for Digital.
21	DATA11	P2	I/O	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
22	DATA12	P2	I/O	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
23	DATA13	P2	I/O	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
24	TMO	I/O	P2	TEST pin. Leave open. (Internally Pull-down with approx. 100k-ohm)
25	DATA14	P2	I/O	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
26	DATA15	P2	I/O	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
27	DVDD	D	P	Power supply pins for Digital.

28	DVSS	D	G	Ground pins for Digital.
29	DATA16	P2	I/O	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
30	PVDD2	P2	P	Power supply pins for I/O(CLKIN, DATA[17:0], HDI, VDI)
31	DATA17	P2	I/O	Data Input pin Refer “Data input Format”. In case of PDN pin = Low, Hi-z states is possible.
32	VDI	P2	I/O	In case of slave Synchronization operation mode, Vertical Sync timing should be input. In case of PDN pin = Low, Hi-z states is possible.
33	HDI	P2	I/O	In case of slave Synchronization operation mode, Horizontal Sync timing should be input. In case of PDN pin = Low, Hi-z states is possible.
34	CLKIN	P2	I	Clock Input Pin Composite Video Encoder Mode: Input 27MHz Clock. Component Video Encoder Mode: Either 27MHz or 74.25MHz clock is input. (Depending on Input Video Format) High Speed Video DAC Mode: Max input clock is 54MHz. Prohibited Hi-z States
35	HDO	P2	O	Horizontal Sync Timing signal output pin. In case of PDN pin = Low, this pin outputs Low.
36	VDO	P2	O	Vertical Sync Timing signal output pin. In case of PDN Pin = Low, this pin outputs Low.
37	TEST1	I	P2	TEST pin. Connect to DVSS. (Internally Pull-down with approx. 100k-ohm)
38	FLT	A	O	Filter Pin for PLL. 4.7nF capacitor and 820-ohm resistor should be connected as shown in “11. SYSTEM CONNECTION EXAMPLE”
39	DACO3	A	O	DAC3 output pin. Output signal is set by register Composite Video Encoder mode: Pr or R Component Video Encoder mode: CVBS High Speed Video DAC mode: Depending on Input data. Load resistor is 300-ohm
40	DACO2	A	O	DAC2 output pin. Output signal is set by register Composite Video Encoder mode: Pb or B Component Video Encoder mode: C High Speed Video DAC mode: Depending on Input data. Load resistor is 300-ohm
41	DACO1	A	O	DAC1 output pin. Output signal is set by register Composite Video Encoder mode: Y or CVBS Component Video Encoder mode: Y or G High Speed Video DAC mode: Depending on Input data. Load resistor is 300-ohm
42	AVSS	A	G	Ground pin for Analog
43	AVDD	A	P	Power supply pin for Analog.
44	VREF	A	I	to be connected to AVDD via a 0.1 uF capacitor
45	BYPASS	A	O	Output pin to output On-Chip VREF voltage. Should be connected to AVSS via a larger-than 0.1 uF capacitor.
46	BVSS	A	G	Ground pin for Substrate. Connect to AVSS.
47	IREF	A	O	Reference Current Output pin for DAC Should be connected to AVSS via a 3.3 K ohm (+/- 1 %) resistor.
48	TEST0	I	P1	TEST pin. Connect to DVSS. (Internally Pull-down with approx. 100k-ohm)

Power A: AVDD D: DVDD P1: PVDD1 P2: PVDD2
I/O: Input/Output pin I: Input pin O: Output pin G: Ground pin P: Power Supply pin

Pull Up / Down Pins

Pin Name	Pull-up/Down	Pull-Up/Down Resistor
TEST0	Pull Down	Approx. 100k-ohm
TEST1	Pull Down	Approx. 100k-ohm
TMO	Pull Down	Approx. 100k-ohm

5. Electrical Characteristics

■ Absolute Maximum Ratings (* Power supply voltages are values where each ground pin(DVSS=AVSS) is at 0V)

Parameter	Min.	Max.	Unit
Power Supply (VDD) AVDD (DAC,PLL,VREF) DVDD (Digital Core) PDVD1(Digital I/O) PVDD2 (Digital I/O)	-0.3	 4.2 2.2 4.2 4.2	V
Input Voltage (VIN)	-0.3	PVDD1 + 0.3 PVDD2 + 0.3	V
Input Current (IIN)		+/- 10	mA
Storage temperature	-40	125	°C

* All power supply ground pins (DVSS, AVSS) should be at the same potential.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal Operating Specifications are not guaranteed at these extremes.

■ Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Power Supply (VDD) AVDD DVDD PVDD1 PVDD2	 2.7 1.65 DVDD DVDD	 3.0 1.8 1.8 1.8	 3.6 2.0 3.6 3.6	 V
Operating Temperature (TA)	-40		85	°C

■ Analog Characteristics and Power Dissipation (operating voltage AVDD3.0V, DVDD 1.8V Temperature 25°C)

Parameter	Min	Typ.	Max.	Unit	Condition
DAC Resolution		10		bit	
Integral Non-Linearity Error INL		+/- 0.6	+/- 2.0	LSB	Note 1)
Differential Non-Linearity Error DNL		+/- 0.4	+/- 1.0	LSB	Note 1)
Output Full Scale Voltage	1.15	1.28	1.41	V	Load Resistor 300Ω
DAC SNR		54		dB	Note 2)
Output Bandwidth		+/- 1		dB	Note 3)
Unbalances between DACs		1.5	3	%	Note 4)
Internal Reference Voltage		1.43		V	
Internal Reference Drift		60		ppm/°C	
Current Consumption of Analog part		30	40	mA	Note 5)
Current Consumption of Digital part Component Encoder mode Composite Encoder mode DAC mode		 35 8 8	 70 16 16	mA	Note 6)
Current Consumption of Sleep mode		1		mA	
Current Consumption of Power down		10	300	uA	PDN=Low

Note 1. DAC:148MHz Operation
Note 2. 2MHz Sin-wave input. (Noise Band-Width 0 – 30MHz)
Note 3. Output Bandwidth 30MHz: at 148MHz Operation DAC1 (Load Resistor 300ohm) Channel Only External Load Capacitor 10 pF (SubAddress[0x0A] HDAFLT[1:0]=11)
Note 4. Variation when a 700 mV equivalent code is input on DACs.
Note 5. DAC 3ch ON fs=74MHz / Component mode (Y: 30MHz Sin wave, CbCr: 15MHz Sin wave)
Note 6: Clock-rate and Input data is
Composite Video Encoder mode: 515i (27MHz) Internal Color Bar
Component Video Encoder mode: 1080i (74Mhz) Y: 30MHz Sin wave, CbCr: 15MHz Sin wave)
High Speed DAC mode: 54MHz Clock 20MHz SIn wave Data input.

■ Digital Input / Output DC Characteristics

(AVDD=2.7-3.6V, DVDD=1.65-2.0V, PVDD1= 1.65-3.6V, PVDD2 = 1.65-3.6V Ta= -40-85°C)

Parameter	Symbol	MIN	TYP	MAX	unit	Condition
High Level Input Voltage 1	VIH1	0.70 PVDD1			V	Note. 1
High Level Input Voltage 2	VIH2	0.70 PVDD2			V	Note. 2
Low Level Input Voltage 1	VIL1			0.30 PVDD1	V	Note. 1
Low Level Input Voltage 2	VIL2			0.30 PVDD2	V	Note. 2
High Level Output Voltage	VOH	0.80 PVDD2			V	Note. 3 IOH = -600 uA
Low Level Output Voltage	VOL			0.20 PVDD2	V	Note. 3 IOL = 1.4 mA
Input pin Leakage Current	ILIKG			±10	uA	Note. 4
I2C High Level Input Voltage	VIHC	0.77PVDD1			V	Note. 5
I2C Low Level Input Voltage	VILC			0.21PVDD1	V	Note. 5
I2C Low Level Output Voltage	VOL2			0.4	V	Note. 6 IOLC=3mA

Note. 1. PDN pin.
Note. 2. CLKIN, DATA[17:0], HDI, VDI pins
Note. 3. HDO, VDO pins
Note. 4. CLKIN, DATA[17:0], HDI, VDI, PDN, SELA, SDA, SCL pins
Note. 5. SELA, SDA, SCL pins
Note. 6. SDA pin

■ AC Timing

(AVDD=2.7-3.6V, DVDD=1.65-2.0V, PVDD1 = DVDD-3.6V, PVDD2 = DVDD-3.6V Ta: -40□-85°C)

(1) CLKIN

(1-1) Component Video Encoder / Composite Video Encoder mode

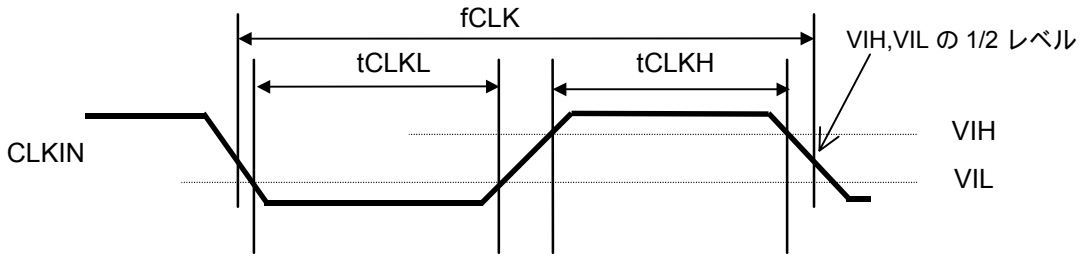

Fig. 7

parameter	Symbol	min	Typ	max	unit	Note
CLKIN	fCLK		74.25		MHz	74.25 / 74.175MHz
			27			27MHz(*)
CLKIN Pulse Width H	tCLKH	4.04			nsec	74.25/74.175MHz
		15.0				27MHz
CLKIN Pulse Width L	tCLKL	4.04			nsec	74.25 / 74.175MHz
		15.0				27MHz

(*) Accuracy of frequency may affect to color display.

(1-2) Video DAC mode

parameter	Symbol	min	typ	max	unit	Note
CLKIN	fCLK	6		54	MHz	
CLKIN Pulse Width H	tCLKH	7.4			nsec	
CLKIN Pulse WIdth L	tCLKL	7.4			nsec	

(2) Pixel Data Input Timing

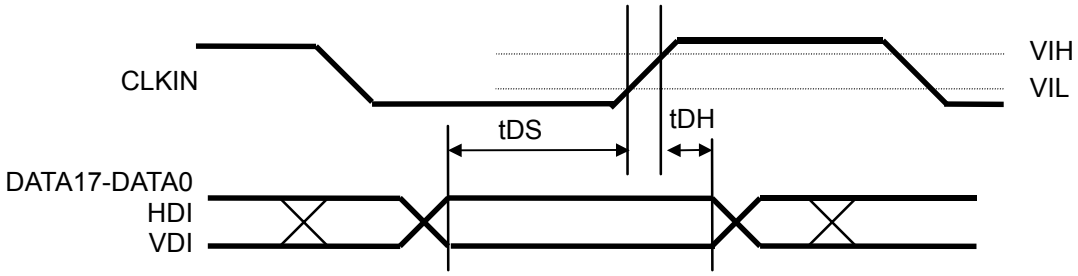

Fig. 8

parameter	Symbol	min	typ	max	unit
Data Setup Time	tDS_HD	*3.3*			nsec
Data Hold Time	tDH_HD	*3.3*			nsec

Note) DATA17:DATA0, HDI, VDI can be captured inverted clock edge by resister setting

(3) HSYNC Pulse Width

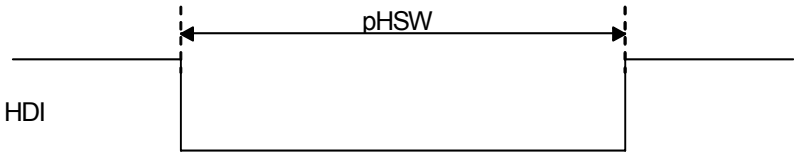

Fig. 9

parameter	Symbol	min	typ	max	unit	Note
HSYNC Pulse Width	pHSW	15	128		CLKs	D1 Video 27MHz
		15	64			D2 Video 27MHz
		15	272			D3, D4 Video 74.25MHz

(4) PDN Pulse Width

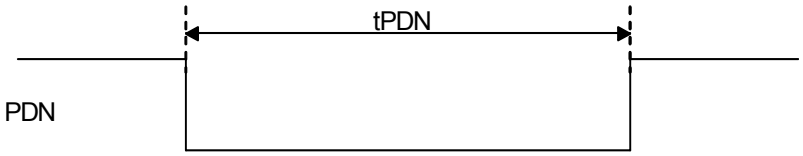

Fig. 10

Parameter	Synbol	min	typ	max	unit	備考
PDN Pulse Width	tPDN	100			ns	

(5) Power Up sequence
There are no order restriction to make power up, AVDD, DVDD, PVDD1, PVDD2.
Clock input is not necessary to write register.

(5-1) The sequence for power down mode after power-up.
Clock input to the CLKIN pin is necessary to guarantee “Current Consumption of Power down”
(r) : Register-bit

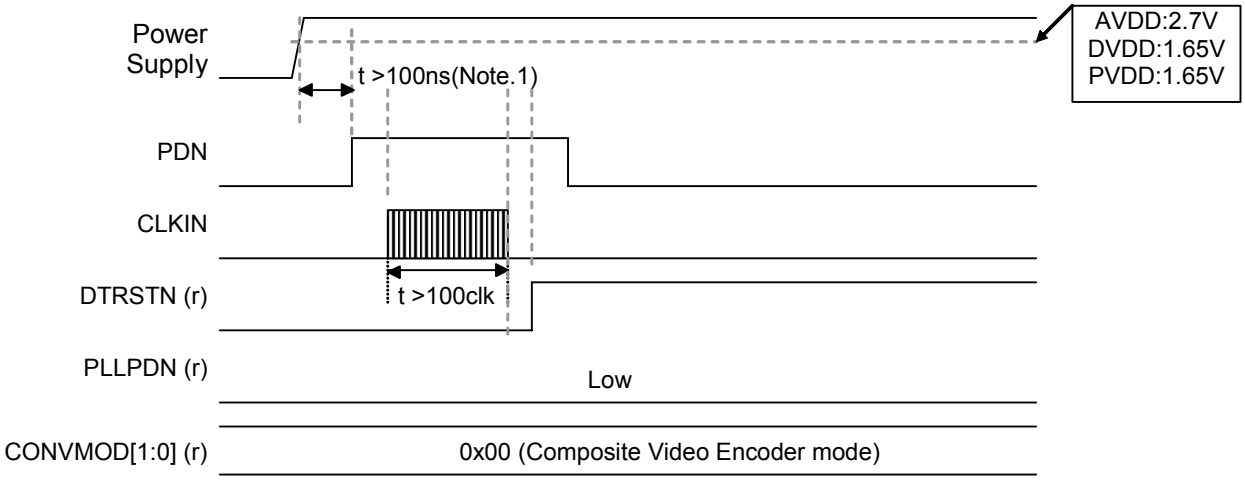

Fig. 11 Power-Up sequence (To make Power down state after power-up)

Note.1) Please wait 100ns for make PDN pin low after the Voltage of Power Supply becomes stable enough,

(5-2) Setting to Composite Video Encoder mode after power-up
After initializing with PDN-pin = Low, AK8826 is Composite Video Encoder mode.
(r) : Register-bit

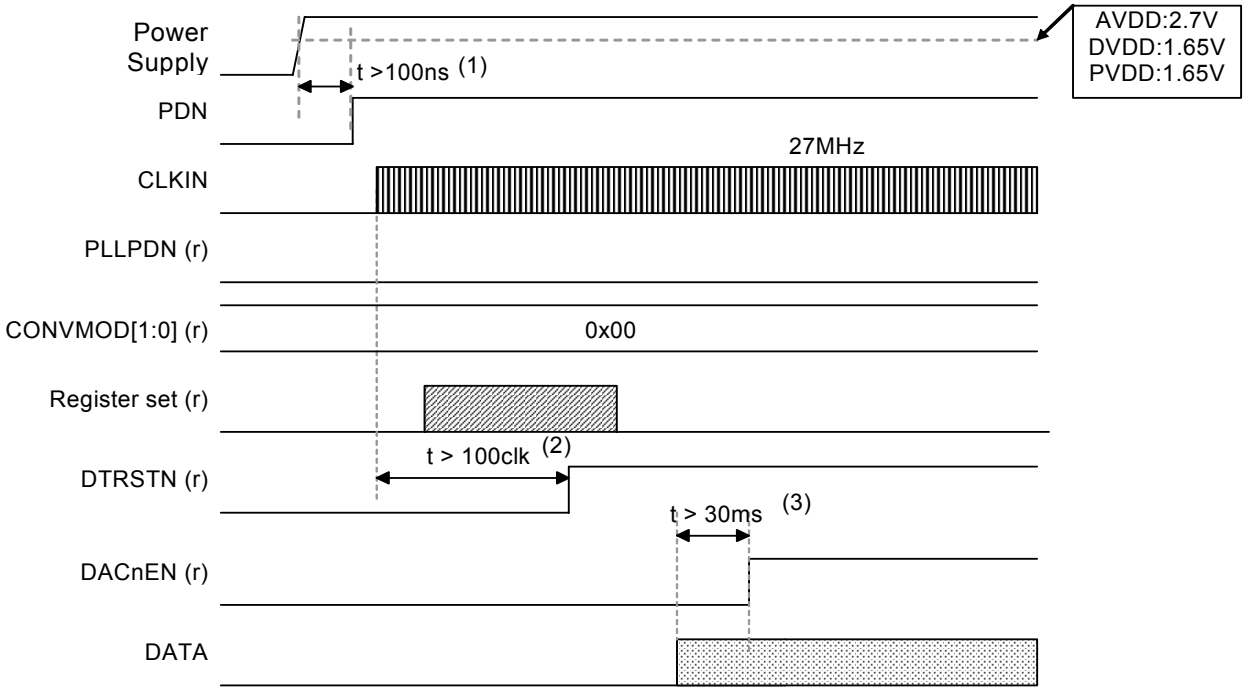

Fig. 12 Power-Up sequence (To set Composite Video Encoder mode after power-up)

(1) PDN-pin should be Low states more than 100ns after power-up.
(2) To initialize in Composite Video Encoder Block. Clock input is ncessary to CLKIN-pin. DTRSTN-bit should be 0 more than 100clock count.
(3) BT656 Interface mode operation, it is more than 1-Frame periode to synchronize with input data. To avoid displaying noise etc, DAC should be ON after synchronization.

(5-3) Setting to Component Video Encoder mode after power-up

After initializing with PDN-pin = Low, AK8826 is Composite Video Encoder mode.
Set to Component Video Encoder mode by register setting. (Set CONVMOD[1:0]-bit =[01])
(r) Shows Register-bit

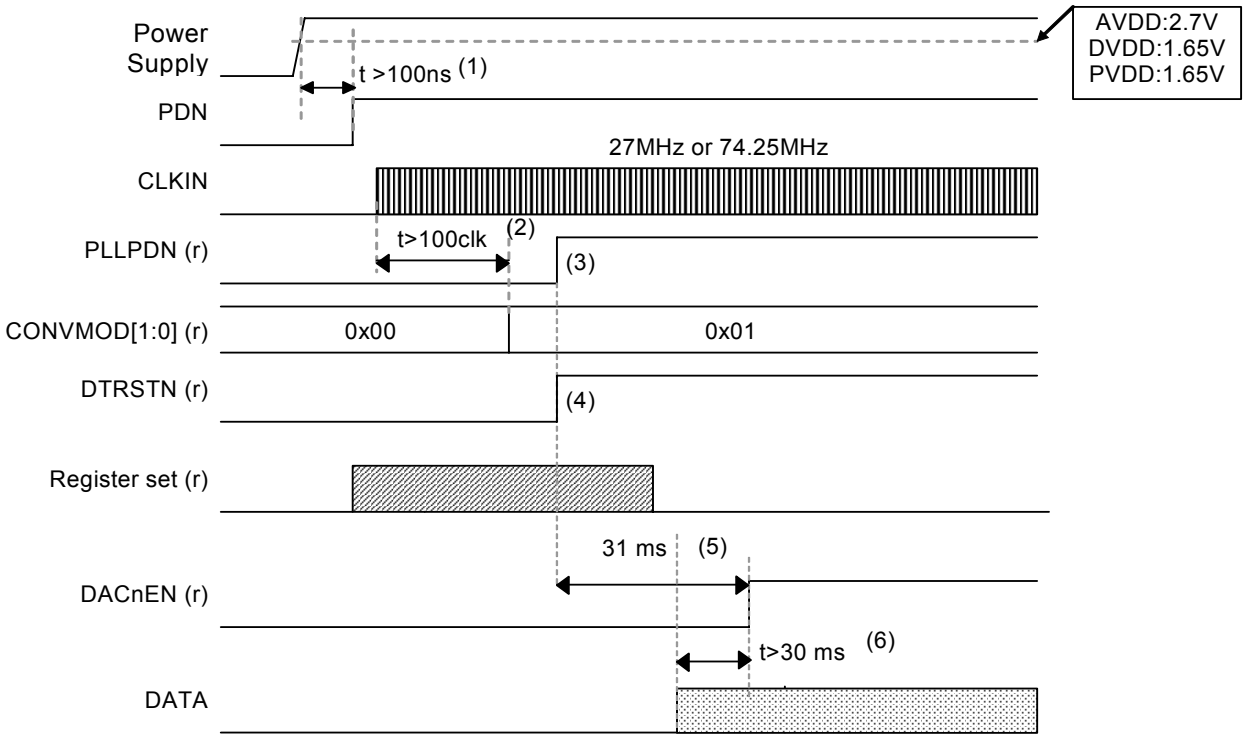

Fig. 13 Power-Up sequence (To set Component Video Encoder mode after power-up)

(1)	PDN-pin should be Low states more than 100ns after power-up.
(2)	Set to Component Video Encoder mode after 100clock count with Clock Input to CLKIN-pin.
(3)	PLLPDN-bit should be set to High after setting Component Video Encoder mode.
(4)	DTRSTN-bit shoud be set to High after setting component Video Encoder mode.
(5)(6)	After setting PLLPDN -bit = High, wait more than 31ms, then set DAC ON.

(5-4) Setting to High Speed Video DAC mode after power-up
After initializing with PDN-pin = Low, AK8826 is Composite Video Encoder mode.
Set to Component Video Encoder mode by register setting. (Set CONVMOD[1:0]-bit =[10])
(r) shows Register-bit

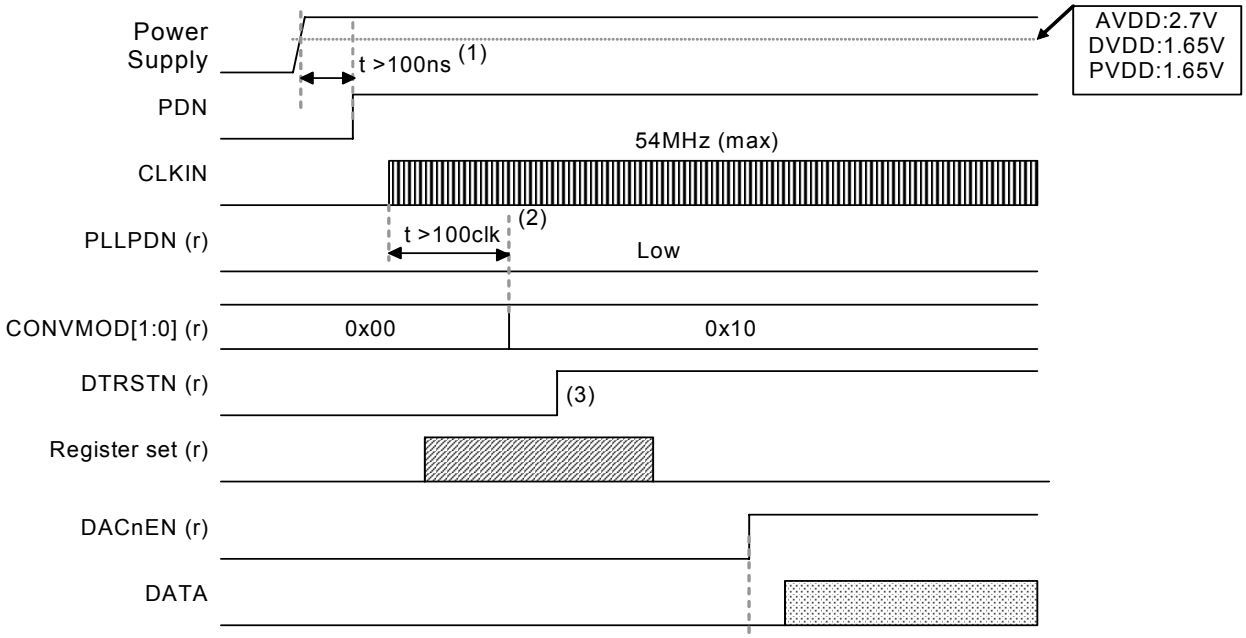

Fig. 14 Power-Up sequence (To set High Speed Video DAC mode after power-up)

(1) PDN-pin should be Low states more than 100ns after power-up.
(2) Set to High Speed DAC mode after 100clock count with Clock Input to CLKIN-pin.
(3) Set to DTRSTN-bit should be High after setting High Speed Video DAC mode

(6) Power-Down Sequence and reset sequence after power-down release

Before setting to PDN=LOW, DTRSTN(r) should be Low to initialize.
After power-down release (PDN =LOW -> High), wait for 10ms for Analog Reference Voltage / Current becomes stable.
During PDN=Low (Power down States), either with clock-in or clock-not in is
During PDN = Low, AVDD / DVDD can be power-off.
Power down sequence is shown as Fig. 16. (r) means Register-bit.
PDN = Low makes AK8826 initialize condition, so that after power-down release, make sure register setting.

(6-1) **Power-Down and power-down release Sequence from Composite Video Encoder mode**

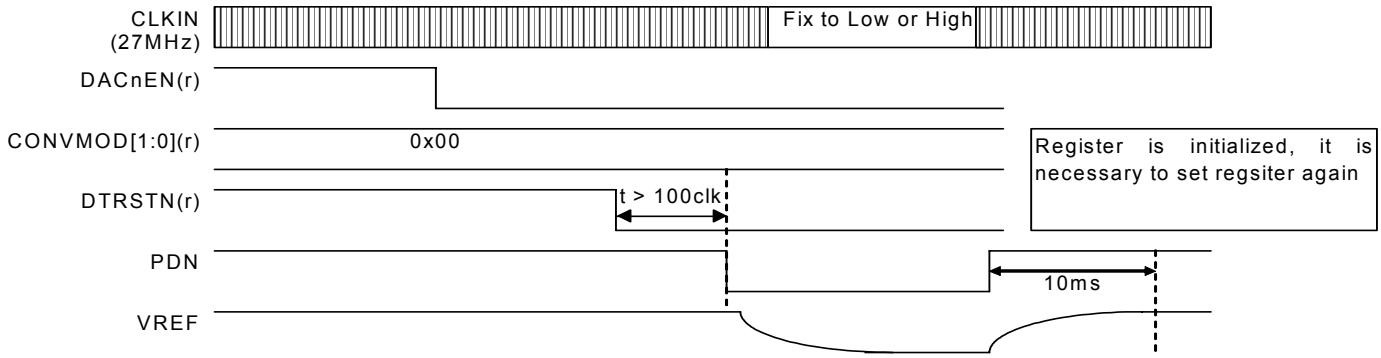

Fig. 15 Power-Down and power-down release Sequence from Composite Video Encoder mode

(6-2) **Power-Down and power-down release Sequence from Component Video Encoder mode**

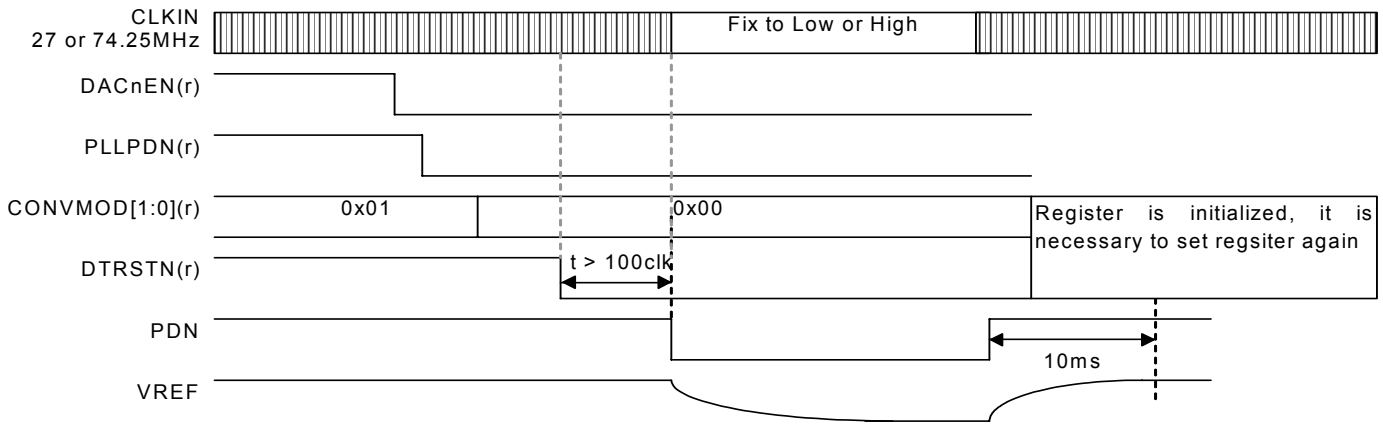

Fig. 16 Power-Down and power-down release Sequence from Component Video Encoder mode

(6-3) **Power-Down and power-down release Sequence from High Speed Video DAC mode**

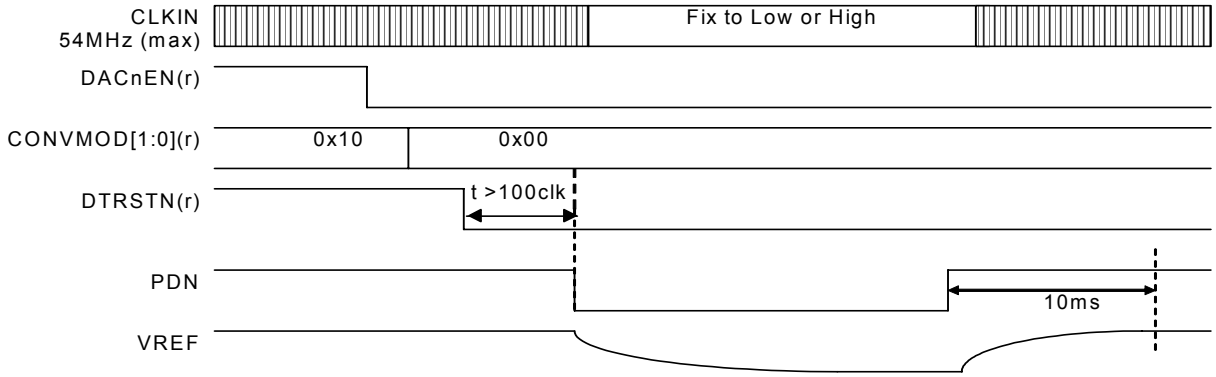

Fig. 17 Power-Down and power-down release Sequence from Component Video Encoder mode

(7) I²C Timing
(7-1) Timing 1

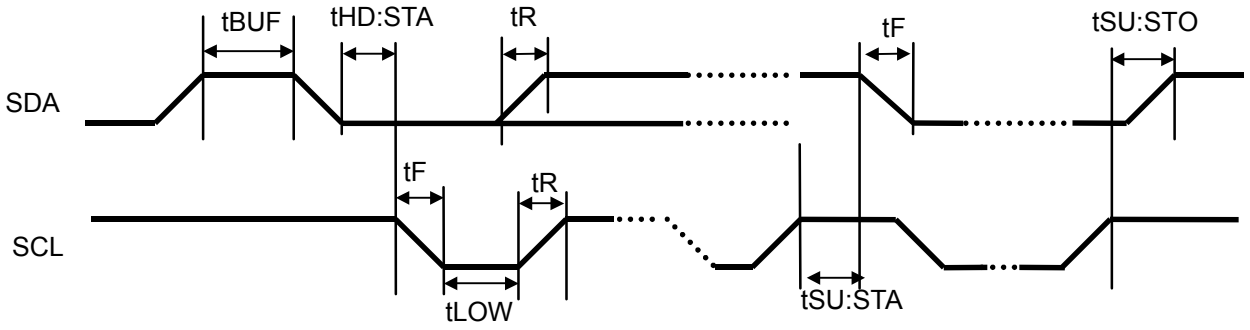

Fig. 18 I²C Timing 1

parameter	symbol	min	max	unit
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

The above I2C Bus related timings are I2C Bus specifications, and they are not the device limits. For details, refer to I2C Bus Specifications.

(7-2) Timing 2

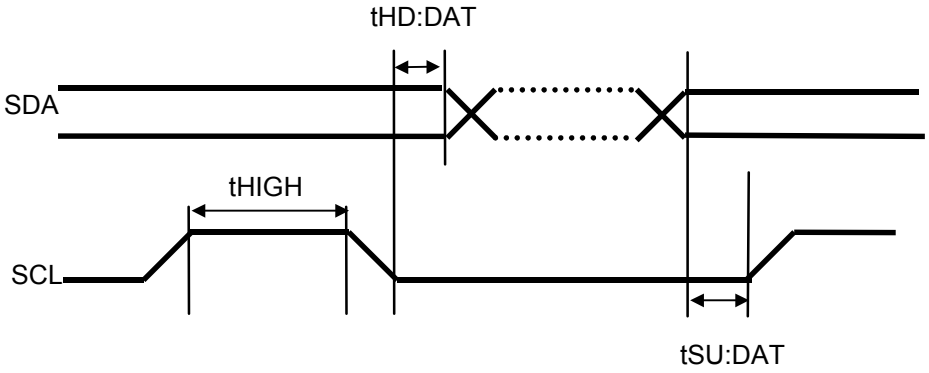

Fig. 19 I²C Timing 2

parameter	symbol	min	max	unit
Data Setup Time	tSU:DAT	100 (note1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9 (note2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

note 1 : when to use in I2C Bus Standard mode, tSU : DAT > = 250 nsec must be satisfied.
note 2 : when the AK8826 is used on not-extended tLOW Bus (used at tLOW = minimum specification), this condition must be satisfied.

R/W operation to the register is possible without Clock input to CLKIN-pin.

6. Common Function Specification

This section describes common function specifications among Composite Video Encoder, Component Video Encoder, High Speed Video DAC function Block.

■ Device Control Interface

The AK8826 is controlled via I2C Bus Control Interface.

[I2C Bus Slave Address]

I2C Slave Address is selectable to be either 0x40 or 0x42 by SELA pin setting.

SELA -pin	SLAVE Address
Low (PVSS1)	0x40
High (PVDD1)	0x42

A6	A5	A4	A3		A2	A1	A0	R/W
0	1	0	0		0	0	SELA	

[I2C Control Sequence]

(1) Write Sequence

When the Slave Address of the AK8826 Write mode is received at the first byte, Sub-Address at the second byte and Data at the third & succeeding bytes are received.

There are 2 operations in Write sequence—

A sequence to write at every single byte, and a sequential write operation to write multiple bytes successively.

(a) Single byte Write sequence

S	Slave Address	w	A	Sub Address	A	Data	A	Stp
	8-bits		1-bit	8-bits	1-bit	8-bits	1-bit	

(b) Multiple Byte (m-bytes) Write Sequence (Sequential Write Operation)

S	Slave Address	w	A	Sub Address(n)	A	Data(n)	A	Data(n+1)	A	…	Data(n+m)	A	stp
	8-bits		1	8-bits	1	8-bits	1	8-bits	1		8-bits	1	

(2) Read Sequence

When the Slave Address of the AK8826 Read Mode is received at the first byte, data at the second and succeeding bytes are transmitted from the AK8826.

S	Slave Address	w	A	Sub Address(n)	A	rS	Slave Address	R	A	Data1	A	Data2	A	Data3	A	…	Data n	Ā	stp
	8-bits		1	8-bits	1		8-bits		1	8-bits	1	8-bits	1	8-bits	1		8-bits	1	

Abbreviated Terms listed above mean :

S, rS : Start Condition
A : Acknowledge (SDA low)
Ā : Not Acknowledged (SDA high)
Stp : Stop Condition
R / W : 1 : Read, 0 : Write

: to be controlled by the Master Device. To be output by micro-computer normally.

: to be controlled by the Slave Device. To be output by the AK8826.

Note: At the MutipleByte Read/Write Sequence, read or write register operation cannot done at one-time.
Add[0x00] - Add[0x35] operation is done, then Add[0x36] - Add[0x3F] should be done.
To read or to write Test Register, 1 Byte Read/Write sequence should be done.

■ Mode Select

AK8826 has 3-function block as Composite Video Encoder, Component Video Encoder and High Speed Video DAC.These functions are selected by CONVMOD[1:0]-bit of **I/O Data Format Register (R/W) [Sub Address 0x0B]**.
At mode change timing, CONVMOD[1:0]-bit and DACnEN-bit of **DAC Control Register(R/W) [Sub Address 0x0D]** and PLLPDN-bit of **Powerdown Mode Register (R/W) [Sub Address 0x06]** should be taken care.

I/O Data Format Register
Sub Address 0x0B **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	**bit 3**	**bit 2**	bit 1	bit 0
HDSDMASE	YC2RGB	Reserved	DTFMT	**CONVMOD1**	**CONVMOD0**	INPFMT1	INPFMT0

CONVMOD[1:0]-bit	Mode	Note
00	Composite Video Encoder mode	Component Video Encoder Block becomes power down state automatically. PLL Block is still working, PLLPDN-bit can make PLL block to power down state.
01	Component Video Encoder mode	Composite Video Encoder Block becomes Power down states automatically. PLLPDN-bit should be set to “1” for this mode.
10	High Speed Video DAC mode	Composite/Component Video Encoder Block become power down state automatically. PLLPDN-bit should be set to “0” .
11	Reserved	Reserve set

DAC Control Register
Sub Address 0x0D **default Value 0x00**

bit 7	bit 6	bit 5	bit 4	**bit 3**	**bit 2**	**bit 1**	**bit 0**
Reserved	Reserved	OLVL	DTRSTN	**CVBSSEL**	**DAC3EN**	**DAC2EN**	**DAC1EN**

Output signal from DAC1/2/3 with setting DACnEN-bit =1 (n=1,2,3)

	CONVMOD[1:0]-bit			condition
	00		01	
	CVBSSEL=0	CVBSSEL=1		
DAC1 output	Y	CVBS	Y	DAC1EN=1
DAC2 output	C	-	Pb	In CVBSSEL=1 case, DAC2EN-bit and DAC3EN-bit should be set 0. (Output signal from DAC2, DAC3 is 0)
DAC3 output	CVBS	-	Pr	

Powerdown Mode Register
Sub Address 0x06 < HD Block > **Default Value 0x00**

bit 7	bit 6	bit 5	bit 4	bit 3	**bit 2**	bit 1	bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	**PLLPDN**	SLPEN1	SLPEN0

When setting to Component mode, PLLPDN-bit should be set to “1” since x2 PLL is necessary to work for Component Video Encoder mode.

PLLPDN-bit	Operation
0	PLL is power down states
1	PLL is working. Component Video Encoder mode, this bit should be set 1.

Mode switching sequence

(1) Component Video Encoder mode to Composite Video Encoder mode

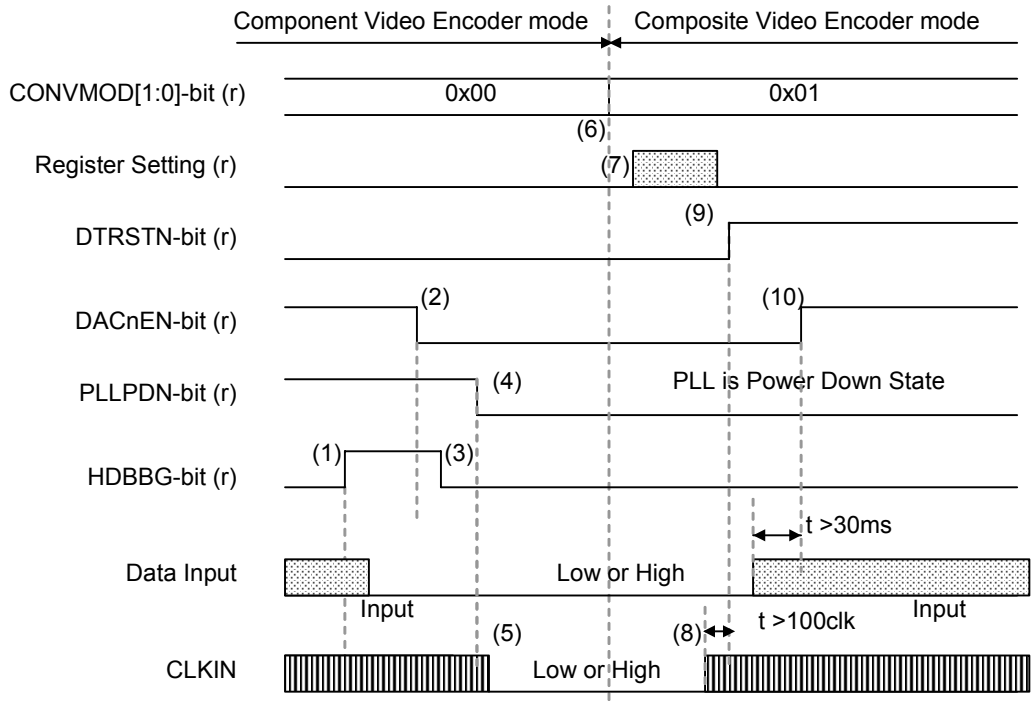

Fig. 20 Mode Switching sequence (Component Video Encoder mode to Composite Video Encoder mode)

(1) To avoid making noise, Black Burst Generator is On, then stop inputting data.
(2) Turn Off DACs.
(3) Black Burst Generator OFF.
(4) Set PLLPDN-bit = 0 (PLL Block becomes Power Down States)
(5) Stop Clock Input to CLKIN pin.
(6) Mode Change from Componet VIdeo Encoder mode to Composite Video Encoder mode.
(7) Set Sync-mode, Output Signal etc.
(8) Chang clock, if necessary.
It is allows that changing clock without stopping clock input, however Process(6), (7) should be done before clock change.
(9) Set DTRSTN=1 after DTRSTN-bit =0.
DTRSTN-bit =0 periode should be more than 100-clk counts with clock input.
(10) Turn On DACs after more than 30ms later