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AK8858

PS/SD Multi Format Video Decoder

Overview

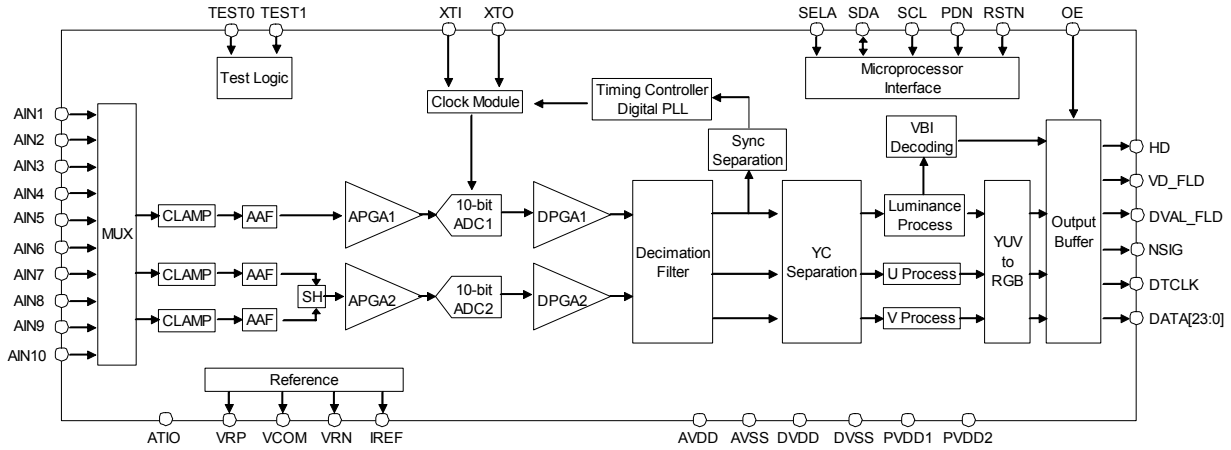
The AK8858 is a single-chip digital video decoder for composite, s-video, 525i/625i component and 525p/625p component video signals. Its output data is in YCbCr and RGB format. Its pixel clock is generated internally and synchronized with the input signal. Microprocessor access is via I2C interface.

Features

- Decodes composite and S-Video signals NTSC/ PAL-B, D, G, H, I, N, Nc, M, 60 /SECAM
- Decode 525i / 625i YPbPr component video signals
- Decode 525p / 625p YPbPr component video signals
- 10 input channel
- 10-bit 54MHz ADC 2 channel
- Internally built PLL
- Internal analog bandwidth filter
- Programmable Gain Amp (PGA) (-3.25dB～10dB)
- Adaptive automatic Gain Control (AGC)
- Auto Color Control (Composite and S-Video signals)
- Image adjustment (Contrast, Brightness, Saturation, HUE, Sharpness)
- Automatic input signal detection (NTSC/ PAL/ SECAM detect、Interlace/ Progressive detect)
- Adaptive 2-D Y/C separation
- Output data format
  YCbCr 4:2:2 or RGB 8:8:8
- Output interface
  (YCbCr)
    Interlace: ITU-R BT.656 (8bit 27MHz) and 16bit 13.5MHz with EAV/ SAV
    Progressive: 16bit 27MHz and 8bit 54MHz with EAV/ SAV
  (RGB)
    Interlace: 8bit:8bit:8bit 13.5MHz with EAV/ SAV
    Progressive: 8bit:8bit:8bit 27MHz with EAV/ SAV
  *EAV/ SAV output can be disabled via register
- HD, VD, DVALID and FIELD (VD, DVALID, FIELD can be select up to 2 output via register setting)
- Closed Caption / WSS / CGMS-A signal decoding (output via register).
- Macrovision signal detection (Rovi certification)
- I2C control
- Powerdown function
- Internal VREF
- Core supply voltage: 1.70~2.00V
- I/O power supply: 1.70~3.60V
- Operating temperature: −40°C~105°C
- 80-pin LQFP package (12.0mm x 12.0mm)

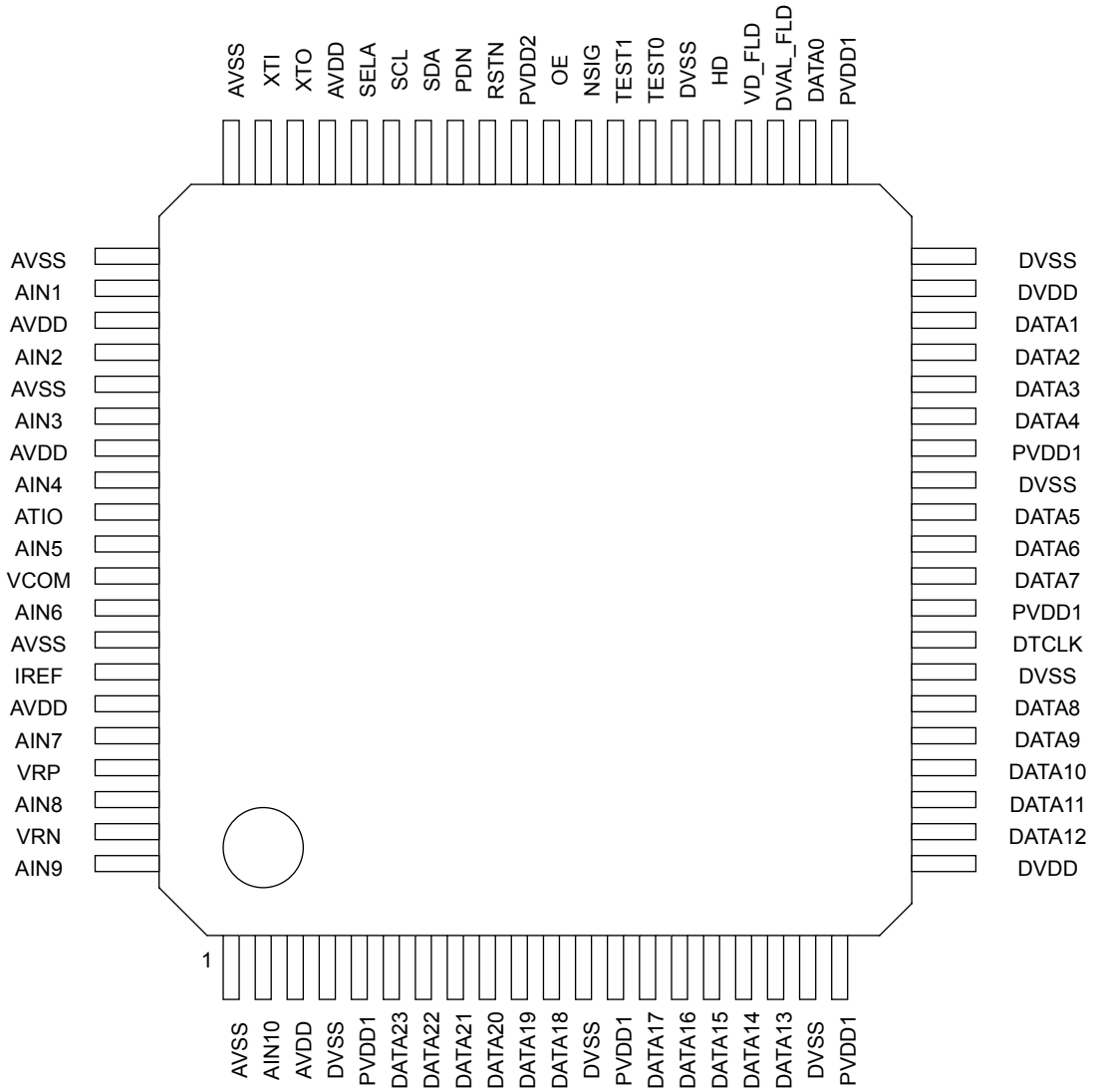
Features

[1] Functional block diagram



[2] Pin assignment

80-pin LQFP package (12.0mm x 12.0mm)



[3] Pin function description

[3.1] Pin function

Pin No.	Symbol	P/S	I/O	Functional Description
1	AVSS	A	G	Analog ground pin.
2	AIN10	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
3	AVDD	A	P	Analog power supply pin.
4	DVSS	D	G	Digital ground pin.
5	PVDD1	P1	P	I/O power supply pin.
6	DATA23	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
7	DATA22	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
8	DATA21	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
9	DATA20	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
10	DATA19	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
11	DATA18	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
12	DVSS	D	G	Digital ground pin.
13	PVDD1	P1	P	I/O power supply pin.
14	DATA17	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
15	DATA16	P1	O (I/O)	DATA output pin. Used as output pin in RGB 8:8:8 output.(*1) If test mode, it is I/O pin.
16	DATA15	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
17	DATA14	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
18	DATA13	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
19	DVSS	D	G	Digital ground pin.
20	PVDD1	P1	P	I/O power supply pin.
21	DVDD	D	P	Digital power supply pin.
22	DATA12	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
23	DATA11	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
24	DATA10	P1	O (I/O)	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1) If test mode, it is I/O pin.
25	DATA9	P1	O	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1)
26	DATA8	P1	O	DATA output pin. Used as output pin in 16-bit output and RGB 8:8:8 output mode.(*1)

[Power supply] A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[Input/Output] I: intput pin, O: output pin, I/O: input/output pin, P: power supply pin, G: ground connection pin

(*1)See {[3.2] Output pin state} for relation of output to OE/PDN and RSTN pin status.

Pin No.	Symbol	P/S	I/O	Functional Description
27	DVSS	D	G	Digital ground pin.
28	DTCLK	P1	O	Data clock output pin.(*1)
29	PVDD1	P1	P	I/O power supply pin.
30	DATA7	P1	O	DATA output pin.(*1)
31	DATA6	P1	O	DATA output pin.(*1)
32	DATA5	P1	O	DATA output pin.(*1)
33	DVSS	D	G	Digital ground pin.
34	PVDD1	P1	P	I/O power supply pin.
35	DATA4	P1	O	DATA output pin.(*1)
36	DATA3	P1	O	DATA output pin.(*1)
37	DATA2	P1	O	DATA output pin.(*1)
38	DATA1	P1	O	DATA output pin.(*1)
39	DVDD	D	P	Digital power supply pin.
40	DVSS	D	G	Digital ground pin.
41	PVDD1	P1	P	I/O power supply pin.
42	DATA0	P1	O	DATA output pin.(*1)
43	DVAL_FLD	P1	O (I/O)	DVALID/ FIELD signal output pin. DVALID signal output / FIELD signal output can be selected by register setting.(*1) If test mode, it is I/O pin.
44	VD_FLD	P1	O (I/O)	VD/ FIELD signal output pin VD signal output / FIELD signal output can be selected by register setting.(*1) If test mode, it is I/O pin.
45	HD	P1	O (I/O)	HD signal output pin.(*1) If test mode, it is I/O pin.
46	DVSS	D	G	Digital ground pin.
47	TEST0	P2	I	Pin for test mode setting. Connect to DVSS.
48	TEST1	P2	I	Pin for test mode setting. Connect to DVSS.
49	NSIG	P2	O	Shows status of synchronization with input signal Low: Signal present (synchronized). High: Signal not present or not synchronized.(*1)
50	OE	P2	I	Output Enable pin. Low: Digital output pin in Hi-z output mode. High: Data output mode. Hi-z input to OE pin is prohibited.
51	PVDD2	P2	P	Microprocessor I/F power supply pin.
52	RSTN	P2	I	Reset signal input pin. Hi-z input is prohibited. Low: Reset. High: Normal operation.
53	PDN	P2	I	Power-down control pin. Hi-z input is prohibited. Low: Power-down. High: Normal operation.
54	SDA	P2	I/O	I2C data pin. Connect to PVDD2 via a pull-up register. Hi-z input possible when PDN=L.
55	SCL	P2	I	I2C clock input pin. Connect to PVDD2 via a pull-up register. Hi-z input possible when PDN=L.
56	SELA	P2	I	I2C bus address selector pin. PVDD2 connection: Slave address [0x8A] DVSS connection: Slave address [0x88]
57	AVDD	A	P	Analog power supply pin.

[Power supply] A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[Input/Output] I: intput pin, O: output pin, I/O: input/output pin, P: power supply pin, G: ground connection pin

(*1)See {[3.2] Output pin state} for relation of output to OE/PDN and RSTN pin status.

Pin No.	Symbol	P/S	I/O	Functional Description
58	XTO	A	O	Crystal connection pin. Use 24.576 MHz crystal. When PDN=L, output level is AVSS. If crystal is not used, connect to NC or AVSS.
59	XTI	A	I	Crystal connection pin. Use 24.576 MHz crystal resonator. For input from 24.576 MHz crystal oscillator, use this pin.
60	AVSS	A	G	Analog ground pin.
61	AVSS	A	G	Analog ground pin.
62	AIN1	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
63	AVDD	A	P	Analog power supply pin.
64	AIN2	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
65	AVSS	A	G	Analog ground pin.
66	AIN3	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
67	AVDD	A	P	Analog power supply pin.
68	AIN4	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
69	ATIO	A	I/O	Aanalog test pin. For normal operation, connect to AVSS.
70	AIN5	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
71	VCOM	A	O	Common internal voltage for AD converter. Connect to AVSS via 0.1uF ceramic capacitor (±10%).
72	AIN6	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
73	AVSS	A	G	Analog ground pin.
74	IREF	A	O	Analog circuit reference current setting pin. Connect to AVSS via 6.8KΩ (±1% accuracy) resistor.
75	AVDD	A	P	Analog power supply pin.
76	AIN7	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
77	VRP	A	O	Internal reference positive voltage pin for AD converter. Connect to AVSS via 0.1uF ceramic capacitor (±10%).
78	AIN8	A	I	Analog video signal input pin.Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
79	VRN	A	O	Internal reference negative voltage pin for AD converter. Connect to AVSS via 0.1uF ceramic capacitor (±10%).
80	AIN9	A	I	Analog video signal input pin. Connect via 0.033 μF capacitor and voltage-splitting resistors as shown in page 107. If it is not used, connect to NC.

[Power supply] A: AVDD, D: DVDD, P1: PVDD1, P2: PVDD2

[Input/Output] I: intput pin, O: output pin, I/O: input/output pin, P: power supply pin, G: ground connection pin

(*1)See {[3.2] Output pin state} for relation of output to OE/PDN and RSTN pin status.

[3.2] Output pin state

Relation of output to OE/PDN and RSTN pin status.

OE	PDN	RSTN	DATA[23:0], DTCLK, HD, VD_FLD, DVAL_FLD	NSIG
L	x	x	Hi-Z output	L output
H	L		L output	L output
H	H	L	L output	L output
		H	DOUT	DOUT

(x: Don't care, DOUT: Data output)

State of DATA pin except for RGB 8:8:8 format output

YCbCr8bit output			YCbCr16bit output		
DATA[23:16]	DATA[15:8]	DATA[7:0]	DATA[23:16]	DATA[15:8]	DATA[7:0]
Low output	Low output	DOUT	Low output	DOUT	DOUT

(DOUT: Data output)

In the absence of AIN signal input, output will be black data (Y=0x10, Cb/Cr=0x80).
(Blueback output can be obtained by register setting). *(Sub Address: 0x0D [3:2])

[4] Electrical specifications

[4.1] Absolute maximum ratings

Parameter	Min	Max	Unit	Notes
Supply voltage				
DVDD, AVDD	−0.3	2.2	V	
PVDD1, PVDD2	−0.3	4.2	V	
Analog input pin voltage A (VinA)	−0.3	AVDD + 0.3 (≤ 2.2)	V	(*1)
Digital input pin voltage P1 (VioP1)	−0.3	PVDD1 + 0.3 (≤ 4.2)	V	(*2)
Digital output pin voltage P2 (VioP2)	−0.3	PVDD2 + 0.3 (≤ 4.2)	V	
Input pin current (IIn)	−10	10	mA	Power supply pin is not included
Storage temperature	−40	150	°C	

(*1) DTCLK, DATA [23:0], HD, VD_FLD, DVAL_FLD

(*2) OE, SELA, PDN, RSTN, SDA, SCL, NSIG, TEST0, TEST1

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0V (Reference Voltage).
All power supply grounds (AVSS, DVSS) should be at the same electric potential.
If digital output pins are connected to data bus, the data bus operating voltage should be in the same range as shown above from the digital output pin.
The setting other than above may cause the eternal destruction to the deivce.
Normal operational is not guaranteed for the above setting.

[4.2] Recommended operating conditions

Parameter	Min	Typ	Max	Unit	Condition
Analog supply voltage (AVDD) Digital supply voltage (DVDD)	1.70	1.80	2.00	V	AVDD = DVDD
MPU I/F supply voltage (PVDD1) Data output i/F supply voltage (PVDD2)	1.70	1.80	3.60	V	PVDD1 ≥ DVDD PVDD2 ≥ DVDD
Operating temperature (Ta)	−40		85	°C	

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0V (Reference Voltage).
All power supply grounds (AVSS, DVSS) should be at the same electric potential.

[4.3] DC characteristics

(Ta: −40°C~85°C / DVDD=AVDD=1.7V~2.0V / PVDD1=DVDD~3.6V / PVDD2=DVDD~3.6V)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Digital P2 input high voltage(*1)	VPIH	0.8PVDD2			V	PVDD2<2.7V
		0.7PVDD2			V	PVDD2≥2.7V
Digital P2 input low voltage(*1)	VPIL			0.2PVDD2	V	PVDD2<2.7V
				0.3PVDD2	V	PVDD2≥2.7V
XTI input high voltage	VXIH	0.8AVDD				
XTI input low voltage	VXIL			0.2AVDD		
Digital input leak current(*1)	IL			±10	uA	
Digital P1 output high voltage(*2)	VOH1	0.7PVDD1			V	IOH1 = −600uA
Digital P1 output low voltage(*2)	VOL1			0.3PVDD1	V	IOL1 = 1mA
Digital P1 output Hi-z leak current (*2)	HIL			±10	uA	
NSIG output high voltage	VOH2	0.7PVDD2			V	IOH2 = −600uA
NSIG output low voltage	VOL2			0.3PVDD2	V	IOL2 = 1mA
I2C(SDA)L output	VOLC			0.4 0.2 PVDD2	V	IOLC = 3mA PVDD2≥2.0V PVDD2<2.0V

(*1) Collective term for SDA, SCL, SELA, OE, PDN, RSTN, TEST0 and TEST1 pins.

(*2) Collective term for DTCLK, DATA [23:0], HD, VD_FLD and DVAL_FLD pins.

[4.4] Analog characteristics

(AVDD=1.8V, Ta=25˚C)

[4.4.1] Input Range

Parameter	Symbol	Min	Typ	Max	Units	Condition
Input range	VIMX	0		0.60	Vpp	

[4.4.2] AAF (Anti-Aliasing Filter)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Pass band ripple	Gp	−1		+1	dB	Progressive signal: ~12MHz Interlace signal: ~6MHz
Stop band blocking	Gs	20	30		dB	Progressive signal: 54MHz Interlace signal: 27MHz

[4.4.3] Analog PGA

Parameter	Symbol	Min	Typ	Max	Units
Resolution	RES		2		bit
Minimum gain	GMN		-3		dB
Maximum gain	GMX		6		dB
Gain step	GST	2.75	3	3.25	dB

[4.4.4] ADC

Parameter	Symbol	Min	Typ	Max	Units	Condition
Resolution	RES		10		bit	
Operating clock frequency	FS		54		MHz	Progressive decode : Y signal
			27			Interlace decode : Y signal Progressive decode : PbPr signal
Intergral nonlinearity	INL		±1.0	±2.0	LSB	
Differential nonlinearity	DNL		±0.5	±1.0	LSB	
S/N	SN		53		dB	Fin=1MHz*, FS=54MHz, PGA GAIN default setting
S/(N+D)	SND		52		dB	Fin=1MHz*, FS=54MHz PGA GAIN default setting
Full scale Gain matching	IFGM			5	%	
ADC internal common voltage	VCOM		0.96		V	
ADC internal positive VREF	VRP		1.26		V	
ADC internal negative VREF	VRN		0.66		V	

*Fin = AIN input signal frequency

[4.4.5] Current consumption

(AVDD = DVDD = PVDD1 = PVDD2 = 1.8V, Ta = −40~85˚C)

Parameter	Symbol	Min	Typ	Max	Units	Condition
(Active mode)						
Total	IDD		110	151	mA	ADC 3ch operational(*1)
Analog block	AIDD		68		mA	ADC 3ch operational(*1)
			60		mA	YC: ADC 2ch operational(*2)
			35		mA	CVBS: ADC 1ch operational(*2)
Digital block	DIDD		28		mA	(*1) With crystal connected Load condition: CL=15pF
I/O block	PIDD		14		mA	
(Power down mode)						PDN=L(DVSS)(*3)
Total	SIDD		≤1	100	uA	
Analog block	ASIDD		≤1		uA	
Digital block	DSIDD		≤1		uA	
I/O block	PSIDD		≤1		uA	

(*1) Progressive YPbPr signal decode

(*2) Reference value

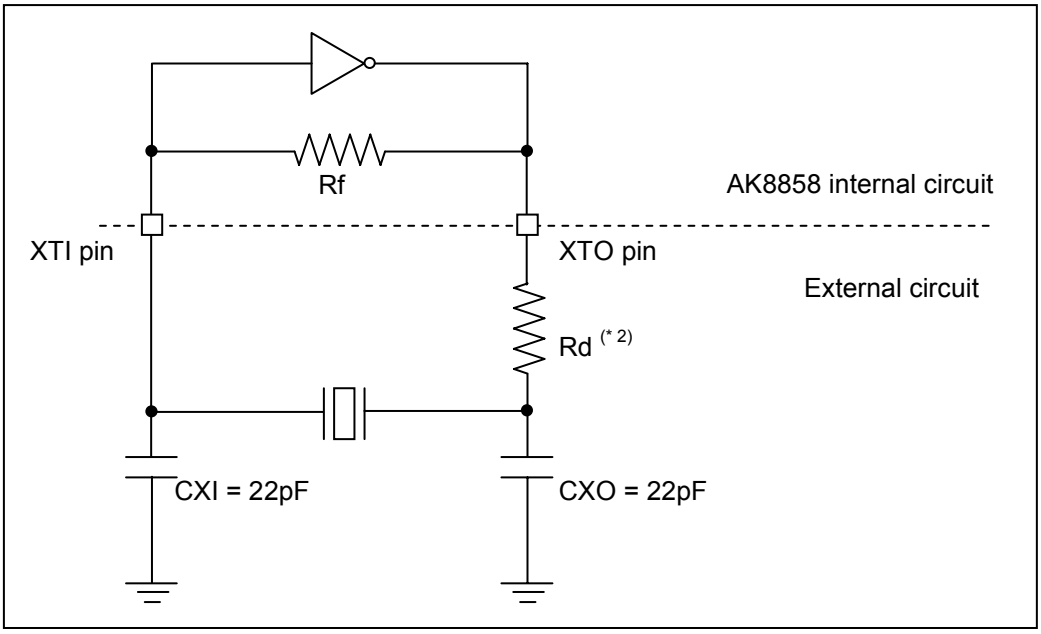
(*3) OE pin and RSTN pin must always be brought to the voltage polarity to be used or to ground level

[4.4.6] Crystal circuit block

Parameter	Symbol	Min	Typ	Max	Units	Notes
Frequency	f0		24.576		MHz	
Frequency tolerance	Δf / f			±100	ppm	
Load capacitance	CL		15		pF	
Effective equivalent resistance	Re			100	Ω	(*1)
Crystal parallel capacitance	CO		0.9		pF	
XTI terminal external connection load capacitance	CXI		22		pF	CL=15pF
XTO terminal external connection load capacitance	CXO		22		pF	CL=15pF

(*1) Effective equivalent resistance generally may be taken as Re = {R1 x (1+CO/CL)2}. (R1 is the crystal series equivalent resistance)

Example connection

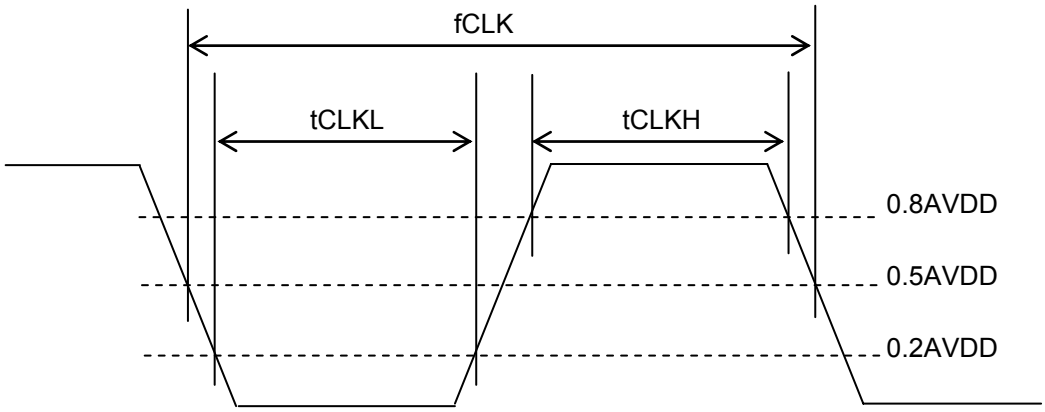


(*2) Determine need for and appropriate value of limiting resistance (Rd) in accordance with the crystal specifications.

[5] AC Timing

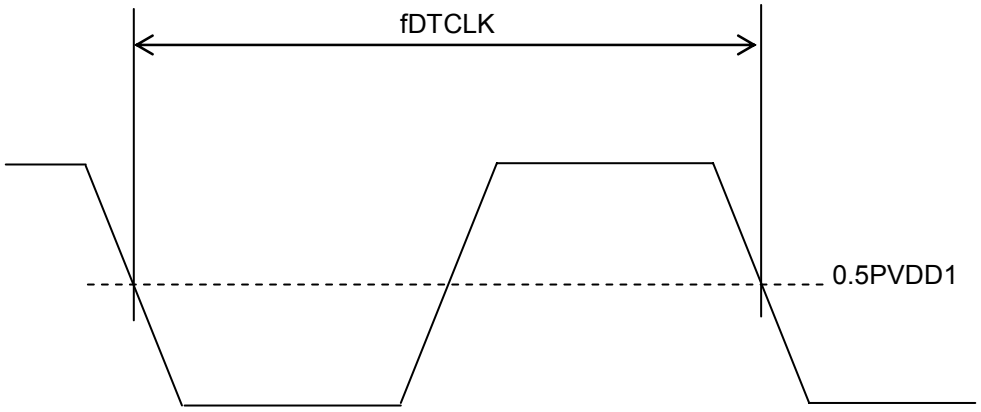
(1.70≤DVDD≤2.00, DVDD≤PVDD1≤3.60, DVDD≤PVDD2≤3.60)
(Ta = −40~85˚C, Load condition: CL=15pF)

[5.1] Clock input



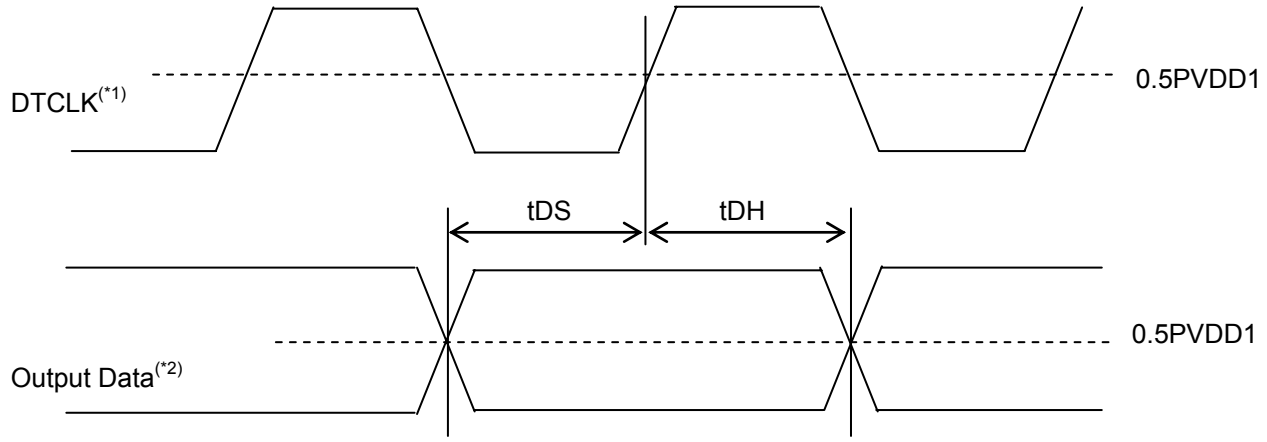
Parameter	Symbol	Min	Typ	Max	Units
Input CLK	fCLK		24.576		MHz
CLK pulse width H	tCLKH	16			nsec
CLK pulse widthL	tCLKL	16			
Frequency tolerance				±100	ppm

[5.2] Clock output (DTCLK output)



Parameter	Symbol	Min	Typ	Max	Units	Condition
DTCLK	fDTCLK		13.5		MHz	(Interlace) 16bit YCbCr output (Interlace) RGB output
			27			(Interlace) 8bit YCbCr output (Progressive) 16bit YCbCr output (Progressive) RGB output
			54			(Progressive) 8bit YCbCr output

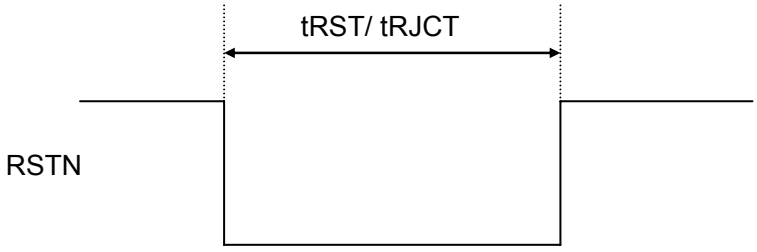
[5.3] Output data timing



Parameter	Symbol	Min	Typ	Max	Units	Condition
Output Data Setup Time	tDS	20			nsec	(Interlace) 16bit YCbCr output (Interlace) RGB output
		10				(Interlace) 8bit YCbCr output (Progressive) 16bit YCbCr output (Progressive) RGB output
		5				(Progressive) 8bit YCbCr output
Output Data Hold Time	tDH	20			nsec	(Interlace) 16bit YCbCr output (Interlace) RGB output
		10				(Interlace) 8bit YCbCr output (Progressive) 16bit YCbCr output (Progressive) RGB output
		5				(Progressive) 8bit YCbCr output

(*1) It is possible to invert the polarity of DTCLK by setting register. (Sub Address: 0x07[7]).
(*2)Output Data is general term of DATA [23:0], HD, VD_FLD and DVAL_FLD.

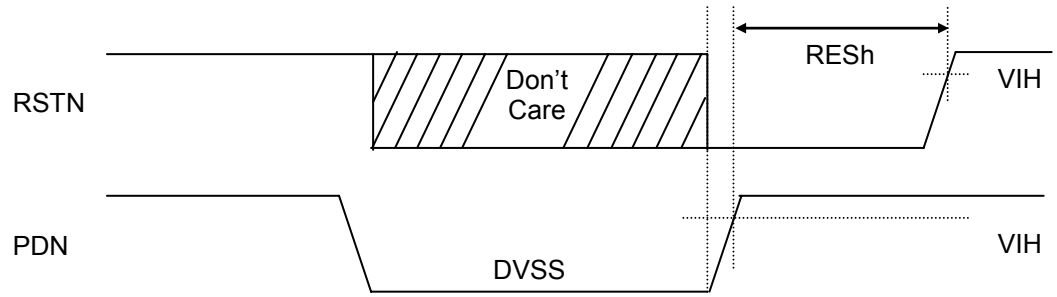
[5.4] Reset pulse



Parameter	Symbol	Min	Typ	Max	Units
RSTN pulse width	tRST	500			nsec
RSTN pulse eject	tRJCT			50	

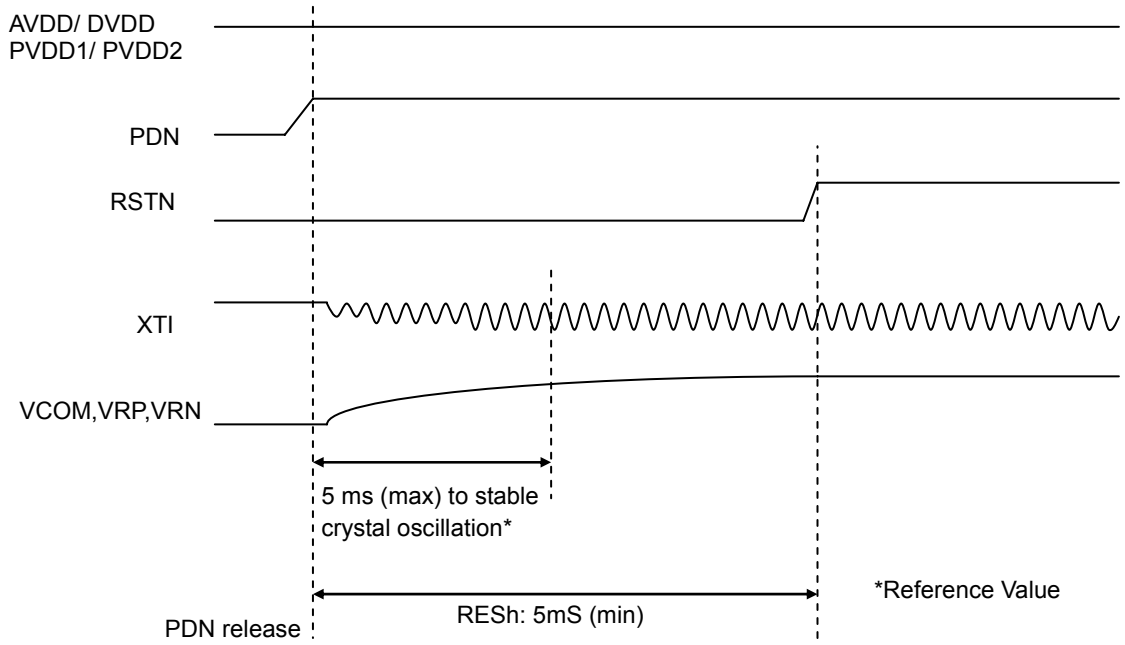
[5.5] Power-down release sequence

Reset must be applied after PDN release (PDN=Hi).

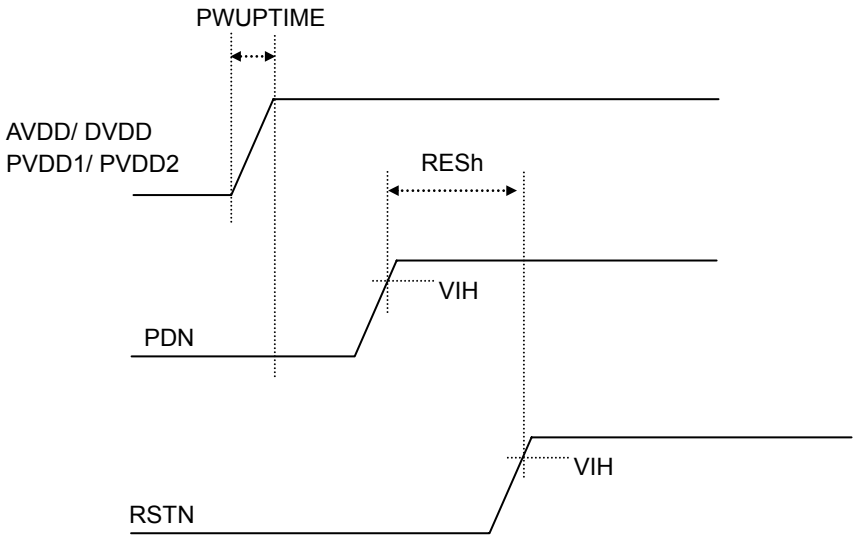


Parameter	Symbol	Min	Typ	Max	Units
Reset width after PDN release	RESh	5			ms

To perform power-down, all control signals must always be brought to the voltage polarity to be used or to ground level.



[5.6] Power-on sequence

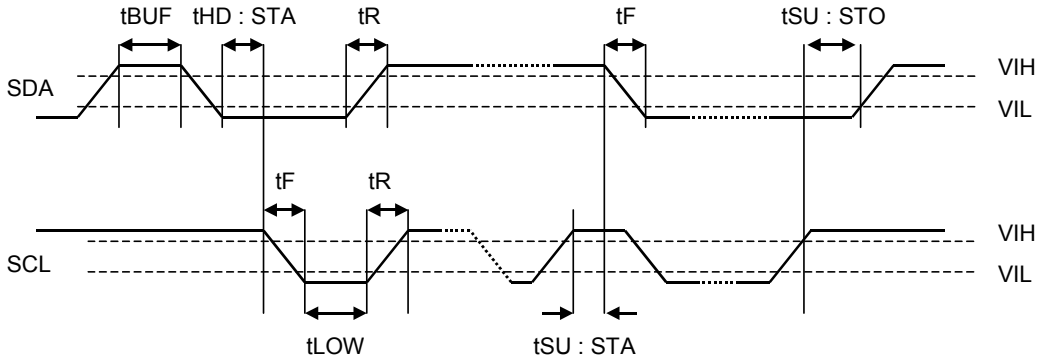


Parameter	Symbol	Min	Typ	Max	Units
POWERUP TIME	PWUPTIME			100	msec
Reset width after PDN release	RESh	5			

At power-on, PDN must be set to ground level (PDN=Low).
AVDD/DVDD/PVDD1/PVDD2 should be raised at power-on less than 100msec.
After PDN release, RSTN must stay on Low level more than 5msec.

[5.7] I2C bus input timing

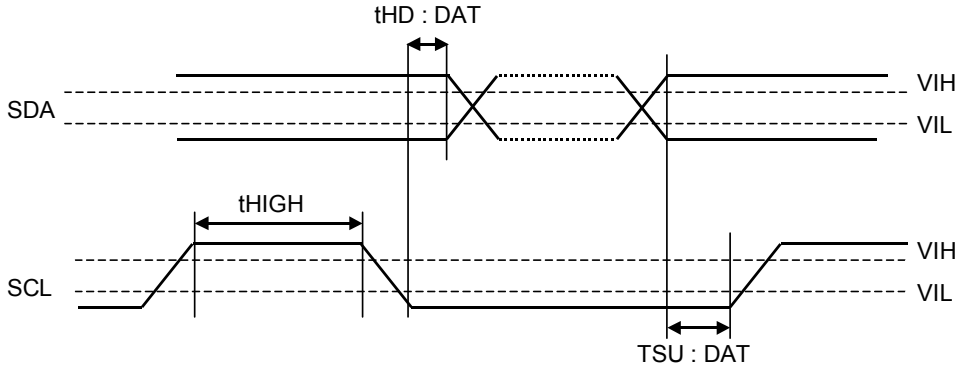
[5.7.1] Timing 1



Parameter	Symbol	Min	Max	Units
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

*The timing relating to the I2C bus is as stipulated by the I2C bus specification, and not determined by the device itself. For details, see I2C bus specification.

[5.7.2] Timing 2



Parameter	Symbol	Min	Max	Units
Data Setup Time	tSU:DAT	100(*1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9(*2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

(*1) If I2C is used in standard mode, tSU:DAT≥250ns is required.

(*2) This condition must be met if the AK8858 is used with a bus that does not extend tLOW (to use tLOW at minimum specification).

[6] Functional overview

The following key functions are characteristic of the AK8858 and its operational performance.

(1) It accepts composite video signal (CVBS), S-video and component YPbPr input with 10 input pins available for this purpose.The decode signal is selected via register setting.

(2) It contains an internal analog band limiting filter (anti-aliasing) in front of the AD converter input.

(3) Its analog circuit clamps the input signal to the sync tip (analog sync tip clamp). Its digital circuit clamps the digitized input data to the pedestal level (digital pedestal clamp).

(4) It has auto detection mode via register setting which automatically recognizes the input signal category.

(5) Its adaptive AGC function enables measurement of the input signal size and determination of the input signal level.

(6) Its ACC function enables measurement of the input signal color burst size and determination of the appropriate color burst level.

(7) It performs adaptive two-dimensional Y/C separation, in which its phase detector selects the best correlation from among vertical, horizontal, and diagonal samples and optimum Y/C separation mode.

(8) Its digital pixel spacing adjustor can align vertical positions by vertical pixel positioning.

(9) Its operated in line-locked, frame-locked, or fixed clock mode with automatic transition and optimum mode selection by automatic scanning.

(10) In PAL-B, D, G, H, I and N decoding, it can perform phase-difference correction for each line.

(11) Its output interface is ITU-R BT.656 (EAV/SAV) compliant. For connection of devices having no ITU-R BT.656 interface, it shows the active video region by HD/ VD/ DVALID/ FIELD signal output.

(12) Its output data format is in YCbCr format and RGB (8:8:8) format.

(13) It judges the chroma signal quality from the color burst of the input signal, and can apply color kill if the signal quality is judged insufficient. It can also apply color kill if the color decode PLL clock control.

(14) Its image quality adjustment function includes contrast, brightness, hue, color saturation, and sharpness adjustment.

(15) Its luminance and color signal band limiting filter are adjustable via register setting.

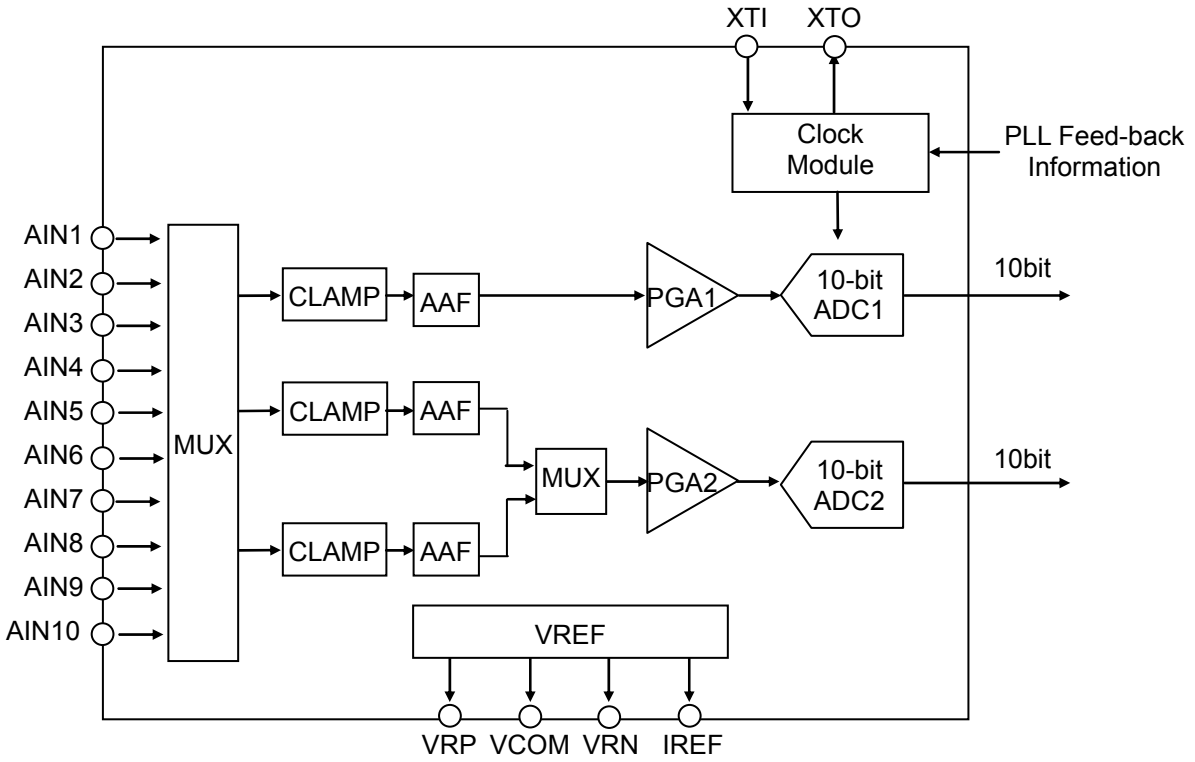
(16) It can decode conflated closed caption data, WSS signals, VBID(CGMS-A) and write them separately to the storage register.

(17) Its enables Macrovision signal type notification, in cases where the Macrovision signal is included in the decoded data.

[7] Functional description

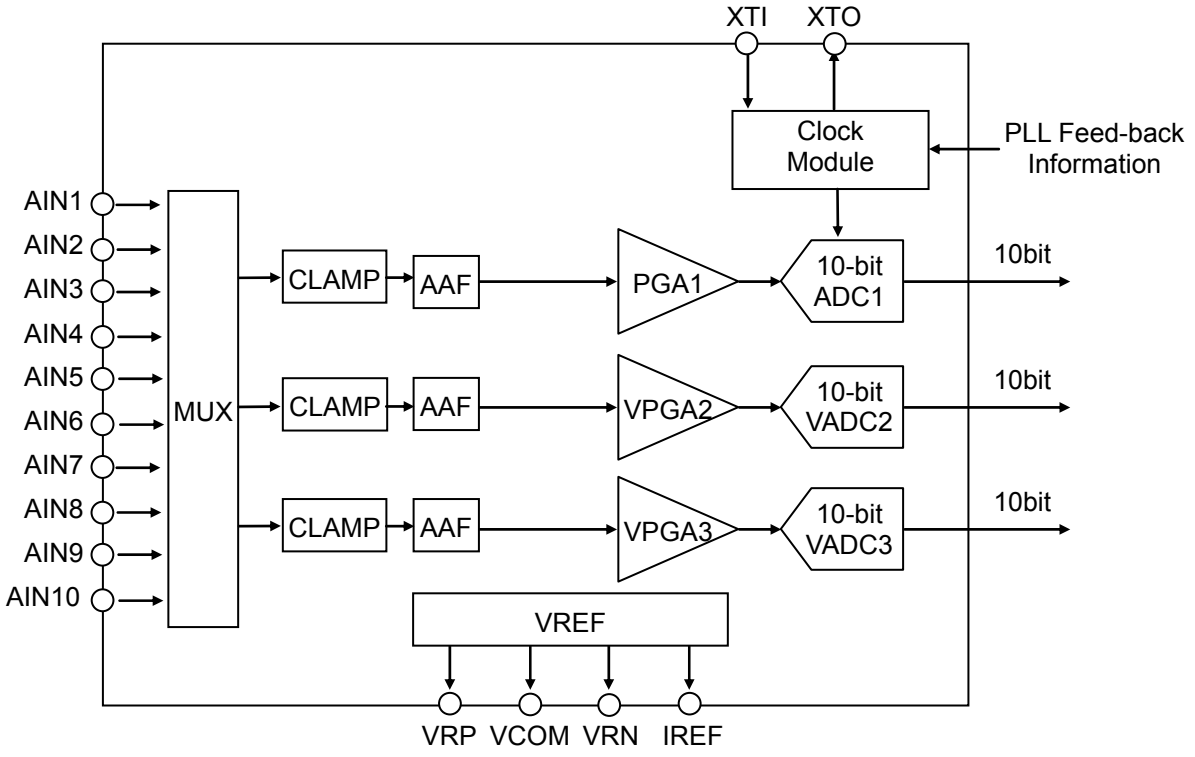
[7.1] Analog circuit description

Analog circuit block is shown below.



When decode YPbPr component video signal, Pb/Pr signal is converted to digital data by PGA2 and ADC2 after the data was sampled at sample hold circuit.

Time sharing operational status of ADC and PGA is shown below (PGA2 and ADC2 is shown as VPGA2, VADC2, VPGA3 and VADC3).



[7.1.1] CVBS signal decoding

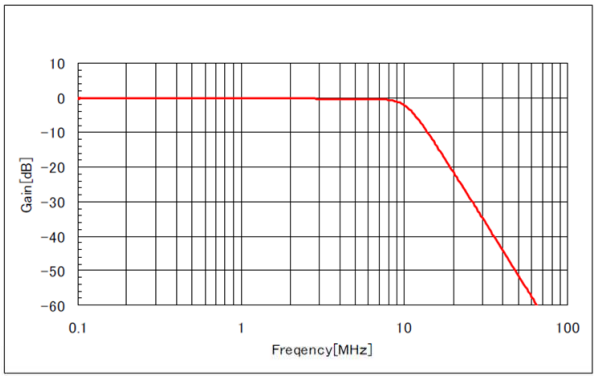
The data is converted to digital at PGA1 and ADC1. Sampling clock is 27MHz.
The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows: ±1dB (~6MHz), −30dB (27MHz)

[7.1.2] S(Y/C) video signal decoding

Y signal data is converted to digital at PGA1 and ADC1. Sampling clock is 27MHz.
C signal data is converted to digital at PGA2 and ADC2. Sampling clock is 27MHz.
The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows: ±1dB (~6MHz), −30dB (27MHz)

[7.1.3] 525i/625i YPbPr component video signal decoding

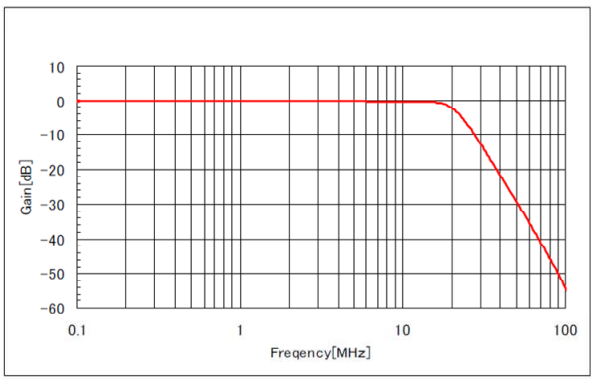
Y signal data is converted to digital at PGA1 and ADC1. Sampling clock is 27MHz.
Pb signal data is converted to digital at VPGA2 and VADC2. Sampling clock is 27MHz.
Pr signal data is converted to digital at VPGA3 and VADC3. Sampling clock is 27MHz.
The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows: ±1dB (~6MHz), −30dB (27MHz)



AAF Chracteristic (except Progressive)

[7.1.4] 525p/625p YPbPr component video signal decoding

Y signal data is converted to digital at PGA1 and ADC1. Sampling clock is 54MHz.
Pb signal data is converted to digital at VPGA2 and VADC2. Sampling clock is 27MHz.
Pr signal data is converted to digital at VPGA3 and VADC3. Sampling clock is 27MHz.
The characteristics of internal analog limiting filter (anti-aliasing), which is in front of the AD converter input, are as follows: ±1dB (~12MHz), −30dB (54MHz)



AAF Chracteristic (Progressive)

[7.2] Analog Interface

The AK8858 accepts composite video signal (CVBS), S(Y/C) video signal, YPbPr component video signal (D1/D2) input with 10 input pins available for this purpose.

Sub Address:0x00 Default Value:0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLKMOD	SELSRC1	SELSRC0	ADC3SEL	ADC2SEL	ADC1SEL2	ADC1SEL1	ADC1SEL0
Default Value							
0	0	0	0	0	0	0	0

The connection settings are shown below.

ADC1SEL[2:0]-bit: Input selection for ADC1. (for CVBS or Y)

Setting	ADC1 Input
000	AIN1
001	AIN2
010	AIN3
011	AIN4
100	AIN5
101	AIN6

ADC2SEL-bit: Input selection for ADC2 (VADC2). (for C or Pb)

Setting	ADC2 Input
0	AIN7
1	AIN8

ADC3SEL-bit: Input selection for ADC3 (VADC2). (for Pr)

Setting	ADC3 Input
0	AIN9
1	AIN10

SELSRC[1:0]-bit: Decode signal type setting bit.

Setting	Input signal
00	Composite (CVBS) video signal
01	S-Video signal
10	Component video signal
11	Analog power-down (CLAMP, AAF, PGA, ADC is power-down)

[7.3] Input Clock mode

CLKMOD-bit: Input clock setting bit.

Setting	Input clock
0	For crystal
1	External clock input (clock generator)

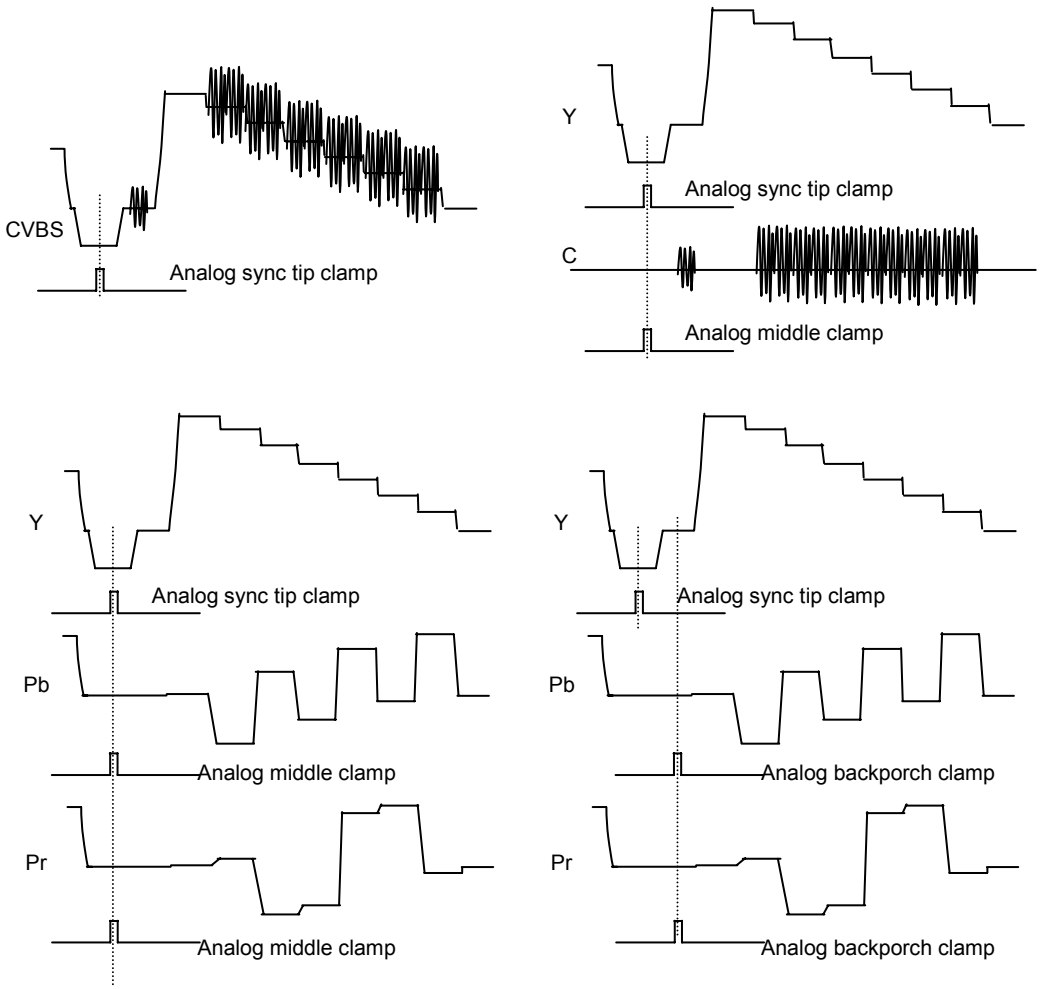
[7.4] Analog clamp circuit

The analog circuit of the AK8858 clamps the input signal to the reference level. The way to clamp the input signal is as follows.

The clamp timing pulse, with its origin at the falling edge of the internally synchronized and separated sync signal, is generated at approximately the central position of the sync signal.

Input signal		Clamp Level	Clamp pulse position
Composite (CVBS) video signal		Sync tip level	Sync tip
S(Y/C) video signal	Y signal	Sync tip level	Sync tip
	C signal	Pedestal level	Sync tip of Y
Component video signal	Y signal	Sync tip level	Sync tip
	Pb signal	Pedestal level	Clamp timing is performs by sync tip clamp or backporch clamp. If Pb and Pr signal have sync signl, set clamp timing to backporch clamp.
	Pr signal	Pedestal level	

Clamp Timing Pulse



Additionary, the AK8858 can change the position, width and current value of clamp pulse via register Clamp Control 1 Register (R/W) [Sub Address 0x01] and Clamp Control 2 Register (R/W) [Sub Address 0x02].

Sub Address: 0x01 Default Value: 0x00

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
CLP-WIDTH1	CLP-WIDTH0	CLP-STAT1	CLP-STAT0	Reserved	BCLP-STAT2	BCLP-STAT1	BCLP-STAT0
Default Value							
0	0	0	0	0	0	0	0

Sub Address: 0x02 Default Value: 0x01

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reserved	Reserved	Reserved	YPBPRCP	UDG1	UDG0	CLPG1	CLPG0
Default Value							
0	0	0	0	0	0	0	1

BCLPSTAT[2:0]-bit: Set the position of analog backporch clamp pulse.

Setting	Clamp position	Notes
000	Same position with “CLPSTAT” setting	
001	(1/128)H delay from “CLPSTAT” setting	
010	(2/128)H delay from “CLPSTAT” setting	
011	(3/128)H delay from “CLPSTAT” setting	
100	(4/128)H advance from “CLPSTAT” setting	
101	(3/128)H advance from “CLPSTAT” setting	
110	(2/128)H advance from “CLPSTAT” setting	
111	(1/128)H advance from “CLPSTAT” setting	

Set only the position of analog backporch clamp pulse.

CLPSTAT[1:0]-bit: Set the position of clamp pulse.

Setting	Clamp position	Notes
00	Sync tip/ middle/ bottom clamp: Center of horizontal sync Backporch clamp: Center of backporch interval	
01	(1/128)H delay	
10	(2/128)H advance	
11	(1/128)H advance	

The positions of all clamp pulse are changed.

CLPWIDTH[1:0]-bit: Set the clamp pulse width. Pulse width is change according to sampling clock units.

Setting	Clamp width	Notes
00	7 clock	Clock units 525i, 625i: 27MHz 525p, 625p: 54MHz
01	15 clock	
10	31 clock	
11	63 clock	

The width of all clamp pulse is changed.

YPBPRCP-bit: Set the clamp position of PbPr signal of YPbPR component video signal.

Setting	Clamp position	Notes
0	Sync tip timing	
1	Backporch timing	