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AK8859VN

NTSC/PAL/SECAM Digital Video Decoder

Overview

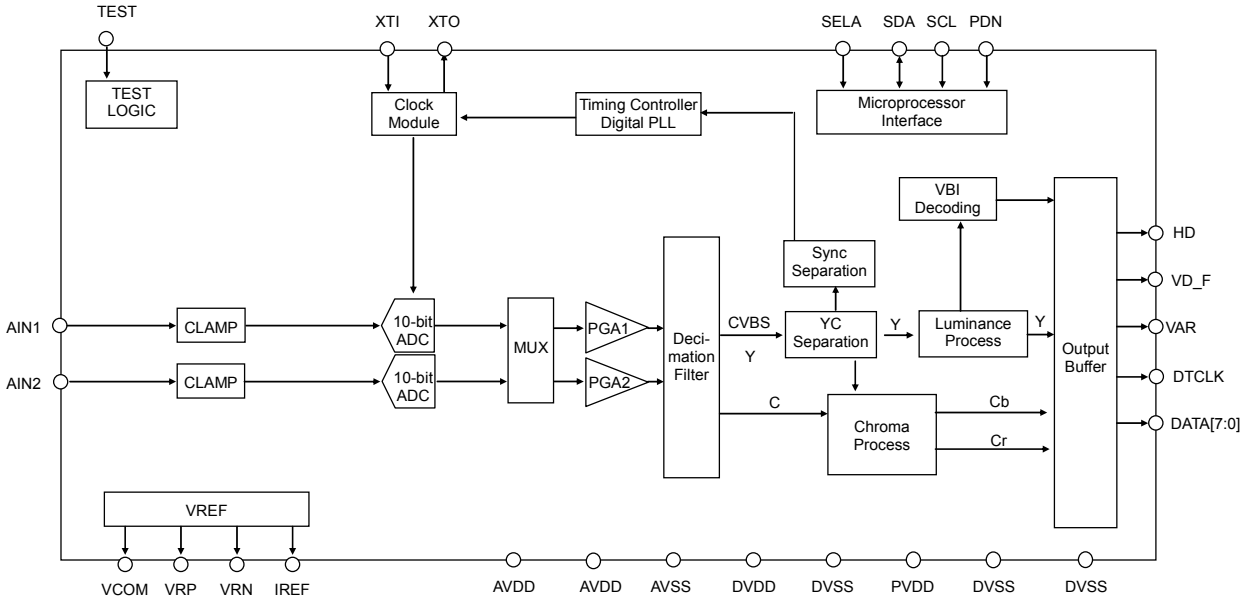
The AK8859VN is a single-chip digital video decoder for composite and S-video signals. Its output data is in YCbCr format and compliant with ITU-R BT.601 and ITU-R BT.656 standard interface. Its output also included HD / VD / FIELD and DVALID signals. Its operational temperature is between ranges of -40°C ~ 105°C. Microprocessor access is via I^2C interface.

Features

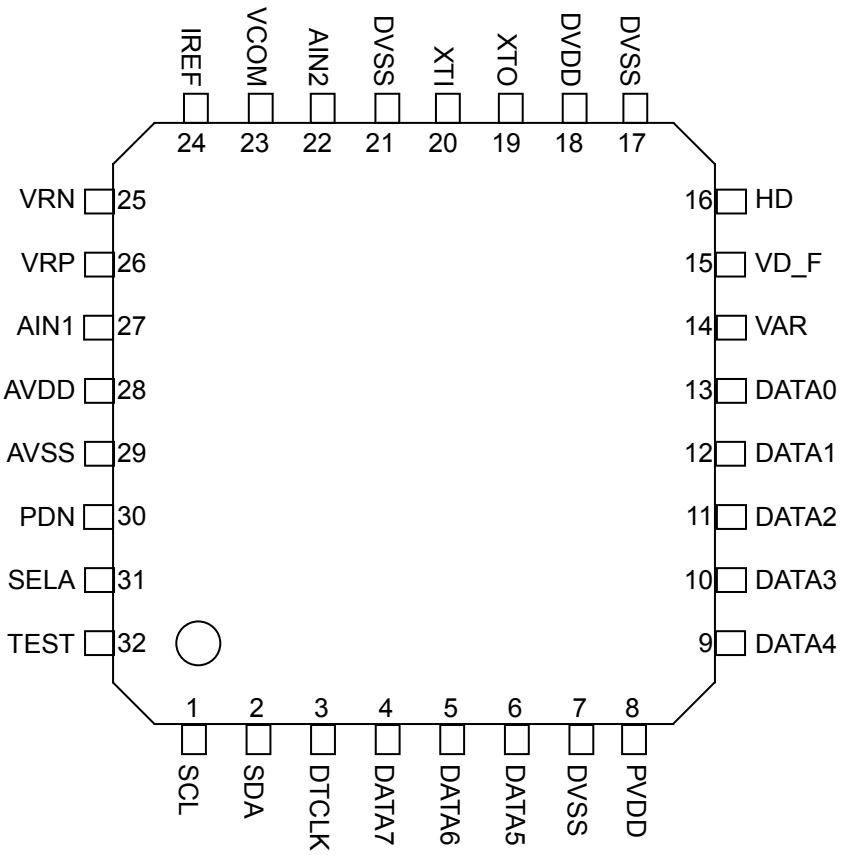
- Decodes composite and S-Video signals NTSC-J, M, 4.43 / PAL-B, D, G, H, I, N, Nc, M, 60 / SECAM
- 2 input channel
- 10-bit 27MHz ADC 2 channel
- Digital PGA
- Adaptive Automatic Gain Control (AGC)
- Auto Color Control (ACC)
- Image adjustment (Contrast, Saturation, Brightness, Hue, Sharpness)
- Automatic input signal detection
- Adaptive 2-D Y/C separation
- Output data format: ITU-R BT.601 (YCbCr, 4:2:2, 8bit)
- Output interface: ITU-R BT.656 (4:2:2, 8bit parallel) with EAV/SAV
  HD, VD, FIELD and DVALID signal timing output
- Closed Caption signal decoding (output via register)
- VBID (CGMS-A) signal decoding (output via register)
- WSS signal decoding (output via register)
- Macrovision signal detection (Macrovision certification)
- Powerdown function
- I^2C control
- Core supply voltage: 1.70 ~ 2.00V
- I/O power supply: 1.70 ~ 3.60V
- Operating temperature: -40°C ~ 105°C
- 32-pin QFN package (5.0mm x 5.0mm)

Contents

[1.] Functional block diagram



[2.] Pin assignment



[3.] Pin function description
[3.1.] Pin function

Pin No.	Symbol	P/S	I/O	Functional Description
1	SCL	P	I	I^2C clock input pin. Connect to PVDD via a pull-up register. Hi-z input possible when PDN=L.
2	SDA	P	I/O	I^2C data pin. Connect to PVDD via a pull-up register. Hi-z input possible when PDN=L.
3	DTCLK	P	O	Data clock output pin. The output clock is approximately 27MHz.
4	DATA7	P	O (I/O)	DATA output pin (MSB).
5	DATA6	P	O (I/O)	DATA output pin.
6	DATA5	P	O (I/O)	DATA output pin.
7	DVSS	D	G	Digital ground pin.
8	PVDD	P	P	I/F power supply pin.
9	DATA4	P	O (I/O)	DATA output pin.
10	DATA3	P	O (I/O)	DATA output pin.
11	DATA2	P	O (I/O)	DATA output pin.
12	DATA1	P	O (I/O)	DATA output pin.
13	DATA0	P	O (I/O)	DATA output pin (LSB).
14	VAR	P	O (I/O)	DVALID / FIELD / NSIG / LINE signal output pin. DVALID/FIELD/NSIG/LINE signal output can be selected by register setting.
15	VD_F	P	O (I/O)	VD / FIELD signal output pin. VD/ FIELD signal output can be selected by register setting.
16	HD	P	O (I/O)	HD signal output pin.
17	DVSS	D	G	Digital ground pin.
18	DVDD	D	P	Digital power supply pin.
19	XTO	D	O	Crystal connection pin. Use 24.576 MHz crystal. When PDN=L, output level is DVSS. If crystal is not used, connect to NC or DVSS.
20	XTI	D	I	Crystal connection pin. Use 24.576 MHz crystal resonator. For input from 24.576 MHz crystal oscillator, use this pin.

[Power Supply]: A-AVDD, D-DVDD, P-PVDD
[I/O]: I–Input pin, O–Output pin, I/O–In Out pin, P–Power Supply pin, G–Ground pin
See section [3.2.](Output pin state) for relationship between PDN-pin and each register.

Pin No.	Symbol	P/S	I/O	Functional Description
21	DVSS	D	G	Digital ground pin.
22	AIN2	A	I	Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
23	VCOM	A	O	Common internal voltage for AD converter. Connect to AVSS via ≥0.1μF (+/−5% accuracy) ceramic capacitor.
24	IREF	A	O	Analog circuit reference current setting pin. Connect to AVSS via 6.8KΩ (+/−1% accuracy) resistor.
25	VRN	A	O	Internal reference negative voltage pin for AD converter. Connect to AVSS via ≥0.1 μF (+/−1% accuracy) ceramic capacitor.
26	VRP	A	O	Internal reference positive voltage pin for AD converter. Connect to AVSS via ≥0.1 μF (+/−1% accuracy) ceramic capacitor.
27	AIN1	A	I	Analog video signal input pin. Connect via 0.033μF capacitor and voltage-splitting resistors. If not used, connect to NC.
28	AVDD	A	P	Analog power supply pin.
29	AVSS	A	G	Analog ground pin.
30	PDN	P	I	Power-down control pin. Hi-z input is prohibited. Low: Power-down. High: Normal operation.
31	SELA	P	I	I^2C bus address selector pin.
32	TEST	P	I	Pin for test mode setting. Connect to DVSS.

[Power Supply]: A-AVDD, D-DVDD, P-PVDD
[I/O]: I–Input pin, O–Output pin, I/O–In Out pin, P–Power Supply pin, G–Ground pin
See section [3.2.](Output pin state) for relationship between PDN-pin and each register.

[3.2.] Output pin state

PDN -pin	Register setting					Digital output pins state				
	OEN -bit	DL -bit	VD_FL -bit	VAR -bit	HL -bit	DATA[7:0]	VD_F	VAR	HD	DTCLK
L	X	X	X	X	X	Low				
H	H	X	X	X	X	Hi-z				
H	L	L	L	L	L	DOUT	DOUT	DOUT	DOUT	DOUT
H	L	H	H	H	H	Low	Low	Low	Low	DOUT

[4.] Electrical characteristics

[4.1.] Absolute maximum ratings

Parameter		Min.	Max.	Unit	Notes
Supply voltage	AVDD, DVDD	-0.3	2.2	V	
	PVDD	-0.3	4.2		
Analog input pin voltage		-0.3	AVDD+0.3(≦2.2)	V	
Digital input pin voltage D		-0.3	DVDD+0.3(≦2.2)	V	XTI,XTO pin
Digital output pin voltage P		-0.3	PVDD+0.3(≦4.2)	V	(*1)
Input pin current (Iin)		-10	10	mA	Power supply pin is not included.
Storage temperature		-40	125	°C	

(*1) Collective term for DTCLK, DATA[7:0], HD, VD_F, VAR, SELA, PDN, SDA, SCL, TEST pins.

- The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0V (Reference Voltage).
- All power supply grounds (AVSS, DVSS) should be at the same electric potential.
- If digital output pins are connected to data bus, the data bus operating voltage should be in the same range as shown above from the digital output pin.
- The setting other than above may cause the eternal destruction to the device.
- Normal operational is not guaranteed for the above setting.

[4.2.] Recommended operating conditions

Parameter	Min.	Typ.	Max.	Unit	Condition
Analog supply voltage (AVDD) Digital supply voltage (DVDD)	1.70	1.80	2.00	V	AVDD=DVDD
I/F supply voltage (PVDD)	1.70	1.80	3.60	V	PVDD≧DVDD
Operating temperature (Ta)	-40		105	°C	

- The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0V (Reference Voltage).
- All power supply grounds (AVSS, DVSS) should be at the same electric potential.

[4.3.] DC characteristics

(Ta: -40°C~105°C / DVDD=AVDD=1.7V~2.0V / PVDD=DVDD~3.6V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Digital input high voltage(*1)	VIH	0.7PVDD			V	
Digital input low voltage(*1)	VIL			0.3PVDD	V	
Digital input leak current(*1)	IL			±10	uA	
Digital output high voltage(*2)	VOH	0.8PVDD			V	IOH = -600uA
Digital output low voltage(*2)	VOL			0.2PVDD	V	IOL = 1mA
Digital output Hi-z leak current(*2)	HIL			±10	uA	
I^2C (SDA)L output	VOLC			0.4 0.2PVDD	V	IOLC = 3mA PVDD≧2.0V PVDD＜2.0V
XTI input high voltage	VXIH	0.8DVDD			V	
XTI input low voltage	VXIL			0.2DVDD	V	

(*1) Collective term for SELA, PDN, SDA, SCL, TEST pins.

(*2) Collective term for DTCLK, DATA[7:0], HD, VD_F, VAR pins.

[4.4.] Analog characteristics

(AVDD=1.8V, Ta=25˚C)

[4.4.1.] Input range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input range	VIMX	0	0.50	0.60	Vpp	

[4.4.2.] ADC

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Resolution	RES		10		bit	
Operating clock frequency	FS		27		MHz	
Integral nonlinearity	INL		±1.0	±2.0	LSB	
Differential nonlinearity	DNL		±0.5	±1.0	LSB	
S/N	SN		53		dB	Fin=1MHz*, FS=27MHz, Input range=0.6Vpp
S/(N+D)	SND		51		dB	Fin=1MHz*, FS=27MHz, Input range=0.6Vpp
ADC internal common voltage	VCOM		0.96		V	
ADC internal positive VREF	VRP		1.36		V	
ADC internal negative VREF	VRN		0.56		V	

[4.4.3.] Current consumption

(AVDD = DVDD = PVDD = 1.8V, Ta = -40 ~ 105˚C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
（Active mode）						
Total	IDD		45	62	mA	S(Y/C) video signal input
Analog block	AIDD		27		mA	S(Y/C) video signal input
			19		mA	Composite video signal input*
			10		mA	No-signal input*
Digital block	DIDD		13		mA	S(Y/C) video signal input With crystal (Xtal) connected. Load condition: CL=15pF
I/F block	PIDD		5		mA	
（Power down mode）						
Total	SIDD		≦1	200	uA	
Analog block	ASIDD		≦1		uA	
Digital block	DSIDD		≦1		uA	
I/F block	PSIDD		≦1		uA	

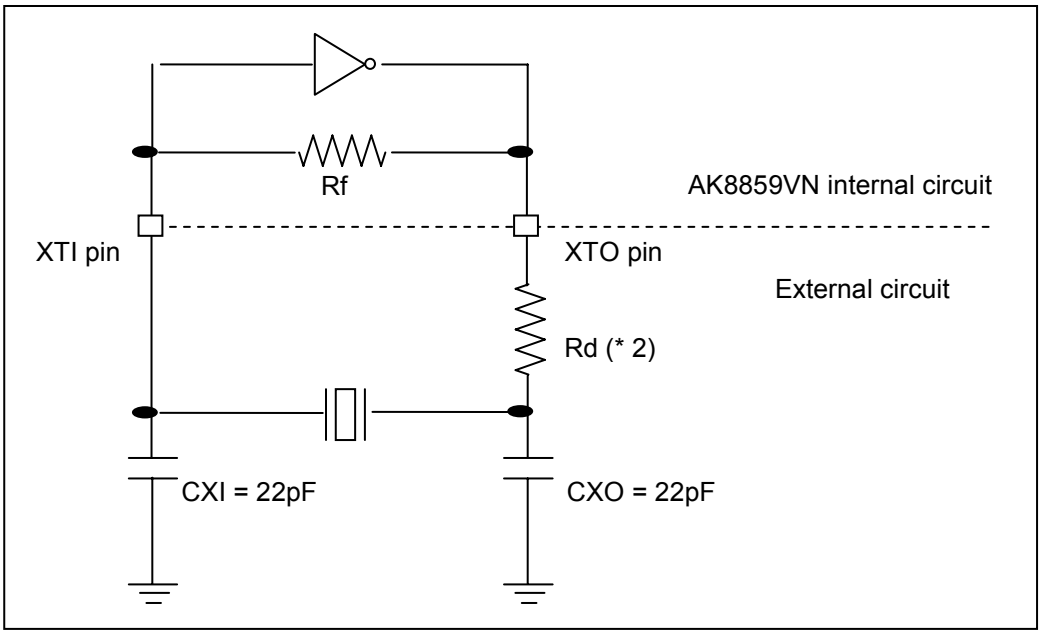
*Reference value.

[4.4.4.] Crystal circuit block

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Frequency	f0		24.576		MHz	
Frequency tolerance	Δf / f			±100	ppm	
Load capacitance	CL		15		pF	
Effective equivalent resistance	Re			100	Ω	(*1)
Crystal parallel capacitance	CO		0.9		pF	
XTI terminal external connection load capacitance	CXI		22		pF	If CL=15pF
XTO terminal external connection load capacitance	CXO		22		pF	If CL=15pF

(*1) Effective equivalent resistance generally may be taken as Re = R1 x $(1+CO/CL)^2$, where R1 is the crystal series equivalent resistance.

Example connection

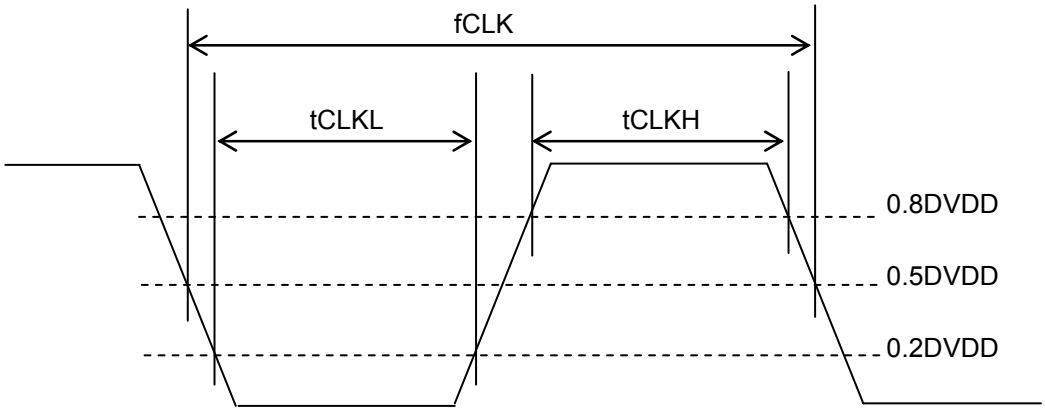


(*2) Determine need for and appropriate value of limiting resistance (Rd) in accordance with the crystal specifications.

[5.] AC Timing

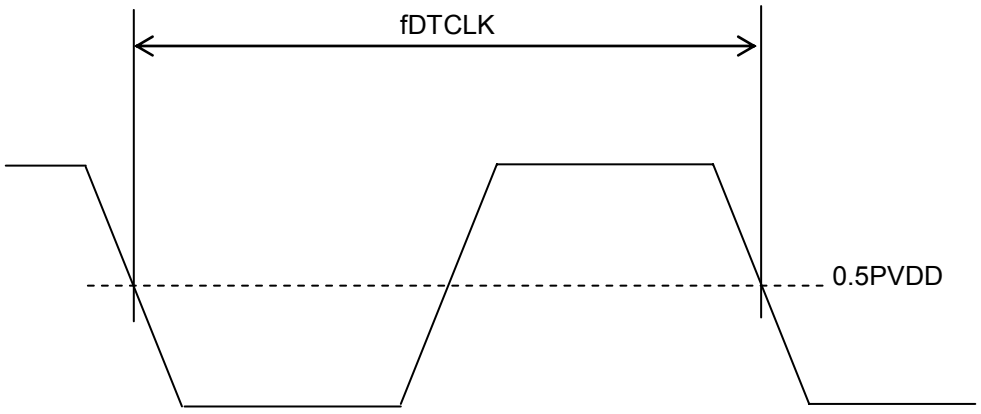
(1.70≦DVDD≦2.00, DVDD≦PVDD≦3.60, Load condition: CL=15pF)

[5.1.] External clock input



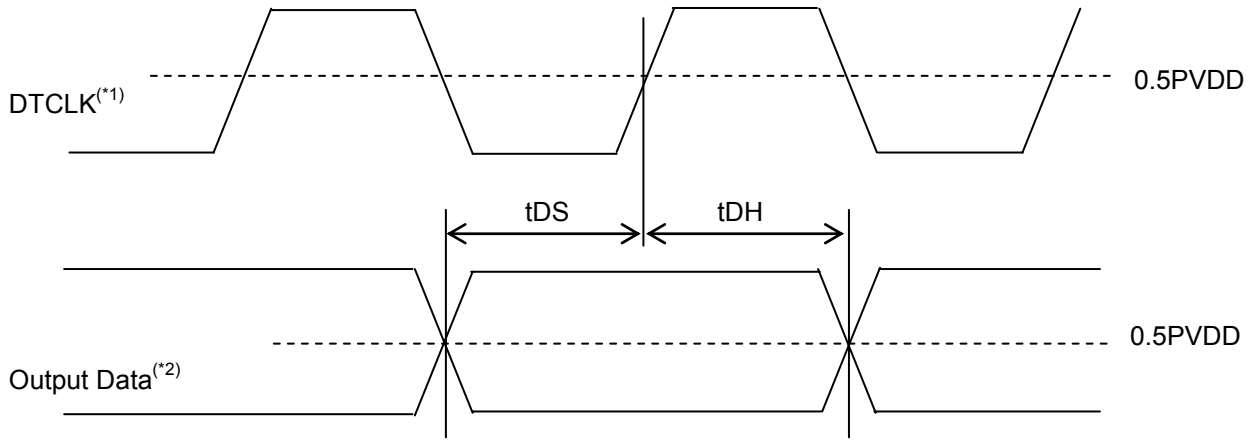
Parameter	Symbol	Min.	Typ.	Max.	Unit
Input CLK	fCLK		24.576		MHz
CLK pulse width H	tCLKH	16			nsec
CLK pulse width L	tCLKL	16			nsec
Frequency tolerance				±100	ppm

[5.2.] Clock output (DTCLK)



Parameter	Symbol	Min.	Typ.	Max.	Unit
DTCLK	fDTCLK		27		MHz

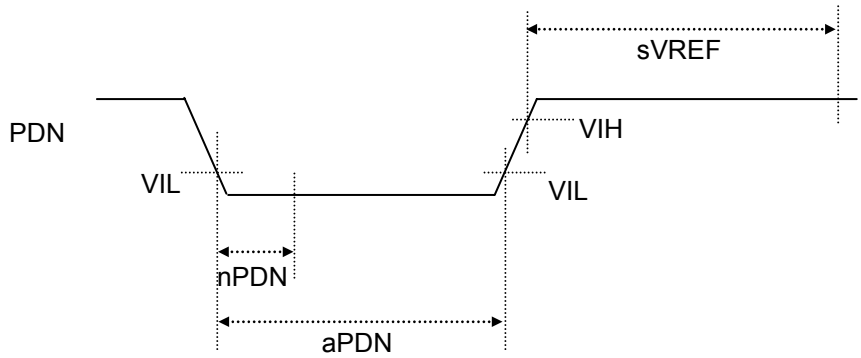
[5.3.] Output data timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
Output Data Setup Time	tDS	10			nsec
Output Data Hold Time	tDH	10			nsec

(*1) It is possible to invert the polarity of DTCLK via register setting.
(*2) Output Data is general term of DATA[7:0], HD, VD_F, and VAR.

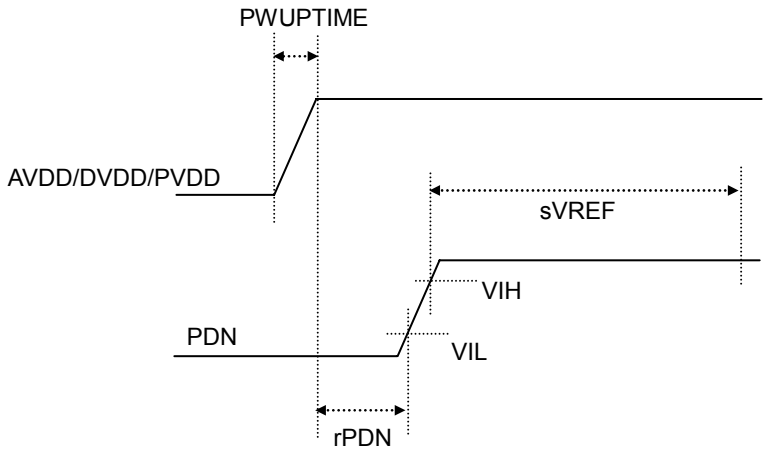
[5.4.] Power down sequence



Parameter	Symbol	Min.	Typ.	Max.	Unit
Power down pulse removal period	nPDN			50	nsec
Power down pulse width	aPDN	500			nsec
VREF stabilization period	sVREF	10			msec

At power down, DTCLK pin, DATA[7:0] pin, HD pin, VD_F pin and VAR pin is Low output.
After power down released, DATA[7:0] pin, HD pin, VD_F pin and VAR pin is stay Low output if no register setting apply. Register setting only apply after VREF stabilization period.

[5.5.] Power-on sequence

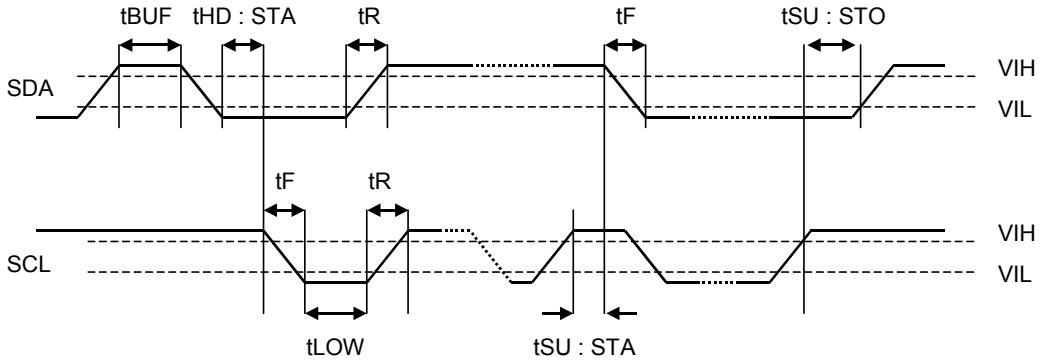


Parameter	Symbol	Min.	Typ.	Max.	Unit
POWERUP TIME	PWUPTIME			100	msec
Power down release	rPDN	500			nsec
VREF stabilization period	sVREF	10			msec

At power-on, PDN must be set to ground level (PDN=Low).
AVDD/DVDD/PVDD should be raised at power-on less than 100msec.
After power down released, DATA[7:0] pin, HD pin, VD_F pin and VAR pin is stay Low output if no register setting apply. Register setting only apply after VREF stabilization period.

[5.6.] I²C bus input timing

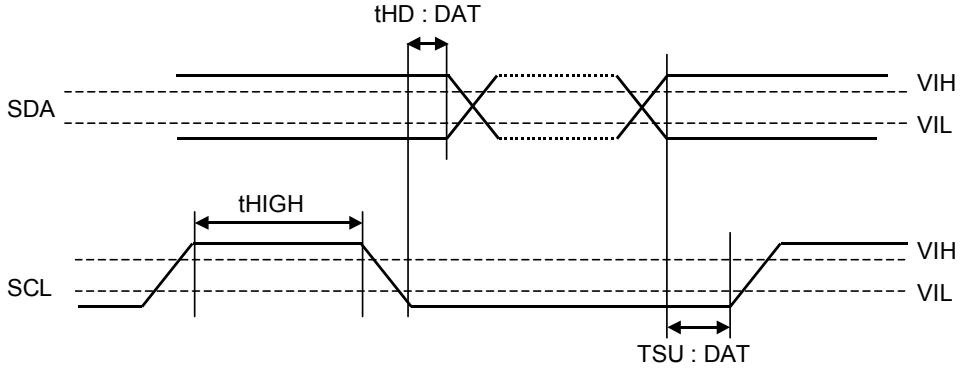
[5.6.1.] Timing 1



Parameter	Symbol	Min.	Typ.	Unit
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

Note : The timing relating to the I²C bus is as stipulated by the I²C bus specification, and not determined by the device itself. For details, see I²C bus specification.

[5.6.2.] Timing 2



Parameter	Symbol	Min.	Max.	Unit
Data Setup Time	tSU:DAT	100(*1)		nsec
Data Hold Time	tHD:DAT	0.0	0.9(*2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

(*1) If I²C is used in standard mode, tSU: DAT ≥250ns is required.

(*2) This condition must be met if the AK8859VN is used with a bus that does not extend tLOW (to use tLOW at minimum specification).

[6.] Functional overview

○ It accepts composite video signal (CVBS) and S-Video with 2 input pins available for this purpose. The decode signal is selected via register setting.

○ It can decode the following input video signal via register setting:
- NTSC-M, J / NTSC-4.43 / PAL-B,D,G,H,I,N / PAL-Nc / PAL-M / PAL-60 / SECAM
- In addition, it has auto detection mode via register setting which automatically recognizes the input signal category.

○ It output interface is ITU-R BT.656 compliant.
(It may not be possible, however to meet these requirement if the input signal quality is poor.)

○ For connection of devices having no ITU-R BT.656 interface, it shows the active video region by DVALID signal output.

○ Its analog circuit of the AK8859VN clamps the input signal to the sync tip. Its digital circuit clamps the digitized input data to the pedestal level.

○ Its VBI data slicing function enables output of the slicing results as ITU-R BT.601 format digital data.

○ It has digital PGA built internally and can be adjusted in the range of −4.06dB～6.90dB by register setting.

○ Its adaptive AGC function enables measurement of the input signal size and determination of the input signal level.

○ It performs adaptive two-dimensional Y/C separation, in which its phase detector selects the best correlation from among vertical, horizontal, and diagonal samples and optimum Y/C separation mode.

○ Its digital pixel spacing adjustor can align vertical positions by vertical pixel positioning.

○ Its operates in line-locked, frame-locked, or fixed clock mode with automatic transition and optimum mode selection by automatic scanning.

○ Its ACC function enables measurement of the input signal color burst size and determination of the appropriate color burst level.

○ It judges the chroma signal quality from the color burst of the input signal, and can apply color kill if the signal quality is judged insufficient. It can also apply color kill if the color decode PLL clock control.

○ Its image quality adjustment function includes contrast, brightness, hue and color saturation adjustment.

○ It can decode conflated Closed Caption Data, Closed Caption Extended Data, WSS, VBID(CGMS-A) and write them separately to the storage register.

○ Its monitoring register enables monitoring of a number of internal functions.

○ Its enables Macrovision signal type notification, in cases where the Macrovision signal is included in the decoded data.

[7.] Functional Description

[7.1.] Analog interface

The AK8859VN accepts composite (CVBS) and S-Video (Y/C) signals, with 2 input pins available for this purpose. The decode signal is selected via the register.

Input signal selection Sub Address: 0x00 [1:0]

Name	Definition	Notes
AINSEL0 ~ AINSEL1	[AINSEL1 : AINSEL0] [00]: AIN1 (CVBS) [01]: AIN2 (CVBS) [10]: AIN1(Y) / AIN2(C) (S-Video) [11]: No-signal input (Analog circuit is set to power-down*)	

*Clamp and ADC block is power-downed.

In used with AINSEL[1:0]=[11], Ouput data is depend on NSIGMD[1:0]–bit. However, in used with NSIGMD[1:0]=[10], DATA[7:0]-pin, HD-pin, VD_F-pin and VAR-pin output Low.

[7.2.] Clock mode

The AK8859VN input clock can be selected between internal built crystal and external clock input via register setting. The input clock frequency is 24.576MHz.

Clock mode setting Sub Address: 0x00 [7]

Name	Definition	Notes
CLKMD	[0]: For crystal [1]: External clock input (clock generator)	

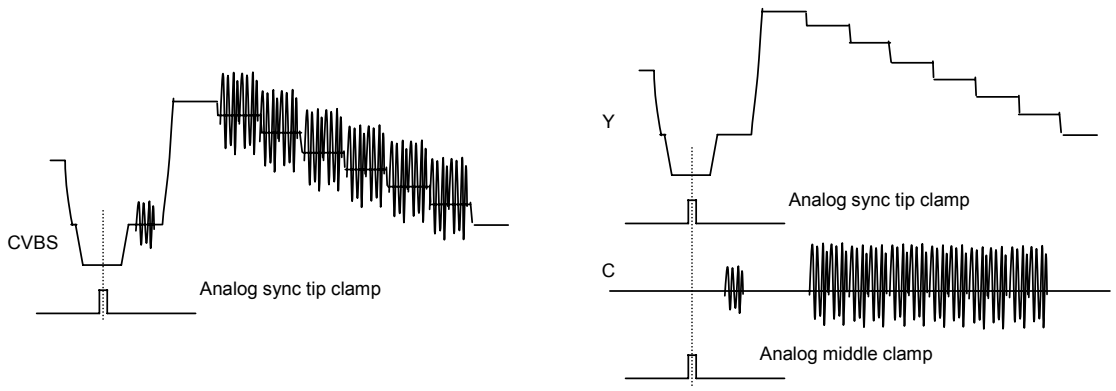
[7.3.] Analog clamp circuit

The analog circuit of AK8859VN clamps the input signal to the reference level. The way to clamp the input signal is show as follows.

○ When decode composite (CVBS) video signal
Clamp timing is performs by sync tip clamp (analog sync tip clamp).
The clamp timing pulse, with its origin at the falling edge of the internally synchronized and separated sync signal, is generated at approximately the central position of the sync signal.

○ When decode S-Video (Y/C) signal
(Y signal): Clamp timing is performs by sync tip clamp (analog sync tip clamp).
The clamp timing pulse, with its origin at the falling edge of the internally synchronized and separated sync signal, is generated at approximately the central position of the sync signal.
(C signal): Clamp timing is performs by middle clamp (analog middle clamp).
The clamp timing pulse is generated exactly at the same timing of Y signal clamp pulse.

Clamp timing pulse



Furthermore, the AK8859VN can change the position, width, and current value of clamp pulse via register.

Set the current value of clamp in analog block Sub Address: 0x01 [1:0]

Name	Definition	Notes
CLPG0 ~ CLPG1	[00]: Min. [01]: Middle 1 {=(Min. x 3)} [10]: Middle 2 {=(Min. x 5)} [11]: Max. {=(Min. x 7)}	Default setting is [00]

Set the clamp pulse width Sub Address: 0x01 [4]

Name	Definition	Notes
CLPWIDTH	[0]: 275nsec [1]: 555nsec	Default setting is [0]

[7.4.] Input video signal categorization

The AK8859VN video input signal categorization can be selected via register. The AK8859VN can decode the following video signal:

NTSC-M, J
NTSC-4.43
PAL-B, D, G, H, I, N
PAL-Nc
PAL-M
PAL-60
SECAM

Input video signal categorization register setting is show as follows.

Subcarrier frequency setting Sub Address: 0x02 [1:0]

Name	Definition	Notes
VSCF0 ~ VSCF1	[VSCF1 : VSCF0] (MHz) [00]: 3.57954545 (NTSC-M,J) [01]: 3.57561149 (PAL-M) [10]: 3.58205625 (PAL-Nc) [11]: 4.43361875(PAL-B,D,G,H,I,N,60, NTSC-4.43, SECAM)	

Color encode format setting Sub Address: 0x02 [3:2]

Name	Definition	Notes
VCEN0 ~ VCEN1	[VCEN1 : VCEN0] [00]: NTSC [01]: PAL [10]: SECAM [11]: Reserved	

Line frequency setting Sub Address: 0x02 [4]

Name	Definition	Notes
VLF	[0]: 525-Line (NTSC-M,J, NTSC-4.43, PAL-M,60) [1]: 625-Line (PAL-B,D,G,H,I,N, PAL-Nc, SECAM)	

Monochrome mode setting Sub Address: 0x02 [5]

Name	Definition	Notes
BW	[0]: Not monochrome (monochrome mode OFF) [1]: Decode as monochrome signal (monochrome mode ON)	

When composite video signal decode is selected, in the monochrome mode (BW=1), the input signal is treated as a monochrome signal, and all sampling data digitized the AD converter passes through the luminance process and is processed as luminance signal, and the CbCr code is output as 0x80 (601 level data) regardless of the input. When S-video (Y/C) signal decode is selected, only luminance signal is decode as an output.

Setup processing setting Sub Address: 0x02 [6]

Name	Definition	Notes
SETUP	[0]: Setup absent setting [1]: Setup present setting	

With the Setup present setting, the luminance and color signals are processed as follows:
Yout = (Yin-7.5)/0.925
Uout = Uin/0.925, Vout = Vin/0.925

[7.5.] Auto detection mode of input signal

The video input signal of the AK8859VN can be automatically detected (auto detection mode) via register.

Settings for auto detection mode of input signal Sub Address: 0x02 [7]

Name	Definition	Notes
AUTODET	[0]: OFF (manual setting) [1]: ON	

In auto detection mode, the AK8859VN can detect the following parameters.

Number of lines per frame:

525 (Line)
625 (Line)

Subcarrier frequency:

3.57954545 (MHz)
3.57561149 (MHz)
3.58205625 (MHz)
4.43361875 (MHz)

Color encoding formats:

NTSC
PAL
SECAM

Monochrome signal*:

Not monochrome
Monochrome

(*Note: Automatic monochrome detection is active if the color kill setting is ON.)

The detected result of auto detection mode is reflected to Input Video Status Register.
This enables the host to distinguish among the formats NTSC-M,J / NTSC-4.43 / PAL-B,D,G,H,I,N / PAL-M / PAL-Nc / PAL-60 / SECAM and monochrome.
It should be noted that it does not detect NTSC-M, NTSC-J or PAL-B,D,G,H,I,N formats.

Sub Address: 0x18 “Input Video Status Register”

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FIXED	UNDEF	ST_B/W	ST_VLF	ST_VCEN1	ST_VCEN0	ST_VSCF1	ST_VSCF0

[7.6.] Limiting auto detection candidates of input signal

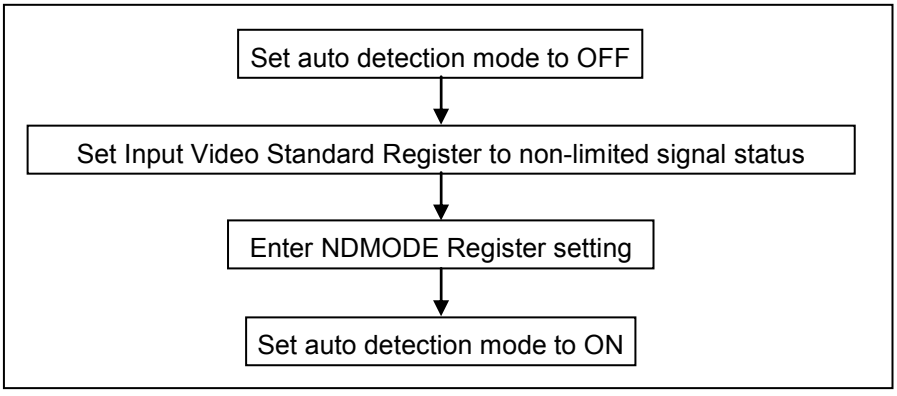
In auto detection mode, the candidates for detection can be limited via register.

Sub Address: 0x03 “NDMODE Register”

Name	Definition	Notes
NDPALM	[0]: PAL-M candidate [1]: PAL-M non-candidate	
NDPALNC	[0]: PAL-Nc candidate [1]: PAL-Nc non-candidate	
NDSECAM	[0]: SECAM candidate [1]: SECAM non-candidate	
Reserved	Reserved	
NDNTSC443	[0]: NTSC-4.43 candidate [1]: NTSC-4.43 non-candidate	
NDPAL60	[0]: PAL-60 candidate [1]: PAL-60 non-candidate	
ND525L	[0]: 525Line candidate [1]: 525Line non-candidate	
ND625L	[0]: 625Line candidate [1]: 625Line non-candidate	

In making the above register settings, the following restrictions apply.

1. Setting both NDNTSC443-bit and NDPAL60-bit to 1 is prohibited.
2. Setting both ND525L-bit and ND625L-bit to 1 is prohibited.
3. To limit candidate formats, it is necessary to have the auto detection mode OFF while first setting the register to non-limited signal status and next the NDMODE settings, and then setting the auto detection mode to ON.



[7.7.] VBI blanking interval data output

In the AK8859VN, the settings for the output code and vertical blanking intervals for the output signal are as follows.

Setting vertical blanking intervals (VBLANK) Sub Address: 0x04 [2:0]

Name	Setting value	525/625	Vertical blanking interval	Notes
VBIL0 ~ VBIL2	[001]	525	Line1~Line20 及び Line263.5~Line283.5	+1Line
		625	Line623.5~Line24.5 及び Line311~Line336	
	[010]	525	Line1~Line21 及び Line263.5~Line284.5	+2Lines
		625	Line623.5~Line25.5 及び Line311~Line337	
	[011]	525	Line1~Line22 及び Line263.5~Line285.5	+3Lines
		625	Line623.5~Line26.5 及び Line311~Line338	
	[000]	525	Line1~Line19 及び Line263.5~Line282.5	default
		625	Line623.5~Line23.5 及び Line311~Line335	
	[101]	525	Line1~Line16 及び Line263.5~Line279.5	-3Lines
		625	Line623.5~Line20.5 及び Line311~Line332	
	[110]	525	Line1~Line17 及び Line263.5~Line280.5	-2Lines
		625	Line623.5~Line21.5 及び Line311~Line333	
	[111]	525	Line1~Line18 及び Line263.5~Line281.5	-1Line
		625	Line623.5~Line22.5 及び Line311~Line334	
	[100]	Reserved	Reserved	

As indicated in this table, the default values are:

(525i) Line1~Line19 and Line263.5~Line282.5

(625i) Line623.5~Line23.5 and Line311~Line335

The other specific values are set by entering the difference from these default values.

[7.8.] Output data code Min/Max

The AK8859VN data code output format (Y:Cb:Cr=4:2:2) is compliant with ITU-R BT.601.
All internal calculating operations are made with Min = 1, Max = 254.
With LIMIT601-bit set to [1], codes 1~15 and 236~254 are respectively clipped to 16, 235.

Setting for output data code Min/Max Sub Address: 0x04 [3]

Name	Setting value	Output data code Min.~Max.	Notes
LIMIT601	[0]	Y: 1~254 Cb, Cr: 1~254	Default
	[1]	Y: 16~235 Cb, Cr: 16~240	

In case of LIMIT601=[0] and EAVSAVN-bit=[1]*, the output code Min/Max is 0～255.

*Sub Address: 0x08 [2]

[7.9.] V-bit

In the AK8859VN, the settings for V-bit handling in ITU-R BT.656 format are as follows.

Setting for V-bit handling in ITU-R BT.656 format Sub Address: 0x04 [4]

Name	Setting value	525-line		625-line	
		V-bit=0	V-bit=1	V-bit=0	V-bit=1
TRSVSEL	[0] BT. 656-3	Line10~Line263 Line273~Line525	Line1~Line9 Line264~Line272	Line23~Line310 Line336~Line623	Line1~Line22 Line311~Line335 Line624~Line625
	[1] BT. 656-4 and SMPTE125M	Line20~Line263 Line283~Line525	Line1~Line19 Line264~Line282		

These values are unaffected by the VBIL[2:0]-bit setting.

[7.10.] Slice function

The results of VBI slicing by the AK8859VN slicing function are output as ITU-R BT.601 digital data. The VBI interval is set via VBIL[2:0]-bits. VBI slicing is performed in the luminance in the luminance signal processing path, so that the Cb/Cr value of the effective line 601 output code is output at the same level as the corresponding luminance signal.

Setting for slice level Sub Address: 0x04 [5]

Name	Definition
SLLVL	[0]: 25IRE [1]: 50IRE

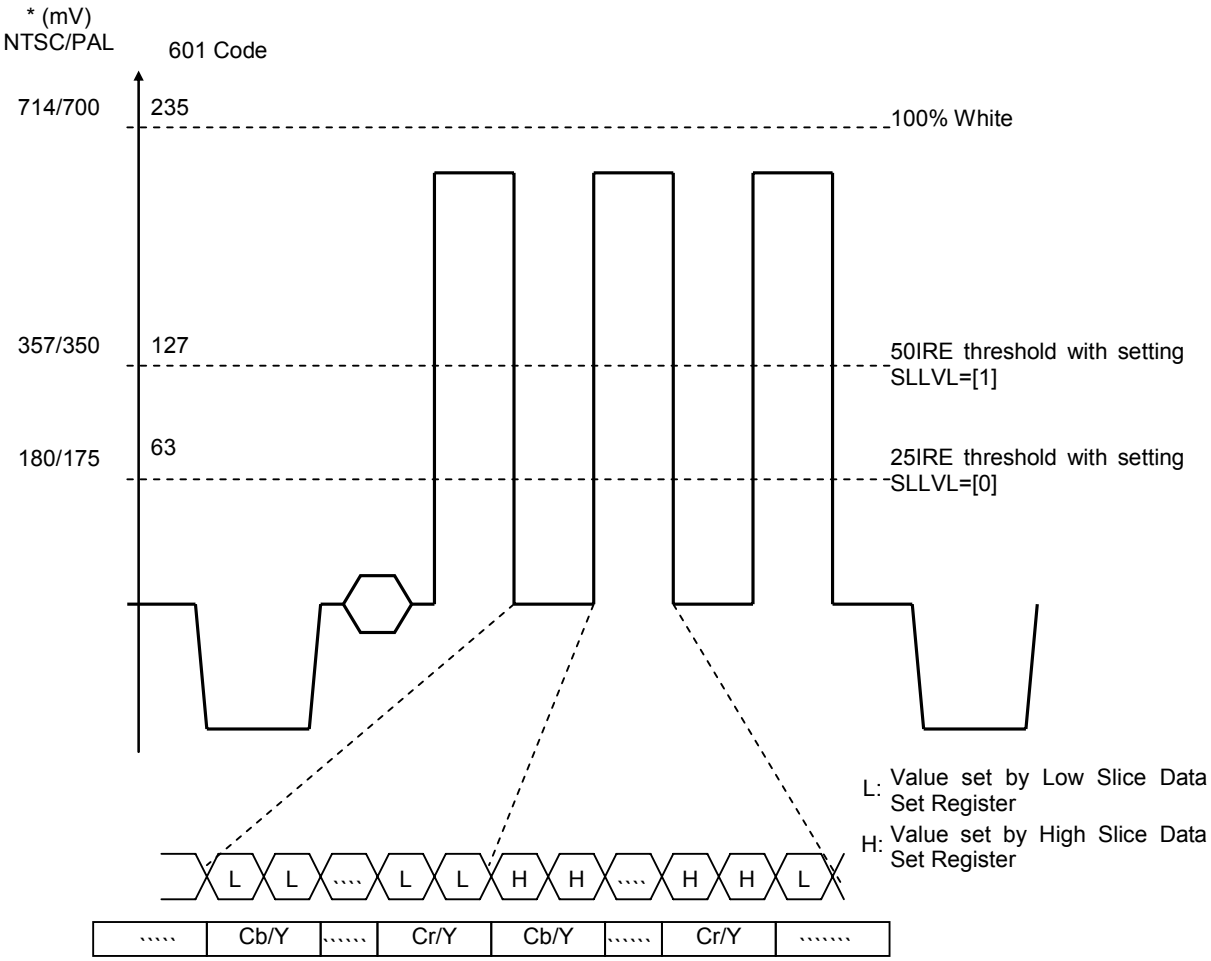
Hi/Low Slice Data Set Register of output data, as follows.

Setting for higher of two values resulting from slicing Sub Address: 0x11

Name	Definition
H0 ~ H7	Default: 0xEB(235) Note that a setting of 0x00 or 0xFF corresponds to a special 601 code.

Setting for lower of two values resulting from slicing Sub Address: 0x12

Name	Definition
L0 ~ L7	Default: 0x10(16) Note that a setting of 0x00 or 0xFF corresponds to a special 601 code.



*Threshold values (mV) are approximate

High/Low conversion is performed for either the Cb/Y or the Cr/Y combination. The above figure is an example of the conversion points for Cb/Y.

[7.11.] VBI period decode data

The AK8859VN decode data during VBI period can be selected via register.

Settings for decode data in the VBI period Sub Address: 0x04 [7:6]

Name	Setting value	Decode data	Notes
VBIDEC0 ~ VBIDEC1	[00]	Black level output	Y = 0x10 Cb/Cr = 0x80
	[01]	Monochrome mode	Y = data converted to 601 level Cb/Cr = 0x80
	[10]	Sliced data output	Y/Cb/Cr = value corresponding to slice level (Value set at Hi/Low Slice Data Set Register)
	[11]	Reserved	Reserved

Note: (525i) Lne1～Line9 and Line263.5～Line272.5
(625i) Line623.5～Line6.5 and Line311～Line388
During the above period, these values are unaffected by the VBIDEC[1:0]-bits setting.
The output code during this period is black level code (Y=0x10, Cb/Cr=0x80).

[7.12.] Output pin status

The AK8859VN output from the DATA[7:0]-pin, VD_F-pin, VAR-pin and HD-pin can each be fixed at Low via register.

Setting each digital output pins fixed to Low output Sub Address: 0x05 [3:0]

Name	Definition	Notes
DL	[0]: Normal output [1]: [D7: D0] pin output fixed at Low.	Default: Low output
VD_FL	[0]: Normal output [1]: VD_F pin output fixed at Low.	Default: Low output
VARL	[0]: Normal output [1]: VAR pin output fixed at Low.	Default: Low output
HL	[0]: Normal output [1]: HD pin output fixed at Low.	Default: Low output

In addition, the output from the DTCLK, DATA[7:0], VD_F, VAR and HD pins can be set to Hi-z output via register.

Setting digital output pins* to Hi-z output Sub Address: 0x05 [4]

Name	Definition	Notes
OEN	[0]: Normal output [1]: Hi-Z output	Default: [0] Normal output

*Collective term for DTCLK, DATA[7:0], HD, VD_F and VAR pins.

However, the PDN pin states will have priority regardless of these register setting. When PDN pin is Low output, the output from the DTCLK, DATA[7:0], VD_F, VAR and HD pins is Low output.

The relation between PDN pin and digital output pin status is show as follows:

PDN -pin	Register setting					Digital output pins status				
	OEN-bit	DL-bit	VD_FL-bit	VAR-bit	HL-bit	DATA[7:0]	VD_F	VAR	HD	DTCLK
L	X	X	X	X	X	Low				
H	H	X	X	X	X	Hi-z				
H	L	L	L	L	L	DOUT	DOUT	DOUT	DOUT	DOUT
H	L	H	H	H	H	Low	Low	Low	Low	DOUT

*DOUT is normal output.