Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AK8963

3-axis Electronic Compass

1. Features

A 3-axis electronic compass IC with high sensitive Hall sensor technology.
Best adapted to pedestrian city navigation use for cell phone and other portable appliance.

Functions:

- 3-axis magnetometer device suitable for compass application
- Built-in A to D Converter for magnetometer data out
- 14-/16-bit selectable data out for each 3 axis magnetic components
  - Sensitivity: 0.6 μT/LSB typ. (14-bit)
    0.15μT/LSB typ. (16-bit)
- Serial interface
  - I^2C bus interface.
    Standard mode and Fast mode compliant with Philips I^2C specification Ver.2.1
  - 4-wire SPI
- Operation modes:
  Power-down, Single measurement, Continuous measurement, External trigger measurement, Self test and Fuse ROM access.
- DRDY function for measurement data ready
- Magnetic sensor overflow monitor function
- Built-in oscillator for internal clock source
- Power on Reset circuit
- Self test function with built-in internal magnetic source

Operating temperatures:

- -30°C to +85°C

Operating supply voltage:

- Analog power supply +2.4V to +3.6V
- Digital Interface supply +1.65V to analog power supply voltage.

Current consumption:

- Power-down: 3 μA typ.
- Measurement:
  - Average power consumption at 8 Hz repetition rate: 280μA typ.

Package:

AK8963C 14-pin WL-CSP (BGA): 1.6 mm × 1.6 mm × 0.5 mm (typ.)
AK8963N 16-pin QFN package: 3.0 mm × 3.0 mm × 0.75 mm (typ.)

2. Overview

AK8963 is 3-axis electronic compass IC with high sensitive Hall sensor technology.
Small package of AK8963 incorporates magnetic sensors for detecting terrestrial magnetism in the X-axis, Y-axis, and Z-axis, a sensor driving circuit, signal amplifier chain, and an arithmetic circuit for processing the signal from each sensor. Self test function is also incorporated. From its compact foot print and thin package feature, it is suitable for map heading up purpose in GPS-equipped cell phone to realize pedestrian navigation function.

AK8963 has the following features:

(1) Silicon monolithic Hall-effect magnetic sensor with magnetic concentrator realizes 3-axis magnetometer on a silicon chip. Analog circuit, digital logic, power block and interface block are also integrated on a chip.

(2) Wide dynamic measurement range and high resolution with lower current consumption.

Output data resolution:	14-bit (0.6 μT/LSB)
	16-bit (0.15 μT/LSB)
Measurement range:	± 4900 μT
Average current at 8Hz repetition rate:	280μA typ.

(3) Digital serial interface
- I^2C bus interface to control AK8963 functions and to read out the measured data by external CPU. A dedicated power supply for I^2C bus interface can work in low-voltage apply as low as 1.65V.
- 4-wire SPI is also supported. A dedicated power supply for SPI can work in low-voltage apply as low as 1.65V.

(4) DRDY pin and register inform to system that measurement is end and set of data in registers are ready to be read.

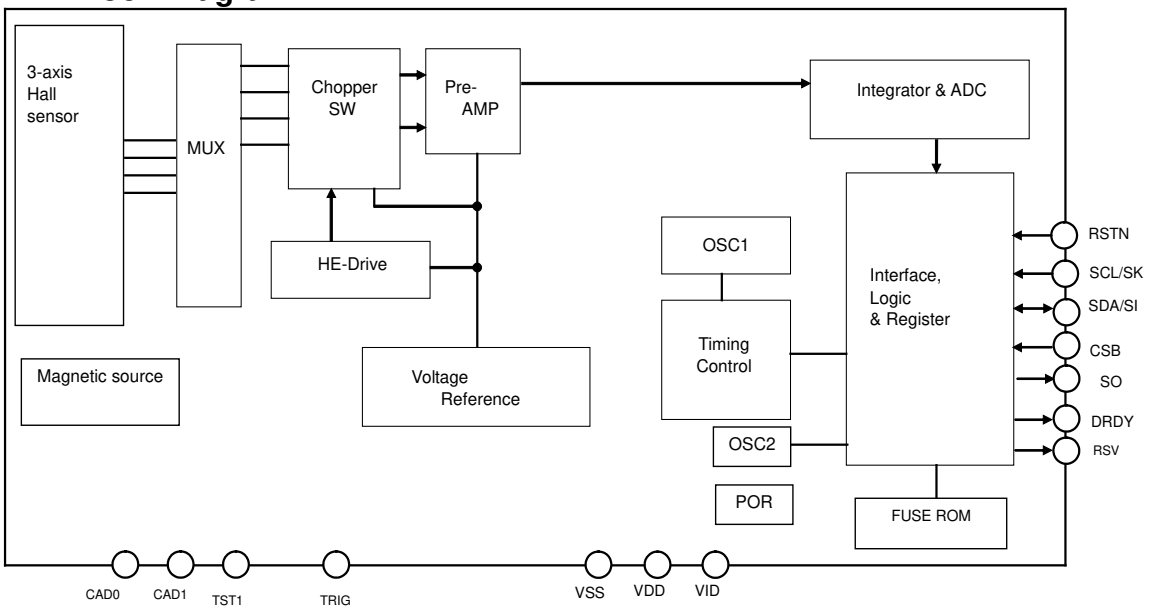
(5) Device is worked by on-chip oscillator so no external clock source is necessary.

(6) Self test function with internal magnetic source to confirm magnetic sensor operation on end products.

3. Table of Contents

4. Circuit Configuration

4.1. Block Diagram



4.2. Block Function

Block	Function
3-axis Hall sensor	Monolithic Hall elements.
MUX	Multiplexer for selecting Hall elements.
Chopper SW	Performs chopping.
HE-Drive	Magnetic sensor drive circuit for constant-current driving of sensor
Pre-AMP	Fixed-gain differential amplifier used to amplify the magnetic sensor signal.
Integrator & ADC	Integrates and amplifies pre-AMP output and performs analog-to-digital conversion.
OSC1	Generates an operating clock for sensor measurement. 12MHz(typ.)
OSC2	Generates an operating clock for sequencer. 128kHz(typ.)
POR	Power On Reset circuit. Generates reset signal on rising edge of VDD.
Interface Logic & Register	Exchanges data with an external CPU. DRDY pin indicates sensor measurement end and data is ready to be read. I^2C bus interface using two pins, namely, SCL and SDA. Standard mode and Fast mode are supported. The low-voltage specification can be supported by applying 1.65V to the VID pin. 4-wire SPI is also supported by SK, SI, SO and CSB pins. 4-wire SPI works in VID pin voltage down to 1.65V, too.
Timing Control	Generates a timing signal required for internal operation from a clock generated by the OSC1.
Magnetic Source	Generates magnetic field for self test of magnetic sensor.
FUSE ROM	Fuse for adjustment

4.3. Pin Function

QFN Pin No.	WLCSP Pin No.	Pin name	I/O	Power supply system	Type	Function
1	A1	DRDY	O	VID	CMOS	Data Ready output pin. "H" active. Informs measurement ended and data is ready to be read.
2	A2	CSB	I	VID	CMOS	Chip select pin for 4-wire SPI. "L" active. Connect to VID when selecting I^2C bus interface.
3	A3	SCL	I	VID	CMOS	When the I^2C bus interface is selected (CSB pin is connected to VID) SCL: Control data clock input pin Input: Schmidt trigger
		SK				When the 4-wire SPI is selected SK: Serial clock input pin
5	A4	SDA	I/O	VID	CMOS	When the I^2C bus interface is selected (CSB pin is connected to VID) SDA: Control data input/output pin Input: Schmidt trigger, Output: Open drain
		SI	I			When the 4-wire SPI is selected SI: Serial data input pin
15	B1	VDD	-	-	Power	Analog Power supply pin.
4	B3	RSV	O	VID	CMOS	Reserved. Keep this pin electrically non-connected.
6	B4	SO	O	VID	CMOS	When the I^2C bus interface is selected (CSB pin is connected to VID) Hi-Z output. Keep this pin electrically non-connected.
						When the 4-wire SPI is selected Serial data output pin
13	C1	VSS	-	-	Power	Ground pin.
14	C2	TST1	I	VDD	CMOS	Test pin. Pulled down by 100kΩ internal resister. Keep this pin electrically non-connected or connect to VSS.
7	C3	TRG	I	VID	CMOS	External trigger pulse input pin. Enabled only in External trigger mode. Pulled down by 100kΩ internal resister. When External trigger mode is not in use, keep this pin electrically non-connected or connect to VSS.
8	C4	VID	-	-	Power	Digital interface positive power supply pin.
12	D1	CAD0	I	VDD	CMOS	When the I^2C bus interface is selected (CSB pin is connected to VID) CAD0: Slave address 0 input pin Connect to VSS or VDD.
						When the 4-wire serial interface is selected Connect to VSS.
11	D2	CAD1	I	VDD	CMOS	When the I^2C bus interface is selected (CSB pin is connected to VID) CAD1: Slave address 1 input pin Connect to VSS or VDD.
						When the 4-wire serial interface is selected Connect to VSS.
10	D4	RSTN	I	VID	CMOS	Reset pin. Resets registers by setting to "L". Connect to VID when not in use.

5. Overall Characteristics

5.1. Absolute Maximum Ratings

Vss=0V

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage (Vdd, Vid)	V+	-0.3	+4.3	V
Input voltage	VIN	-0.3	(V+)+0.3	V
Input current	IIN	-	±10	mA
Storage temperature	TST	-40	+125	°C

(Note 1) If the device is used in conditions exceeding these values, the device may be destroyed. Normal operations are not guaranteed in such exceeding conditions.

5.2. Recommended Operating Conditions

Vss=0V

Parameter	Remark	Symbol	Min.	Typ.	Max.	Unit
Operating temperature		Ta	-30		+85	°C
Power supply voltage	VDD pin voltage	Vdd	2.4	3.0	3.6	V
	VID pin voltage	Vid	1.65		Vdd	V

5.3. Electrical Characteristics

The following conditions apply unless otherwise noted:
Vdd=2.4V to 3.6V, Vid=1.65V to Vdd, Temperature range=-30°C to 85°C

5.3.1. DC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level input voltage 1	VIH1	CSB RSTN TRG		70%Vid			V
Low level input voltage 1	VIL1					30%Vid	V
High level input voltage 2	VIH2	SK/SCL SI/SDA		70%Vid		Vid+0.5	V
Low level input voltage 2	VIL2			-0.5		30%Vid	V
High level input voltage 3	VIH3	CAD0 CAD1		70%Vdd			V
Low level input voltage 3	VIL3					30%Vdd	V
Input current 1	IIN1	SK/SCL SI/SDA CSB RSTN	Vin=Vss or Vid	-10		+10	μA
Input current 2	IIN2	CAD0 CAD1	Vin=Vss or Vdd	-10		+10	μA
Input current 3	IIN3	TRG	Vin=Vid			100	μA
Input current 4	IIN4	TST1	Vin=Vdd			100	μA
Hysteresis input voltage (Note 2)	VHS	SCL SDA	Vid≥2V	5%Vid			V
			Vid<2V	10%Vid			V
High level output voltage 1	VOH1	SO DRDY	IOH≥-100μA	80%Vid			V
Low level output voltage 1	VOL1		IOL≤+100μA			20%Vid	V
Low level output voltage 2 (Note 3)(Note 4)	VOL2	SDA	IOL≤3mA Vid≥2V			0.4	V
			IOL≤3mA Vid<2V			20%Vid	V
Current consumption (Note 5)	IDD1	VDD VID	Power-down mode Vdd=Vid=3.0V		3	10	μA
	IDD2		When magnetic sensor is driven		5	10	mA
	IDD3		Self-test mode		9	15	mA
	IDD4		(Note 6)		0.1	5	μA

(Note 2) Schmitt trigger input (reference value for design)
(Note 3) Maximum load capacitance: 400pF (capacitive load of each bus line applied to the I^2C bus interface)
(Note 4) Output is open-drain. Connect a pull-up resistor externally.
(Note 5) Without any resistance load
(Note 6) (case1)Vdd=ON, Vid=ON, RSTN pin = "L". (case2)Vdd=ON, Vid=OFF(0V),RSTN pin = "L".

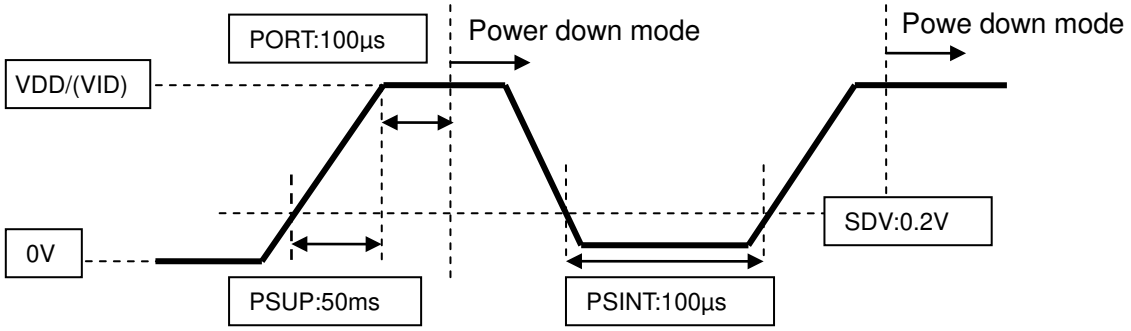
(case3)Vdd=Off(0V), Vid=On.

5.3.2. AC Characteristics

Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Power supply rise time (Note 7)	PSUP	VDD VID	Period of time that VDD (VID) changes from 0.2V to Vdd (Vid). (Note 8)			50	ms
POR completion time (Note 7)	PORT		Period of time after PSUP to Power-down mode (Note 8)			100	µs
Power supply turn off voltage	SDV	VDD VID	Turn off voltage to enable POR to restart (Note 8)			0.2	V
Power supply turn on interval (Note 7)	PSINT	VDD VID	Period of time that voltage lower than SDV needed to be kept to enable POR to restart (Note 8)	100			µs
Wait time before mode setting	Twat			100			µs

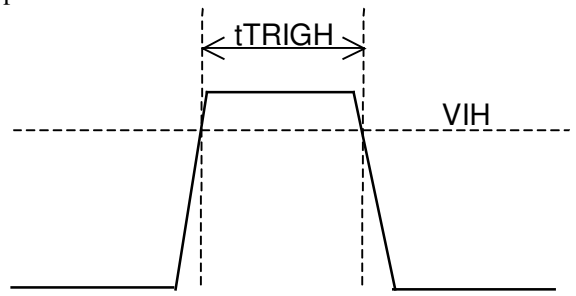
(Note 7) Reference value for design

(Note 8) When POR circuit detects the rise of VDD/VID voltage, it resets internal circuits and initializes the registers. After reset, AK8963 transits to Power-down mode.

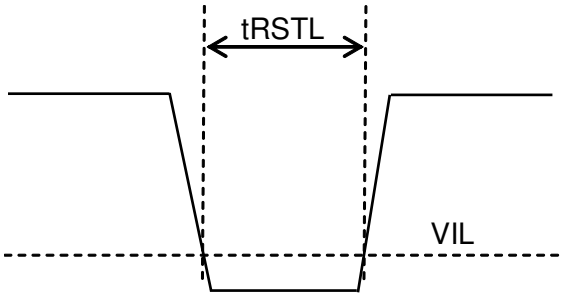


Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Trigger input effective pulse width	tTRIGH	TRG		200			ns
Trigger input effective frequency (Note 9)	tTRIGf	TRG				100	Hz

(Note 9) The value when the period of time from the end of the measurement to the next trigger input is 1.3ms.



Parameter	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Reset input effective pulse width (“L”)	tRSTL	RSTN		5			μs



5.3.3. Analog Circuit Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Measurement data output bit	DBIT	BIT = “0”		14		bit
		BIT = “1”		16		
Time for measurement	TSM	Single measurement mode		7.2	9	ms
Magnetic sensor sensitivity	BSE	Tc=25°C (Note 10)				
		BIT = “0”	0.57	0.6	0.63	μT/LSB
		BIT = “1”	0.1425	0.15	0.1575	
Magnetic sensor measurement range (Note 11)	BRG	Tc=25°C (Note 10)	±4912			μT
Magnetic sensor initial offset (Note 12)		Tc=25°C BIT = “0”	-500		500	LSB

(Note 10) Value after sensitivity is adjusted using sensitivity fine adjustment data stored in Fuse ROM. (Refer to 8.3.11 for how to adjust.)
(Note 11) Reference value for design
(Note 12) Value of measurement data register on shipment without applying magnetic field on purpose.

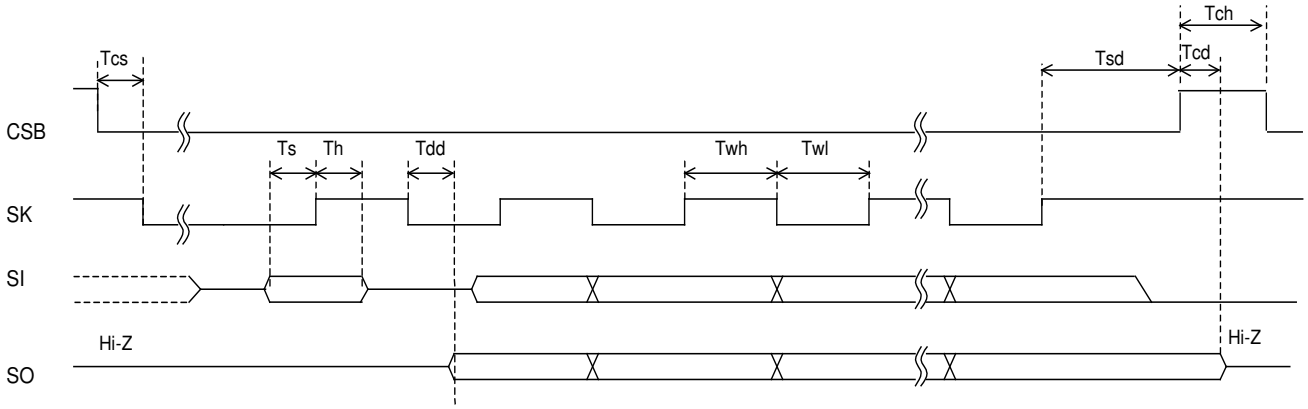
5.3.4. 4-wire SPI

4-wire SPI is compliant with mode 3

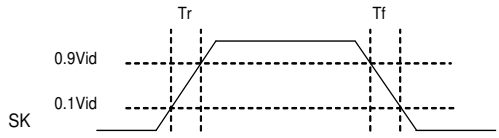
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CSB setup time	Tcs		50			ns
Data setup time	Ts		50			ns
Data hold time	Th		50			ns
SK high time	Twh	Vid≥2.5V	100			ns
		2.5V>Vid≥1.65V	150			ns
SK low time	Twl	Vid≥2.5V	100			ns
		2.5V>Vid≥1.65V	150			ns
SK setup time	Tsd		50			ns
SK to SO delay time (Note 13)	Tdd				50	ns
CSB to SO delay time (Note 13)	Tcd				50	ns
SK rise time (Note 14)	Tr				100	ns
SK fall time (Note 14)	Tf				100	ns
CSB high time	Tch		150			ns

(Note 13) SO load capacitance: 20pF
(Note 14) Reference value for design.

[4-wire SPI]



[Rise time and fall time]



5.3.5. I²C Bus Interface

CSB pin = "H"

I²C bus interface is compliant with Standard mode and Fast mode. Standard/Fast mode is selected automatically by fSCL.

(1) Standard mode

fSCL≤100kHz

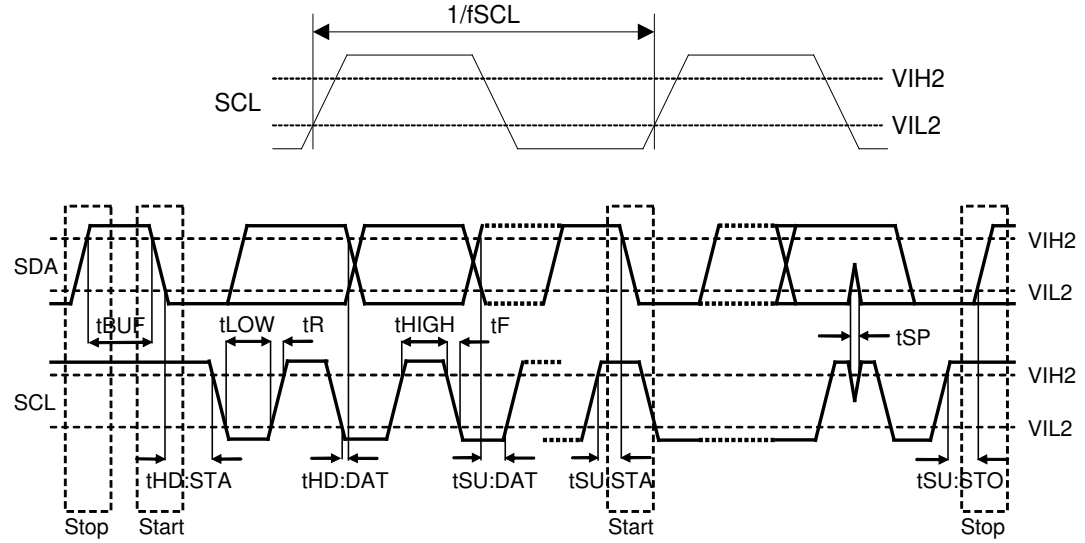
Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			100	kHz
tHIGH	SCL clock "High" time	4.0			μs
tLOW	SCL clock "Low" time	4.7			μs
tR	SDA and SCL rise time			1.0	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	4.0			μs
tSU:STA	Start Condition setup time	4.7			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	250			ns
tSU:STO	Stop Condition setup time	4.0			μs
tBUF	Bus free time	4.7			μs

(2) Fast mode

100kHz<fSCL≤400kHz

Symbol	Parameter	Min.	Typ.	Max.	Unit
fSCL	SCL clock frequency			400	kHz
tHIGH	SCL clock "High" time	0.6			μs
tLOW	SCL clock "Low" time	1.3			μs
tR	SDA and SCL rise time			0.3	μs
tF	SDA and SCL fall time			0.3	μs
tHD:STA	Start Condition hold time	0.6			μs
tSU:STA	Start Condition setup time	0.6			μs
tHD:DAT	SDA hold time (vs. SCL falling edge)	0			μs
tSU:DAT	SDA setup time (vs. SCL rising edge)	100			ns
tSU:STO	Stop Condition setup time	0.6			μs
tBUF	Bus free time	1.3			μs
tSP	Noise suppression pulse width			50	ns

[I²C bus interface timing]



6. Functional Explanation

6.1. Power States

When VDD and VID are turned on from Vdd=OFF (0V) and Vid=OFF (0V), all registers in AK8963 are initialized by POR circuit and AK8963 transits to Power-down mode.

All the states in the table below can be set, although the transition from state 2 to state 3 and the transition from state 3 to state 2 are prohibited.

Table 6.1

State	VDD	VID	Power state
1	OFF (0V)	OFF (0V)	OFF (0V). It doesn't affect external interface. Digital input pins other than SCL and SDA pin should be fixed to "L"(0V).
2	OFF (0V)	1.65V to 3.6V	OFF (0V). It doesn't affect external interface.
3	2.4V to 3.6V	OFF (0V)	OFF (0V). It doesn't affect external interface. Digital input pins other than SCL and SDA pin should be fixed to "L" (0V).
4	2.4V to 3.6V	1.65V to Vdd	ON

6.2. Reset Functions

When the power state is ON, always keep Vid≤Vdd.
Power-on reset (POR) works until Vdd reaches to the operation effective voltage (about 1.4V: reference value for design) on power-on sequence. After POR is deactivated, all registers are initialized and transits to power down mode.

When Vdd=2.4 ~ 3.6V, POR circuit and VID monitor circuit are active. When Vid=0V, AK8963 is in reset status and it consumes the current of reset state (IDD4).

AK8963 has four types of reset;

(1) Power on reset (POR)
When Vdd rise is detected, POR circuit operates, and AK8963 is reset.
(2) VID monitor
When Vid is turned OFF (0V), AK8963 is reset.
(3) Reset pin (RSTN)
AK8963 is reset by Reset pin. When Reset pin is not used, connect to VID.
(4) Soft reset
AK8963 is reset by setting SRST bit.

When AK8963 is reset, all registers are initialized and AK8963 transits to Power-down mode.

6.3. Operation Modes

AK8963 has following seven operation modes:

(1) Power-down mode
(2) Single measurement mode
(3) Continuous measurement mode 1
(4) Continuous measurement mode 2
(5) External trigger measurement mode
(6) Self-test mode
(7) Fuse ROM access mode

By setting CNTL1 register MODE[3:0] bits, the operation set for each mode is started.
A transition from one mode to another is shown below.

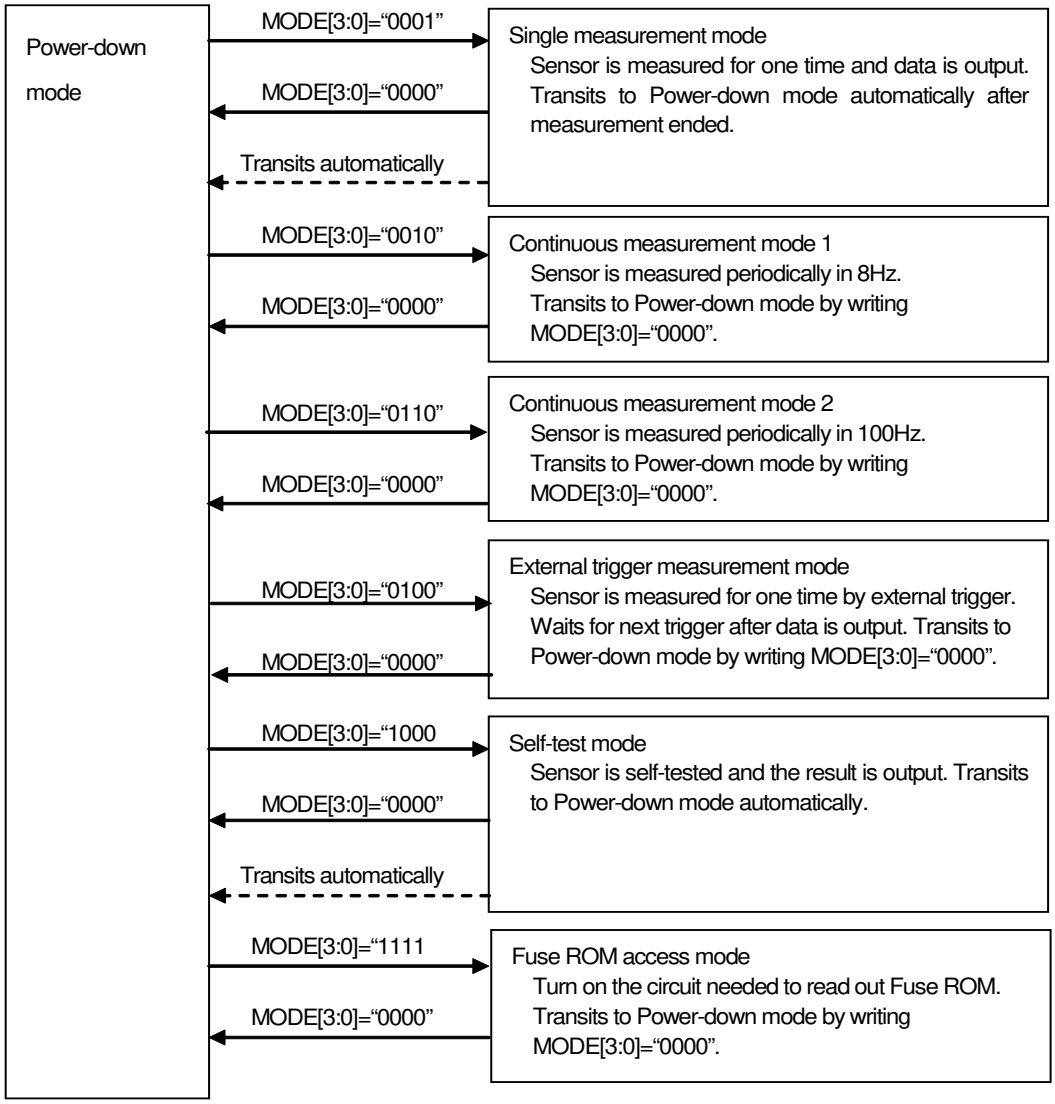


Figure 6.1 Operation modes

When power is turned ON, AK8963 is in power-down mode. When a specified value is set to MODE[3:0], AK8963 transits to the specified mode and starts operation. When user wants to change operation mode, transit to power-down mode first and then transit to other modes. After power-down mode is set, at least 100μs(Twat) is needed before setting another mode.

6.4. Description of Each Operation Mode

6.4.1. Power-down Mode

Power to almost all internal circuits is turned off. All registers are accessible in power-down mode. However, fuse ROM data cannot be read correctly. Data stored in read/write registers are remained. They can be reset by soft reset.

6.4.2. Single Measurement Mode

When single measurement mode (MODE[3:0]="0001") is set, sensor is measured, and after sensor measurement and signal processing is finished, measurement data is stored to measurement data registers (HXL to HZH), then AK8963 transits to power-down mode automatically. On transition to power-down mode, MODE[3:0] turnes to "0000". At the same time, DRDY bit in ST1 register turnes to "1". This is called "Data Ready". When any of measurement data register (HXL to HZH) or ST2 register is read, DRDY bit turnes to "0". It remains "1" on transition from Power-down mode to another mode. DRDY pin is in the same state as DRDY bit. (Refer to Figure 6.2.)

When sensor is measuring (Measurement period), measurement data registers (HXL ~ HZH) keep the previous data. Therefore, it is possible to read out data even in measurement period. Data read out in measurement period are previous data. (Refer to Figure 6.3.)

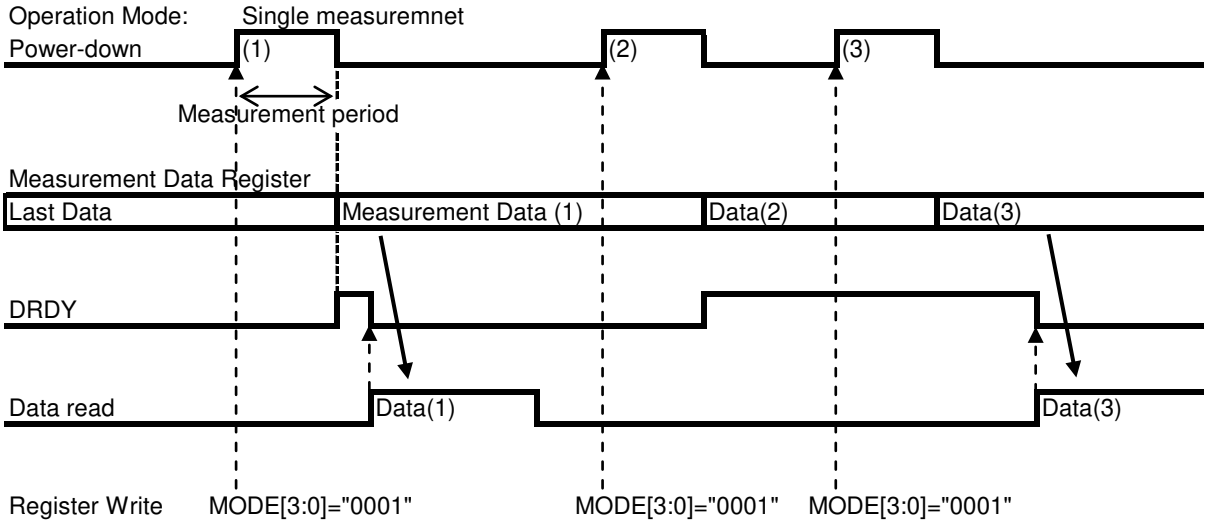


Figure 6.2 Single measurement mode: when data is read out of measurement period

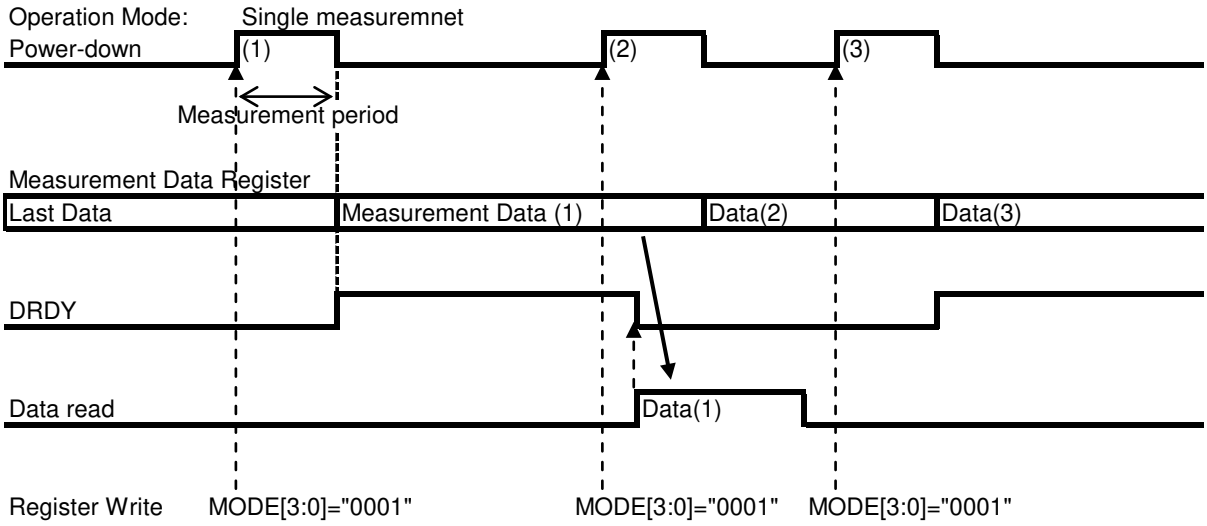


Figure 6.3 Single measurement mode: when data read started during measurement period

6.4.3. Continuous Measurement Mode 1 and 2

When continuous measurement mode 1 (MODE[3:0]="0010") or 2 (MODE[3:0]="0110") is set, sensor is measured periodically at 8Hz or 100Hz respectively. When sensor measurement and signal processing is finished, measurement data is stored to measurement data registers (HXL ~ HZH) and all circuits except for the minimum circuit required for counting cycle lentgh are turned off (PD). When the next measurement timing comes, AK8963 wakes up automatically from PD and starts measurement again.
Continuous measurement mode ends when power-down mode (MODE[3:0]="0000") is set. It repeats measurement until power-down mode is set.
When continuous measurement mode 1 (MODE[3:0]="0010") or 2 (MODE[3:0]= "0110") is set again while AK8963 is already in continuous measurement mode, a new measurement starts. ST1, ST2 and measurement data registers (HXL ~ HZH) will not be initialized by this.

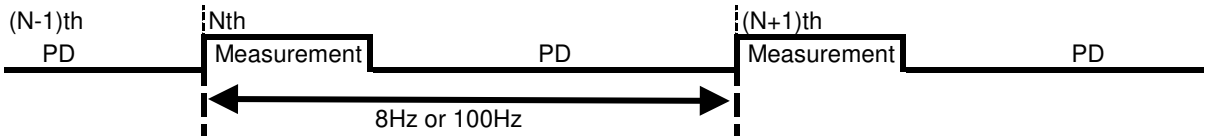


Figure 6.4 Continuous measurement mode

6.4.3.1. Data Ready

When measurement data is stored and ready to be read, DRDY bit in ST1 register turnes to "1". This is called "Data Ready". DRDY pin is in the same state as DRDY bit. When measurement is performed correctly, AK8963 becomes Data Ready on transition to PD after measurement.

6.4.3.2. Normal Read Sequence

(1) Check Data Ready or not by any of the following method.
- Polling DRDY bit of ST1 register
- Monitor DRDY pin

When Data Ready, proceed to the next step.

(2) Read ST1 register (not needed when polling ST1)
DRDY: Shows Data Ready or not. Not when "0", Data Ready when "1".
DOR: Shows if any data has been skipped before the current data or not. There are no skipped data when "0", there are skipped data when "1".

(3) Read measurement data
When any of measurement data register (HXL ~ HZH) or ST2 register is read, AK8963 judges that data reading is started. When data reading is started, DRDY bit and DOR bit turnes to "0".

(4) Read ST2 register (required)
HOFL: Shows if magnetic sensor is overflown or not. "0" means not overflown, "1" means overflown.
When ST2 register is read, AK8963 judges that data reading is finished. Stored measurement data is protected during data reading and data is not updated. By reading ST2 register, this protection is released. It is required to read ST2 register after data reading.

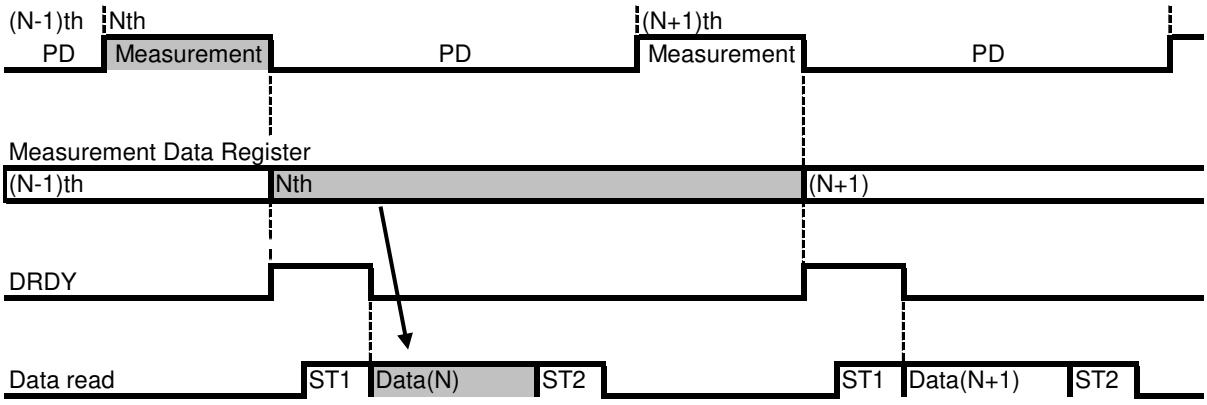


Figure 6.5 Normal read sequesnce

6.4.3.3. Data Read Start During Measurement

When sensor is measuring (Measurement period), measurement data registers (HXL ~ HZH) keep the previous data. Therefore, it is possible to read out data even in measurement period. If data is started to be read during measurement period, previous data is read.

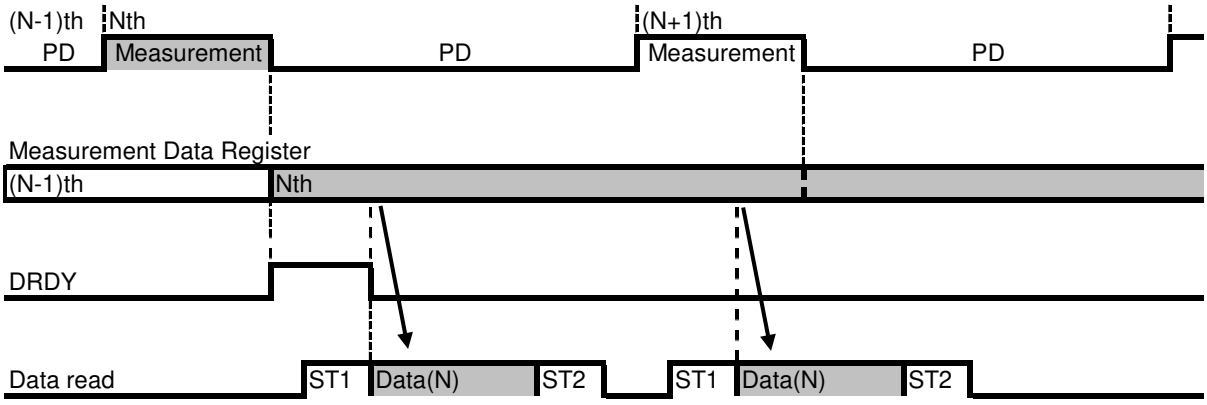


Figure 6.6 Data read start during measuremnet

6.4.3.4. Data Skip

When Nth data was not read before (N+1)th measurement ends, Data Ready remains until data is read. In this case, a set of measurement data is skipped so that DOR bit turnes to "1". (Refer to Figure 6.7)
When data reading started after Nth measurement ended and did not finish reading before (N+1)th measurement ended, Nth measurement data is protected to keep correct data. In this case, a set of measurement data is skipped and not stored so that DOR bit turnes to "1". (Refer to Figure 6.8)
In both case, DOR bit turnes to "0" at the next start of data reading.

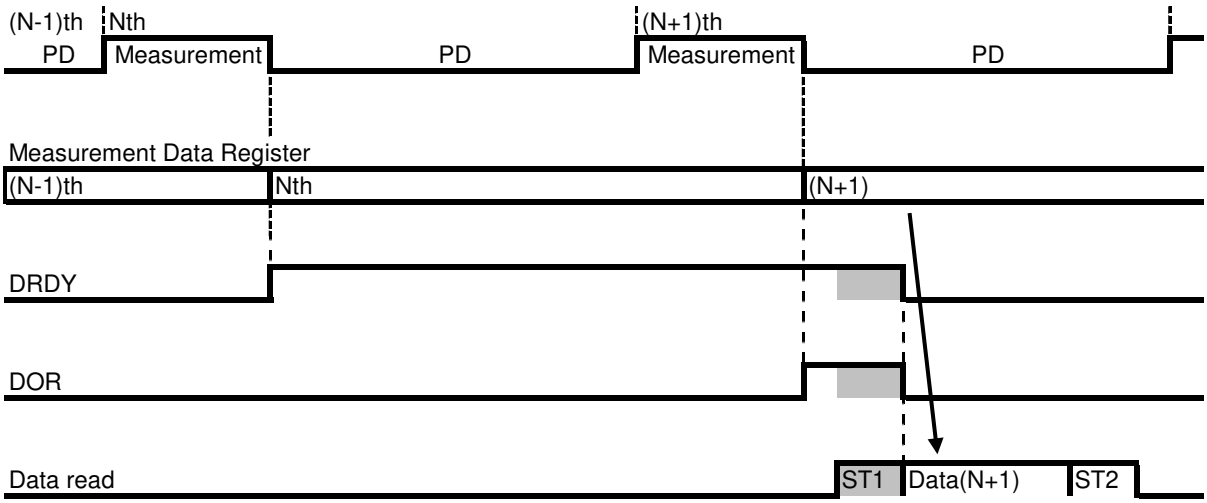


Figure 6.7 Data Skip: When data is not read

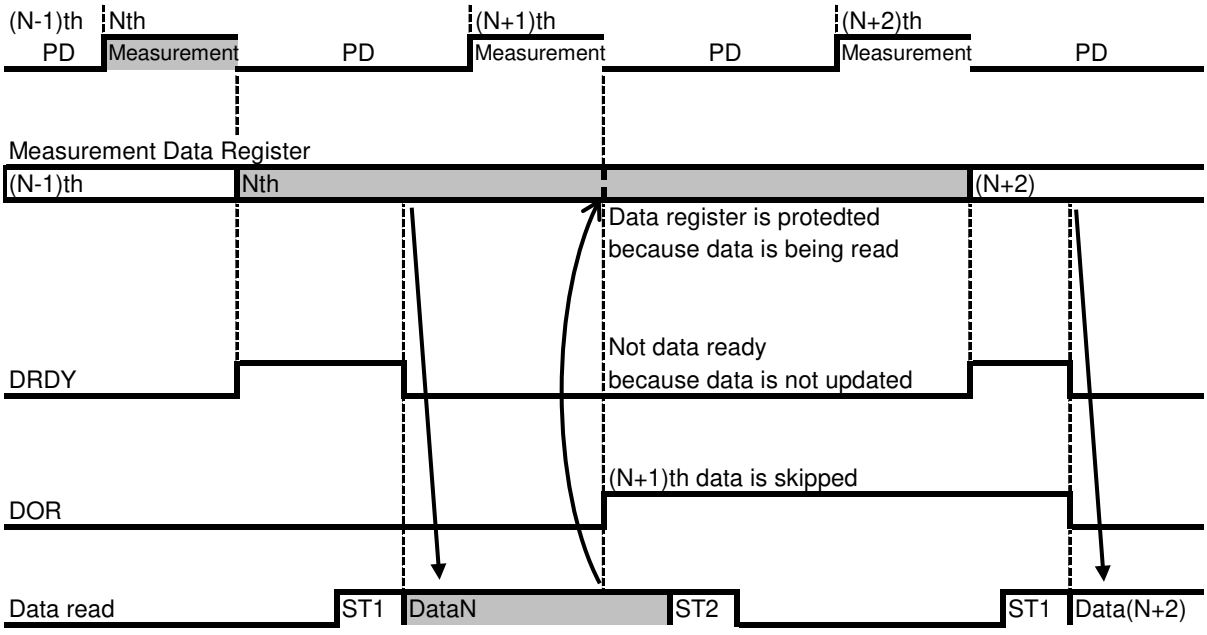


Figure 6.8 Data Skip: When data read has not been finished before the next measurement ends

6.4.3.5. End Operation

Set power-down mode (MODE[3:0]="0000") to end continuous measurement mode.

6.4.3.6. Magnetic Sensor Overflow

AK8963 has the limitation for measurement range that the sum of absolute values of each axis should be smaller than 4912μT.

$$|X|+|Y|+|Z| < 4912\mu T$$

When the magnetic field exceeded this limitation, data stored at measurement data are not correct. This is called Magnetic Sensor Overflow.

When magnetic sensor overlow occurs, HOFL bit turns to "1". When the next measurement starts, it returns to "0".

6.4.4. External Trigger Measurement Mode

When external trigger measurement mode (MODE[3:0]="0100") is set, AK8963 waits for trigger input. When a pulse is input from TRG pin, sensor measurement is started on the rising edge of TRG pin. When sensor measurement and signal processing is finished, measurement data is stored to measurement data registers (HXL to HZH) and all circuits except for the minimum circuit required for trigger input waiting are turned off (PD state). When the next pulse is input, AK8963 wakes up automatically from PD and starts measurement again.

External trigger measurement mode ends when power-down mode (MODE[3:0]="0000") is set. AK8963 keeps waiting for the trigger input until the power-down mode is set.

When external trigger measurement mode (MODE[3:0]="0100") is set again while AK8963 is already in external trigger measurement mode, it starts to wait for the trigger input again. The trigger input is ignored while sensor is measuring.

Data read sequence and functions of read-only registers in external trigger measurement mode is the same as continuous measurement mode.

6.4.5. Self-test Mode

Self-test mode is used to check if the sensor is working normally.
When self-test mode (MODE[3:0]="1000") is set, magnetic field is generated by the internal magnetic source and sensor is measured. Measurement data is stored to measurement data registers (HXL to HZH), then AK8963 transits to power-down mode automatically.
Before setting self-test mode, write "1" to SELF bit of ASTC register. Data read sequence and functions of read-only registers in self-test mode is the same as single measurement mode.

When self-test is end, write "0" to SELF bit then proceed to other operation.

<Self-test Sequence>
(1) Set Power-down mode. (MODE[3:0]="0000")
(2) Write "1" to SELF bit of ASTC register (other bits in this register should be kept "0")
(3) Set Self-test Mode. (MODE[3:0]="1000")
(4) Check Data Ready or not by any of the following method.
    - Polling DRDY bit of ST1 register
    - Monitor DRDY pin
    When Data Ready, proceed to the next step.
(5) Read measurement data (HXL to HZH)
(6) Write "0" to SELF bit of ASTC register
(7) Set Power-down mode. (MODE[3:0]="0000")

<Self-test Judgement>
When measurement data read by the above sequence is in the range of following table after sensitivity adjustment (refer to 8.3.11), AK8963 is working normally.

14-bit output(BIT="0")

	HX[15:0]	HY[15:0]	HZ[15:0]
Criteria	-50 =< HX =< 50	-50 =< HY =< 50	-800 =< HZ =< -200

16-bit output(BIT="1")

	HX[15:0]	HY[15:0]	HZ[15:0]
Criteria	-200 =< HX =< 200	-200 =< HY =< 200	-3200 =< HZ =< -800

6.4.6. Fuse ROM Access Mode

Fuse ROM access mode is used to read Fuse ROM data. Sensitivity adjustment data for each axis is stored in fuse ROM.
Set Fuse ROM Access mode (MODE[3:0]="1111") before reading Fuse ROM data. When Fuse ROM Access mode is set, circuits reauired for reading fuse ROM are turned on.
After reading fuse ROM data, set power-down mode (MODE[3:0]="0000") before the transition to another mode.

7. Serial Interface

AK8963 supports I^2C bus interface and 4-wire SPI. A selection is made by CSB pin. When used as 3-wire SPI, set SI pin and SO pin wired-OR externally.

CSB pin="L": 4-wire SPI
CSB pin="H": I^2C bus interface

7.1. 4-wire SPI

The 4-wire SPI consists of four digital signal lines: SK, SI, SO, and CSB, and is provided in 16bit protocol. Data consists of Read/Write control bit (R/W), register address (7bits) and control data (8bits).
To read out all axes measuremen data (X, Y, Z), an option to read out more than one byte data using automatic increment command is available. (Sequencial read operation)

CSB pin is low active. Input data is taken in on the rising edge of SK pin, and output data is changed on the falling edge of SK pin. (SPI MODE3)
Communication starts when CSB pin transits to "L" and stops when CSB pin transits to "H". SK pin must be "H" during CSB pin is in transition. Also, it is prohibited to change SI pin during CSB pin is "H" and SK pin is "H".

7.1.1. Writing Data

Input 16 bits data on SI pin in synchronous with the 16-bit serial clock input on SK pin. Out of 16 bits input data, the first 8 bits specify the R/W control bit (R/W="0" when writing) and register address (7bits), and the latter 8 bits are control data (8bits). When any of addresses listed on Table 8.1 is input, AK8963 recognizes that it is selected and takes in latter 8 bits as setting data.
If the number of clock pulses is less than 16, no data is written. If the number of clock pulses is more than 16, data after the 16th clock pulse on SI pin are ignored.
It is not compliant with sereal write operation for multiple addresses.

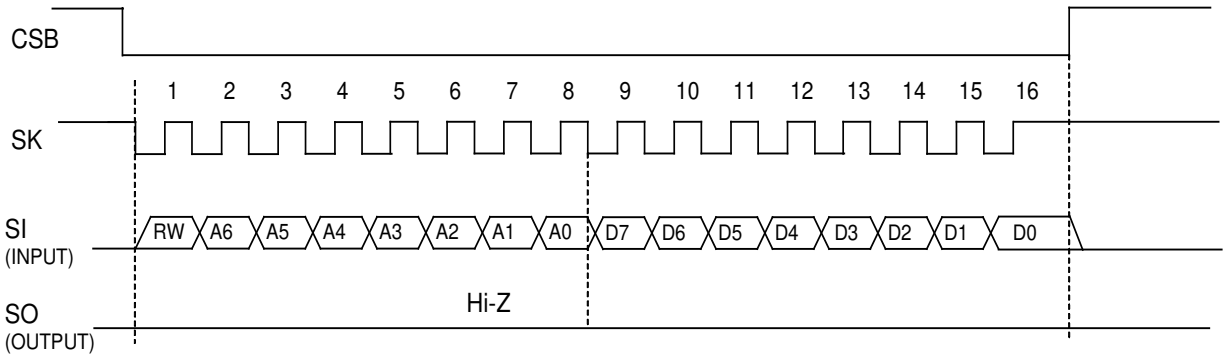


Figure 7.1 4-wire SPI Writing Data

7.1.2. Reading Data

Input the R/W control bit (R/W="1") and 7 bit register address on SI pin in synchronous with the first 8 bits of the 16 bits of a serial clock input on SK pin. Then AK8963 outputs the data held in the specified register with MSB first from SO pin.

When clocks are input continuously after one byte of data is read, the address is incremented and data in the next address is output. Accordingly, after the falling edge of the 15th clock and CSB pin is "L", the data in the next address is output on SO pin. When CSB pin is driven "L" to "H", SO pin is placed in the high-impedance state.

AK8963 has two incrementation lines; 00H ~ 0CH and 10H ~ 12H. For example, data is read as follows: 00H -> 01H ... -> 0BH -> 0CH -> 00H -> 01H ..., or 10H -> 11H -> 12H -> 10H …

0DH and 0EH are reserved addresses. Do not access to those addresses. When specified address is other than 00H ~ 12H, AK8963 recognizes that it is not selected and keeps SO pin in high-impedance state. Therefore, user can use other addresses for other devices.

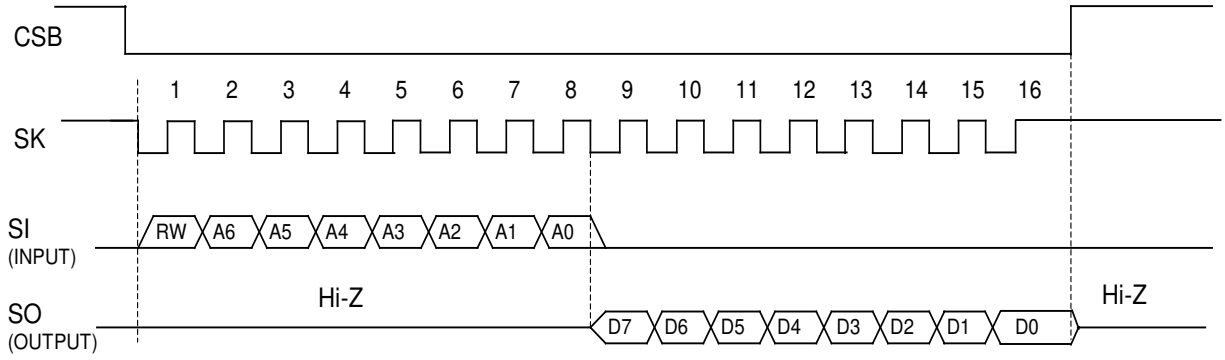


Figure 7.2 4-wire SPI Reading Data

7.2. I²C Bus Interface

The I²C bus interface of AK8963 supports the standard mode (100 kHz max.) and the fast mode (400 kHz max.).

7.2.1. Data Transfer

To access AK8963 on the bus, generate a start condition first.
Next, transmit a one-byte slave address including a device address. At this time, AK8963 compares the slave address with its own address. If these addresses match, AK8963 generates an acknowledgement, and then executes READ or WRITE instruction. At the end of instruction execution, generate a stop condition.

7.2.1.1. Change of Data

A change of data on the SDA line must be made during "Low" period of the clock on the SCL line. When the clock signal on the SCL line is "High", the state of the SDA line must be stable. (Data on the SDA line can be changed only when the clock signal on the SCL line is "Low".)
During the SCL line is "High", the state of data on the SDA line is changed only when a start condition or a stop condition is generated.

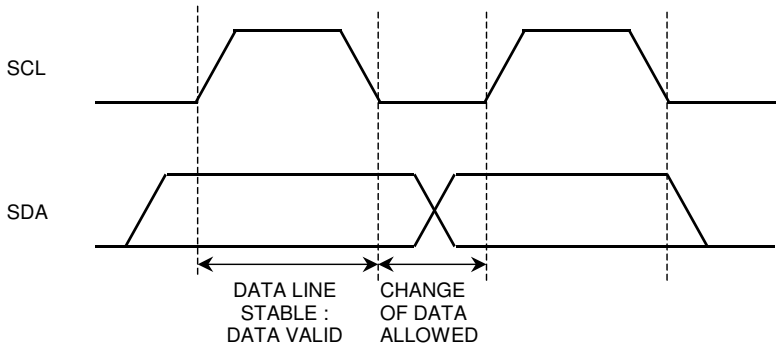


Figure 7.3 Data Change

7.2.1.2. Start/Stop Condition

If the SDA line is driven to "Low" from "High" when the SCL line is "High", a start condition is generated. Every instruction starts with a start condition.
If the SDA line is driven to "High" from "Low" when the SCL line is "High", a stop condition is generated. Every instruction stops with a stop condition.

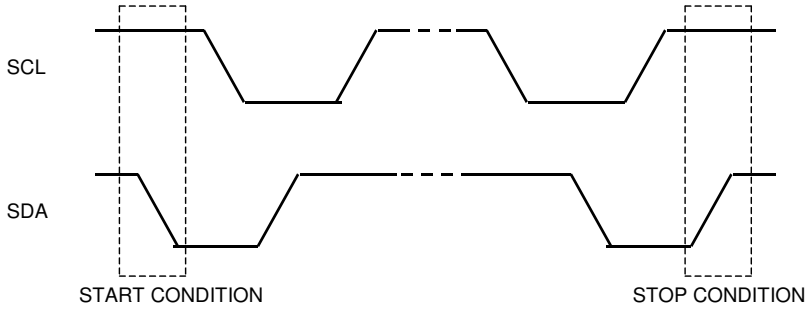


Figure 7.4 Start and Stop Conditions

7.2.1.3. Acknowledge

The IC that is transmitting data releases the SDA line (in the "High" state) after sending 1-byte data.
The IC that receives the data drives the SDA line to "Low" on the next clock pulse. This operation is referred as acknowledge. With this operation, whether data has been transferred successfully can be checked.
AK8963 generates an acknowledge after reception of a start condition and slave address.
When a WRITE instruction is executed, AK8963 generates an acknowledge after every byte is received.
When a READ instruction is executed, AK8963 generates an acknowledge then transfers the data stored at the specified address. Next, AK8963 releases the SDA line then monitors the SDA line. If a master IC generates an acknowledge instead of a stop condition, AK8963 transmits the 8bit data stored at the next address. If no acknowledge is generated, AK8963 stops data transmission.

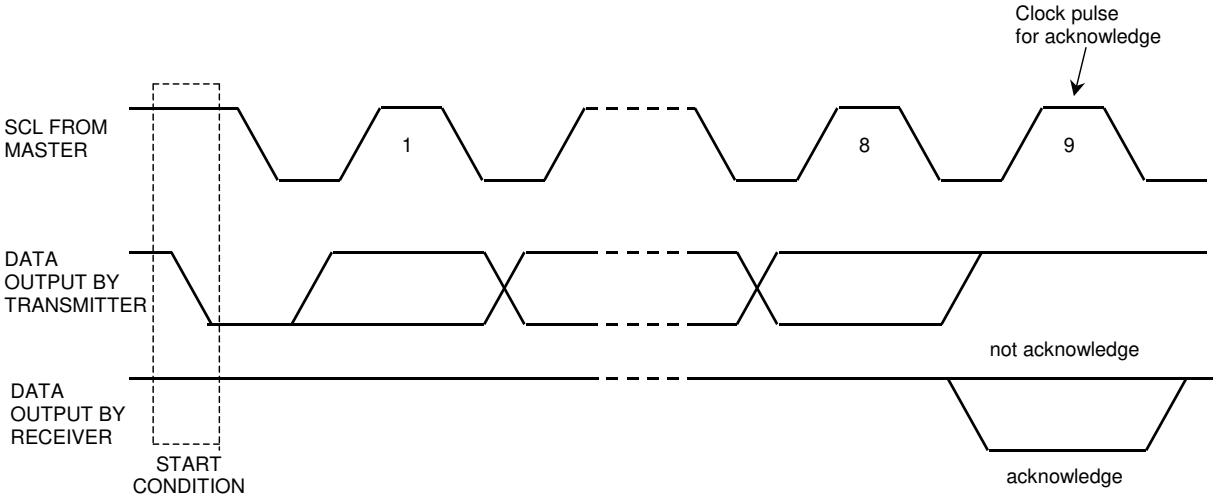


Figure 7.5 Generation of Acknowledge

7.2.1.4. Slave Address

The slave address of AK8963 can be selected from the following list by setting CAD0/1 pin. When CAD pin is fixed to VSS, the corresponding slave address bit is “0”. When CAD pin is fixed to VDD, the corresponding slave address bit is “1”.

Table 7.1 Slave Address and CAD0/1 pin

CAD1	CAD0	Slave Address
0	0	0CH
0	1	0DH
1	0	0EH
1	1	0FH

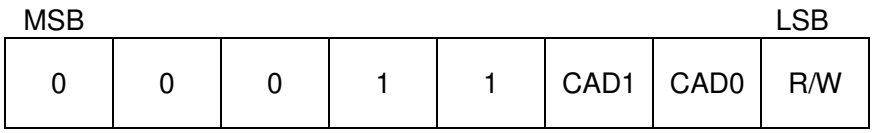


Figure 7.6 Slave Address

The first byte including a slave address is transmitted after a start condition, and an IC to be accessed is selected from the ICs on the bus according to the slave address.
When a slave address is transferred, the IC whose device address matches the transferred slave address generates an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit.
When the R/W bit is set to "1", READ instruction is executed. When the R/W bit is set to "0", WRITE instruction is executed.

7.2.2. WRITE Instruction

When the R/W bit is set to "0", AK8963 performs write operation.

In write operation, AK8963 generates an acknowledge after receiving a start condition and the first byte (slave address) then receives the second byte. The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration.

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0

Figure 7.7 Register Address

After receiving the second byte (register address), AK8963 generates an acknowledge then receives the third byte.

The third and the following bytes represent control data. Control data consists of 8 bits and is based on the MSB-first configuration. AK8963 generates an acknowledge after every byte is received. Data transfer always stops with a stop condition generated by the master.

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

Figure 7.8 Control Data

AK8963 can write multiple bytes of data at a time.

After reception of the third byte (control data), AK8963 generates an acknowledge then receives the next data. If additional data is received instead of a stop condition after receiving one byte of data, the address counter inside the LSI chip is automatically incremented and the data is written at the next address.

The address is incremented from 00H to 0CH or from 10H to12H. When the address is in 00H~0CH, the address goes back to 00H after 0CH. When the address is in 10H~12H, the address goes back to 10H after 12H. Actual data is written only to Read/Write registers (refer to 8.2).

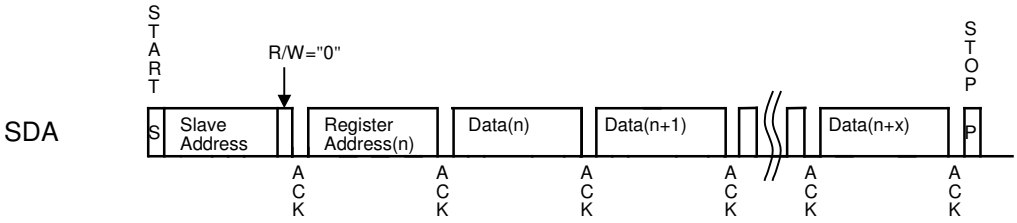


Figure 7.9 WRITE Instruction

7.2.3. READ Instruction

When the R/W bit is set to "1", AK8963 performs read operation.
If a master IC generates an acknowledge instead of a stop condition after AK8963 transfers the data at a specified address, the data at the next address can be read.
Address can be 00H~0CH and/or 10H~12H.When address is counted up to 0CH in 00H~0CH, the next address returns to 00H. When address is counted up to 12H in 10H~12H, the next address returns to 10H.
AK8963 supports one byte read and multiple byte read.

7.2.3.1. One Byte READ

AK8963 has an address counter inside the LSI chip. In current address read operation, the data at an address specified by this counter is read.
The internal address counter holds the next address of the most recently accessed address.
For example, if the address most recently accessed (for READ instruction) is address "n", and a current address read operation is attempted, the data at address "n+1" is read.
In one byte read operation, AK8963 generates an acknowledge after receiving a slave address for the READ instruction (R/W bit="1"). Next, AK8963 transfers the data specified by the internal address counter starting with the next clock pulse, then increments the internal counter by one. If the master IC generates a stop condition instead of an acknowledge after AK8963 transmits one byte of data, the read operation stops.

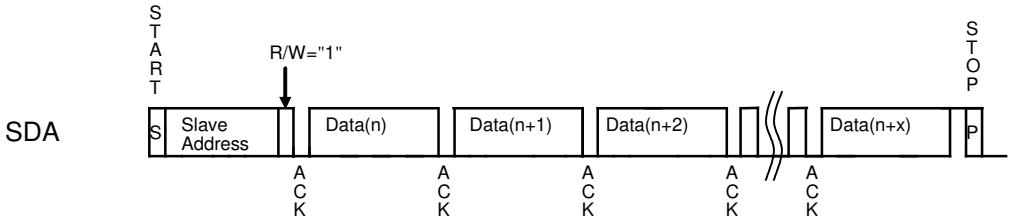


Figure 7.10 One Byte READ

7.2.3.2. Multiple Byte READ

By multiple byte read operation, data at an arbitrary address can be read.
The multiple byte read operation requires to execute WRITE instruction as dummy before a slave address for the READ instruction (R/W bit="1") is transmitted. In random read operation, a start condition is first generated then a slave address for the WRITE instruction (R/W bit="0") and a read address are transmitted sequentially.
After AK8963 generates an acknowledge in response to this address transmission, a start condition and a slave address for the READ instruction (R/W bit="1") are generated again. AK8963 generates an acknowledge in response to this slave address transmission. Next, AK8963 transfers the data at the specified address then increments the internal address counter by one. If the master IC generates a stop condition instead of an acknowledge after data is transferred, the read operation stops.

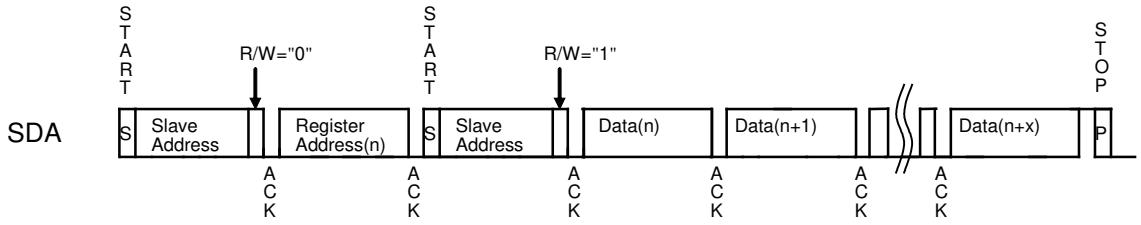


Figure 7.11 Multiple Byte READ