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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

AK8996/W

Pressure Sensor Interface IC

The AK8996 is a pressure sensor interface IC that features compensation for temperature drift and sensor variation. It is designed to excite and interface to a bridge sensor. Variations in the sensor can be corrected via compensation values stored in integrated non-volatile memory (EEPROM). Compensation values are obtained from measurement results for a set of offset voltages and temperature drift, along with a set of bridge voltages and temperature drift, including characteristics of the AK8996. The AK8996 is available in either a 16-pin QFN package or in wafer form.

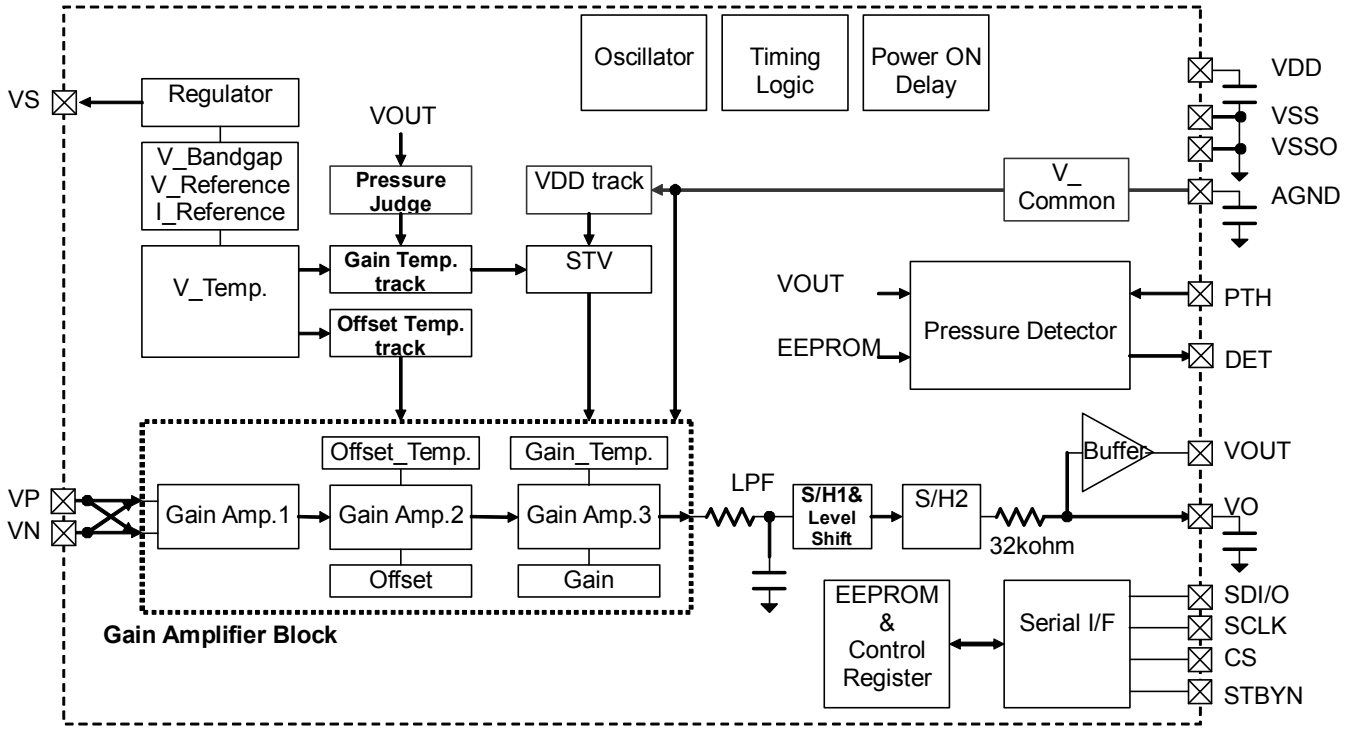
Features

- **Pressure sensor compensation and excitation IC (Analog output)**
- **Low power consumption: 350µA typ. @ 100Hz sampling**
- **Standby function: 1µA max.**
- **Low-voltage operation: 2.2 to 3.6V, 5V±10%**
- **Operating temperature range: -40 to 105ºC**
- **Integrated span voltage switching function (by a factor of 5, typ.)**
  - **Resolution: Gain Amp. 1: 3-bits; Gain Amp. 2:1-bit**
    Adjustment step: factor of 1/step (by a factor of 2 to 9);
    factor of 1/step (by a factor of 1 and 2)
- **Integrated sensor output compensation**
  - **Offset voltage adjustment**
    - **Resolution: Rough: 4-bits; Fine: 7-bits**
    - **Adjustment step: Rough: 7.5%/step; Fine 0.125%/step @VDD: 5.0V**
  - **Offset voltage temperature drift adjustment (1st/2nd order coefficient)**
    - **Resolution: 10-bits; 8-bits**
    - **Adjustment step: 0.196%/step; 0.787%/step**
  - **Output span voltage adjustment**
    - **Resolution: 9-bits**
    - **Adjustment value: 100/[100+0.25*N](%) N: -256 to +255**
  - **Sensitivity temperature drift adjustment (1st/2nd order coefficient)**
    - **Resolution: 10-bits; 8-bits**
    - **Adjustment step: 0.196%/step; 0.787%/step**
- **Integrated output reference voltage switching function**
  - **Resolution: Rough 5-bits; Fine 6-bits**
  - **Adjustment step: 0.0005*VDD/step (0.0785*VDD to 0.9215*VDD) @VO**
- **Integrated criteria adjustment function for determining positive/negative pressure**
  - **Resolution: 10-bits**
  - **Adjustment step: 0.001*VDD/step (0.05*VDD to 0.95*VDD)**
- **Integrated output gain (buffer gain) switching function (by a factor of 4, typ.)**
  - **Resolution: 3-bits**
  - **Adjustment step: factor of 0.5/step (by a factor of 2 to 4)**
- **Integrated sampling frequency switching function: 100Hz, 1kHz, 2kHz, 10.24kHz**
- **Ratiometric voltage output**
- **Integrated constant voltage source for pressure sensor**
  : 2.0V @VDD: 2.2 to 3.6V; 4.0V @VDD: 5.0V±10%

- **Integrated reference voltage & reference current generator**
  - **VREF voltage adjustment control**
    - **Resolution: 3-bits**
    - **Adjustment step: 1%/step**
  - **IREF current adjustment control**
    - **Resolution: 4-bits**
    - **Adjustment step: 2.7%/step typ.**
- **Integrated temperature sensor**
  - **Temperature range: -40 to 105°C**
  - **Temperature sensor output voltage adjustment control**
    - **Resolution: 6-bits**
    - **Adjustment step: 0.2%/step**
- **Integrated timer oscillator for intermittent operation (1024 kHz typ.)**
  - **Oscillating frequency adjustment control**
    - **Resolution: 4-bits**
    - **Adjustment step: 5%/step**
- **Integrated EEPROM for compensation values and control data storage**
  - **Size: 157 bits**
  - **Endurance: 1,000 times or more**
  - **Retention time: 10 years or more @Ta: 105°C**
- **Integrated pressure detection/self-diagnosis function**
- **Supply type: Wafer PKG (UQFN16)**

Product name	Supply Type	Note
AK8996	PKG (UQFN16)	
AK8996W	Wafer	

Block Diagram



Overview

The AK8996 is a pressure sensor interface IC that features compensation for temperature drift and sensor variation. It is designed to excite and interface to a bridge sensor. Variations in the sensor can be corrected via compensation values stored in integrated non-volatile memory (EEPROM). Compensation values are obtained from measurement results for a set of offset voltages and temperature drift, along with a set of bridge voltages and temperature drift, including characteristics of the AK8996.

The internal compensation circuit is accomplished through DACs, with 4-bit and 7-bit resolution to adjust offset voltage of the sensor, and the secondary characteristics compensator for the associated temperature drift, coupled with 9-bit resolution to adjust the span voltage and another secondary characteristics compensator for its associated temperature drift. Depending on the application, the internal EEPROM values can be pre-configured to enable adjustment of the reference sensitivity and the output reference voltage. For the adjustment procedure, see the sections on "Adjustment Sequence" and "Functional Description".

Depending on the application, the AK8996's internal EEPROM values can be preconfigured to enable adjustment of the reference sensitivities and output reference voltages. Sampling frequencies can be switched between 100Hz, 1kHz, 2kHz and 10.24kHz using the internal EEPROM data.

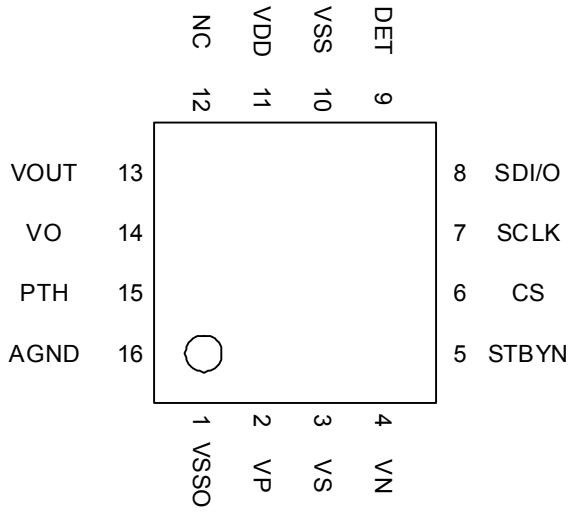
The AK8996 is provided with a pressure detection circuit. If the applied pressure exceeds the defined voltage threshold at the PTH terminal, a high-level signal is output on the DET pin. The threshold can be adjusted by the internal EEPROM data. The AK8996 is also provided with a self-diagnostic function. Upon power-up or at initial operation immediately after exiting standby mode, this self-test feature checks for the required value at the output (VOUT pin), and if an expected value is not available, the output is assumed to be anomalous and a high-level signal is output on the DET pin, in the same manner as with the pressure detection.

Pin Configuration

1. Wafer Configuration

For the detail, please contact your local sales office or authorized distributor.

2. Package Outline (UQFN16)



Adjustment Characteristics

1) Adjustable Sensor Characteristics (Reference Example)

Item	Symbol	Min.	Typ.	Max.	Units	Comments
Drive voltage	Svs1		4		V	
	Svs2		2		V	
Temperature range	Sta	-40		105	°C	
Sensor resistance	Sres1	3	5		kΩ	VDD: 2.2 to 3.6V & 5V±10%
	Sres2	1	2		kΩ	VDD: 2.7 to 3.6V & 5V±10%
Voltage input span range	Sspnin 1	22.22	80	200	mV	VDD: 5V±10% Note)
	Sspnin 2	11.11	40	100	mV	VDD: 2.2 to 3.6V Note)
Voltage span adjustment range	Sspn	100/164	100/100	100/36.25	times	Note)
Offset voltage adjustment range	Soff1	-48		48	mV	VDD: 5V±10% Note)
	Soff2	-24		24	mV	VDD: 2.2 to 3.6V Note)
Sensitivity temp. drift 2nd order coefficient	Sst21	-0.0016		+0.0016		VDD: 5V±10% Note)
	Sst22	-0.0008		+0.0008		VDD: 2.2 to 3.6V Note)
Sensitivity temp. drift 1st order coefficient	Sst11	-0.32		+0.32		VDD: 5V±10% Note)
	Sst12	-0.3		+0.3		VDD: 2.2 to 3.6V Note)
Offset temp. drift 2nd order coefficient	Sot21	-0.0016		+0.0016		VDD: 5V±10% Note)
	Sot22	-0.0008		+0.0008		VDD: 2.2 to 3.6V Note)
Offset temp. drift 1st order coefficient	Sot11	-0.6		+0.6		VDD: 5V±10% Note)
	Sot12	-0.3		+0.3		VDD: 2.2 to 3.6V Note)

Note) Equivalent input values assumed from the output. See 5) Registers Description 5.1.1) Adjustment block register. This adjustment range includes variations in the AK8996.

2) Adjustment Accuracy

Item	Symbol	Min.	Typ. Note2)	Max. Note3)	Units	Comments
Offset adjustment accuracy	Cof		0.063		%FS	
Offset temp. drift adjustment accuracy	Coft		0.101		%FS	
Output span adjustment accuracy	Csn		0.125		%FS	
Sensitivity temp. adjustment accuracy	Csnt		0.003		%FS	
Sensitivity temp. variation step	Csts		0.268		%FS	
Sensitivity supply voltage variation step	Csvs		0.236		%FS	
Final adjustment accuracy Note1)	Call		0.397	1.0	%FS	

Note1) Call=(Cof^2+Coft^2+Csn^2+Csnt^2+Csts^2+Csvs^2)^(1/2)

Note2) Temp.=105ºC, VDD=4.5V, G1=5x, G3=1.25x, BufG=4x, Offset temp. drift 1st/2nd order coefficient=Min./Max., Sensitivity temp. drift 1st/2nd order coefficient=Min.*1/2, VOUT output band-limited (≤500Hz @Fs=10kHz, ≤100Hz@Fs=2kHz, ≤50Hz@Fs=1kHz, ≤5Hz@Fs=100Hz) effective

Note3) Temp.=-40 to 105ºC, VDD=5V±10%, 3.3V±10%, 3.0V±10%, 2.5V±10%, G1/G3/BufG=Min. to Max., Each temperature coefficient=Min. to Max., VOUT output band-limited (≤500Hz @Fs=10kHz, ≤100Hz@Fs=2kHz, ≤50Hz@Fs=1kHz, ≤5Hz@Fs=100Hz) effective

* The calculation of adjustment accuracy is based on our definition as a reference. The accuracy of product depends on your sensor characteristics and adjustment method.

Description of Blocks

Gain Amplifier Block, LPF & S/H1 & Level Shifter, S/H2 & Buffer

The set of these blocks amplifies, compensates and outputs the pressure sensor level with a normal gain ratio of 50:1. This set of blocks intermittently amplifies, compensates, samples and holds the pressure sensor output. The output stage, with an internal resistor of 32kΩ, is band-limited with a combination of external capacitors, providing a low impedance output through a buffer. A percentage designator is used, benchmarked with 4000mVdc output at 100%, reflecting the 50x increase in differential input from 80mVdc.

Block	Functions
Gain Amp. 1 (G1)	A low-noise high-gain amplifier at the front end. The differential signal is increased by a factor of 5 (typically) (with factors of 2 to 9, in single-factor steps).
Gain Amp. 2 Offset_Temp. Offset Offset Temp. track (G2)	The G1 differential output is converted to single-ended with reference to AGND and typically amplified by a factor of 1 (1 or 2). The preloaded compensation data in the EEPROM enables the pressure sensor offset voltage and offset temperature secondary characteristics to be compensated. Offset adj. Resolution: Rough: 4-bits; Fine: 7-bits Adj. step: Rough: 7.5%; Fine: 0.125% @VDD: 5V Offset temp. drift. Resolution: 1st order coeff: 10-bits; 2nd order coeff: 8-bits Adj. step: 1st order coeff: 0.196%; 2nd order coeff: 0.787%
Gain Amp. 3 Gain_Temp. Gain (G3)	Amplifies the G2 output by a factor of 1.25 (typically). The preloaded compensation data in the EEPROM enables the pressure sensor span voltage and sensitivity temperature secondary characteristics to be compensated. Span adj. Resolution: 9-bits Adj. value: 100/[100+0.25*N](%) N: -256 to +255
STV VDD track Gain Temp. track (STV)	Supply voltage and sensitivity temperature variation compensation circuit. Monitors the AGND voltage to detect the magnitude of supply voltage variation; the pressure sensor sensitivity temperature secondary characteristics compensation values are calculated for entry into G3 using the temperature sensor output voltage and preloaded compensation data (EEPROM data). Sensitivity temperature drift Resolution: 1st order coeff: 10-bits; 2nd order coeff: 8-bits Adj. step: 1st order coeff: 0.196%; 2nd order coeff: 0.787%
Pressure Judge	Compares the pressure sensor VOUT pin output voltage to the threshold voltage to define the sensitivity temperature secondary characteristics compensation coefficient. Pressure determination threshold adj. Resolution: 10-bits Adj. step: 0.001*VDD (0.05*VDD – 0.95*VDD) Note that upon powering up and exiting standby (STBYN pin from low to high), the precise pressure cannot be determined until the VOUT pin output settles, depending on the external capacitance value of the VO pin. When the VOUT pin output voltage is more than the output reference voltage, the positive (+) sensitivity temperature secondary characteristic compensation coefficient is selected; but when the VOUT pin output voltage is less than the output reference voltage, the negative (-) sensitivity temperature secondary characteristic compensation coefficient is selected. Note) If the output reference voltage is half of VDD, pressure threshold adjustment is unnecessary. Even if the compensation coefficient +/- is not used, pressure threshold adjustment is required if the output reference voltage is set to a value other than half of VDD.
LPF	Anti-aliasing filter to eliminate the fold-back noise generated in the sample-and-hold circuit (S/H 1&2) in the later stage. The cutoff frequency is fc=60kHz.

Block	Functions
S/H1& Level shift	Doubles the LPF output for the sample and hold. It also modifies the output reference voltage. Output ref. voltage adj. Resolution: Rough: 5-bits; Fine: 6-bits Adj. step: 0.0005*VDD (0.0785*VDD – 0.9215*VDD) Description is with reference to VO pin. Note) If the output reference voltage is half of VDD, output reference voltage adjustment is unnecessary.
S/H2	Sample-and-hold circuit. A 32kΩ resistor is connected to the output stage. The combination with an external capacitor creates the LPF characteristics. Change the external capacitance value according to the desired signal band for detection using the following equation: fc=1/(2*π*32kΩ*C) (Hz) If the application does not require a low-impedance output, the VO pin output can be used as an alternative. In this case, set the EEPROM data to disable the buffer. Disabling the buffer allows for lower power dissipation. However, since the VO pin has a 32kΩ output impedance, connecting a resistive load will cause output voltage inaccuracies. Note also that the gain retained in the buffer cannot be achieved.
Buffer	Buffer to produce a band-limited output with low impedance. Typically provides a fourfold output (2x to 4x, in 0.5 steps). Reprogramming the EEPROM allows the buffer to be disabled for low power dissipation. (See S/H2.)
Timing Logic	Generates timing sync signals for internal operation and sampling frequencies for sensor output signals. Sampling frequencies can be selected from the EEPROM. Sampling frequency (fs): 100Hz (default); 1 kHz; 2kHz; 10.24kHz
Regulator	Constant voltage generator circuit to drive the sensor. The drive voltage can be selected from the EEPROM depending on the supply voltage being used. Drive voltage: 4.0V @VDD: 5V±10% (default); 2.0V @VDD: 2.2 to 3.6V
Pressure Detector	Pressure detection circuit and self-diagnosis circuit. The pressure range can be selected depending on the EEPROM data for the pressure detector. • Pressure above a certain value is detected (determined by threshold). • Pressure below a certain value is detected (determined by inverted threshold). • Pressure above or below a certain value is detected (determined both by a threshold and an inverted threshold). The DET pin goes high when the detected pressure exceeds the threshold. The detection threshold value can be set by entering it via the PTH pin or using the EEPROM data in the AK8996. Note that upon powering up and exiting standby (STBYN pin from low to high) the precise pressure cannot be determined until the VOUT pin output settles, depending on the setup and external capacitance value of the VO pin. The self-diagnostic circuit ensures that the output (VOUT pin) produces a given value by fixing the VP and VN pins at half of VDD upon power-up, or only at initial operation immediately after exiting the standby mode. In the event of any anomalies, signals go high at the DET pin. To reset the self-diagnostic circuit, set the STBYN low or recycle the power. Bear in mind that the self-diagnostic circuit does not detect all of the failure modes of the AK8996.

Reference Section & Others

Block	Functions
V_Bandgap (VBG) V_Reference (VREF) I_Reference (IREF)	Generates the reference voltage or bias current required for each circuit. Adjust the VREF voltage so that it is equivalent to 1.0V. VREF voltage adj. Resolution: 3-bits Adj. step: 1% step Adjust the IREF current so that it is equivalent to 20μA. IREF current adj. Resolution: 4-bits Adj. step: 2.7% steps typically
Oscillator (OSC)	Oscillator to generate timing sync signals for internal operation and sampling frequencies for sensor output signals. Adjust the oscillating frequency to 1024kHz. OSC adj. Resolution: 4-bits Adj. step: 5% steps
V_temp. (VTMP)	Temperature sensor for converting the ambient temperature to voltage. Adjust the temperature sensor output voltage (VTMP voltage) so that it is equivalent to VREF voltage at 25ºC. VTMP voltage adj. Resolution: 6-bits Adj. step: 0.2% (0.67°C) steps
V_Common (VCOM)	Generates analog circuit reference voltage 1/2VDD. Connect 10nF capacitance to this pin for stabilization. Since the output cannot drive current, do not connect a resistive load. The internal power-up circuit causes it to start up within the settling time for stable analog operation (Start Up valid time).
Power ON Delay (PODLY)	Upon power-up or exit from standby mode (low to high at the STBYN pin), this circuit generates the settling time for stable analog operation using the internal Power Up circuit. This circuit oversees the startup time for VREF or IREF and disables the OSC to prevent improper operation. When the settling time for stable analog operation expires, the OSC is enabled. Start up the supply voltage within 200 μsec (0.8*VDD<). If power-up is not started within 200 μsec, the AK8996 may enter the test mode. Note that the AK8996 may not function properly in the test mode (For the description of the function, refer to the Functional Description **9) Note on the AK8996 Power-up**). When recycling the power with the VDD pin and STBYN pin interconnected, it should be monitored to ensure that the supply voltage is below 0.1*VDD to enable the power-on reset.
Serial I/F	Serial interface for accessing EEPROM.
EEPROM & Control Register	EEPROM and control register (volatile memory). Used to store compensation values and measurement modes and to set up the measurement modes for adjustment.

Pin Assignments and Functions

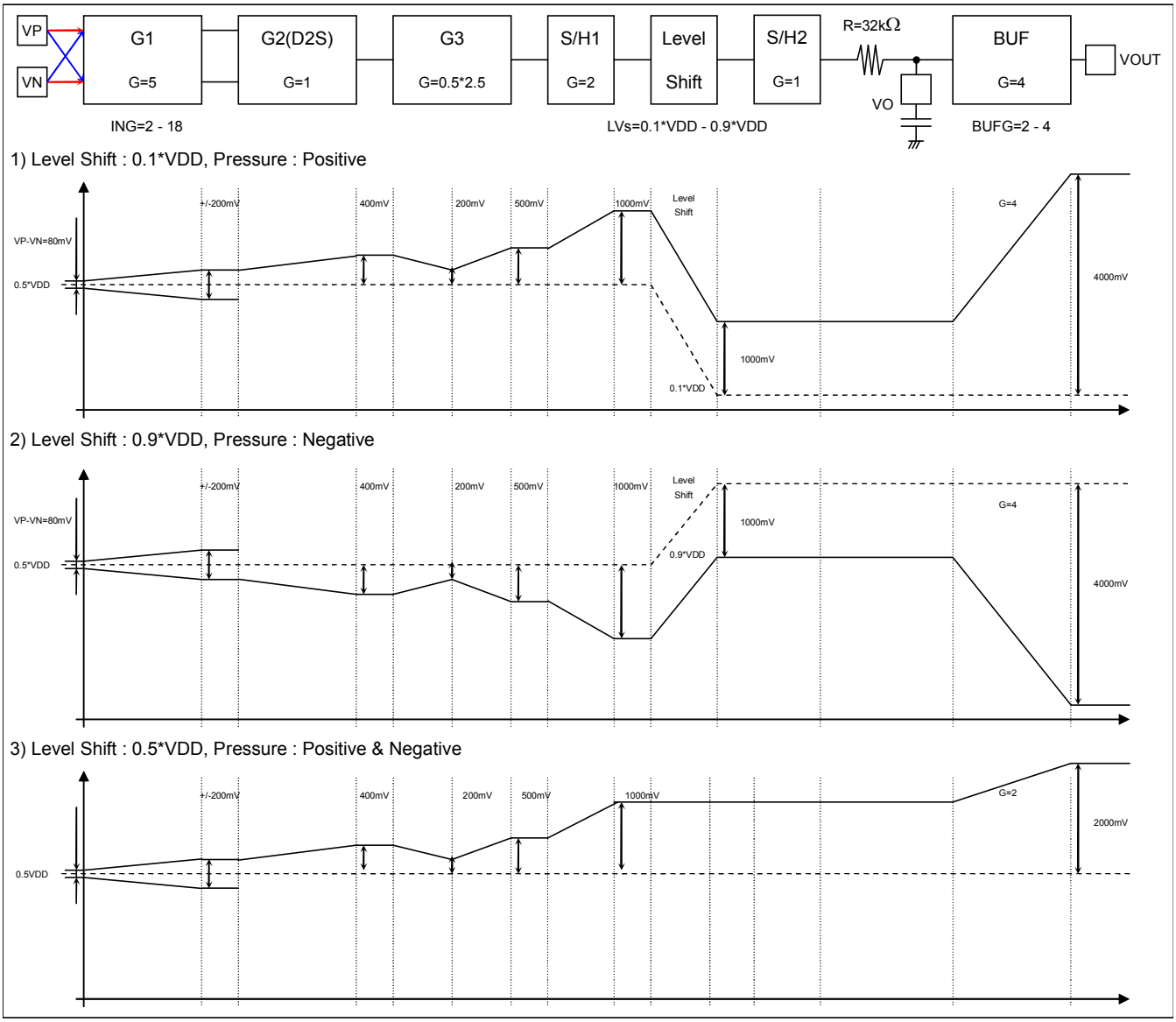
PAD	Name	I/O	C load max.	R load min.	Type	Comments
1	VSSO	O			GND	
2	VP	I			Analog	
3	VS	O	30pF	1kΩ	Analog	VDD > 2.7V
				3kΩ		VDD > 2.2V
4	VN	I			Analog	
5	STBYN	I			CMOS	Schmitt trigger input Connected to VDD when not in use.
6	CS	I			CMOS	Pull-down resistor (100kΩ) included
7	SCLK	I			CMOS	Pull-down resistor (100kΩ) included
8	SDI/O	I/O			CMOS	Pull-down resistor (100kΩ) included
9	DET	O			CMOS	
10	VSS				GND	
11	VDD				Power	
12	NC					Do not connect
13	VOUT	O	50pF	10kΩ	Analog	VDD > 2.7V
				20kΩ		VDD > 2.2V
14	VO	O	3μF		Analog	Due to the internal 32kΩ output resistor, resistive load connection is prohibited
15	PTH	I			Analog	
16	AGND	O			Analog	10nF connection; resistive load connection prohibited

Pin Descriptions

PAD	Name	Functions	Pin conditions			
			STBYN: "L"	DET: "H" EOUT[0]: "L"	DET: "H" EOUT[0]: "H"	Start up Note)
1	VSSO	Reference voltage output pin	-	-	-	-
2	VP	Sensor differential signal input pin (+ve)	Hi-Z			Hi-Z
3	VS	Constant voltage supply pin for sensor drive	Hi-Z			Hi-Z
4	VN	Sensor differential signal input pin (-ve)	Hi-Z			Hi-Z
5	STBYN	Standby pin ("L": Standby)	VSS	VDD	VDD	VDD
6	CS	Chip select pin	-	-	-	-
7	SCLK	Serial clock pin	-	-	-	-
8	SDI/O	Data I/O pin	-	-	-	-
9	DET	Output pin for pressure detection (high at detection) and output pin for abnormal self-diagnostic detection (high at detection)	VSS	VDD	VDD	VSS
10	VSS	Reference voltage pin	-	-	-	-
11	VDD	+ Power supply pin	-	-	-	-
12	NC		-	-	-	-
13	VOUT	Sensor signal pin	Hi-Z		Hi-Z	AGND
14	VO	Capacitance connection pin for sensor signal band-limiting	Hi-Z			AGND
15	PTH	Pin for pressure detection and self-diagnosis threshold input	-	-	-	-
16	AGND	Analog ground with external capacitance for stabilization	Hi-Z			AGND

Note) **See "Operation Sequence."**

Level Diagram



Electrical Characteristics

1) Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Units	Comments
Supply voltage	VDD	-0.3	6.5	V	
Input voltage	VDIN	VSS-0.3	VDD+0.3	V	
Input current	IIN	-10	10	mA	
Output current	IOUT	-10	10	mA	
Storage temp.	TST	-55	125	°C	EEPROM retention characteristics < 105ºC

Note) Operation at or beyond these limits may result in permanent damage to the device.

2) Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Units	Comments
Operating temp.	Ta	-40		105	°C	
Supply voltage	VDD1	2.2	3.0	3.6	V	EVD[0]=1
	VDD2	4.5	5.0	5.5	V	EVD[0]=0

3) Supply Voltage Current (See Functional Description)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Min.	Typ. Note1)	Max.	Units	Comments
Supply voltage current 0 note)	IDD0			1	μA	At standby
Supply voltage current 1 note)	IDD1		350	450	μA	Sampling frequency: 100Hz
Supply voltage current 2 note)	IDD2		250	340	μA	Sampling frequency: 100Hz Buffer OFF (EBU[0]=1)
Supply voltage current 3 note)	IDD3		570	680	μA	Sampling frequency: 1kHz
Supply voltage current 4 note)	IDD4		820	980	μA	Sampling frequency: 2kHz
Supply voltage current 5 note)	IDD5		2550	2850	μA	Sampling frequency: 10.24kHz

Note) At the time of measurement, a 3kΩ resistor load is applied to the VS pin, no load is applied to the VO&VOUT pin, and AGND is applied to the VP&VN pin.

Note1) Supply voltage current when VDD = 5.0V (EVD[0]=0).

4) EEPROM Characteristics

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Min.	Typ.	Max.	Units
EEPROM write voltage	Evdd	2.7			V
EEPROM write temp.	Eta	-40		85	°C
EEPROM endurance	Etime	1000			times
EEPROM data retention time	Ehold	10			years

5) Digital DC Characteristics

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Units
High level input voltage	VIH	1, 2		0.7*VDD	-	-	V
Low level input voltage	VIL	1, 2		-	-	0.3*VDD	V
High level input current 1	IIH1	1		+10	-	+200	μA
High level input current 2	IIH2	2		-10	-	+10	μA
Low level input current	IIL	1, 2		-10	-	+10	μA
High level output voltage	VOH	3	IOH= -200μA	0.9*VDD	-	-	V
Low level output voltage	VOL	3	IOL= +200μA	-	-	0.1*VDD	V

1 SDI(/O), SCLK, CS (integrated 100kΩ pull-down resistor)
2 STBYN (Schmitt trigger)
3 SD(I/)O, DET

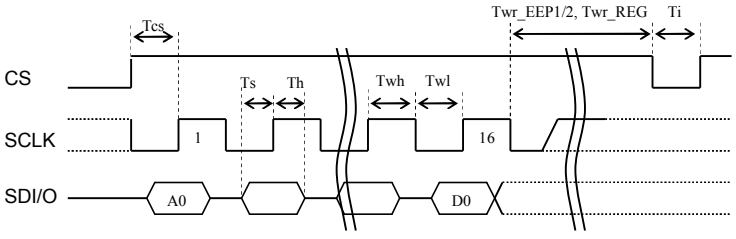
6) Digital AC Characteristics

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

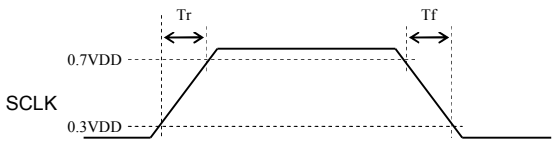
Item	Symbol	Min.	Typ.	Max.	Units
Write time (EEPROM address write)	Twr_EEP1	5		100	msec
Write time (EEPROM batch write)	Twr_EEP1	10		100	msec
Write time (register)	Twr_REG	300			nsec
CS setup time	Tcs	100			nsec
Data setup time	Ts	100			nsec
Data hold time	Th	100			nsec
SCLK high time	Twh	500			nsec
SCLK low time	Twl	500			nsec
SCLK → SDO delay time	Td			200	nsec
Idle time	Ti	100			nsec
SCLK rising time Note)	Tr			10	nsec
SCLK falling time Note)	Tf			10	nsec

Note) Design reference value; no production test performed.

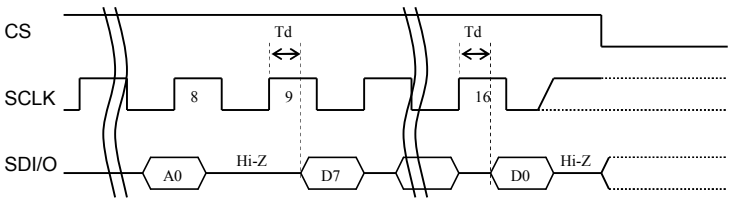
[Serial I/F timing (Write)]



[SCLK Raising/Falling timing]



[Serial I/F timing (Read)]

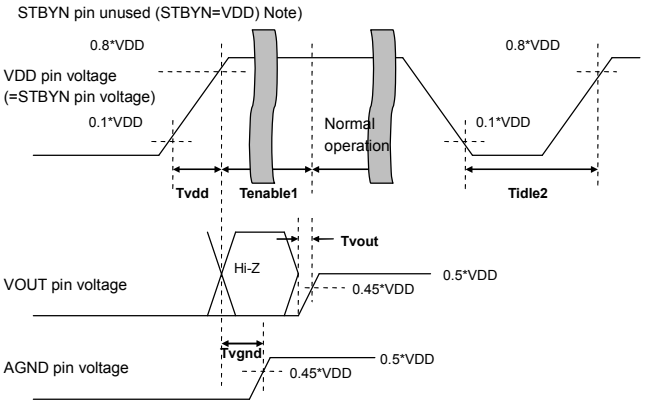


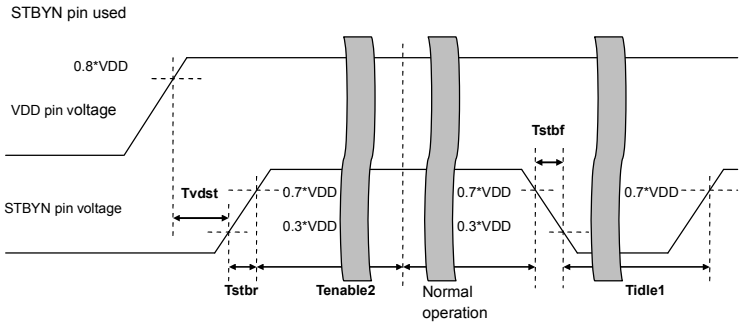
7) Power-Up and Standby Exit Time

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Min.	Typ.	Max.	Units	Comments
Power-up time	Tvdd			200	μsec	See Functional Description **9) Note on the AK8996 Power-up**
Standby exit time	Tvdst	10			nsec	
Standby rise time	Tstbr			10	nsec	
Standby fall time	Tstbf			10	nsec	
Standby valid time	Tidle1	1			msec	
	Tidle2	30			msec	VDD pin voltage<0.1*VDD
VOUT output rise time	Tvout			20	μsec	VO pin external capacitance<0.1μF
AGND output rise time	Tvgnd		150	250	μsec	AGND pin external capacitance: 10nF
Settling time for stable analog operation	Tenable1		280	465	μsec	
	Tenable2		350	495	μsec	

Note) Design reference value; no production test performed.



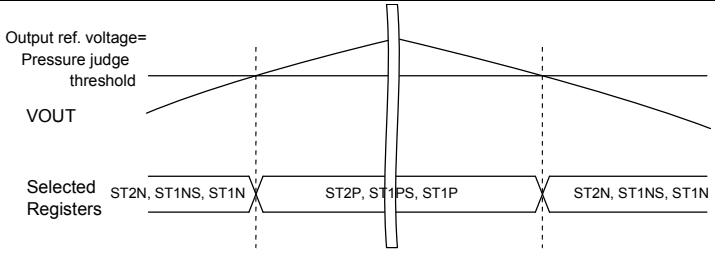


Note) When recycling the power with the VDD and STBYN pins connected, ensure that the supply voltage is below 0.1*VDD to enable the power on reset.

8) Pressure Determination Circuit (Pressure Judge)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

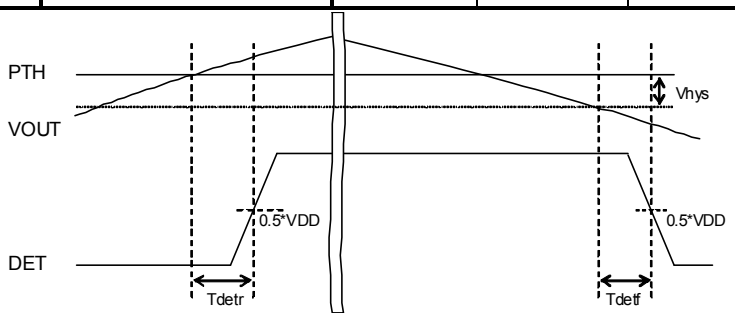
Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Pressure judge threshold	Vjudi	Unadjusted AM[3:0]:9h DET output	0.48*VDD	0.5*VDD	0.52*VDD	V	DET pin
Pressure judge threshold adjustment range	Vjud+	With respect to Vjudi Max: EPJLV[9:0]=23Eh		0.95*VDD		V	DET pin
	Vjud-	With respect to Vjudi Min: EPJLV[9:0]=1C2h		0.05*VDD		V	DET pin
Adj. Step	Vjstp			0.001 *VDD		V	DET pin



9) Pressure Detector

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Pressure detection threshold External input range	Vdeto5+	EINT1[1:0]=01 EINT2[0]=0 VDD=5V±5%	0.5*VDD		0.95*VDD	V	
	Vdeto3+	EINT1[1:0]=01 EINT2[0]=0 EVD[0]=1 VDD=2.2 - 3.6V	0.5*VDD		0.90*VDD		
Pressure detection threshold Internal set value	Vdeti	Unadjusted AM[3:0]:5h DET out EINT1[1:0]=01 EINT2[0]=1	0.72*VDD	0.74*VDD	0.76*VDD	V	
Pressure detection threshold Internal set value Adjust. width	Vdet5+	With respect to Vdeti Max: EPT[3:0]=7h VDD=V±5%		0.95*VDD		V	
	Vdet3+	EINT1[1:0]=01 EINT2[0]=0 EVD[0]=1 EPT[3:0]=6,7h prohibited VDD=2.2 - 3.6V		0.89*VDD			
	Vdet-	With respect to Vdeti Min: EPT[3:0]=8h		0.50*VDD		V	
Adjust. step	Vdstp			0.03*VDD		V	
Hysteresis voltage	Vhysi	Unadjusted AM[3:0]:7h DET out EINT1[1:0]=01	0.008 *VDD	0.020 *VDD	0.032 *VDD	V	
Hysteresis voltage Adjust. width	Vhys+	With respect to Vhysi Max: EHYS[2:0]=0h		0.0		V	
	Vhys-	With respect to Vhysi Min: EHYS[2:0]=7h		-0.0175 *VDD		V	
Adjust. step	Vhstp			-0.0025 *VDD		V	
Pressure detection time	Tdetr	EINT1[1:0]=01		450	600	µsec	
Pressure non-detection time	Tdetf	EINT1[1:0]=01		450	600	µsec	
Pressure detector Disable time Adjust. width	Tasdis+	EAS[2:0]=7h ESF[1:0]=3h EINT1[1:0]=01		12.5		msec	
		0.1		msec			



10) Self-Diagnostic Circuit

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Self-diagnostic normal operation judgment range	Vself	EINT1[1:0]=10	0.48*VDD -0.1		0.52*VDD +0.1	V	
Self-diagnostic detection time	Tself	EINT1[1:0]=10		450	600	µsec	

11) Analog Characteristics

11-1) Reference Section

11-1-1) Reference Section Characteristics

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
VREF voltage	Vr0	Unadjusted AM[3:0]:1h DET out	0.97	1.0	1.04	V	
VREF adj. width	Vr+	With respect to Vr0 Max: EVR[2:0]=3h		+30		mV	
	Vr-	With respect to Vr0 Min: EVR[2:0]=4h		-40		mV	
VREF adj. step	Vrstp			10		mV	
VS voltage	VS51	After VREF adj. VS pin out Load resistance: 3kΩ	3.88	4.00	4.12	V	
	VS52	Load resistance: 1kΩ	3.88	4.00	4.12		VDD>2.7V
	VS31	After VREF adj. VS pin out Load resistance: 3kΩ	1.94	2.00	2.06	V	
	VS32	Load resistance: 1kΩ	1.94	2.00	2.06		VDD>2.7V
IREF current	Ir0	Unadjusted AM[3:0]:2h DET out	16.15	20	24.98	µA	
IREF adj. width	Ir+	With respect to Ir0 Max: EIR[3:0]=7h		+4.81		µA	
	Ir-	With respect to Ir0 Min: EIR[3:0]=8h		-3.40		µA	
IREF adj. step	Irstp			0.547		µA	
OSC freq.	Fr0	Unadjusted AM[3:0]:3h DET out	768	1024	1288	kHz	
OSC adj. width	Fr+	With respect to Fr0 Max: EFR[3:0]=4h		204.8		kHz	
	Fr-	With respect to Fr0 Min: EFR[3:0]=Ch		-204.8		kHz	
OSC adj. step	Frstp			51.2		kHz	

11-1-1) Reference Section Characteristics (Continued)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
VTMP voltage	Vt0	Unadj. (Temp = 25°C) AM[3:0]:4h DET out	0.936	1.0	1.062	V	
VTMP adj. width	Vt0+	With respect to Vt0 Max: ETM[5:0]=1Fh		+62		mV	
	Vt0-	With respect to Vt0 Min: ETM[5:0]=20h		-64		mV	
VTMP adj. step	Vt0stp			2.0		mV	
VTMP temp variation	Vt	Temp = -40 to 105°C		3.0		mV/°C	Note)
AGND voltage	Vag		0.5*VDD -0.06	0.5*VDD	0.5*VDD +0.06	V	

Note) Design reference value; no production test performed.

11-1-2) Reference Section (packaged version only) Characteristics (note)

Unless otherwise specified, VDD = 4.5 to 5.5V, Temperature = -40 to 105ºC

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
VREF voltage	Vr0P	AM[3:0]:1h DET out	0.99	1.0	1.01	V	After adj.
VS voltage	VS51P	Load resistance: 3kΩ	3.88	4.00	4.12	V	After adj.
	VS52P	Load resistance: 1kΩ	3.88	4.00	4.12		After adj.
IREF current	Ir0P	AM[3:0]:2h DET out	18	20	22	µA	After adj.
OSC freq.	Fr0P	AM[3:0]:3h DET out	921.6	1024	1126.4	kHz	After adj.
VTMP voltage	Vt0P	AM[3:0]:4h DET out	0.994	1.0	1.006	V	After adj. @25°C

Note) Factory default adjustment is referenced to 5V mode (EVD[0]=0). If 3V mode (EVD[0]=1) is used, readjustment is required

11-2) Gain Amplifier and Other Blocks

Unless otherwise specified, the following requirements apply.

- Reference Section is complete with adjustment.
- For supply voltage of 5V (3V), the level diagram includes G1 gain of 5x, Level shift 0.1*VDD and BUFF gain of 4x (see level diagram 1) and the output voltage 4000mV (2000mV) is set as 100% based on a differential input of 80mV (40mV).

11-2-1) Overall Characteristics

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Std. gain	Gtyp	VP/VN → VOUT		50		times	
Input common voltage	Vicom		0.45VS	0.5*VS	0.55VS	V	
Output common voltage	Vcom0	VP/VN → VOUT VP=VN=0.5*VS		0.1*VDD		V	
Max. output range	Vmax+	VP/VN → VOUT	0.9*VDD			V	
	Vmax-	VP-VN=VSS or VDD			0.1*VDD	V	
Non-input noise	Nout	VP/VN → VOUT VP=VN=Open VO external capacitance: 10nF			1,000	µVrms	@1Hz - 100kHz Note)

Note) Value for 50x nominal gain. Design reference value; no production test performed.

11-2-2) G1/2 Gain Adjustment Circuit

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode							
Unadjusted G1/2 output voltage	Vg10	VP-VN=80mV VDD=5V±5% EIG[2:0]=0h, EIG[3]=0	145	160	175	mV	
	Vg02	VP-VN=40mV VDD=2.2 - 3.6V EIG[2:0]=0h, EIG[3]=0 EVD[0]=1	73.0	80	87.0	mV	
G1 adjustment range	G1sc+	EIG[2:0]=7h		9		times	
	G1sc-	EIG[2:0]=0h		2		times	
Adj. step	G1sc stp			1		times	
G2 adj.	G2sc+	EIG[3]=1		2		times	
	G2sc-	EIG[3]=0		1		times	

11-2-3) Offset Voltage Adjustment Circuit

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode							
Unadjusted output voltage	Vo01	VDD=5V±5%	0.5*VDD –30	0.5*VDD	0.5*VDD +30	mV	
	Vo02	VDD=2.2-3.6V EVD[0]=1	0.5*VDD –15	0.5*VDD	0.5*VDD +15	mV	
Offset rough adj. DAC adj. range	Ocmp+	EOC[10]=0h EOC[9:7]=7h		+52.5		%	
	Ocmn+	EOC[10]=1h EOC[9:7]=7h		-52.5		%	
Adj. step	Ocm stp			7.5		%	
Offset fine adj. DAC adj. range	Ocl+	EOC[10]=0h EOC[6:0]=3Fh		+7.875		%	
	Ocl-	EOC[10]=1h EOC[6:0]=3Fh		-7.875		%	
Adj. step	Ocl stp			0.125		%	

11-2-4) Span Voltage Adjustment Circuit

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage adjustment							
Unadjusted Span voltage	Vs01	VP-VN=80 mV@5V	480	500	520	mV	
	Vs02	VP-VN=40 mV@3V EVD[0]=1	240	250	260	mV	
Span adj. range	Sc+	ESC[8:0]=0FFh		100/36.25		times	
	Sc-	ESC[8:0]=100h		100/164		times	
Adj. Step	Sc stp	N=-256 - +255		100/(100+0.25*N)		times	

11-2-5) Offset Temperature Drift & Sensitivity Temperature Drift Adjustment Circuit

11-2-5-1) Quadratic Function Generator (a*Temp^2+b*Temp+c)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
2nd order coeff. a Adj. range 1	A2nd5+	VDD=5V±5%		+0.0016			
	A2nd5-			-0.0016			
Adj. step 1	A2nd5 stp			1.260E-5			
2nd order coeff. a Adj. range 2	A2nd3+	VDD=2.2 - 3.6V		+0.0008			
	A2nd3-			-0.0008			
Adj. step 2	A2nd3 stp			0.630E-5			

Note) Design reference value; no production test performed.

11-2-5-2) Offset Linear Function Generator (d*Temp+e)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
1st order coeff. d Adj. range 1	D2ndO5+	VDD=5V±5%		+0.60			
	D2ndO5-			-0.60			
Adj. step 1	D2ndO5 stp			0.0012			
1st order coeff. d Adj. range 2	D2ndO3+	VDD=2.2 - 3.6V		+0.30			
	D2ndO3-			-0.30			
Adj. step 2	D2ndO3 stp			0.00060			

Note) Design reference value; no production test performed.

11-2-5-3) Sensitivity Linear Function Generator (d*Temp+e)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
1st order coeff. d Adj. range 1	D2ndS5+	VDD=5V±5%		+0.32			
	D2ndS5-			-0.32			
Adj. step 1	D2ndS5 stp			0.000626			
1st order coeff. d Adj. range 2	D2ndS3+	VDD=2.2 - 3.6V		+0.30			
	D2ndS3-			-0.30			
Adj. step 2	D2ndS3 stp			0.00060			

Note) Design reference value; no production test performed.

11-2-6) Supply Voltage & Temperature Sensitivity Variation Adjustment Circuit (ST & SV)

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
Sensitivity variation characteristics to supply voltage	SV1	Unadjusted SV circuit initial operation			5.0	%	With respect to target value
	SV2	SV circuit 2nd operation		±0.25		%	With respect to SV1
Sensitivity variation characteristics to operating temperature	ST1	Unadjusted ST initial operation			5.0	%	With respect to target value
	ST2	ST circuit 2nd operation		±0.25		%	With respect to ST1

11-2-7) LPF, S/H1&2, & Buffer

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
LPF freq. response	Fc1		40	60	80	kHz	
S/H1&2 gain	SHG		1.935	2	2.065	times	
S/H1&2 out pre-adj. error	SHerr		-20	0	20	mV	
S/H2 output resistance post-adj. error	Rout		24.6	32	39.4	kΩ	
BUF gain adj. width	Bufg+	EOG[2:0]=4h		4		times	
	Bufg-	EOG[2:0]=0h		2		times	
Adj. step	Bufgstp			0.5		times	10kΩ
BUF output (VOUT) drive characteristics	Rbuf1+	Load resistance: 20 kΩ	0.9*VDD			V	
	Rbuf1-				0.1*VDD	V	
	Rbuf2+	Load resistance: 10 kΩ	0.9*VDD			V	VDD>2.7V
	Rbuf2-				0.1*VDD	V	VDD>2.7V

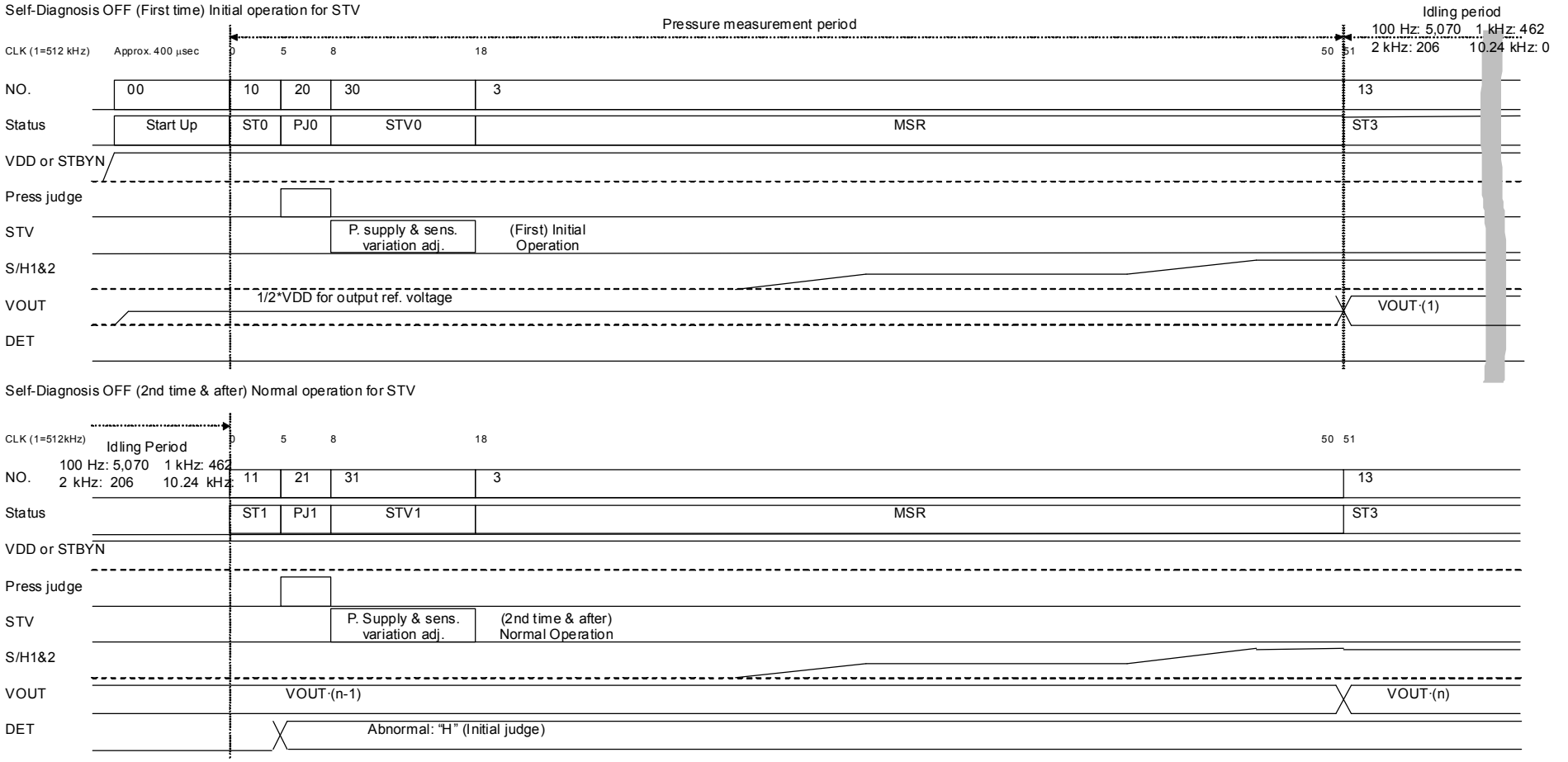
11-2-8) Level shift

Unless otherwise specified, VDD = 2.2 to 5.5V, Temperature = -40 to 105ºC, register default

Item	Symbol	Conditions	Min.	Typ.	Max.	Units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
Output reference voltage Rough adj. width (Level shift)	Vlv0	Unadjusted AM[3:0]:9h VS input → VO out	0.5*VDD –0.02	0.5*VDD	0.5*VDD +0.02	V	VO pin
	Vlvr+	Vlv0 reference Max: ELV[10:6]=1Fh		0.890 *VDD		V	VO pin
	Vlvr-	Vlvo reference Min: ELV[10:6]=0Fh		0.110 *VDD		V	VO pin
	Vlrstp			0.026 *VDD		V	VO pin
Output reference voltage Fine adj. width (Level shift)	Vlvf+	Vlv0 reference Max: ELV[10]=1h, ELV[5:0]=3Fh		0.0315 *VDD		V	VO pin
	Vlvf-	Vlv0 reference Min: ELV[10]=0h, ELV[5:0]=3Fh		-0.0315 *VDD		V	VO pin
	Vlfstp			0.0005 *VDD		V	VO pin

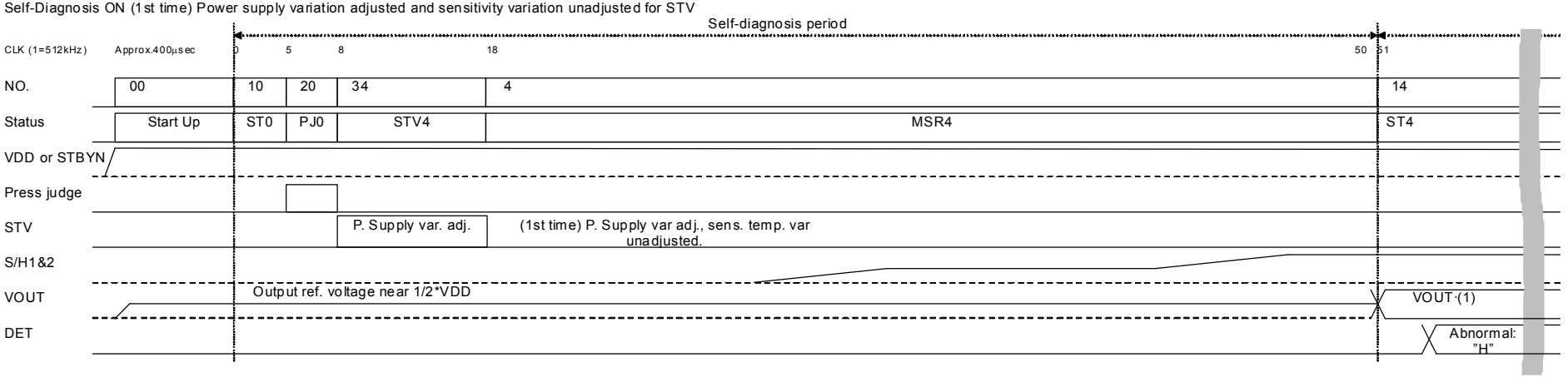
Operation Sequence

1. Normal Operation Timing (Pressure Detector Valid)

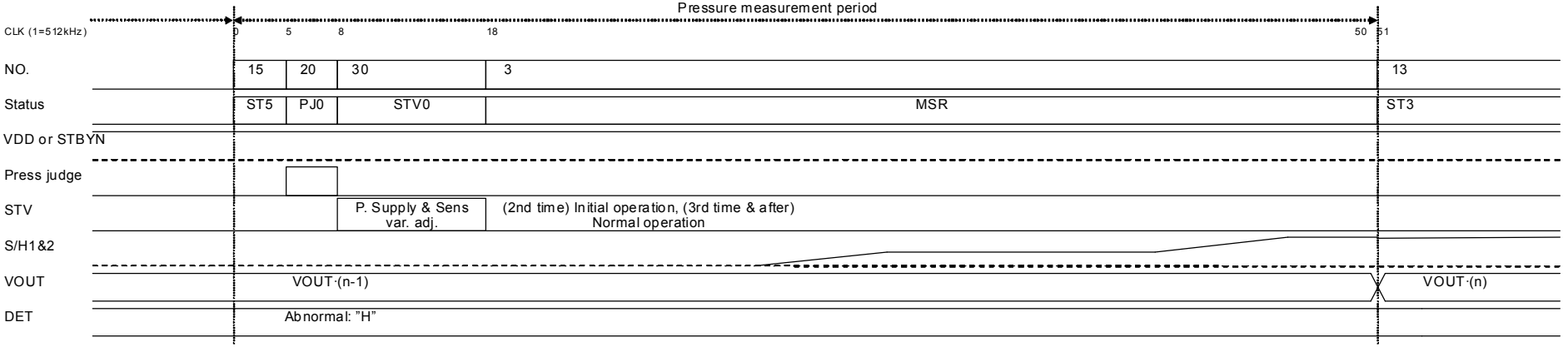


2. Operation Timing when the Self-Diagnosis Circuit is Valid (Pressure Detector Valid)

Self-Diagnosis ON (1st time) Power supply variation adjusted and sensitivity variation unadjusted for STV



Self-Diagnosis ON (2nd time) Initial operation for STV



3. Description of Operation Timing Status

3.1 Normal Operation Timing

No.	State	CLK	Operations
00	Start Up		Analog circuit settling time for stable operation. Analog reference circuits as VREF & IREF start up and configured output reference voltage is provided at VOUT pin.
10	ST0		Clock count start Analog circuit startup
20	PJ0	CLK=5	Pressure judge circuit not in operation
30	STV0	CLK=8	STV initial operation
3	MSR	CLK=18	Output pressure (VP-VN) to VOUT
13	ST3	CLK=51	Idling With fs=10.24kHz setup, no idling and in continuous operation. Idling period 100Hz 5,070 CLK 1kHz 482 CLK 2kHz 206 CLK 10.24kHz 0 CLK
11	ST1	CLK1=51 or 256 or 512 or 5120	Pressure detection operation and analog circuit startup
21	PJ1	CLK=5+CLK1	Pressure judge circuit operation (Positive/negative pressure determination)
31	STV1	CLK=8+CLK1	STV normal operation
:	:	:	:

3.2 Self-Diagnostic Circuit in Operation

No.	State	Trigger	Operations
00	Start Up		Analog circuit settling time for stable operation. Analog reference circuits VREF & IREF start up and configured output reference voltage is provided at VOUT pin.
10	ST0		Clock count start Analog circuit startup
20	PJ0	CLK=5	Pressure judge circuit not in operation
34	STV4	CLK=8	SV initial operation (ST not in operation)
4	MSR4	CLK=18	VP&VN pin fixed to 1/2*VS; given value output to VOUT
14	ST4	CLK=51	Self-diagnostic circuit operation & idling Back to normal operation on completing self-diagnosis in 50 CLK.
15	ST5	CLK=100	Analog circuit startup
20	PJ0	CLK=105	Pressure judge circuit not in operation
30	STV0	CLK=108	STV initial operation
3	MSR	CLK=118	Output pressure (VP-VN=0V) to VOUT
:	:	:	:(Same as operation after ST3 in 3.1 Normal Operation Timing)