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Preliminary **AK8998/W/D**

The AK8998 is a pressure sensor interface IC that features compensation for temperature drift and sensor variation. It is designed to excite and interface to a bridge sensor. Variations in the sensor can be corrected via compensation values stored in integrated non-volatile memory (EEPROM). Compensation values are obtained from measurement results for a set of offset voltages and temperature drift, along with a set of bridge voltages and temperature drift, including characteristics of the AK8998. The AK8998 is available in a 16-pin QFN package, in wafer form and in a tray.

Features

- **Pressure sensor compensation and excitation IC (Analog output)**
- **Supply voltage current: 7.1mA max @10kHz sampling**
- **Supply voltage: 3.0V±5%, 3.3V±5%, 5.0V±5%**
- **Operating temperature range: -20 to 85ºC**
- **Integrated sensor output compensation (AK8998 Input conversion)**
  - **Offset voltage adjustment**
    - **Adjustment range: Rough ±13 to ±373mV / Fine ±1 to ±34mV @5.0V**
    - **Adjustment step: Rough 2 to 53mV /step / Fine 0.01 to 0.27mV /step @5.0V**
  - **Offset voltage temperature drift adjustment (1st order coefficient)**
    - **Adjustment range: ±0.04 to ±1.23mV/ºC @5.0V**
    - **Adjustment step: 0.2 to 4.8µV/ºC @5.0V**
  - **Output span voltage adjustment (G1, G2, G3)**
    - **Total adjustment range: 5.7 to 261.6mV @5.0V**
    - **G1 adjustment step: 0.95 to 74.7mV /step @5.0V**
    - **G2 adjustment step: 5.7 to 130.8mV /step @5.0V**
    - **G3 adjustment step: 0.01 to 0.40mV /step @5.0V**
  - **Sensitivity temperature drift adjustment (1st order coefficient)**
    - **Adjustment range: -4000ppm/ºC to +2500ppm/ºC or -2500ppm/ºC to +1000ppm/ºC**
    - **Adjustment step: 18ppm/ºC step**
- **Integrated output reference voltage adjustment function**
  - **Adjustment range: 0.02*VDD to 0.98*VDD**
  - **Adjustment step: 10mV /step @5.0V**
- **Integrated sampling frequency switching function: 1kHz, 10kHz**
- **Integrated analog circuit reference voltage stabilizer (Add an external capacitor to AGND pin as needed)**
- **SCF and SMF included for band limitation: fc:1.0kHz, 500Hz, 250Hz**
- **2 wire serial interface (CSCLK, VOUT)**
- **Ratiometric voltage output**
- **Integrated constant voltage source for pressure sensor: 2.2V @ 3.0, 3.3V±5%**
  4.0V or 2.2V @ 5.0V±5%
- **Integrated pressure detectors (x2)**
  - **Detection threshold adjustment control**
    - **Adjustment range: 0.125*VDD to 0.9*VDD**
    - **Adjustment step: 0.025*VDD /step**
  - **Detection threshold external setting function (DET2 / PTH pin use)**
  - **hysteresis voltage adjustment control**
    - **Adjustment range: 0.03*VDD to 0.06*VDD**
    - **Adjustment step: 0.01*VDD /step**
- **Integrated reference voltage & reference current generator**
  - **VREF voltage adjustment control**
    - **Resolution: 3bits**
    - **Adjustment step: 1% /step**

- IREF current adjustment control
  - Resolution: 4bits
  - Adjustment step: 2.8% /step typ.

• Temperature sensor (internal or external)
- Temperature range: -20 to 85 °C
- Internal temperature sensor output voltage adjustment control
  - Resolution: 6 bits
  - Adjustment step: 0.2% /step
- External temperature sensor output voltage adjustment control
  - Resolution: 9 bits（Rough/ Fine=3/6bits）
  - Adjustment step: Rough 10% /step / Fine 0.2% /step
- Integrated external temperature sensor constant current circuit: 50μA typ.

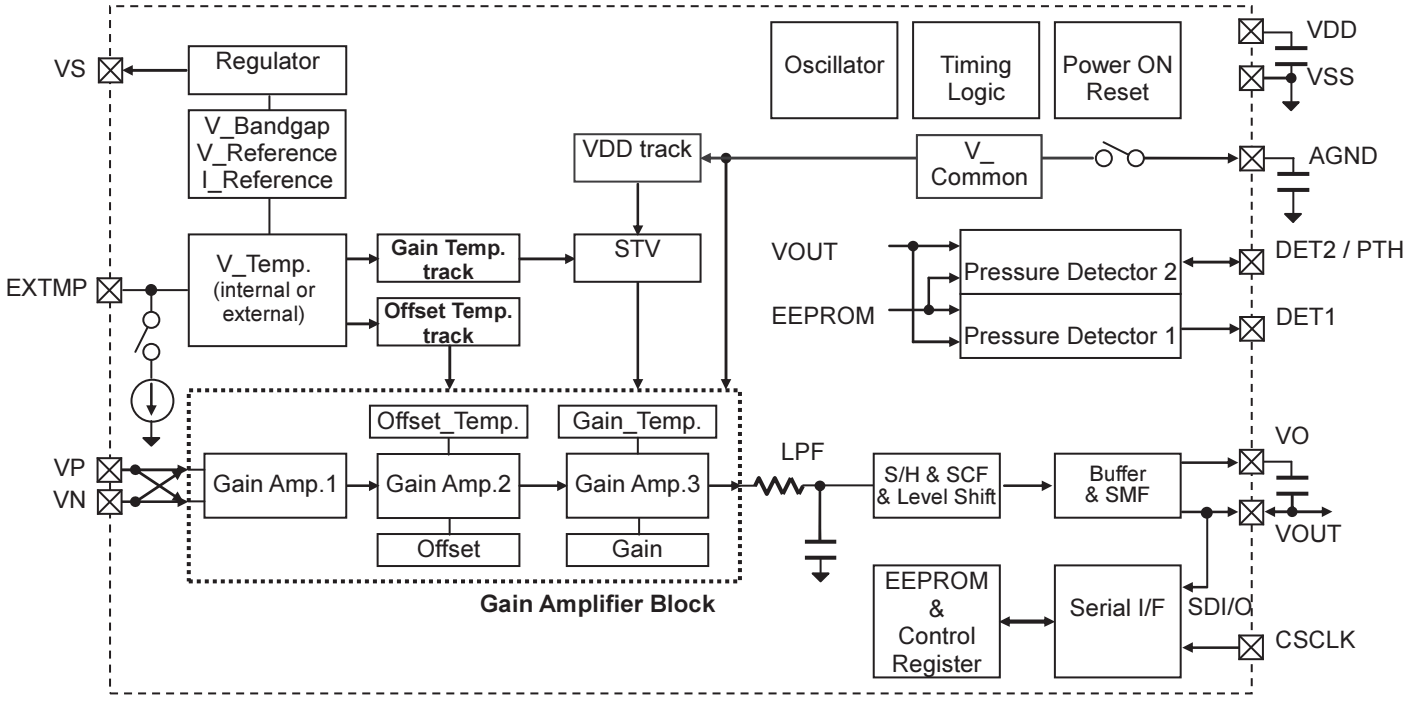
• Integrated oscillator for intermittent operation (1000kHz typ.)
- Oscillating frequency adjustment control
  - Resolution: 4 bits
  - Adjustment step: 5% /step typ.

• Integrated EEPROM for compensation values and control data storage
- Size: 131 bits
- Endurance: 1,000 times or more
- Retention time: 10 years or more @Ta: 85°C

• Supply Type: Tray (Die), Wafer, PKG (UQFN16)

Product name	Supply Type	Comments
AK8998	PKG (UQFN16)	
AK8998W	Wafer	
AK8998D	Tray (Die)	

Block Diagram



Overview

The AK8998 is a pressure sensor interface IC that features compensation for temperature drift and sensor variation.

It is designed to excite and interface to a bridge sensor. Variations in the sensor can be corrected via compensation values stored in integrated non-volatile memory (EEPROM). Compensation values are obtained from measurement results for a set of offset voltages and temperature drift, along with a set of bridge voltages and temperature drift, including characteristics of the AK8998.

The internal compensation circuit is accomplished through a 12-bit resolution DAC (Rough: 4bits, Fine: 8bits) to adjust offset voltage, and the primary characteristics compensator for the associated temperature drift, coupled with 13-bit resolution (G1&G2 Gain adjustment: 5bits, G3 Gain adjustment: 8bits) to adjust the span voltage and another primary characteristics compensator for its associated temperature drift.

The output stage, with an internal resistor of 146kΩ, is band-limited with a combination of external capacitors, providing a low impedance output. And the EEPROM data, if used, enables the internal SCF and SMF. In this case, the band limitation is performed by the internal LPF (fc: 1kHz, 500Hz, 250Hz), eliminating the need for the external capacitors.

EEPROM data can be preconfigured to enable a setup of output reference voltage, designation of the external temperature sensor (when a pressure sensor and AK8998 are separated), selection of a sampling frequency (1kHz or 10kHz), the input polarity, and AGND pin validation.

Two sets of the pressure detectors are provided. When the pressure exceeding the detection threshold stored in the EEPROM is applied, the DET 1 and/or DET2/PTH pins go high (the polarity change is possible by EEPROM). And the detection threshold can be specified externally by EEPROM. In that case, the Pressure Detectors 2 is disabled, and the detection threshold for the Pressure Detectors 1 can be defined by DET2/PTH pin.

It can access to the EEPROM and control register (volatile memory) by a two-wire serial interface of CSCLK and VOUT (at the time of SDI/O mode) pin.

Pin Configuration

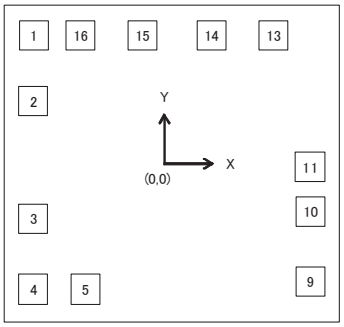
1. Wafer Configuration

1) Die size 2.082mm x 1.662mm
2) Die thickness 280μm
3) PAD size 80μm x 80μm
4) PAD pitch 150μm<
5) Scribe size 80μm
6) Wafer size 6 inch

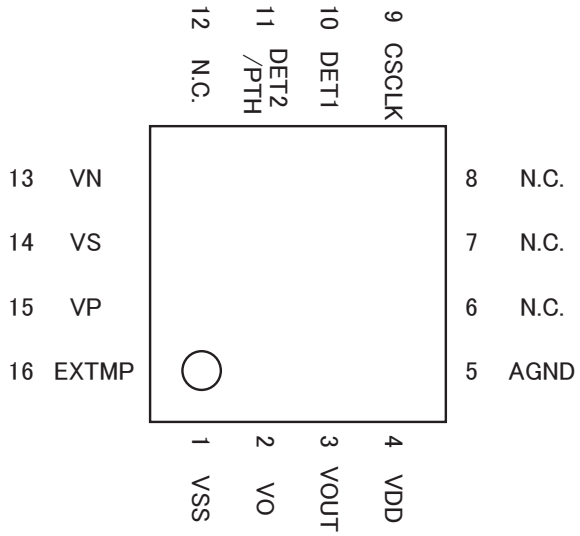
Pin numbers and Pad position

No.	Pin Name	X Location (μm)	Y Location (μm)	No.	Pin Name	X Location (μm)	Y Location (μm)
1	VSS	-894.8	687.2	9	CSCLK	894.8	-544.7
2	VO	-894.8	337.8	10	DET1	894.8	-242.5
3	VOUT	-894.8	-344.7	11	DET2/PTH	894.8	-57.9
4	VDD	-894.8	-687.1	12	N.C.		
5	AGND	-521.7	-684.8	13	VN	749.3	684.8
6	N.C.			14	VS	363.4	684.8
7	N.C.			15	VP	-236.7	684.8
8	N.C.			16	EXTMP	-716.4	684.8

Pad locations (Top view)



2. Package Outline (UQFN16)



Adjustment Characteristics

1) Sensor Characteristics

■VDD: 5V

Item	Symbol	Min.	Typ.	Max.	units	Comments
Drive voltage	Svs1		2.2		V	EVD[1:0]=1h
	Svs2		4.0		V	EVD[1:0]=0h
Temperature range	Sta	-20		85	°C	
Sensor resistance	Sres1	0.82	4.00	6.50	kΩ	EVD[1:0]=1h
	Sres2	1.00	4.00	6.50	kΩ	EVD[1:0]=0h
Voltage input span range	Sspnin1	12.00	44.00	76.00	mV	Sensor1
	Sspnin2	17.00	70.00	125.00	mV	Sensor2
Offset voltage adjustment range	Soff1	-15.00	0.00	15.00	mV	Sensor1
	Soff2	-35.00	0.00	35.00	mV	Sensor2
Sensitivity temp. drift coefficient	Sst1	-4000		2500	ppm/°C	ESTC[0]=1h
	Sst2	-2500		1000	ppm/°C	ESTC[0]=0h
Offset temp. drift coefficient	Sot1	-0.040	0.00	0.040	mV/°C	Sensor1
	Sot2	-0.080	0.00	0.080	mV/°C	Sensor2

■VDD:3, 3.3V

Item	Symbol	Min.	Typ.	Max.	units	Comments
Drive voltage	Svs		2.2		V	
Temperature range	Sta	-20		85	°C	
Sensor resistance	Sres	0.82	4.00	6.50	kΩ	
Voltage input span range	Sspnin1	6.60	24.20	41.80	mV	Sensor1
	Sspnin2	9.00	40.00	70.00	mV	Sensor2
Offset voltage adjustment range	Soff1	-8.25	0.00	8.25	mV	Sensor1
	Soff2	-19.25	0.00	19.25	mV	Sensor2
Sensitivity temp. drift coefficient	Sst1	-4000		2500	ppm/°C	ESTC[0]=1h
	Sst2	-2500		1000	ppm/°C	ESTC[0]=0h
Offset temp. drift coefficient	Sot1	-0.022	0.00	0.022	mV/°C	Sensor1
	Sot2	-0.044	0.00	0.044	mV/°C	Sensor2

Note) The usage combines characteristics of senser 1/2 is not allowed. Such a case as Span voltage is said as the sensor 1 and except is said as the sensor 2).

2) Adjustment Accuracy

Item	Symbol	Min.	Typ. Note4)	Max. Note5)	units	Comments
Offset adjustment accuracy	Cof		0.083		%FS	
Offset temp. drift adjustment accuracy	Coft		0.090		%FS	
Output span adjustment accuracy	Csn		0.125		%FS	
Sensitivity temp. adjustment accuracy	Csnt		0.054		%FS	
Sensitivity supply voltage and temp. variation step	Cstv		0.316		%FS	ESTC[0]=1h
			0.158		%FS	ESTC[0]=0h
Sample and hold circuit output error	Cshe		0.0		%FS	
Offset adjustment accuracy Note1)	Cofall		0.122	1.0	%FS	
Span adjustment accuracy Note2)	Csnall		0.344	1.0	%FS	ESTC[0]=1h
			0.209	1.0	%FS	ESTC[0]=0h
Offset adjustment accuracy Note3)	Call		0.344	1.0	%FS	ESTC[0]=1h
			0.209	1.0	%FS	ESTC[0]=0h

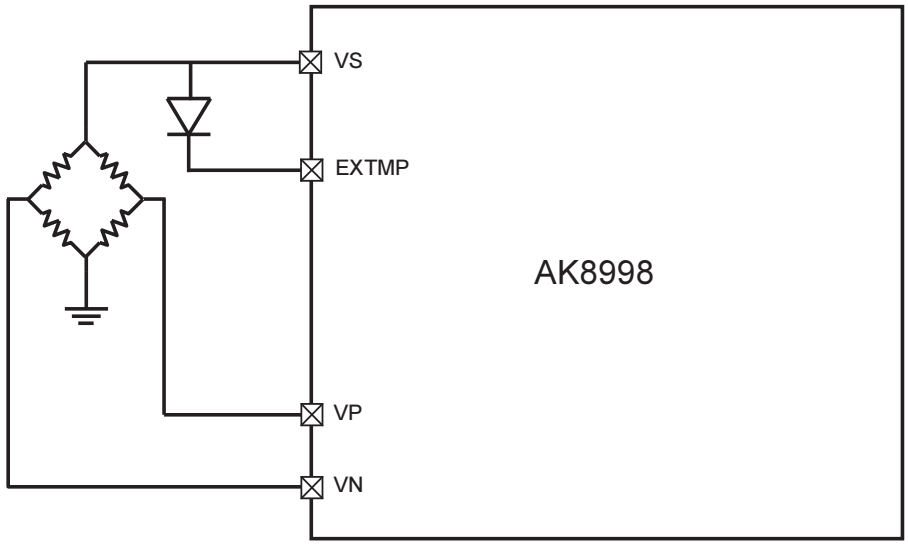
Note1) Cofall=(Cof^2+Coft^2)^(1/2)
Note2) Csnall=(Csn^2+Csnt^2+Cstv^2+Cshe^2)^(1/2)
Note3) Call=max(Cofall,Csnall)
Note4) Temp.=85ºC, VDD=4.75V, G1=10x, G2=1.5x(1.176x), G3=1.8x(2.3x), Offset temp. drift 1st order coefficient=Min./Max., Sensitivity temp. drift 1st order coefficient=Min.*1/2, VOUT output band-limited (≤500Hz @Fs=10kHz, ≤50Hz@Fs=1kHz) effective
Note5) Temp.=-20 to 85ºC, VDD=5V±5%, 3.3V±5%, 3.0V±5%, G1/G2/G3 =Min. to Max., Each temperature coefficient=Min. to Max., VOUT output band-limited (≤500Hz @Fs=10kHz, ≤50Hz@Fs=1kHz) effective

* The adjustment accuracy is based on our definition as a reference. Please be aware the accuracy of product depends on the sensor characteristics and adjustment method.

3) External Temperature Sensor Characteristics

Item	Symbol	Min.	Typ.	Max.	units	Comments
Sensor drive current	Tsdi		50		μA	
Sensor temp. variation	Tss	-2.4	-2.2	-2.0	mV/°C	50μA current drive
Sensor voltage @25°C	Tsv25	550	600	650	mV	50μA current drive

4) Connection of Pressure Sensor and External Temperature Sensor



Description of Blocks

[Gain Amplifier Block, LPF, S/H&SCF& Level shifter, Buffer&SMF]

The set of these blocks amplifies, compensates and outputs the pressure sensor level
This set of blocks intermittently amplifies, compensates, samples and holds the pressure sensor output. The output stage, with an internal resistor of 146kΩ, is band-limited with a combination of external capacitors, providing a low impedance output. SCF and SMF are available for output, eliminating the need for the external capacitors. A percentage designator is used, benchmarked with 4800mVdc output at 100%, reflecting the 60x increase in differential input from 80mVdc.

Block	Functions
Gain Amp. 1/2/3 Gain (G1/2/3)	Gain Amp.1 is a low-noise high-gain amplifier at the front end. The differential signal is amplified by a factor of 10x typ. (5x to 70x). Gain Amp.2 converts the G1 differential output to single-ended with reference to AGND and amplifies by a factor of 1.5x typ. (1.5x or 3.0x) or 1.176x typ. (1.176x or 2.352x). Gain Amp.3 amplifies by a factor of 1.8x typ. (1.1x to 1.8x) or 2.3x typ. (1.4x to 2.3x). G2 gain and G3 gain are changed automatically by sensitivity temperature drift adjustment range change setup (ESTC [0]). Span voltage is adjusted with G1/2/3 Gain (G1/2: rough adjustment, G3: fine adjustment).
Offset_Temp. Offset Offset Temp. track (G2)	The preloaded compensation data in the EEPROM enables the pressure sensor offset voltage and offset temperature drift to be compensated. The following adjustment value is AK8998 input conversion @5.0V. Offset adj.Adj. range Rough ±13 to ±373mV / Fine ±1 to ±34mV Adj. step Rough 2 to 53mV /step / Fine 0.01 to 0.27mV /step Offset temp. drift. adj. Adj. range ±0.04 to ±1.23mV/ ºC Adj. step 0.2 to 4.8µV/ºC step
STV VDD track Gain_Temp. (STV)	Supply voltage and sensitivity temperature variation compensation circuit. Monitors the AGND voltage to calculate the magnitude of supply voltage variation; the pressure sensor sensitivity temperature drift is calculated for entry into G3 using the temperature sensor output voltage and preloaded compensation data (EEPROM data). The sensitivity temperature drift adjustment range can be changed by EEPROM data (ESTC[0]). Sensitivity temp. drift. adj. Adj. range -4000ppm/ ºC to +2500ppm/ ºC or -2500ppm/ ºC to +1000ppm/ ºC Adj. step 18ppm/ ºC step
LPF	Anti-aliasing filter to eliminate the fold-back noise generated in the sample-and-hold circuit (S/H) in the later stage. The cutoff frequency is fc=60kHz.
S/H & Level Shift & SCF	S/H doubles the LPF output and samples and holds it. The output reference voltage can be changed. Output reference voltage adj. Adj. range 0.02*VDD to 0.98*VD Adj. step 0.002*VDD /step SCF is a low-pass filter used for internal band limiting without using the external capacitors. The cutoff frequency (fc: 1kHz /500Hz /250Hz) of the filter can be set by EEPROM.
Buffer & SMF	Buffer to produce a band-limited output with low impedance. Provides 1.111x output. 146kΩ internal resistance and an external capacitor (C) make the LPF characteristics. Change the external capacitance value according to the desired signal band for detection using the following equation: fc=1/(2*π* 146kΩ*C) (Hz) SMF is a low-pass filter (fc=10kHz) used for eliminating the clock noise produced by the SCF in the previous stage. SMF is switched on or off in combination with the previous-stage SCF using the EEPROM data.

Block	Functions
Timing Logic	Generates timing sync signals for internal operation and sampling frequencies for sensor output signals. Sampling frequency (fs): 10kHz or 1kHz
Regulator	Constant voltage generator circuit to drive the sensor. The drive voltage can be selected from the EEPROM depending on the supply voltage being used. Drive voltage: 2.2V @VDD:3, 3.3V±5%, 4.0/2.2V @VDD:5V±5%
Pressure Detector1, 2	Two sets of pressure detection circuits. The pressure range can be individually selected depending on the EEPROM data for the pressure detector. • Pressure above a certain value is detected • Pressure below a certain value is detected The DET1 and DET2/PTH pins go high when the detected pressure exceeds the threshold (the polarity change by EEPROM is possible). The detection threshold can be set by the input of DET2/PTH pin (when only pressure detector 1 is used) or using the EEPROM data in the AK8998. The hysteresis voltage can be adjusted at 2 bits (4 steps), and it varies ratiometrically with respect to the supply voltage as well as the detection threshold. Note that the exact pressure determination cannot be achieved until the VOUT pin output is stabilized at the time of power up or due to the above setup and buffer circuit feedback resistor and external capacitor values.

Reference Section & Others

Block	Functions
V_Bandgap (VBG) V_Reference (VREF) I_Reference (IREF)	Generates the reference voltage or bias current required for each circuit. Adjust the VREF voltage so that it is equivalent to 1.0V. VREF voltage adj. Resolution 3bits Adj. step 1% / step IREF current should be adjusted to 1.0V voltage across 1MΩ external resistor tied to VOUT pin. IREF current adj. Resolution 4bits Adj. step 2.8% / step
Oscillator (OSC)	Oscillator to generate timing sync signals for internal operation and sampling frequencies for sensor output signals. Oscillation frequency is adjusted as the counter result reaches the expected value, the internal counter counts for the period of CSCLK is high (2msec typ.). For the detail, refer to the Functional Description **1) Adjustment Procedure Description (Example)**. OSC adj. Resolution 4bits Adj. step 5% / step
V_temp. (VTMP)	Temperature sensor for converting the ambient temperature to voltage. Adjust the temperature sensor output voltage (VTMP voltage) so that it is equivalent to VREF voltage at 25ºC. And it is also possible to select the external temperature sensor by EEPROM in consideration of the case where a pressure sensor and the AK8998 are separated physically. When the external temperature sensor is chosen, the constant current of 50μA is sinked from the EXTMP pin to VSS. VTMP voltage adj.(internal) Resolution 6bits Adj. step 0.2% / step VTMP voltage adj.(external) Resolution 9bits (Rough/Fine=3/6bits) Adj. step Rough 10% /step / Fine 0.2% /step
V_Common (VCOM)	Generates analog circuit reference voltage 1/2VDD. The internal power-up circuit causes it to start up within the settling time for stable analog operation (Start Up valid time). AGND pin can be validated by EEPROM (EAGND[0]=1h). It is effective to improve the noise characteristic (See recommended connection examples for components). In the case of EAGND[0]=0h, the AGND pin is Hi-Z.
Power ON Reset(POR)	Power Up circuit is for stable analog operation upon power-up. In order to make the power-on reset effective, be sure to power up the supply voltage from below 0.1*VDD.
Serial I/F	Serial interface for accessing EEPROM and control register (volatile memory). It accesses using the CSCLK pin and the VOUT pin.
EEPROM & Control Register	EEPROM and control register (volatile memory). Used to store compensation values and measurement modes and to set up the measurement modes for adjustment.

Pin Assignments and Functions

PAD	Name	I/O	C load max.	R load min.	Type	Comments
1	VSS				GND	
2	VO	I			Analog	Resistive load connection prohibited ESCF[1:0]: Open when 1,2,3h
3	VOUT	O	50pF	9.5kΩ	Analog	Resistance load is connectable with VDD or VSS
		I/O	100pF		CMOS	Pull-down resistor (100kΩ) included when SDI/O mode
		O	300pF		Analog	Adjustment mode
4	VDD				Power	
5	AGND	O			Analog	EAGND[0]: Resistive load connection prohibited when 1h EAGND[0]: Open when 0h
6,7,8	N.C.					Do not connect
9	CSCLK	I			CMOS	Pull-down resistor (100kΩ) included
10	DET1	O			CMOS	
11	DET2 /PTH	O			CMOS	
		I			Analog	EPTH1[0]=1h
12	N.C.					Do not connect
13	VN	I			Analog	
14	VS	O	30pF	1kΩ	Analog	EVD[1:0]=0h
		O	30pF	0.82kΩ	Analog	EVD[1:0]=1, 2, 3h
15	VP	I			Analog	
16	EXTMP	I			Analog	Do not connect when not in use

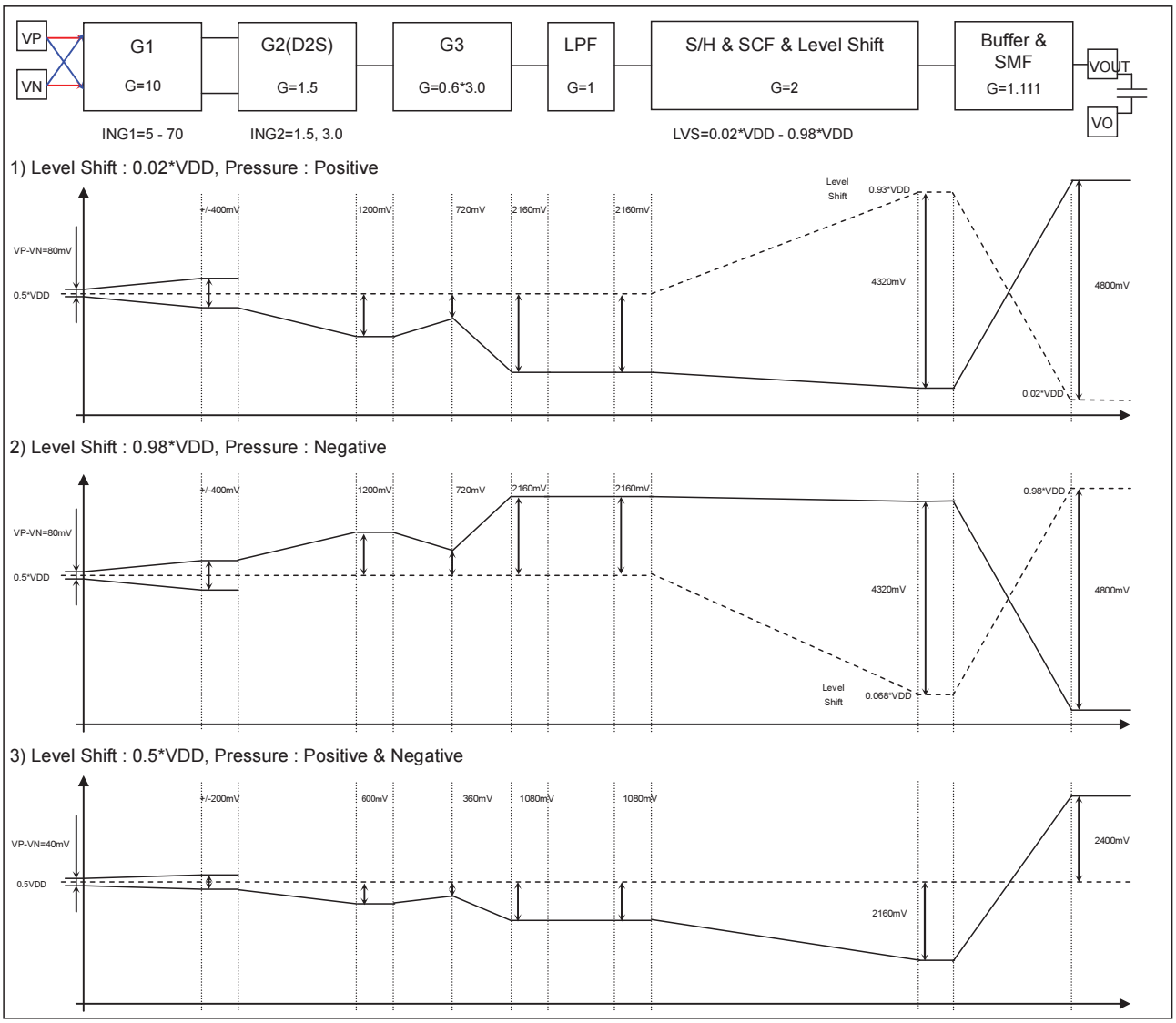
Pin Descriptions

PAD	Name	Functions	Pin conditions			
			Start up Note)	EAGND[0] : "H" / "L"	EINV1/2[0] : "H" / "L"	EINE1/2[0] : "H"
1	VSS	Negative voltage supply pin	-	-	-	-
2	VO	Capacitance connection pin for sensor signal band-limiting	Hi-Z	-	Normal operation	-
3	VOUT	Sensor signal / Data I/O / Calibration interface pin	Hi-Z	-	Normal operation	-
4	VDD	Positive supply voltage pin	-	-	-	-
5	AGND	Analog ground with external capacitance for stabilization	0.5*VDD /Hi-z	0.5*VDD /Hi-z	Normal operation	-
6,7,8	N.C.		-	-	-	-
9	CSCLK	Chip select / Serial clock pin	-	-	-	-
10	DET1	Output pin for pressure detection 1	VDD/VSS	-	VSS/VDD	VSS
11	DET2 /PTH	Output pin for pressure detection 2 / Pressure detection circuit 1 threshold external input	VDD/VSS	-	VSS/VDD	VSS
12	N.C.		-	-	-	-
13	VN	Sensor differential signal input pin (-)	-	-	-	-
14	VS	Constant voltage supply pin for sensor drive	Hi-z	-	Normal operation	-
15	VP	Sensor differential signal input pin (+)	-	-	-	-
16	EXTMP	External temperature sensor voltage input pin	Hi-z	-	-	-

Note) In the case of EAGND[0]="H"/"L" and EINV1/2[0]="H"/"L"

Level Diagram

VDD: 5V (ESTC[0]=1h)



Electrical Characteristics

1) Absolute Maximum Ratings

Item	Symbol	Min.	Max.	units	Comments
Supply voltage	VDD	-0.3	6.5	V	
Input voltage	VDIN	VSS-0.3	VDD+0.3	V	
Input current	IIN	-10	10	mA	
Output current	IOUT	-10	10	mA	
Storage temp.	TST	-55	125	°C	EEPROM retention characteristics ≤85°C

Note) Operation at or beyond these limits may result in permanent damage to the device.

2) Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	units	Comments
Operating temp.	Ta	-20		85	°C	
Supply voltage	VDD1	2.85	3.0	3.15	V	EVD[1:0]=3h
	VDD2	3.135	3.3	3.465	V	EVD[1:0]=2h
	VDD3	4.75	5.0	5.25	V	EVD[1:0]=0h, 1h

3) Supply Voltage Current (See Functional Description)

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Min.	Typ.	Max.	units	Comments
Supply voltage current 1	IDD1		6000	7100	μA	VDD=5V,VS=4V,Fs=10kHz Note1)
Supply voltage current 2	IDD2		4000	5000	μA	VDD=3V,VS=2.2V,Fs=10kHz Note1)
Supply voltage current 3	IDD3		1300	2000	μA	VDD=5V,VS=4V,Fs=1kHz Note1)
Supply voltage current 4	IDD4		1100	1700	μA	VDD=3V,VS=2.2V,Fs=1kHz Note1)
Supply voltage current 5 (SCF & SMF circuit)	IDD5		100	150	μA	VDD=5V
Supply voltage current 6 (Pressure detection circuit 1/2)	IDD6		150	250	μA	VDD=5V
Supply voltage current 7 (External temperature sensor drive circuit)	IDD7		130	200	μA	VDD=5V

Note) At the time of measurement, the VS pin connects 1kΩ load, the VOUT pin is connects no load, and the VP and VN pins supply 0.5*VS.
VREF and VTMP voltage, IREF current and OSC frequency are complete with adjustment.
Note1) SCF&SMFcircuit:Off, External temperature sensor drive circuit:Off

4) EEPROM Characteristics

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Min.	Typ.	Max.	units
EEPROM endurance	Etime	1000			times
EEPROM data retention time	Ehold	10			years

5) Digital DC Characteristics

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	units
High level input voltage	VIH	1		0.7*VDD	-	-	V
Low level input voltage	VIL	1		-	-	0.3*VDD	V
High level input current	IIH	1		+10	-	+200	μA
Low level input current 1	IIL1	2		-10	-	+10	μA
Low level input current 2	IIL2	3		-50	-	+50	μA
High level output voltage	VOH	4	IOH=-200μA	0.9*VDD	-	-	V
Low level output voltage	VOL	4	IOL=+200μA	-	-	0.1*VDD	V

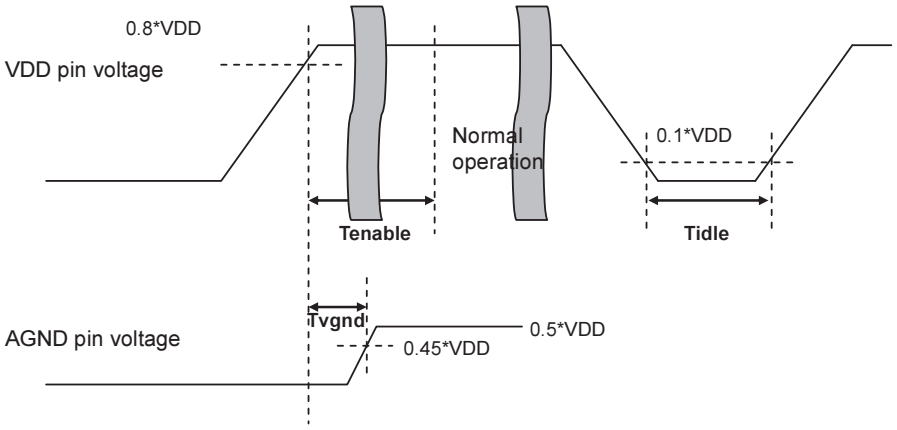
1 CSCLK(integrated 100kΩ pull-down resistor),
VOUT(integrated 100kΩ pull-down resistor when SDI/O mode)
2 CSCLK(integrated 100kΩ pull-down resistor),
3 VOUT(integrated 100kΩ pull-down resistor when SDI/O mode)
4 VOUT(when SDI/O mode), DET1, DET2/PTH

6) Power On/Off time and Analog circuit settling time for stable operation Note)

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Min.	Typ.	Max.	units	Comments
Power On/Off time	Tidle	10			msec	VDD pin voltage <0.1*VDD
Settling time for stable analog operation	Tenable			700	μsec	
AGND output rise time	Tvgnd			330	μsec	EAGND[0]=1h, AGND pin external capacitance: 10nF

Note) Design reference value; no production test performed.



7) Digital AC Characteristics

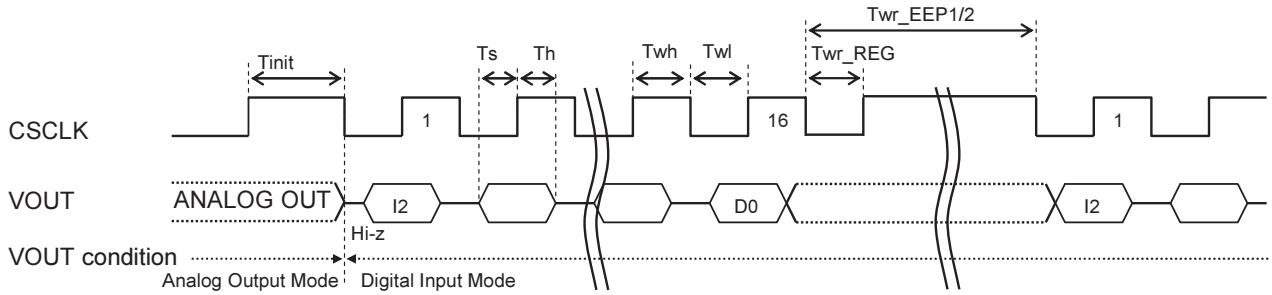
VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Min.	Typ.	Max.	units
Write time (EEPROM address write)	Twr_EEP1	5		100	msec
Write time (EEPROM batch write)	Twr_EEP1	10		100	msec
Write time (Register)	Twr_REG	10			µsec
Digital Mode Transition time	Tinit	1.0			msec
Analog Mode Transition time	Tdigout	0.5			msec
Data setup time	Ts	100			nsec
Data hold time	Th	100			nsec
CSCLK high time	Twh	0.5		100	µsec
CSCLK low time	Twl	0.5		100	µsec
CSCLK→DO delay time Note1)	Td			200	nsec
CSCLK rising time Note 2)	Tr			10	nsec
CSCLK falling time Note 2)	Tf			10	nsec

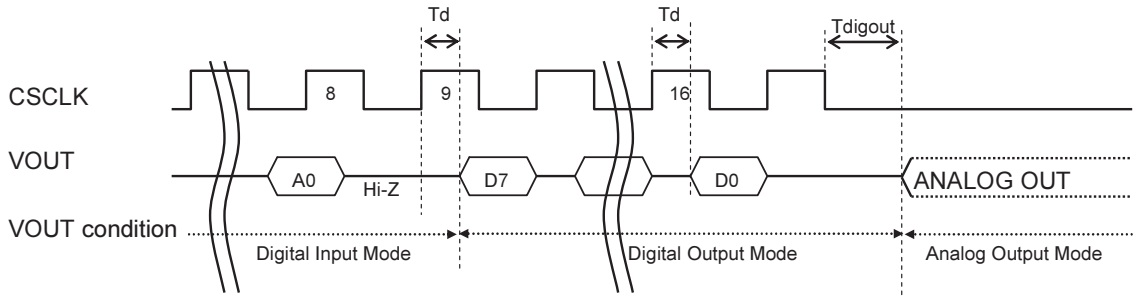
Note1) SDO load capacitance=100pF

Note2) Design reference value; no production test performed.

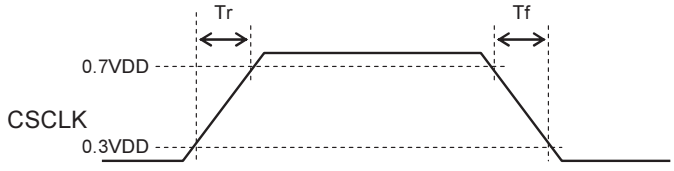
[Serial I/F timing (Write)]



[Serial I/F timing (Read)]



[CSCLK Raising/Falling timing]

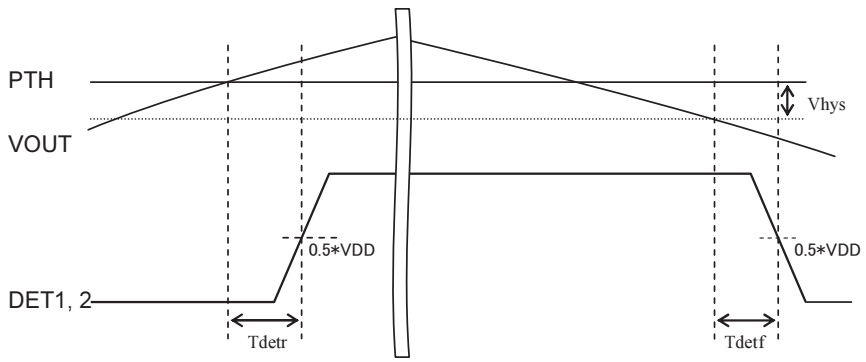


8) Pressure Detector 1 & 2

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Pressure detection threshold External input range	Vdete	EINE1[0]=0h EINE2[0]=1h EPTH1[0]=1h	0.1*VDD		0.9*VDD	V	
Pressure detection threshold Internal set value	Vdet	EPT1, 2[4:0]=00h	0.500 *VDD -0.05	0.500 *VDD	0.500 *VDD +0.05	V	
Pressure detection threshold Internal set value Adjust. width	Vdet+	Max: EPT1, 2[4:0]=10h		0.900 *VDD		V	
	Vdet-	Min: EPT1, 2[4:0]=0Fh		0.125 *VDD		V	
Adjust. step	Vdstp			0.025 *VDD		V	
Hysteresis voltage Adjust. width	Vhys5+	Max: VDD=5V±5% EHYS1, 2[1:0]=01h	0.060 *VDD -0.055	0.060 *VDD	0.060 *VDD +0.055	V	
	Vhys5-	Min: VDD=5V±5% EHYS1, 2[1:0]=10h	0.030 *VDD -0.03	0.030 *VDD	0.030 *VDD +0.03	V	
	Vhys3+	Max: VDD=3, 3.3V±5% EHYS1, 2[1:0]=01h	0.060 *VDD -0.035	0.060 *VDD	0.060 *VDD +0.035	V	
	Vhys3-	Min: VDD=3, 3.3V±5% EHYS1, 2[1:0]=10h	0.030 *VDD -0.02	0.030 *VDD	0.030 *VDD +0.02	V	
Adjust. step	Vhysst			0.010 *VDD		V	
Pressure detection time	Tdetr	ESCF[1:0]=0h			150	µsec	Note)
Pressure non-detection time	Tdetf	ESCF[1:0]=0h			150	µsec	Note)

Note) Design reference value; no production test performed.



9) Analog Characteristics
9-1) Reference Section

9-1-1) Reference Section Characteristics

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
VREF voltage	Vr0	Unadjusted AM[3:0]=1h VOUT out	0.97	1.0	1.04	V	@25 ºC
VREF adj. width	Vr+	With respect to Vr0 Max EVR[2:0]=3h		+30		mV	
	Vr-	With respect to Vr0 Min EVR[2:0]=4h		-40		mV	
VREF adj. step	Vrstp			10		mV	
VS voltage	VS4	After VREF adj. VS pin out Load resistance 1kΩ	3.88	4.00	4.12	V	
	VS2	After VREF adj. VS pin out Load resistance 0.82kΩ	2.134	2.20	2.266	V	
IREF current	Ir0	Unadjusted AM[3:0]=2h VOUT out	0.8	1.00	1.2	μA	@25 ºC
IREF adj. width	Ir+	With respect to Ir0 Max EIR[3:0]=7h		0.24		μA	
	Ir-	With respect to Ir0 Min EIR[3:0]=8h		-0.17		μA	
IREF adj. step	Irstp			0.028		μA	
OSC freq.	Fr0	Unadjusted AM[3:0]=3h VOUT out	0.750	1.000	1.250	MHz	@25 ºC
OSC adj. width	Fr+	With respect to Fr0 Max EFR[3:0]=7h		384		kHz	
	Fr-	With respect to Fr0 Min EFR[3:0]=Bh		-251		kHz	
OSC adj. step	Frstp			50		kHz	
VTMP voltage	Vt0	Unadjusted ETMP[0]=1h AM[3:0]=4h VOUT out	0.938	1.0	1.064	V	@25 ºC
VTMP adj. width (Rough)	Vtr+	With respect to Vt0 ETMP[0]=0h Max ETM[8:6]=6h		+170		mV	
	Vtr-	With respect to Vt0 ETMP[0]=0h Min ETM[8:6]=2h		-170		mV	
Rough adj. step	Vtrstp	ETMP[0]=0h		85		mV	
VTMP adj. width (fine)	Vtf+	With respect to Vt0 ETMP[0]=1h Max ETM[5:0]=20h		+64		mV	
	Vtf-	With respect to Vt0 ETMP[0]=1h Min ETM[5:0]=1Fh		-62		mV	
Fine adj. step	Vtfstp	ETMP[0]=1h		2.0		mV	
VTMP temp variation	Vt	ETMP[0]=1h		4.6		mV/°C	Note)

Note) Design reference value; no production test performed.

9-1-2) Reference Section (packaged version only) Characteristics

VDD=5V±5%, Ta= 25ºC, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
VREF voltage	Vr0P		0.99	1.0	1.01	V	After adj.
VS voltage	VS4P	Load resistance 1kΩ	3.88	4.00	4.12	V	After adj.
	VS2P	Load resistance 0.82kΩ	2.134	2.20	2.266	V	After adj.
IREF current	Ir0P		0.9	1.0	1.1	μA	After adj.
OSC freq.	Fr0P		0.9	1.0	1.1	MHz	After adj.
VTMP voltage	Vt0P	ETMP[0]=1h	0.988	1.0	1.012	V	After adj.

Note) AK8998 is shipped with adjustment at VDD=5V&VS=4V (EVD[1:0]=0h) and internal temperature sensor use (ETMP[0]=1h). If VDD=5V&VS=2.2V (EVD[1:0]=1h), VDD=3.3V&VS=2.2V(EVD[1:0]=2h), VDD=3V&VS=2.2V(EVD[1:0]=3h) and external temperature sensor use (ETMP[0]=0h) are the actual operating condition, readjustment is required. Even if VDD=5V&VS=4V (EVD[1:0]=0h) and internal temperature sensor use (ETMP[0]=1h) are the operating condition, readjustment is recommended.

9-2) Gain Amplifier etc.

Unless otherwise specified, the following requirements apply.

- Reference Section is complete with adjustment.
- For supply voltage of 5V (3V), sensor drive voltage of 4V (2.2V), the level diagram includes G1 gain of 10x, G2 gain of 1.5x, G3 gain of 1.8x, Total gain of 60x, Level shift 0.02*VDD and the output voltage 4800mV (2400mV) is set as 100% based on a differential input of 80mV (40mV).

9-2-1) Overall Characteristics

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Std. gain	Gtyp	VP/VN→VOUT		60		times	
Input common voltage	Vicom		0.45VS	0.5*VS	0.55VS	V	
Output common voltage	Vcom0	VP/VN→VOUT VP=VN=0.5*VS		0.5*VDD		V	
Max. output range	Vmax+	VP/VN→VOUT VP-VN=VSS or VDD	0.98 *VDD			V	
	Vmax-				0.02 *VDD	V	
Noise	Nout1	VP/VN→VOUT VP=VN=Open External feedback capacitance 2.2nF			260	μVrms	@1Hz - 100kHz Note)
	Nout2	VP/VN→VOUT VP=VN=Open ESCF[1:0]=1h			300	μVrms	@1Hz - 100kHz Note)

Note) Value for total gain of 180x (G1 gain: 30x, G2 gain: 1.5x, G3 gain: 1.8x, S/H gain: 2x, Buffer gain: 1.111x). Design reference value; no production test performed.

9-2-2) G1/2 Gain Adjustment Circuit

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode							
Unadjusted G1/2 output voltage	Vg1	VP-VN=80mV VDD=5V±5%	1150	1200	1250	mV	
	Vg2	VP-VN=40mV VDD=3, 3.3±5%	550	600	650	mV	
G1 adjustment range	G1sc+	EIG[3:0]=Ch		5		times	
	G1sc-	EIG[3:0]=0h		70		times	
Adj. Step	G1stp			2,3,5,10		times	
G2 adj.	G2sc1+	EIG[4]=0h,ESTC[0]=1h		3		times	
	G2sc1-	EIG[4]=1h,ESTC[0]=1h		1.5		times	
	G2sc2+	EIG[4]=0h,ESTC[0]=0h		2.352		times	
	G2sc2-	EIG[4]=1h,ESTC[0]=0h		1.176		times	

9-2-3) Offset Voltage Adjustment Circuit

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode							
Unadjusted output voltage	Vo01	VDD=3, 3.3, 5V±5%	0.5*VDD -0.10	0.5*VDD	0.5*VDD +0.10	V	
Offset rough adj. DAC adj. range	Ocr5+	EOCR[3]=0h EOCR[2:0]=7h VDD=5V±5%		+11200		mV	
	Ocr5-	EOCR[3]=1h EOCR[2:0]=7h VDD=5V±5%		-11200		mV	
	Ocr3+	EOCR[3]=0h EOCR[2:0]=7h VDD=3, 3.3±5%		+5600		mV	
	Ocr3-	EOCR[3]=1h EOCR[2:0]=7h VDD=3, 3.3±5%		-5600		mV	
Adj. step	Ocr5stp	VDD=5V±5%		1600		mV	
	Ocr3stp	VDD=3, 3.3±5%		800		mV	
Offset fine adj. DAC adj. range	Ocf5+	EOCF[7]=0h EOCF[6:0]=3Fh VDD=5V±5%		+1016		mV	
	Ocf5-	EOCF[7]=1h EOCF[6:0]=3Fh VDD=5V±5%		-1016		mV	
	Ocf3+	EOCF[7]=0h EOCF[6:0]=3Fh VDD=3, 3.3±5%		+508		mV	
	Ocf3-	EOCF[7]=1h EOCF[6:0]=3Fh VDD=3, 3.3±5%		-508		mV	
Adj. step	Ocf5stp	VDD=5V±5%		8		mV	
	Ocf3stp	VDD=3, 3.3±5%		4		mV	

9-2-4) Span Voltage Adjustment Circuit

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage adjustment							
Unadjusted Span voltage	Vs01	VP-VN=80mV VDD=5V±5%	2010	2160	2310	mV	
	Vs02	VP-VN=40mV VDD=3, 3.3±5%	1005	1080	1155	mV	
Span adj. range	Sc+	ESC[7:0]=00h		100/100		times	
	Sc-	ESC[7:0]=FFh		100/163.75		times	
Adj. Step	Sc stp	N= 0 − +255		100/(100+0.25*N)		times	

9-2-5) Offset Temperature Drift & Sensitivity Temperature Drift Adjustment Circuit

9-2-5-1) Offset Temperature Drift Adjustment Circuit Note)

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
1st order coeff. Adj. range	DO5+	EOT[8]=0h EOT[7:0]=FFh VDD=5V±5%		+36.8		mV/°C	
	DO5-	EOT[8]=1h EOT [7:0]=FFh VDD=5V±5%		-36.8		mV/°C	
	DO3+	EOT[8]=0h EOT[7:0]=FFh VDD=3, 3.3±5%		+22.08		mV/°C	
	DO3-	EOT[8]=1h EOT[7:0]=FFh VDD=3, 3.3±5%		-22.08		mV/°C	
Adj. step	DO5 stp	VDD=5V±5%		0.144		mV/°C	
	DO3 stp	VDD=3, 3.3±5%		0.087		mV/°C	

Note) Design reference value; no production test performed.

9-2-5-2) Sensitivity Temperature Drift Adjustment Circuit Note)

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
1st order coeff. Adj. range	DS1+	ESTC[0]=1h,EST[8]=0h EST[7:0]=8Bh		+2500		ppm/°C	
	DS1-	ESTC[0]=1h,EST[8]=1h EST[7:0]=DEh		-4000		ppm/°C	
	DS2+	ESTC[0]=0h,EST[8]=0h EST[7:0]=38h		+1000		ppm/°C	
	DS2-	ESTC[0]=0h,EST[8]=1h EST[7:0]=8Bh		-2500		ppm/°C	
Adj. step	DS stp			18		ppm/°C	

Note) Design reference value; no production test performed.

9-2-6) Supply Voltage & Temperature Sensitivity Variation Adjustment Circuit (STV) Note)

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
Sensitivity variation characteristics 1 to supply voltage	SV1	SV circuit initial operation, ESTC[0]=1h			5.0	%	
	SV2	SV circuit 2nd operation, ESTC[0]=1h		±0.4		%	Based on SV1
Sensitivity variation characteristics 1 to operating temp.	ST1	ST circuit initial operation, ESTC[0]=1h			5.0	%	
	ST2	ST circuit 2nd operation, ESTC[0]=1h		±0.4		%	Based on ST1
Sensitivity variation characteristics 2 to supply voltage	SV3	SV circuit initial operation, ESTC[0]=0h			5.0	%	
	SV4	SV circuit 2nd operation, ESTC[0]=0h		±0.2		%	Based on SV3
Sensitivity variation characteristics 2 to operating temp.	ST3	ST circuit initial operation, ESTC[0]=0h			5.0	%	
	ST4	ST circuit 2nd operation, ESTC[0]=0h		±0.2		%	Based on ST3

9-2-7) LPF, S/H & Buffer

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
LPF freq. response	Fc1		40	60	80	kHz	
S/H&Buffer gain	SHG		1.935	2.222	2.523	times	
S/H&Buffer out pre-adj. error	SHerr		-65		65	mV	
BUF gain adj. width	Bufg		1.000	1.111	1.222	times	
VOUT output voltage range	Vbuf+	Load resistance 9.5kΩ (with VDD or VSS)	0.98 *VDD			V	
	Vbuf-				0.02 *VDD	V	
BUF feedback resistor value	Rbuf		102	146	190	kΩ	

9-2-8) Level shift

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
Output reference voltage adj. width (Level shift)	Vlv+	Max ELV[8]=1h ELV[7:0]=FFh		1.00 *VDD		V	Note)
	Vlv-	Min ELV[8]=0h ELV[7:0]=FFh		0.00 *VDD		V	Note)
Adj. step	Vlstp			0.002 *VDD		V	

Note) It is limited to 0.98*VDD from 0.02*VDD by the VOUT output range.

9-2-9) SCF & SMF

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

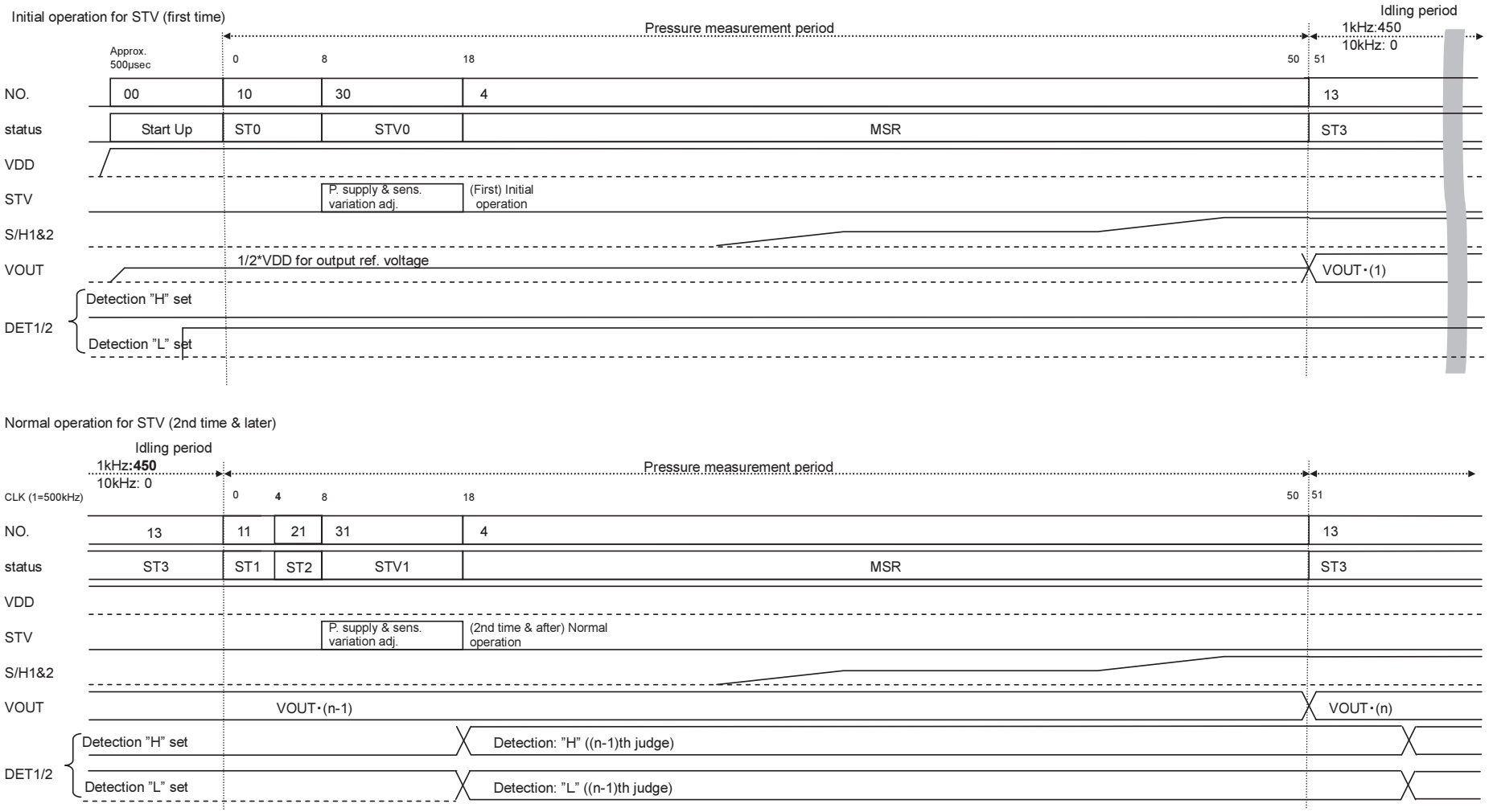
Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Measurement in test mode after offset voltage and span voltage adjustment							
SCF&SMF freq. response	Fc1	ESCF[1:0]=1h 10Hz referenced -3dB	0.8	1.0	1.2	kHz	
	Fc2	ESCF[1:0]=2h 10Hz referenced -3dB	400	500	600	Hz	
	Fc3	ESCF[1:0]=3h 10Hz referenced -3dB	200	250	300	Hz	
SCF&SMF gain	SCFG1	ESCF[1:0]=1h	1.000	1.111	1.222	times	

9-2-10) External temperature sensor drive circuit

VDD=3, 3.3, 5V±5%, Ta=-20 to 85ºC, register default, unless otherwise noted

Item	Symbol	Conditions	Min.	Typ.	Max.	units	Comments
Temperature sensor driving current	Iconst	After IREF adj.	40	50	60	µA	
Input voltage range	Extpv4	VS=4V After VREF adj.	3220	3400	3580	mV	
	Extpv2	VS=2.2V After VREF adj.	1474	1600	1726	mV	

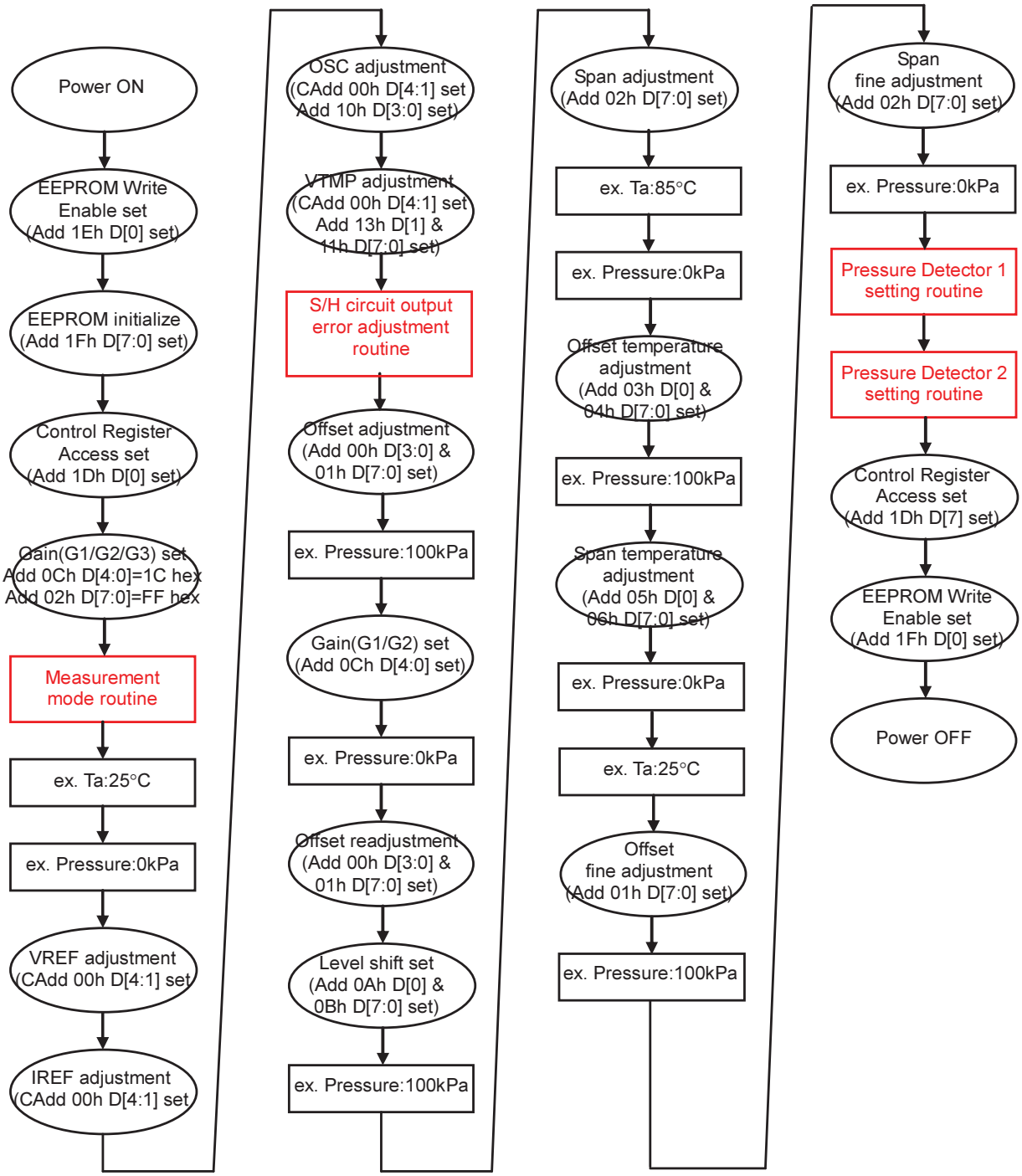
Operation Sequence



Description of Operation Timing Status (pressure detection circuit effective)

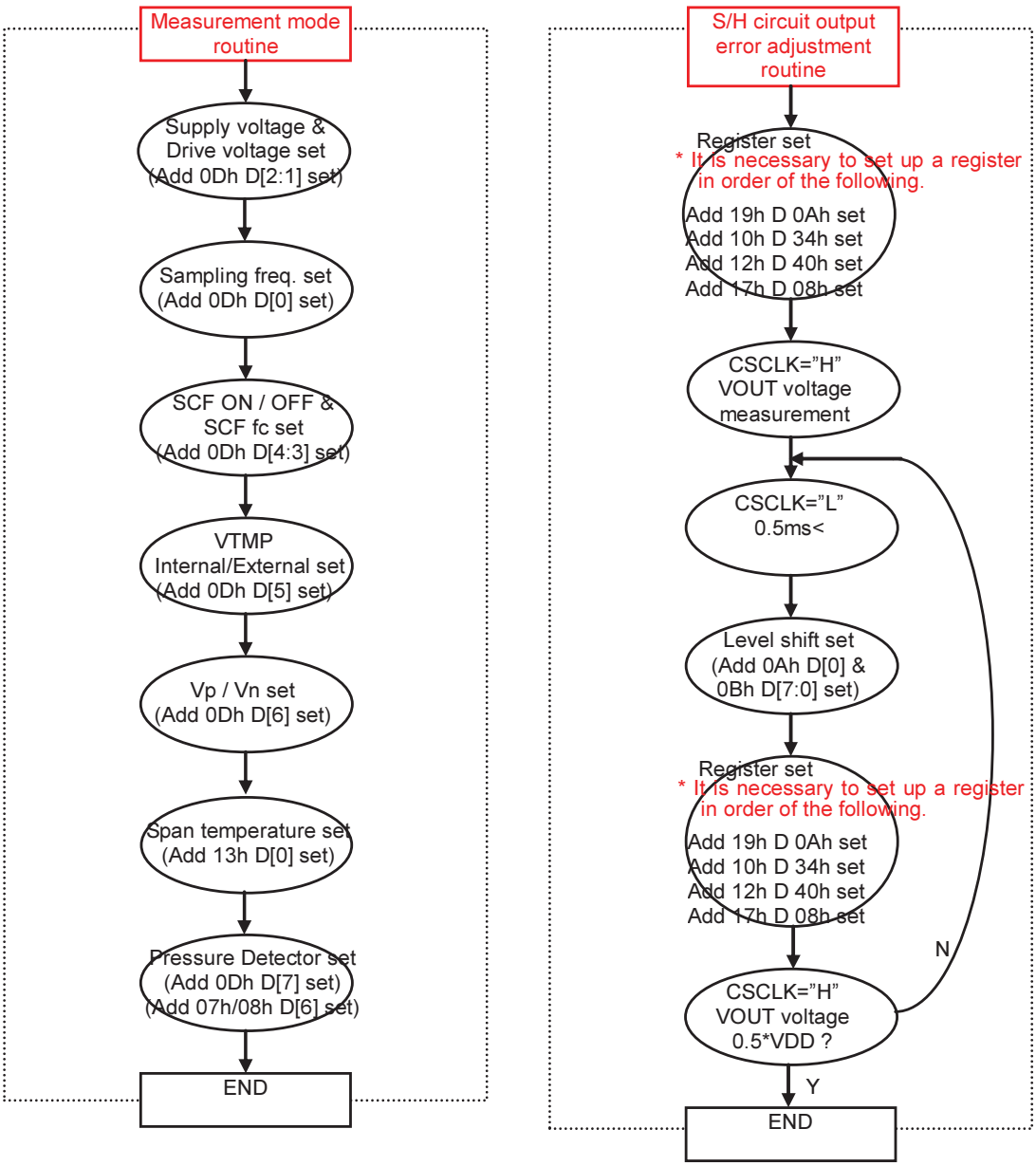
No.	State	CLK	Operations
00	Start Up		It is the time until analog circuits operate stably. Analog reference circuits as VREF, IREF, etc. start up and adjusted output reference voltage is output from the VOUT pin.
10	ST0		Clock count start Analog circuits startup
30	STV0	CLK=8	STV initial operation
4	MSR	CLK=18	The result of pressure correction is output from VOUT pin.
13	ST3	CLK=51	Idling With fs=10kHz, no idling and in continuous operation. Idling period 1kHz 450 CLK 10kHz 0 CLK
11	ST1	CLK1=51	Pressure detection circuit 1 operation and analog circuit startup
21	ST2	CLK=4+CLK1	Pressure detection circuit 2 operation
31	STV1	CLK=8+CLK1	STV normal operation Pressure detection DET1/2 output (the (n-1)th pressure determination)
:	:	:	:

Adjustment Sequence



note1) EEPROM Address is indicated by “Add”,
Control Register Address is indicated by “CAdd”.

note2) Please refer the digital part flow chart
for EEPROM / Control Register writing and reading.


Measurement mode routine
Supply voltage & Drive voltage set (Add 0Dh D[2:1] set)
Sampling freq. set (Add 0Dh D[0] set)
SCF ON / OFF & SCF fc set (Add 0Dh D[4:3] set)
VTMP Internal/External set (Add 0Dh D[5] set)
Vp / Vn set (Add 0Dh D[6] set)
Span temperature set (Add 13h D[0] set)
Pressure Detector set (Add 0Dh D[7] set) (Add 07h/08h D[6] set)
END
S/H circuit output error adjustment routine
Register set
* It is necessary to set up a register in order of the following.
Add 19h D 0Ah set
Add 10h D 34h set
Add 12h D 40h set
Add 17h D 08h set
CSCLK="H" VOUT voltage measurement
CSCLK="L" 0.5ms<
Level shift set (Add 0Ah D[0] & 0Bh D[7:0] set)
Register set
* It is necessary to set up a register in order of the following.
Add 19h D 0Ah set
Add 10h D 34h set
Add 12h D 40h set
Add 17h D 08h set
CSCLK="H" VOUT voltage 0.5*VDD ?
N
Y
END