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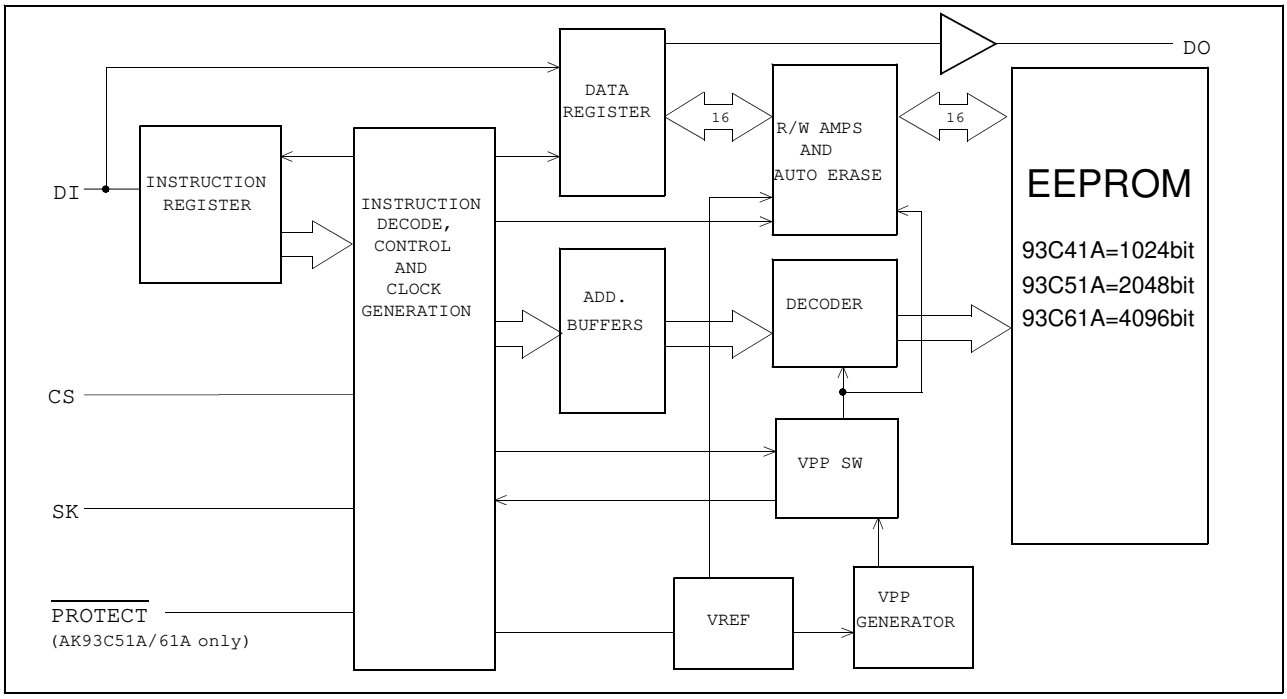
AK93C41A / 51A / 61A

0.9V operation 1K / 2K / 4Kbit Serial CMOS EEPROM

Preliminary

Features

- ADVANCED CMOS EEPROM TECHNOLOGY
- LOW VCC OPERATION ··· Vcc = 0.9V ~ 3.6V
- AK93C41A · · · 1024 bits, 64×16 organization
  AK93C51A · · · 2048 bits, 128×16 organization
  AK93C61A · · · 4096 bits, 256×16 organization
- SERIAL INTERFACE
  - Interfaces with popular microcontrollers and standard microprocessors
- LOW POWER CONSUMPTION
  - 2μA Max. Standby (VCC=3.6V)
- Automatic address increment (READ)
- Automatic write cycle time-out with auto-ERASE
- $\overline{\text{Busy}}$/Ready status signal
- Software controlled write protection
- Hardware write protect for lower block (AK93C51A/61A only)
- IDEAL FOR LOW DENSITY DATA STORAGE
  - Low cost, space saving, 8-pin package (TSSOP)



Block Diagram

General Description

The AK93C41A/51A/61A is a 1024/2048/4096-bit serial CMOS EEPROM divided into 64/128/256 registers of 16 bits each. The AK93C41A/51A/61A has 4 instructions such as READ, WRITE, EWEN and EWDS. Those instructions control the AK93C41A/51A/61A.
The AK93C41A/51A/61A can operate full function under wide operating voltage range from 0.9V to 3.6V. The charge up circuit is integrated for high voltage generation that is used for write operation.
A serial interface of AK93C41A/51A/61A, consisting of chip select (CS), serial clock (SK), data-in (DI) and data-out (DO), can easily be controlled by popular microcontrollers or standard microprocessors. AK93C41A/51A/61A takes in the write data from data input pin (DI) to a register synchronously with rising edge of input pulse of serial clock pin (SK). And at read operation, AK93C41A/51A/61A takes out the read data from a register to data output pin (DO) synchronously with rising edge of SK.
The DO pin is usually in high impedance state. The DO pin outputs "L" or "H" in case of data output or Busy/Ready signal output.

•Software and Hardware controlled write protection
When Vcc is applied to the part, the part automatically powers up in the ERASE/WRITE Disable state. In the ERASE/WRITE disable state, execution of WRITE instruction is disabled. Before WRITE instruction is executed, EWEN instruction must be executed. The ERASE/WRITE enable state continues until EWDS instruction is executed or Vcc is removed from the part.
Execution of a read instruction is independent of both EWEN and EWDS instructions.
The PROTECT pin is available only on the AK93C51A/61A.
AK93C51A・・・When PROTECT pin is tied to GND, PROGRAM operations onto the lower 1Kbit ($00~$3F) will not be executed. When PROTECT pin is tied to VCC, normal operation is enabled. There is an internal pull-down on the PROTECT pin.
AK93C61A・・・When PROTECT pin is tied to GND, PROGRAM operations onto the all erea will not be executed. When PROTECT pin is tied to VCC, normal operation is enabled. There is an internal pull-up on the PROTECT pin.

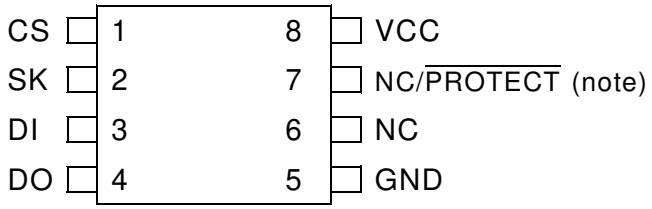
•Busy/Ready status signal
After a write instruction, the DO output serves as a Busy/Ready status indicator. After the falling edge of the CS initiates the self-timed programming cycle, the DO indicates the Busy/Ready status of the chip if the CS is brought high after a minimum of 250ns (Tcs).
DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.
The Busy/Ready status indicator is only valid when CS is active (high). When CS is low, the DO output goes into a high impedance state.
The Busy/Ready signal outputs until a start bit (Logic"1") of the next instruction is given to the part.

■ Type of Products

Model	Memory size	Temp.Range	Vcc	Package
AK93C41AV	1Kbits	-10°C ~ 70°C	0.9V ~ 3.6V	8pin Plastic TSSOP
AK93C51AV	2Kbits	-10°C ~ 70°C	0.9V ~ 3.6V	8pin Plastic TSSOP
AK93C61AV	4Kbits	-10°C ~ 70°C	0.9V ~ 3.6V	8pin Plastic TSSOP

Pin arrangement

AK93C41AV/51AV/61AV



8pinTSSOP

(note) AK93C41A・・NC, AK93C51A/61A・・PROTECT

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PROTECT (AK93C51A/61A only)	Memory Protect AK93C51A PROTECT=L or NC : Protect enable PROTECT=H : Protect disable AK93C61A PROTECT=L or NC : Protect enable PROTECT=H or NC: Protect disable
Vcc	Power Supply
NC	Not Connected

Functional Description

The AK93C41A/51A/61A has 4 instructions such as READ, WRITE, EWEN and EWDS. A valid instruction consists of a Start Bit (Logic"1"), the appropriate Op Code and the desired memory Address location.
The CS pin must be brought low for a minimum of 250ns (Tcs) between each instruction when the instruction is continuously executed.

Instruction	Start Bit	Op Code	Address	Data	Comments
READ	1	10	A5-A0	D15-D0	Reads data stored in memory, at specified address.
WRITE	1	01	A5-A0	D15-D0	Writes register.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
EWDS	1	00	00XXXX		Disables all programming instructions.
WRAL	1	00	01XXXX	D15-D0	Writes all registers.

X: Don't care

table1. Instruction Set for the AK93C41A

Instruction	Start Bit	Op Code	Address	Data	Comments
READ	1	10	X A6-A0	D15-D0	Reads data stored in memory, at specified address.
WRITE	1	01	X A6-A0	D15-D0	Writes register.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
EWDS	1	00	00XXXXXX		Disables all programming instructions.
WRAL	1	00	01XXXXXX	D15-D0	Writes all registers.

X: Don't care

table2. Instruction Set for the AK93C51A

Instruction	Start Bit	Op Code	Address	Data	Comments
READ	1	10	A7-A0	D15-D0	Reads data stored in memory, at specified address.
WRITE	1	01	A7-A0	D15-D0	Writes register.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
EWDS	1	00	00XXXXXX		Disables all programming instructions.
WRAL	1	00	01XXXXXX	D15-D0	Writes all registers.

X: Don't care

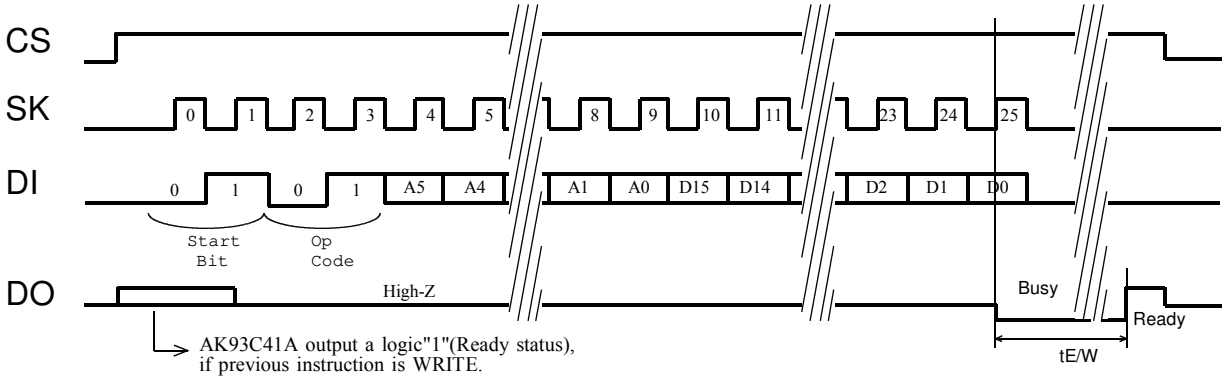
table3. Instruction Set for the AK93C61A

(Note) • The WRAL instruction are used for factory function test only.
User can't use the WRAL instruction.
• The AK93C41A/51A/61A perceives the start bit in the logic"1" and also "01".

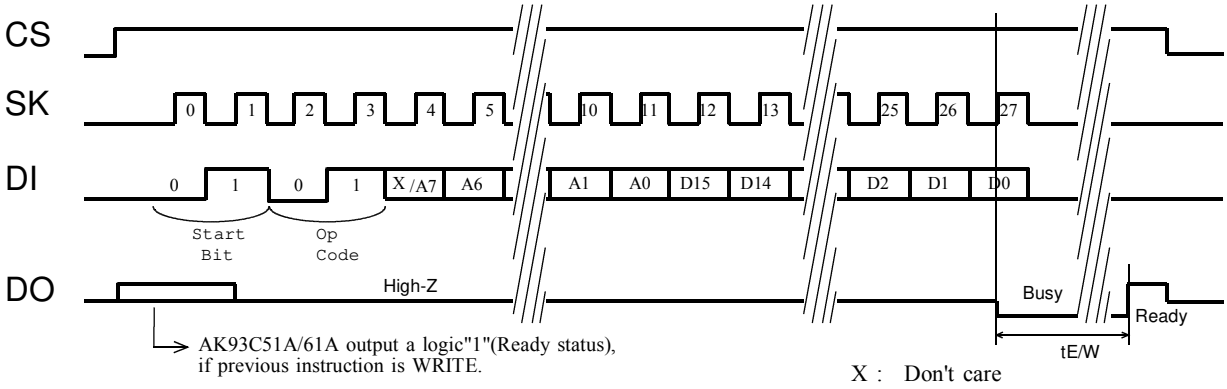
Write

The write instruction is followed by 16 bits of data to be written into the specified address.
The self-timed programming cycle is initiated on the rising edge of the SK clock as the last data bit (D0) is clocked in. The DO indicates the Busy/Ready status of the chip after the self-timed programming cycle is initiated.

The Busy/Ready status indicator is only valid when CS is active (high). When CS is low, the DO output goes into a high impedance state. The Busy/Ready signal outputs until a start bit (Logic"1") of the next instruction is given to the part.
DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.



WRITE (AK93C41A)



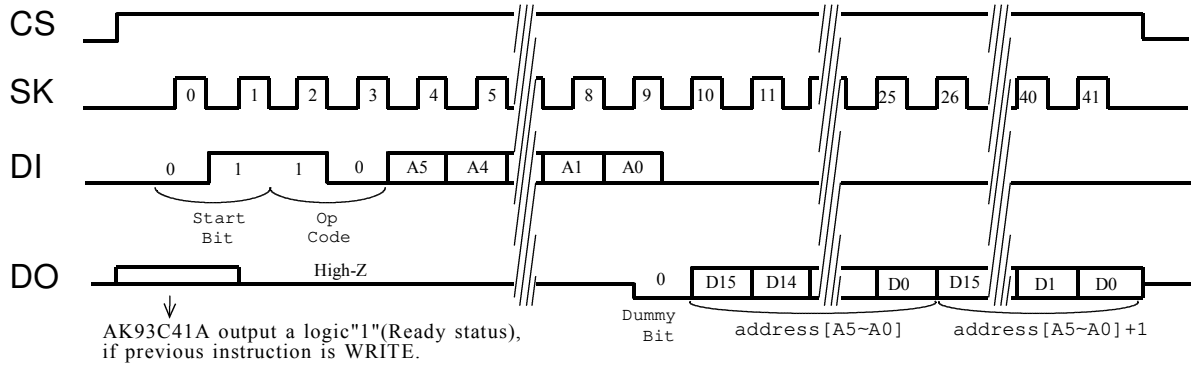
X : Don't care

*Address bit A7 becomes a "don't care" for AK93C51A

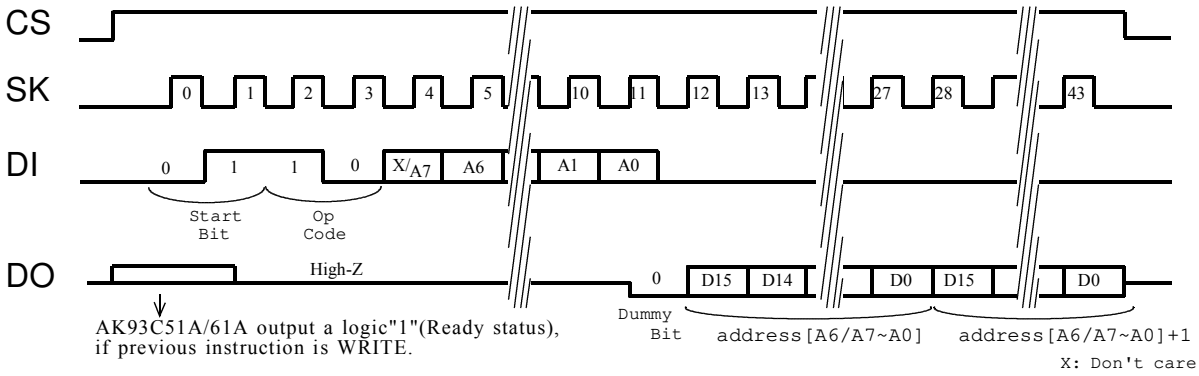
WRITE (AK93C51A/61A)

Read

The read instruction is the only instruction which outputs serial data on the DO pin.
Following the Start bit, first Op code and address are decoded, then the data from the selected memory location is available at the DO pin. A dummy bit (logical "0") precedes the 16-bit data from the selected memory location. The output data changes are synchronized with the rising edges of the serial clock (SK).
The data in the next address can be read sequentially by continuing to provide clock. The address automatically cycles to the next higher address after the 16bit data shifted out.
AK93C41A・・When the highest address is reached ($3F), the address counter rolls over to address $00 allowing the read cycle to be continued indefinitely.
AK93C51A・・When the highest address is reached ($7F), the address counter rolls over to address $00 allowing the read cycle to be continued indefinitely.
AK93C61A・・When the highest address is reached ($FF), the address counter rolls over to address $00 allowing the read cycle to be continued indefinitely.



READ (AK93C41A)

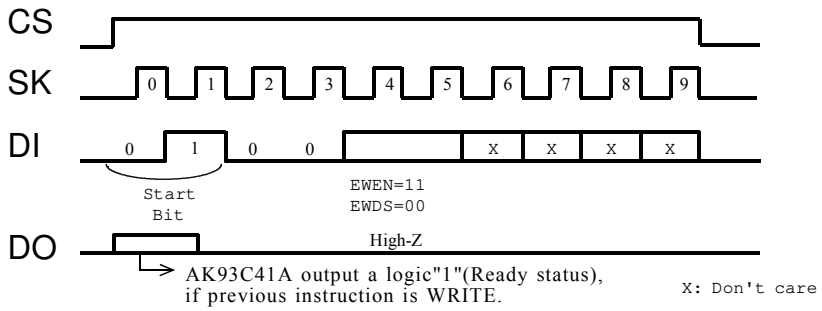


*Address bit A7 becomes a "don't care" for AK93C51A.

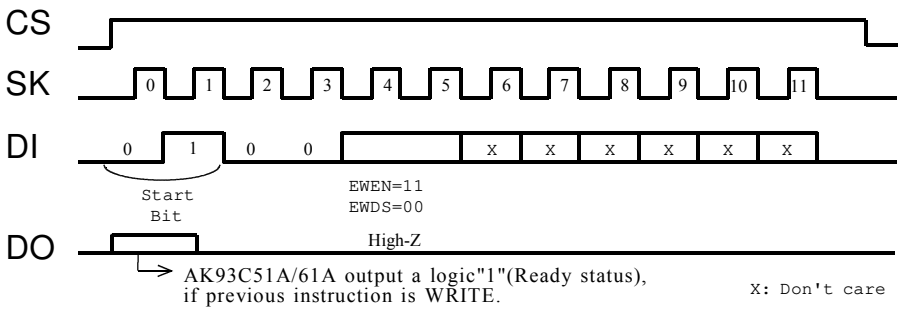
READ (AK93C51A/61A)

EWEN / EWDS

When Vcc is applied to the part, the part automatically powers up in the ERASE/WRITE Disable state. In the ERASE/WRITE disable state, execution of WRITE instruction is disable. Before WRITE instruction is executed, EWEN instruction must be executed. The ERASE/WRITE enable state continues until EWDS instruction is executed or Vcc is removed from the part.
Execution of a read instruction is independent of both EWEN and EWDS instructions.



EWEN/EWDS (AK93C41A)



EWEN/EWDS (AK93C51A/61A)

Precautions for use

The treatment and assembly of AK93C41A/51A/61A require careful attention to electrical over-stress, just like general CMOS devices.
When the part is assembled, human bodies, work benches and measurement equipments should be connected to ground. On the boards, decoupling capacitors (0.1uF) between VCC and GND should be located as near as possible to the part.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	-0.6	+7.0	V
All Input Voltages with Respect to Ground	VIO	-0.6	VCC+0.6	V
Ambient storage temperature	Tst	-65	+150	°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	0.9	3.6	V
Ambient Operating Temperature	Ta	-20	+70	°C

Electrical Characteristics

(1) D.C. ELECTRICAL CHARACTERISTICS

(Ta= -20°C to +70°C, VCC=+0.9V to +3.6V unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
Current Dissipation	ICC1	VCC=3.6V, tSKP=4us, *1		2.5	mA
(WRITE)	ICC2	VCC=0.9V,tSKP=10us,*1		1.0	mA
Current Dissipation	ICC3	VCC=3.6V, tSKP=4us, *1		200	uA
(READ,EWEN,EWDS)	ICC4	VCC=0.9V,tSKP=10us,*1		50	uA
Current Dissipation (Standby)	ICC_{SB}	VCC=3.6V *2		2	uA
Input High Voltage	VIH1	1.8V≤VCC≤3.6V	0.8×VCC	VCC+0.5	V
	VIH2	0.9V≤VCC<1.8V	0.9×VCC	VCC+0.5	V
Input Low Voltage	VIL1	1.8V≤VCC≤3.6V	-0.1	0.2×VCC	V
	VIL2	0.9V≤VCC<1.8V	-0.1	0.1×VCC	V
Output High Voltage	VOH	IOH=-10uA	VCC-0.2		V
Output Low Voltage	VOL	IOL=10uA		0.2	V
Input Leakage (CS,SK,DI pin)	ILI	VCC=3.6V VIN=VCC/GND		±1	uA
Output Leakage (DO pin)	ILO	VCC=3.6V, CS=GND VOUT=VCC/GND		±1	uA

*1 : VIN=VIH/VIL, DO, $\overline{\text{PROTECT}}$=Open

*2 : VIN=VCC/GND, CS=GND, DO, $\overline{\text{PROTECT}}$=Open

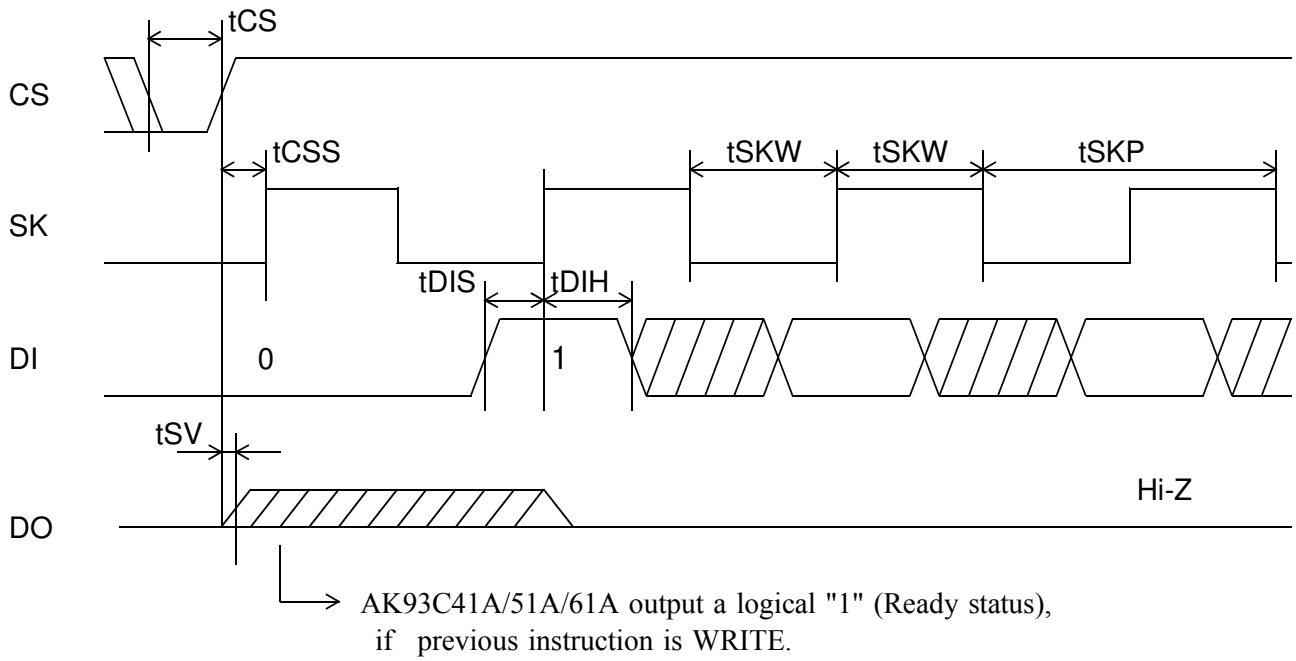
(2) A.C. ELECTRICAL CHARACTERISTICS

(Ta= -20°C to +70°C, VCC=+0.9V to +3.6V unless otherwise specified)

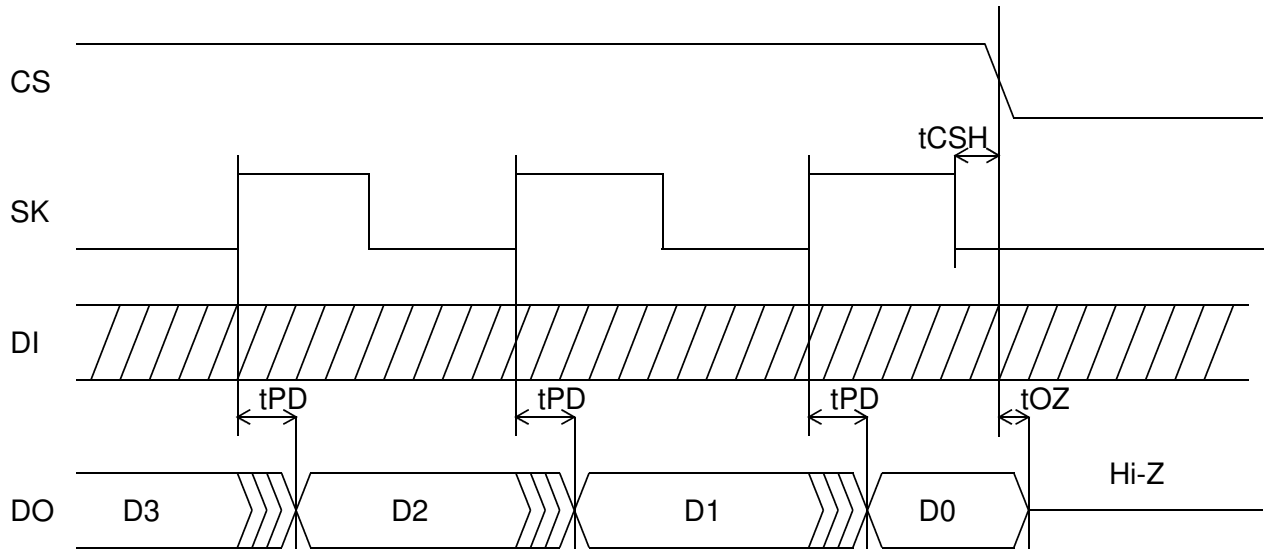
Parameter	Symbol	Condition	Min.	Max.	Unit
SK Cycle Time	tSKP1	1.8V≤VCC≤ 3.6V	4		us
	tSKP2	0.9V≤VCC<1.8V	10		us
SK Pulse Width	tSKW1	1.8V≤VCC≤ 3.6V	2		ns
	tSKW2	0.9V≤VCC<1.8V	5		us
CS Setup Time	tCSS1	1.8V≤VCC≤ 3.6V	100		ns
	tCSS2	0.9V≤VCC<1.8V	1000		ns
CS Hold Time	tCSH1	1.8V≤VCC≤ 3.6V	0		ns
	tCSH2	0.9V≤VCC<1.8V	1000		ns
Data Setup Time	tDIS1	1.8V≤VCC≤ 3.6V	200		ns
	tDIS2	0.9V≤VCC<1.8V	1000		ns
Data Hold Time	tDIH1	1.8V≤VCC≤ 3.6V	200		ns
	tDIH2	0.9V≤VCC<1.8V	1000		ns
Output delay	tPD1	1.8V≤VCC≤ 3.6V, *3		1500	ns
	tPD2	0.9V≤VCC<1.8V, *3		5000	ns
Selftimed Programming Time	tE/W			15	ms
Min CS Low Time	tCS1	1.8V≤VCC≤ 3.6V	250		ns
	tCS2	0.9V≤VCC<1.8V	4000		ns
CS to Status Valid1	tSV1	1.8V≤VCC≤ 3.6V, *3		500	ns
	tSV2	0.9V≤VCC<1.8V, *3		5000	ns
CS to Status Valid2	tSVV1	1.8V≤VCC≤ 3.6V, *3		1000	ns
	tSVV2	0.9V≤VCC<1.8V, *3		5000	ns
CS to Output High-Z	tOZ1	1.8V≤VCC≤ 3.6V		250	ns
	tOZ2	0.9V≤VCC<1.8V		5000	ns

*3 : CL=100pF

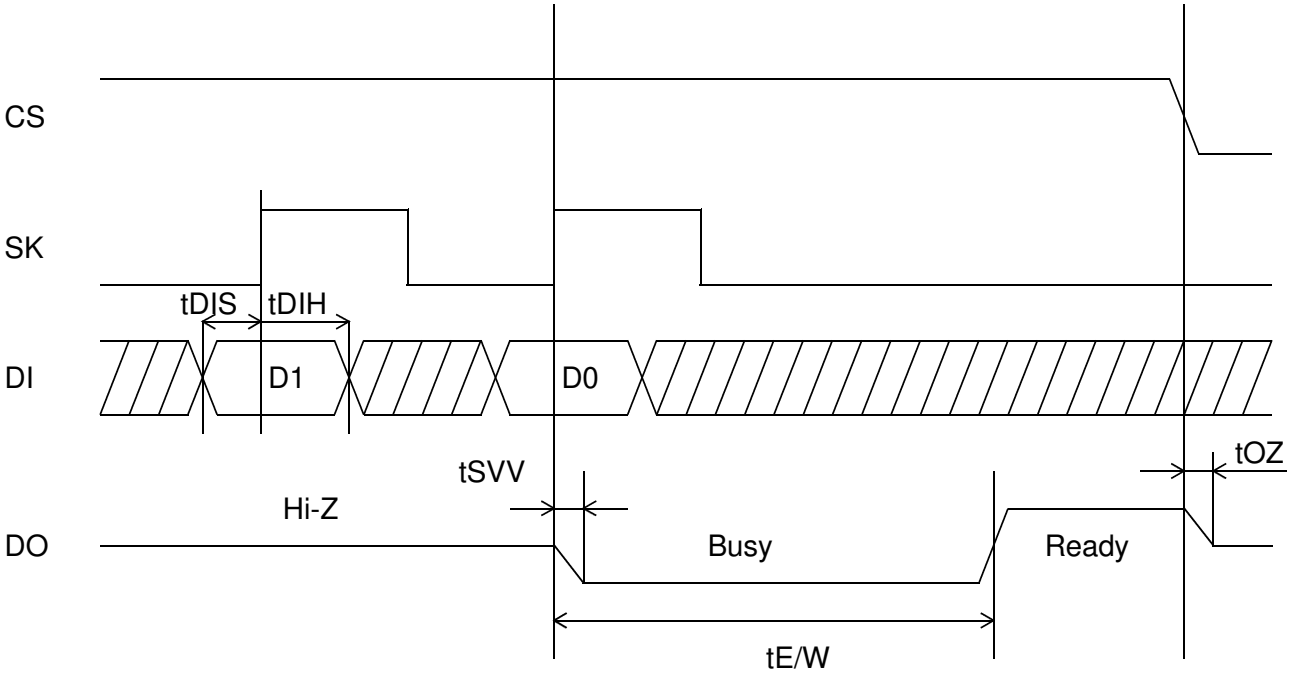
Synchronous Data Timing



The Start of Instruction



The End of Instruction



$\overline{\text{Busy}}$/Ready Signal Output

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