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AK9750
IR Sensor IC with I²C I/F

1. General Description

The AK9750 is an ultra-low power and compact infrared-ray (IR) sensor module. It is composed of four quantum IR sensors and an integrated circuit (IC) for characteristic compensation. The four IR sensors' offset and gain variations are calibrated at shipment. An integral analog-to-digital converter provides 16-bits data outputs. Additional integrated features include a field of view limiter and an optical filter. The AK9750 is suitable for applications including stationary human detection.

2. Features

- ☐ Quantum-type IR Sensor with Four IR Elements
- ☐ 16-bits Digital Outputs to I²C bus
- ☐ Integrated temperature sensor: -10 ~ 60ºC output on I²C bus
- ☐ Interrupt Function

  INT pin can be used as a read-trigger or an interrupt request of signal level monitoring.
- ☐ Built in Switch Mode (Standalone Mode)

  By writing the threshold into the internal EEPROM at the customer's production testing, the presence detection state will be output to the INT pin. In this mode, neither the control by I²C bus nor Host MCU is necessary.
- ☐ Low Voltage Operation: VDD: 1.71 ~ 3.63V
  DVDD: 1.65V ~ VDD
- ☐ Low Current Consumption: Max. 100 µA (@Continuous Mode "0")
  Max. 1µA (@ Power down Mode)
- ☐ Small and Thin Package: 10-pin SON
  Built in a field of view limiter and an optical filter

3. Table of Contents

4. Block Diagram and Functions

4.1. Block Diagram

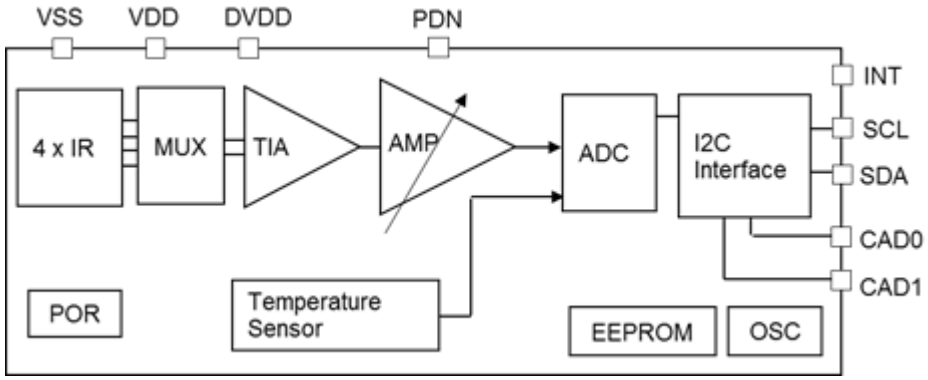


Figure 4.1 AK9750 Block Diagram

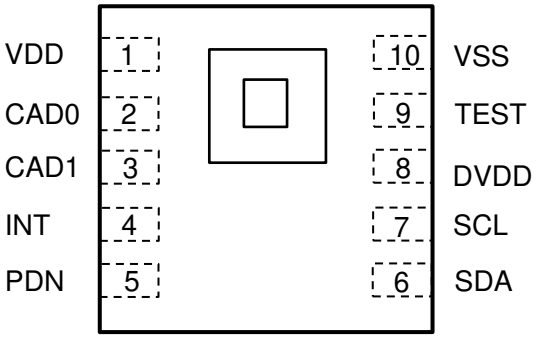
4.2. Block Functions

Table 4.1. Block Functions

Block	Function
4 x IR	Four IR Sensor
MUX	Matrix Switch
TIA	Photocurrents of IR Sensor are converted to voltage signals.
AMP	Programmable gain amplifier to adjust the outputs.
Temperature Sensor	Built-in Temperature Sensor
ADC	The amplifier output and the built-in temperature sensor output are converted to digital signals.
I^2C Interface	Interface to external host controller. SCL and SDA pins are provided for I^2C Interface. The interface operates up to 400kHz rate and down to 1.65V low voltage condition.
EEPROM	EEPROM
OSC	Internal Oscillator.
POR	Power On Reset circuit.

5. Pin Configurations and Functions

5.1. Pin Configurations



Top View

Figure 5.1 Pin Configurations

5.2. Pin Functions

Table 5.1 Pin Functions

Pin No.	Name	I/O	Function
1	VDD	-	Analog Power Supply Pin
2	CAD0	I	Slave address 0. CAD0 pin should be connected to VDD or VSS. Set up an address so that two or more same address of devices do not exist on the same bus.
3	CAD1	I	Slave address 1. CAD0 pin should be connected to VDD or VSS. Set up an address so that two or more same address of devices do not exist on the same bus.
4	INT	O	Functions are selected by INTEN register. INT pin goes “Active”, when the ADC output are ready to be read or the differential signal of two IR sensor(one observes the upper (or left)side and another observes lower (or right) side) exceeds threshold levels. It is composed of an open drain output (N-type transistor). INT pin is connected to DVDD voltage through a pull-up resister, with other open drain or open collector output of the other devices to form “wired-OR”.
5	PDN	I	Power down pin. When PDN pin= “H”, AK9750 can operate. PDN pin is not connected to VDD (or VSS) through a pull-up (or pull-down) resister. This pin must be connected to “H” or “L” voltage level.
6	SDA	I/O	I^2C Data Output Pin. SDA is a bidirectional pin which is used to transmit data into and out of the device. It is composed of a signal input and an open drain output (N-type transistor). SDA is connected to DVDD voltage through a pull-up resistor, and to open drain outputs or open collector outputs of the other devices as “wired-OR”
7	SCL	I	I^2C Clock Input pin. Signal processing is executed at the rising and falling edge of SCL clock. Observe rise time tR and fall time tF. SCL is connected to DVDD voltage through a pull-up resistor.
8	DVDD	-	Digital I/F Power Supply pin.
9	TEST	I	Test pin. TEST pin should be connected to VSS.
10	VSS	-	Ground pin.

6. IR Sensors Configuration / Observable Area

6.1. IR Sensor's Configurations

The four IR sensors which AK9750 includes are arranged as shown in Figure 6.1 IR1(2, 3, 4) is defined as the measurement data of IR sensor 1(2, 3, 4).
The upper (left, lower, right) side is defined as the side on which IR sensor 1(2, 3, 4) is arranged.

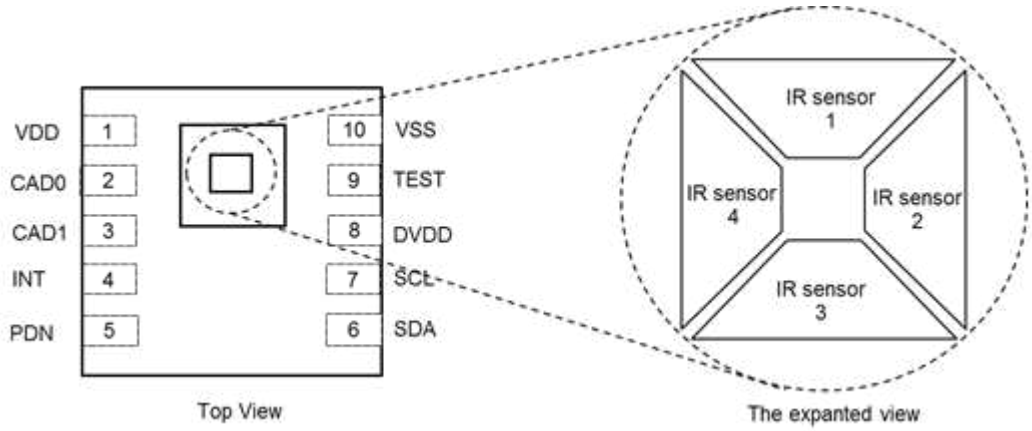


Figure 6.1. IR Sensor's Configurations

6.2. IR Sensor's Observable Area

The each IR sensor's Observable Area is limited by the field of view limiter as shown Figure 6.2.
Area1 (2, 3, 4) is defined as the area which IR Sensor 1(2, 3, 4) can observe. Each sensor detects the diagonal area.

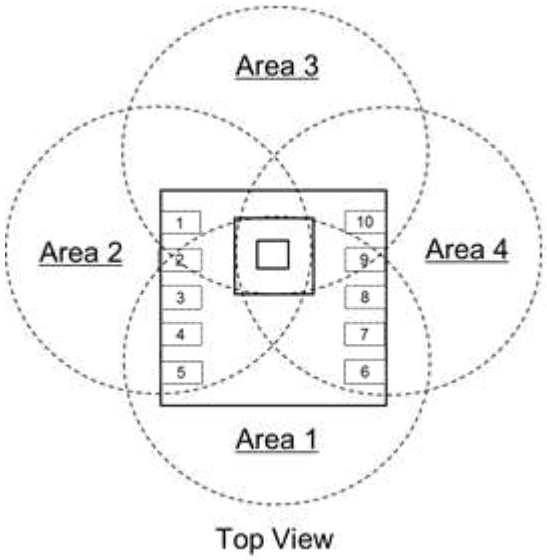


Figure 6.2. IR Sensor's Observable Area

7. Absolute Maximum Ratings

(VSS= 0V)

Parameter		Symbol	Min.	Max.	Unit
Power Supply	VDD pin, DVDD pin	V+	-0.6	4.6	V
Input Current	All pins	Iin	-10	10	mA
Input Voltage (* 1)	CAD0 pin, CAD1 pin, INT pin, PDN pin, TEST pin, SCL pin, SDA pin	Vin	-0.6	4.6	V
Storage Temperature		Tst	-30	85	ºC

Note:
* 1. Vin should be always lower than (V+) + (0.6V).

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

8. Recommended Operating Conditions

(VSS= 0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supply	During normal operation	VDD	1.71	3.3	3.63	V
(* 2)	During the EEPROM write	EVDD	3.00	3.3	3.63	V
Digital Power Supply		DVDD	1.65	3.3	VDD	V
Operating Temperature		Ta	-30	25	85	ºC

Notes:
* 2. VDD should always be higher than DVDD.
* 3. Keep environment no dew condensation.

9. Power Supply Conditions

(Unless otherwise specified, VDD=1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85ºC)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Power Supply Rise Time (* 4, * 5)	Time until VDD, DVDD, and PDN are set to the operating voltage from 0.2V.	VDD pin, DVDD pin	PSUP			50	ms
Power-on Reset Time (* 4, * 5)	Time until AK9750 becomes Power down Mode after PSUP.	VDD pin	PORT			3000	µs
Shutdown Voltage (* 5, * 6)	Shutdown Voltage for POR re-starting.	VDD pin, DVDD pin	SDV			0.2	V
Power Supply Interval Time (* 4, * 5, * 6)	Voltage retention time below SDV1 for POR re-starting.	VDD pin, DVDD pin	PSINT	3000			µs

Notes:

* 4. Reference data only, not tested.
* 5. Power-on Reset circuit detects the rising edge of VDD, resets the internal circuit, and initializes the registers. After Power-on reset, Stand-by Mode is selected.
* 6. The condition that POR surely works at the power-up the power-up again after power supply goes down. Unless this condition is satisfied, the reset may not be correctly expected.

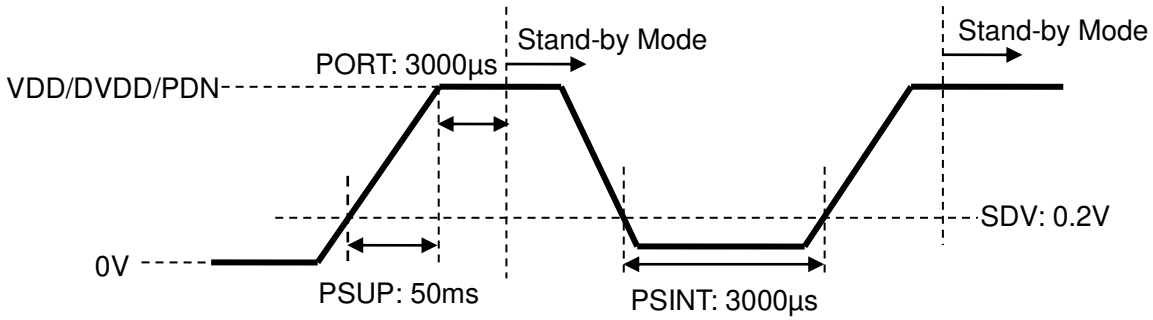


Figure 9.1. Power Supply Conditions

10. Electrical Characteristics

10.1. Analog Characteristics

(Unless otherwise specified, VDD= 1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85ºC)

Parameter		Symbol	Min.	Typ.	Max.	Unit
IR output resolution				16		bit
IR offset code	All output currents of four IR sensors are Zero. ・Reference data only, not tested.		-36	0	36	Code
IR output code	・Ttgt= 50ºC, Ta= 23ºC ±3ºC ・2's complement		2940H	2A1CH	2AF8H	Code
Relative sensitivity variations of four IR sensors	Ta= 23ºC ±3ºC		-3.5		3.5	%
Temperature output resolution				10		bit
Temperature sensor range	・Linear to internal temperature (excludes noise) ・2's complement		-10		60	ºC
			B980H		4380H	Code
Temperature sensor accuracy (* 7)	Ta= 35ºC		-5.5		5.5	ºC
Field of View	The combined range observed by Upper/Lower (Left/Right) ・Reference data only, not tested.	FOV	±48	±55	±66	deg(º)
Averaged current consumption	Power Down Mode PDN= "L"	SIDD			1	μA
	Stand-by Mode PDN= "H", EMODE [2:0] = "000"	IDD0			10	μA
	Continuous Mode 0 PDN= "H", EMODE [2:0] = "100"	IDD1			100	μA
	Continuous Mode 1 PDN= "H", EMODE [2:0] = "101"	IDD2			60	μA
	Continuous Mode 2 PDN= "H", EMODE [2:0] = "110"	IDD3			38	μA
	Continuous Mode 3 PDN= "H", EMODE [2:0] = "111"	IDD4			25	μA
Digital filter cut-off frequency	Eight levels can be selected by setting register. Typ. $Fc=8.8/2^n$ (n=0 ~ 5)	Fc	0.2		9.7	Hz

Note:

* 7. Temperature sensor's output is as the following

Ta= 35ºC, (Temperature sensor's output)= (VDD-1.71) × 1.45+33.5±4.0 [ºC]

10.2. Digital Characteristics

10.2.1. EEPROM

(Unless otherwise specified, VDD= 1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85ºC)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Retention Time	@Ta= 85ºC	Ehold	10			years
Endurance			1000			times

Note:

* 8. VDD (EVDD) should be greater than 3.0V, when writing EEPROM.

10.2.2. DC Characteristics

(Unless otherwise specified, VDD= 1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85°C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
High Level Input Voltage 1		PDN pin	VIH1	80%DVDD			V
Low Level Input Voltage 1		PDN pin	VIL1			20%DVDD	V
High Level Input Voltage 2		SCL pin, SDA pin	VIH2	70%DVDD			V
Low Level Input Voltage 2		SCL pin, SDA pin	VIL2	-0.5		30%DVDD	V
High Level Input Voltage 3		CAD1 pin, CAD0 pin	VIH3	80%VDD			V
Low Level Input Voltage 3		CAD1 pin, CAD0 pin	VIL3			20%VDD	V
High Level Input Voltage 4	DVDD Monitor Function	DVDD pin	VIH4	80%VDD			V
Low Level Input Voltage 4		DVDD pin	VIL4			0.2	V
Hysteresis Voltage (* 9)	DVDD ≥ 2V	SCL pin, SDA pin	VHS	5%DVDD			V
	DVDD < 2V			10%DVDD			V
Low Level Output Voltage 1	IOL= 3mA DVDD ≥ 2V	SDA pin, INT pin	VOL1			0.4	V
Low Level Output Voltage 2	IOL= 3mA DVDD < 2V	SDA pin, INT pin	VOL2			20%DVDD	V

Note:

* 9. Reference data only, not tested.

10.2.3. AC Characteristics (1): Standard Mode (100 kHz)

(Unless otherwise specified, VDD= 1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCL frequency		fSCL			100	kHz
SDA bus idle time to the next command input		fBUF	4.7			µs
Start condition Hold time		tHD:STA	4.0			µs
Clock Low period		tLOW	4.7			µs
Clock High period		tHIGH	4.0			µs
Start condition set-up time		tSU:STA	4.7			µs
Data hold time		tHD:DAT	0			µs
Data set-up time		tSU:DAT	250			ns
Rise time SDA, SCL (* 10)	SDA pin, SCL pin	tR			1.0	µs
Fall time SDA, SCL (* 10)	SDA pin, SCL pin	tF			0.3	µs
Stop condition set-up time		tSU:STO	4.0			µs
EEPROM write time		tWR	10			ms

Note:

* 10. Reference data only, not tested.

10.2.4. AC Characteristics (2): Fast Mode (400 kHz)

(Unless otherwise specified, VDD= 1.71 ~ 3.63V, DVDD= 1.65V ~ VDD, Ta= -30 ~ 85°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCL frequency		fSCL			400	kHz
SDA bus idle time to the next command input		fBUF	1.3			µs
Start condition Hold time		tHD:STA	0.6			µs
Clock Low period		tLOW	1.3			µs
Clock High period		tHIGH	0.6			µs
Start condition set-up time		tSU:STA	0.6			µs
Data hold time		tHD:DAT	0			µs
Data set-up time		tSU:DAT	100			ns
Rise time SDA, SCL (* 11)	SDA pin, SCL pin	tR			0.3	µs
Fall time SDA, SCL (* 11)	SDA pin, SCL pin	tF			0.3	µs
Stop condition set-up time		tSU:STO	0.6			µs
EEPROM write time		tWR	10			ms

Note:

* 11. Reference data only, not tested.

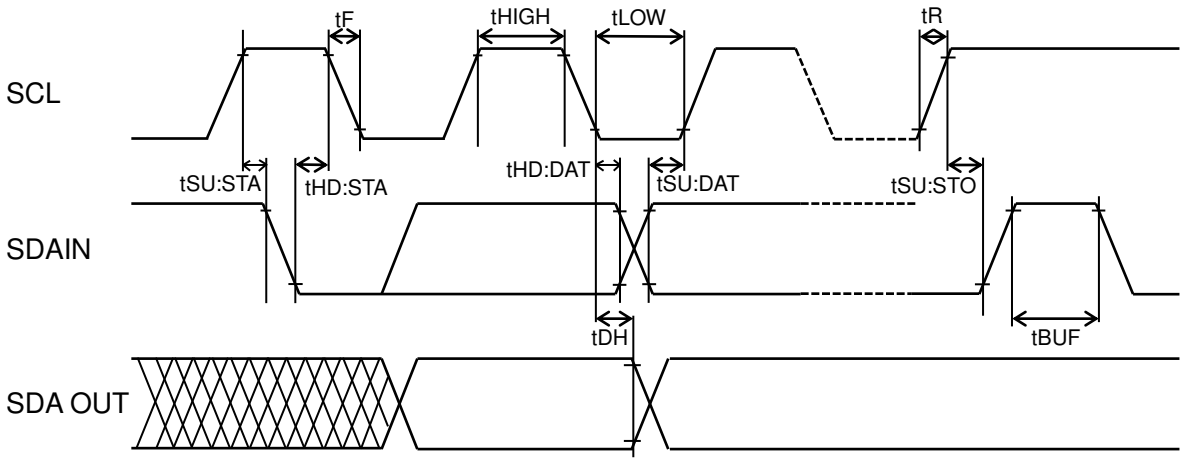


Figure 10.1. Bus Timing

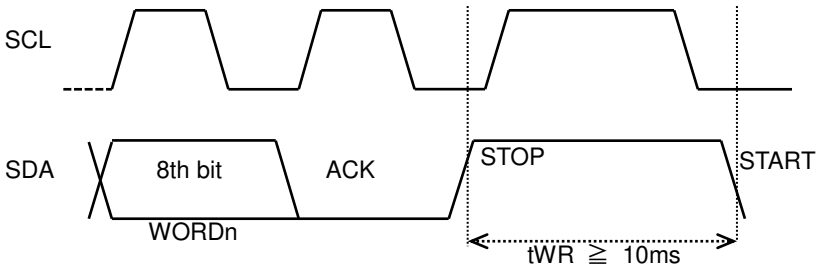


Figure 10.2. EEPROM write time

11. Functional Descriptions

11.1 Power Supply States

When VDD, DVDD and PDN turn on from the state of VDD= DVDD= OFF(0V), Power-on Reset(POR) automatically operates, all registers will be initialized, and the AK9750 will be set to Stand-by Mode. Although all states of the Following table can exist, the state 2 is prohibited.

Table 11.1. Power Supply States and Functions

State	VDD pin	DVDD pin	PDN pin	I^2C	INI pin	Analog Circuit	IDD
1	OFF(0V)	OFF(0V)	"L"	Disable	Unfixed	Power Down	Unknown
2	OFF(0V)	1.65 ~ 3.63V	"H" or "L"	Disable	Unfixed	Power Down	Unknown
3	1.71 ~ 3.63V	OFF(0V)	"L"	Disable	Unfixed	Power Down	Unknown
4	1.71 ~ 3.63V	OFF(0V)	"H"	Disable	Unfixed	Power Down	Unknown
5	1.71 ~ 3.63V	1.65V ~ VDD	"L"	Disable	"H"	Power Down	< 1μA
6	1.71 ~ 3.63V	1.65V ~ VDD	"H"	Enable	"H"	POR circuit only operates	< 10μA

11.2 Reset functions

When VDD turns ON, set up DVDD lower than VDD(DVDD ≤ VDD).
Power-on Reset (POR) operates unit VDD reaches the operating voltage (1.4V Typ.). After POR, all registers are set to initial values, and Stand-by Mode is selected.

AK9750 has five reset functions.

(1) Power-on Reset(POR)
Power-on Reset circuit resets AK9750 by detecting VDD and DVDD rising.
When VDD and DVDD turns ON with PDN pin= "L", POR does not operate, because POR circuit is also in PD state.

(2) Hardware Reset
AK9750 is reset by PDN pin= "L"

(3) Software Reset
AK9750 is reset by setting SRST bit.

(4) DVDD Monitor Reset
When DVDD turns OFF (DVDD ≤ 0.2V), AK9750 is reset.

(5) Power Supply Reset
AK9750 is reset by VDD= 0V.

When AK9750 is reset, all registers are set to initial values.

11.3 Operating Mode

11.3.1. Normal Mode/Switch Mode

AK9750 has two Modes, Normal Mode and Switch Mode.

Normal Mode is the mode which controls AK9750 by using I^2C interface. The digital output the four IR sensors and the internal temperature sensor can be used through the I^2C interface in Normal Mode. INT output also can be used.

Switch Mode is the mode which uses only INT output without using I^2C interface. When the differential output of two sensors (IR1 - IR3 / IR2 - IR4) exceeds the upper / lower thresholds which are set to EEPROM, INT output turns “active”. When the differential output of two sensors (IR1 - IR3 / IR2 - IR4) is in the range which is set to EEPROM, INT output is “non-active”. The hysteresis for the thresholds can be set to EEPROM for avoiding the chattering of INT output. When Switch Mode is used, the threshold and the hysteresis should be set to EEPROM beforehand. When the accuracy of HumanSensing is not cared, Switch Mode can be used.

Normal Mode / Switch Mode selection is controlled by the CAD1 pin and CAD2 pin.
When CAD1 pin and CAD0 pin are set as CAD1 pin= CAD0 pin= “H”, the digital output can be used through the I^2C interface.
When CAD1 pin and CAD0 pin are set as CAD1 pin= CAD0 pin= “H”, Switch Mode is selected. When Switch Mode is selected, SCL pin and SDA pin should be tied to “H”. (Do not access the AK9750 through the I^2C interface in Switch Mode.)

Table 11.2. CAD0 / CAD1 pin Setting and Slave Address

CAD1	CAD0	I^2C output	Slave address	Mode
0	0	Enable	64H	Normal Mode
0	1	Enable	65H	Normal Mode
1	0	Enable	66H	Normal Mode
1	1	Disable	(67H)	Switch Mode

11.3.2. Normal Mode

There are the eight Modes in Normal Mode.

<Normal Mode (CAD0 pin= “L” or CAD1 pin= “L”)>
(1) Power down Mode
(2) Stand-by Mode
(3) Single shot Mode
(4) Continuous Mode 0
(5) Continuous Mode 1
(6) Continuous Mode 2
(7) Continuous Mode 3
(8) EEPROM access Mode

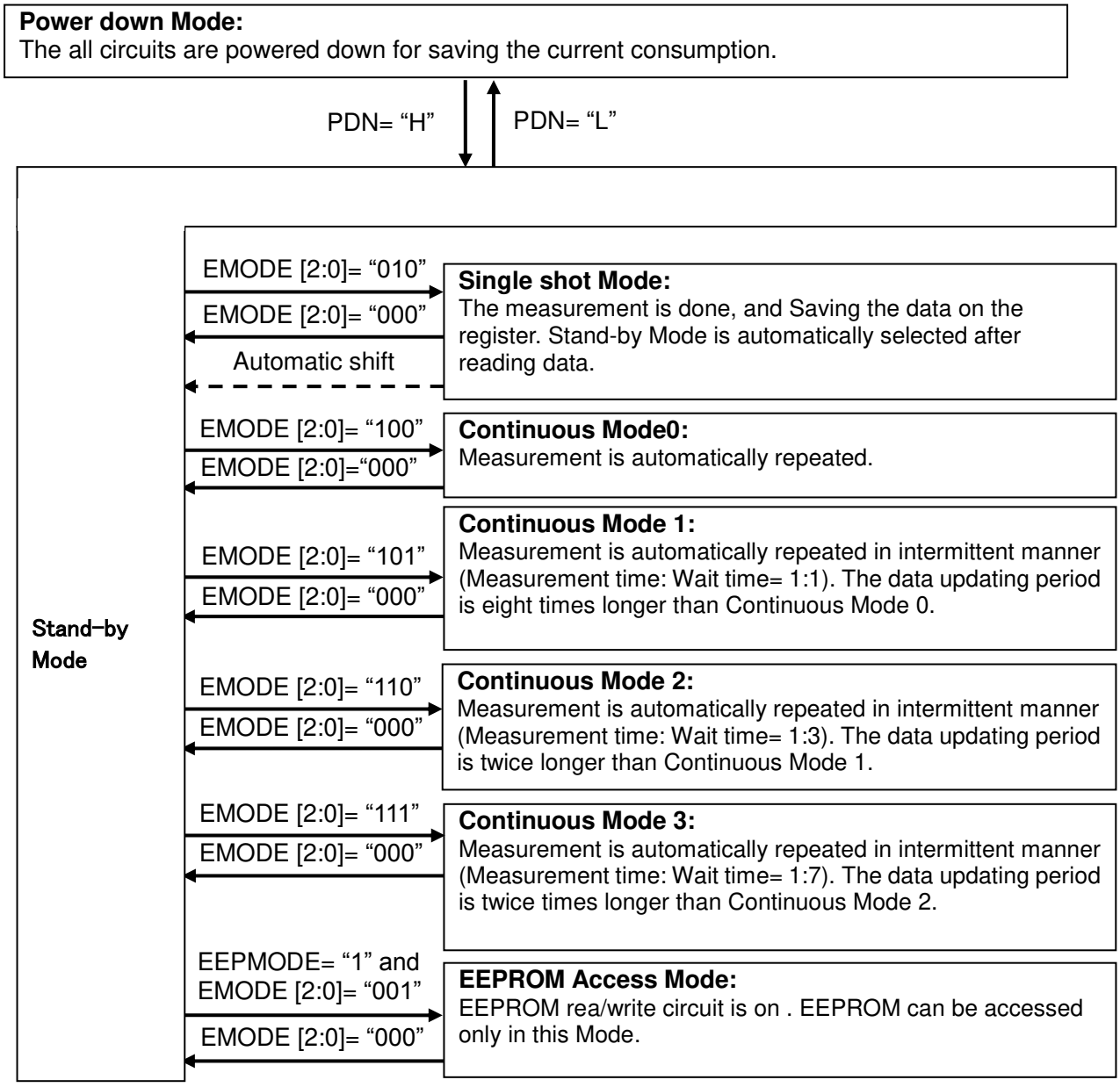


Figure 11.1. Various Modes in normal Mode.

On initial power-on with PDN pin= “H”, AK9750 is in Stand-by Mode. Based on EMODE [2:0] setup, the AK9750 shifts to the selected Mode, and starts operating. Any Mode changing should be done via Stand-by Mode.

11.3.3. Switch Mode

There are two Modes in Switch Mode.

<Switch Mode (CAD0 pin= CAD1 pin= “H”)>
(1) Power down Mode
(2) Measurement Mode

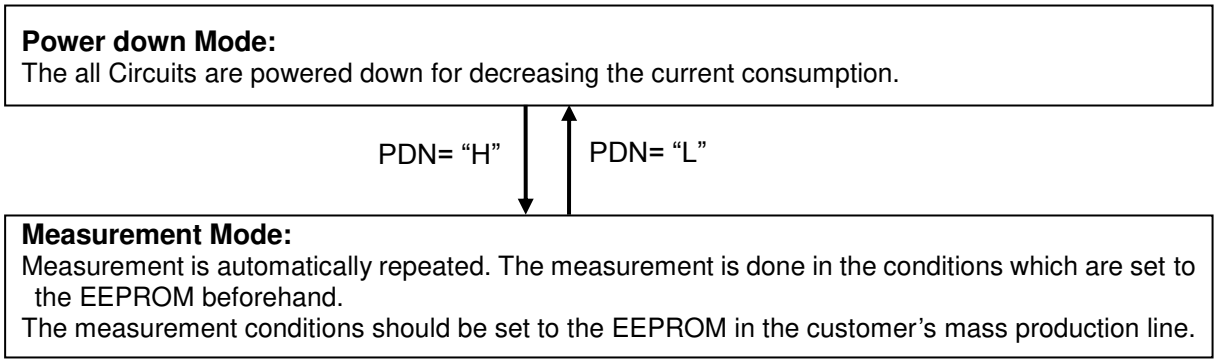


Figure 11.2. Various Modes in Switch Mode

11.4 Descriptions for each Operating Mode

11.4.1. Power down Mode (PDN pin= "L")

All circuits are powered off with PDN pin= "L". The all functions of AK9750 do not work in this Mode.

11.4.2. Stand-by Mode (EMODE [2:0] = "000")

All circuits are powered off except for POR circuit. All registers can be accessed in this Mode.
Read / Write register data are retained, and reset by software reset.
However, EEPROM data cannot be read / written in this Mode. Reading/Writing EEPROM data must be done in EEPROM access Mode.
The data registers (ST1 to ST2) should not be accessed in Stand-by Mode. It causes the malfunction of AK9750.

11.4.3. EEPROM Access Mode (EMODE [2:0] = "001" and EEPMODE= "1")

When EMODE [2:0] bits are changed from Stand-by Mode (EMODE [2:0] = "000") to EMODE [2:0] = "100" and EEPROM bit is set as "1", EEPROM Access Mode is selected. Reading / Writing EEPROM data should be done in EEPROM Access Mode. When EKEY [7:0] bit is set as "A5H" in EEPROM Access Mode, the data can be written to EEPROM.
Data measurement is not done in EEPROM Access Mode.

11.4.4. Single Shot Mode (EMODE [2:0] = "010")

When AK9750 is set to Single shot Mode (EMODE [2:0] = "010"), measurement is done once, and the Measurement data is stored to the measurement data registers (IR1L to TMPH). Then the analog circuits except for POR circuit are automatically powered off. When the registers from ST1 to ST2 are read, the AK9750 automatically shifts to Stand-by Mode (EMODE [2:0] = "000").

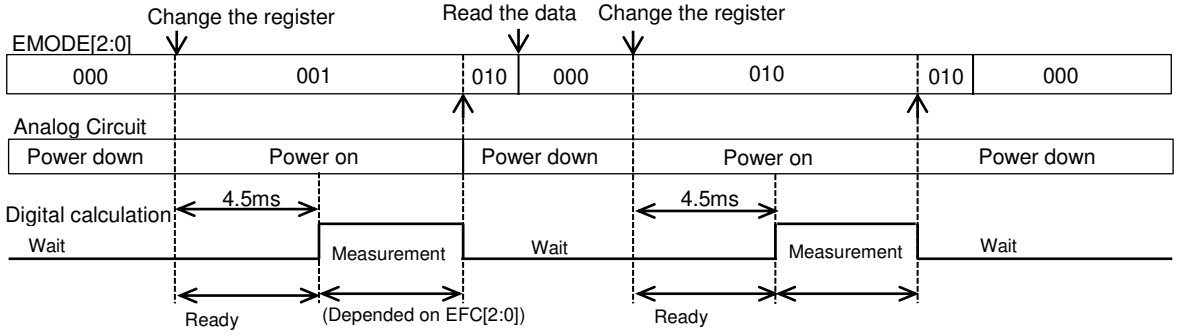


Figure 11.3. Single shot Mode

11.4.5. Continuous Mode 0 (EMODE [2:0] = “100”)

When Continuous Mode 0 (EMODE [2:0] = “100”) is selected the measurement is automatically repeated at the cycle which is determined by the digital filter cut-off frequency (EFC [2:0]).
When a measurement have been done, the measurement data is stored to the measurement register (IR1L to TMPH), and new measurement is started.
This Mode is terminated by setting the AK9750 to Stand-by Mode (EODE [2:0] = “000”).
When EMODE [2:0] is re-written during a measurement, the measurement is interrupted. Then the last data is retained to the register.
When Continuous Mode 0 is selected, a register write command should be executed. If register write command should be executed during a measurement, a right measurement data cannot be gotten.

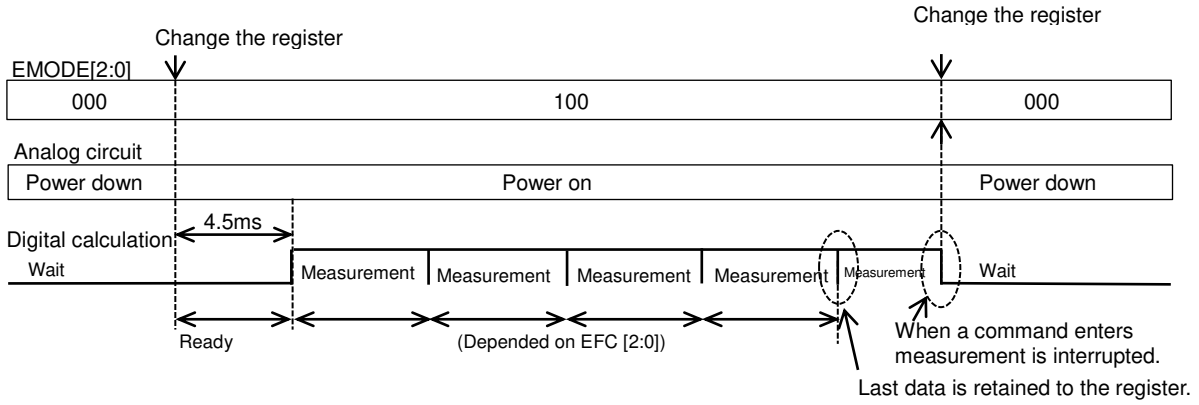


Figure 11.4. Continuous Mode 0

11.4.6. Continuous Mode 1,2,3 (EMODE [2:0] = “101”, “110”, “111”)

When Continuous Mode 1, 2, and 3 (EMODE [2:0] = “101”, “110”, “111”) are selected, a measurement and a wait are automatically repeated at the cycle according to the selected measurement Mode (EMODE [2:0]) and the digital filter cut-off frequency (EFC [2:0]).
A wait time length depends on the measurement Mode. When a measurement has been done, the measurement data is stored to the measurement register (IR1L to TMPH).
This Mode is terminated by setting the AK9750 to Stand-by Mode (EMODE [2:0] = “000”).
When EMODE [2:0] is re-written during a measurement, the measurement is interrupted. Then the last data is retained to the register.
When Continuous Mode 1, 2, and 3 is selected, a register write command should be executed. If a register write command should be executed during a measurement, a right measurement data cannot be gotten.

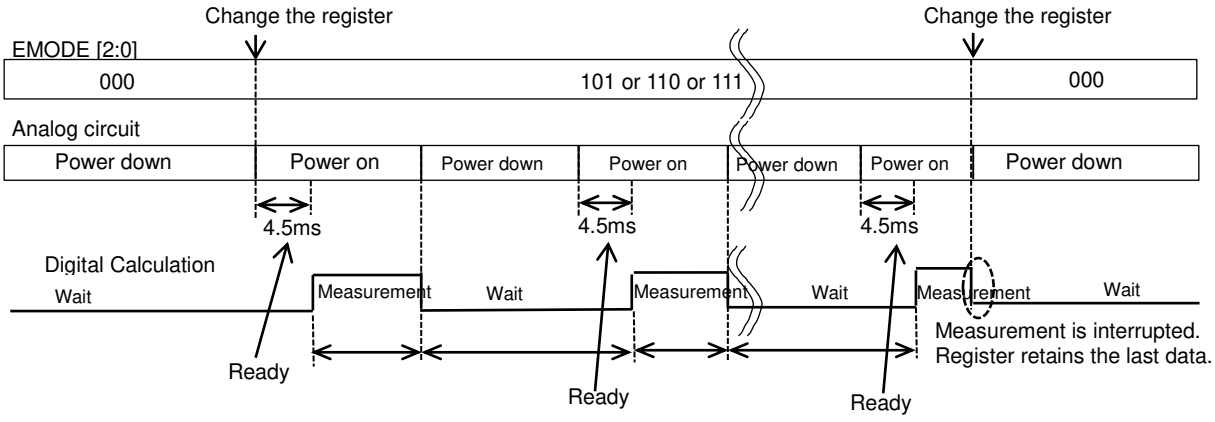


Figure 11.5. Continuous Mode 1, 2, and 3

11.5 Read Measurement Data

When a measurement data is stored to the measurement register, DRDY bit of ST1 register changes to "1". This state is called "Data Ready". It can be set up so that INT output "H", when the DRDY bit is "1", by setting up the interruption register.

The read-out procedure is detailed here. (Single shot Mode is used as an example.)
The same procedure can also be applied the Continuous Mode 0 (1, 2, and 3).

11.5.1. Normal Read-out Procedure

(1) Read-out ST1 registers
DRDY: DRDY shows whether the state is "Data Ready" or not.
DRDY = "0" means "No Data Ready".
DRDY = "1" means "Data Ready".

It is recommended that measurement data is read-out with DRDY = "1".

DOR: DOR shows whether there are any data which was not read out before initiating the current read.
DOR= "0" means that there are no data which was not read out before initiating the current read.
DOR= "1" means that there are data which was not read out before initiating the current read.

(2) Reading measurement data
Once a data read is initiated from one of the measurement data registers (IR1L to TMP) or the ST2 register, the AK9750 recognizes that a data read-out has begun. When a data read-out is initiated, DRDY and DOR change to "0".

(3) Reading ST2 Resisters (Required Operation)
The AK9750 recognizes that a data read-out has finished out the ST2 registers. Because the measurement data registers are protected while reading out, data is not updated. Data protection of the measurement data registers is canceled by reading out the ST2 register. The ST2 register must be read out after accessing the measurement data register.

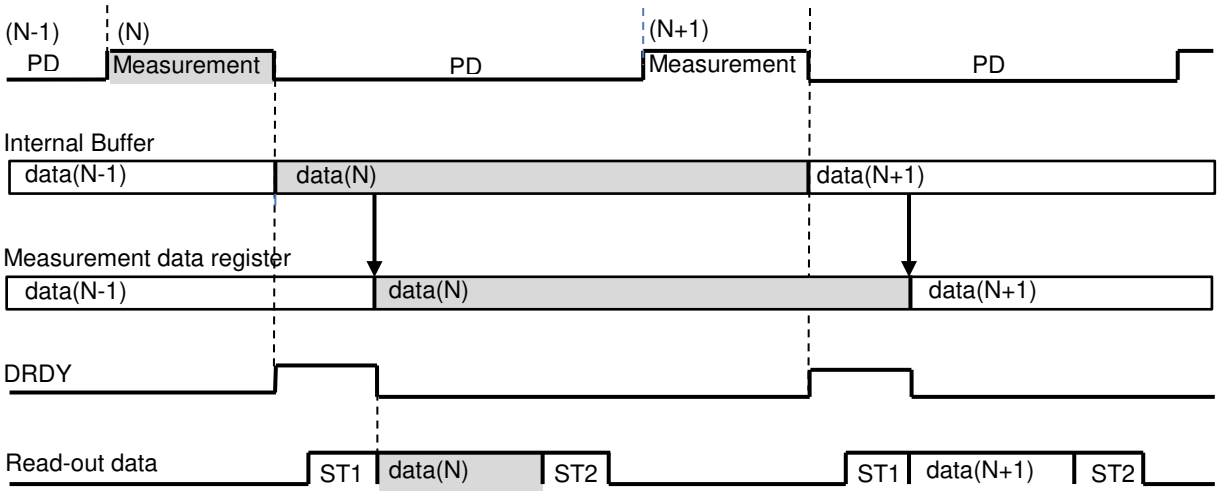


Figure 11.6. Normal Read-out Procedure

11.5.2. Read-out Data within a measurement Period

The measurement data register is retained within a measurement period, so the data can be read out within the measurement period. When data is read out within the measurement period, the previous data retained is read out.

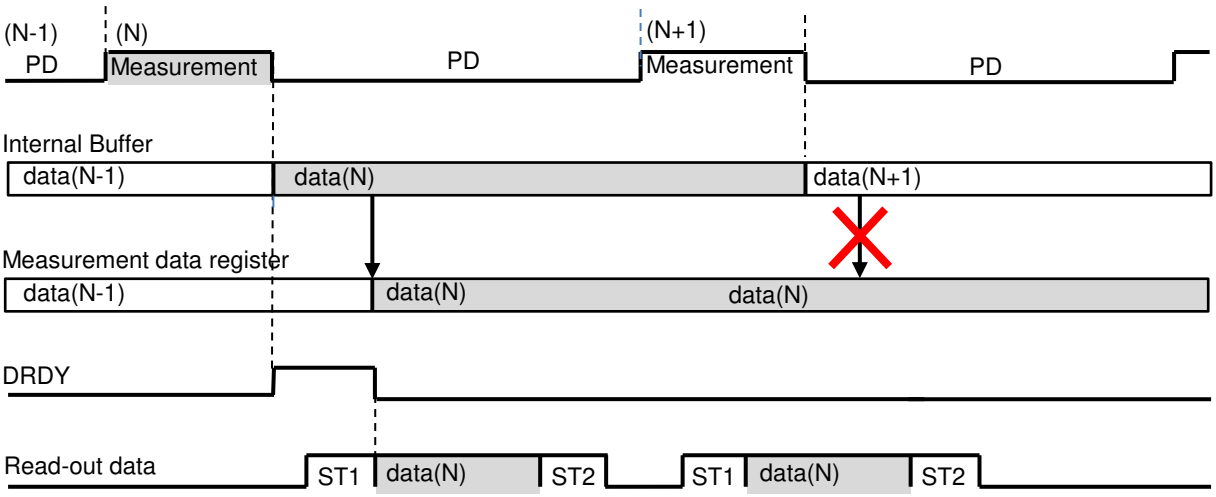


Figure 11.7. Read-out data within a measurement period

11.5.3. Skipping Data

When measurement data is not read out between the end points of (N+1)th and Nth measurement, DRDY is held until the measurement data is read out. In this case, because the Nth data was skipped, the DOR bit is “1”.

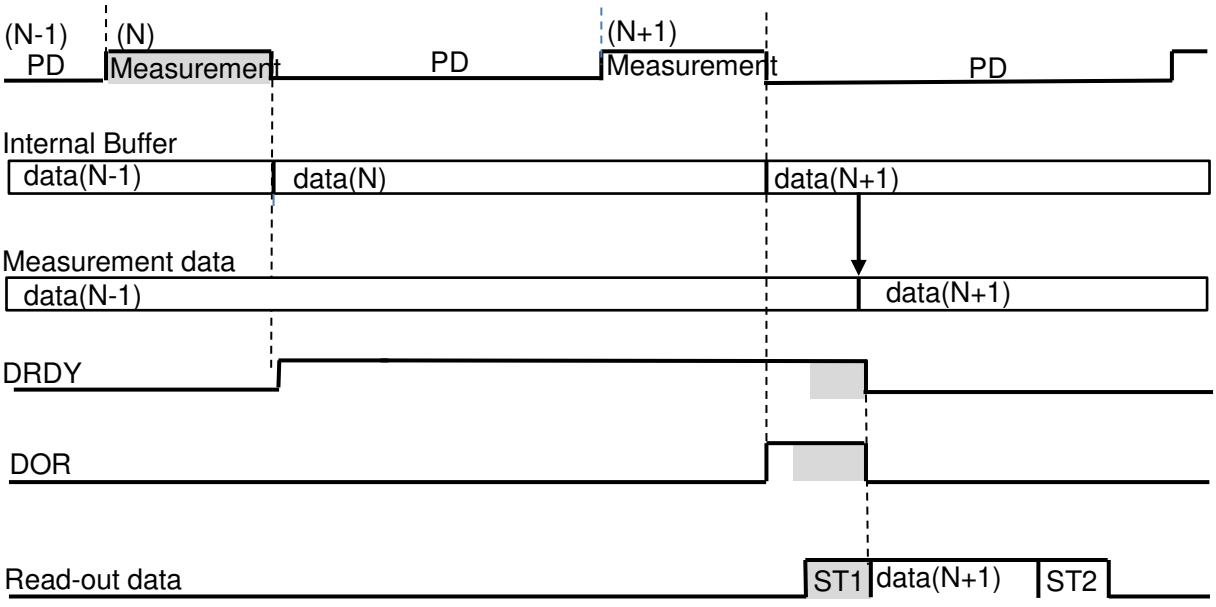


Figure 11.8. Skipping Data

When a data read begins after the end of the Nth measurement, and when data read cannot be completed until the end of the (N+1)th measurement, the measurement data registers are protected to read data normally. In this case, because the(N+1)th data has been skipped, the DOR bit transitions to "1".

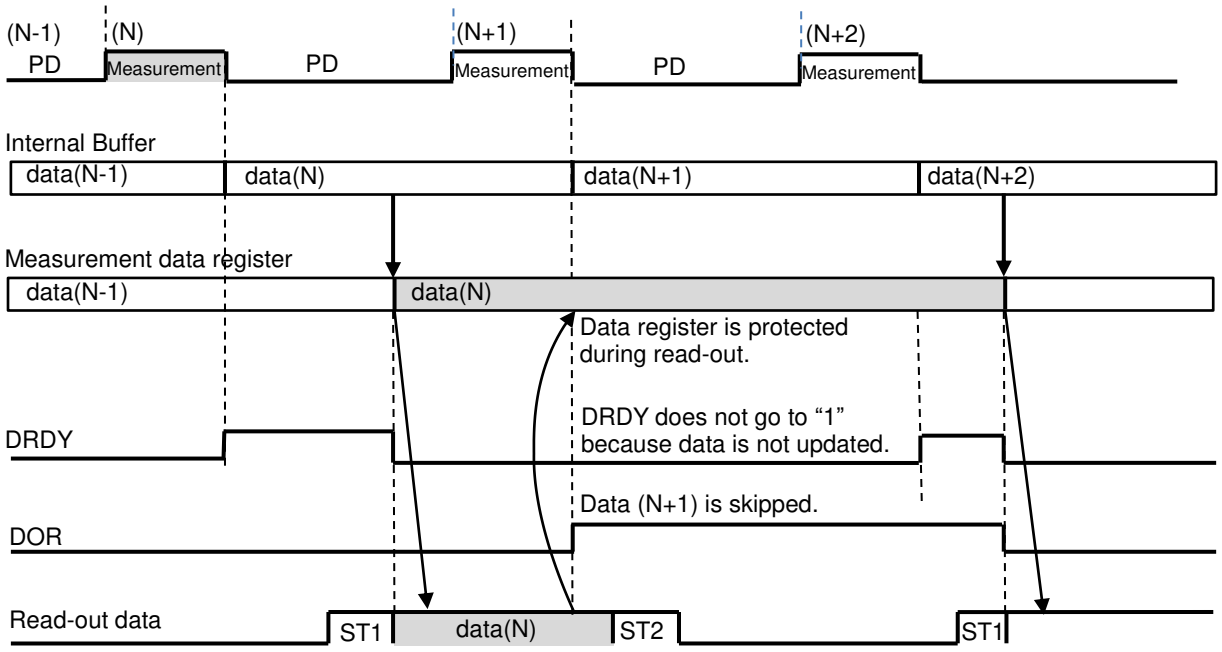


Figure 11.9. The data read cannot be completed until the beginning of the next measurement.

In both of these cases, the DOR bit changes to "0" from "1", at the start of reading data if DRDY is "1".

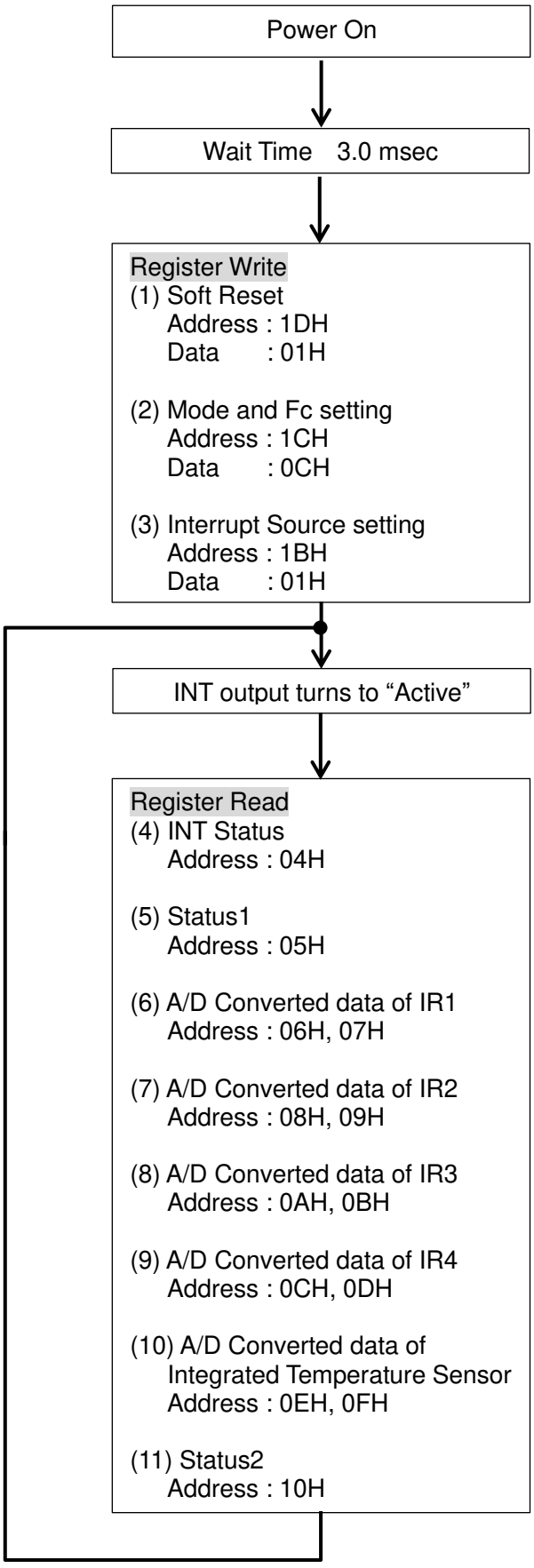
11.5.4. End Operation

Select Stand-by Mode (EMODE [2:0] = "000") to complete the Continuous Mode 0 (1, 2, and 3).

11.5.5. Example of Read-out Procedure

Example of read-out procedure of AK9750 data is shown in the following.
The below settings are assumed.

- Continuous Mode 0
  --> Measurement is automatically repeated.
- Digital Filter Cutoff Frequency Fc=0.6Hz
- Data ready interrupt setting is enable.
  --> INT output turns to "Active" at the timing of data ready.
  After that, HOST MCU should read out the data.


Power On
Wait Time 3.0 msec
Register Write
(1) Soft Reset
Address : 1DH
Data : 01H
(2) Mode and Fc setting
Address : 1CH
Data : 0CH
(3) Interrupt Source setting
Address : 1BH
Data : 01H
INT output turns to “Active”
Register Read
(4) INT Status
Address : 04H
(5) Status1
Address : 05H
(6) A/D Converted data of IR1
Address : 06H, 07H
(7) A/D Converted data of IR2
Address : 08H, 09H
(8) A/D Converted data of IR3
Address : 0AH, 0BH
(9) A/D Converted data of IR4
Address : 0CH, 0DH
(10) A/D Converted data of
Integrated Temperature Sensor
Address : 0EH, 0FH
(11) Status2
Address : 10H

12. Serial Interface

The I^2C bus interface of the AK9750 supports Standard Mode (Max. 100kHz) and High Speed Mode (Max. 400kHz).

12.1. Data Transfer

Initially the start condition should be input to access the AK9750 through the bus. Next, send a one byte slave address, which includes the device address. The AK9750 compares the a¥slave address, and if these addresses match, the AK9750 generates an acknowledge signal and executes a Read / Write command. The stop condition should be input after executing a command.

12.1.1. Changing state of the SDA line

The SDA line state should be changed only while the SCL line is “L”. The SDA line state must be maintained while the SCL line is “H”. The SDA line state can be changed while the SCL line is “H”, only when a Start Condition or a Stop Condition is input.

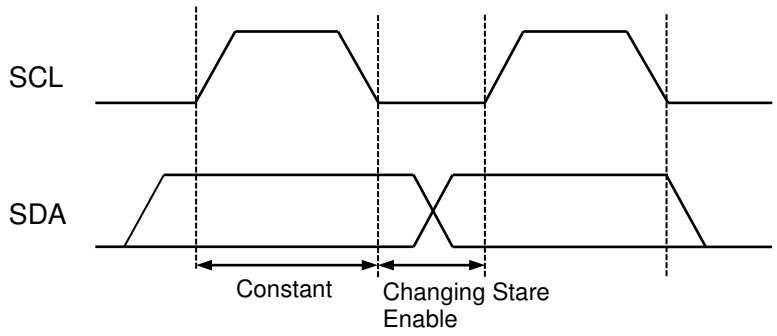


Figure 12.1.Changing state of SDA line

12.1.2. Start / Stop Conditions

A Start Condition is generated when the SDA line state is changed from “H” to “L” while the SCL line is “H”. All command start from a Start condition.
A Stop condition is generated when the SDA line state is changed from “L” to “H” while the SCL line is “H”. All command end after a Stop condition.

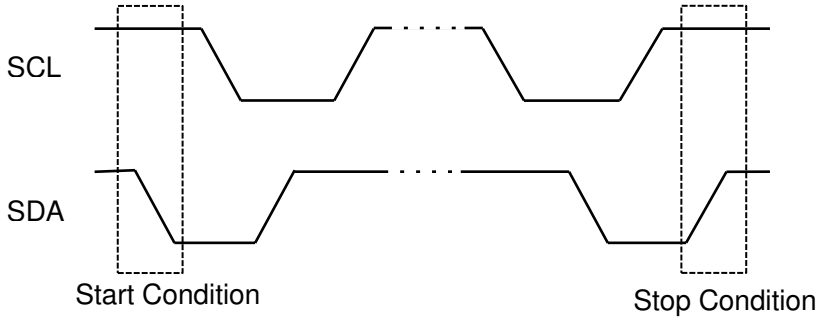


Figure 12.2. Start / Stop Conditions

12.1.3. Acknowledge

The device transmitting data will release the SDA line after transmitting one byte of data (SDA line state is “H”). The device receiving data will pull the SDA line to “L” during the next clock. This operation is called “Acknowledge”. The Acknowledge signal can be used to indicate successful data transfers.

The AK9750 will output an acknowledge signal after receiving a Start condition and Slave address.

The AK9750 will output an acknowledge signal after receiving each byte, when the WRITE instruction is transmitted.

The AK9750 will transmit the data stored in the selected address after outputting an acknowledge signal, when a READ instruction is transmitted. Then the AK9750 will monitor the SDA line after releasing the SDA line. If the master device generates an Acknowledge instead of Stop condition, the AK9750 transmits an 8-bit data stored in the next address. When the Acknowledge is not generated, transmitting data is terminated.

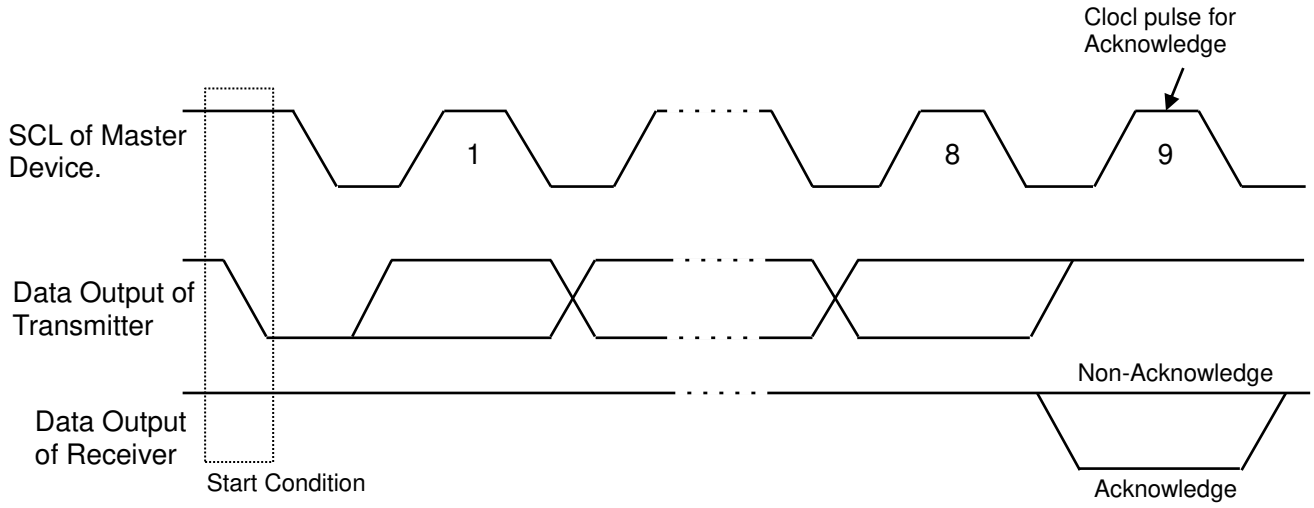


Figure 12.3. Acknowledge

12.1.4. Slave Address

The Slave address of the AK9750 can be selected from the following list by setting the CAD0/1 pins. When the CAD0/1 pins are connected to VSS, the Slave address bit is = "0". When the CAD0/1 pins are connected to VDD, the Slave address bit is "1". Do not set up "CAD1 pin = CAD0 pin = 1" while the I^2C interface is used, because the "CAD1 pin = CAD0 pin = 1" state is only for Switch Mode.

Table 12.1. CAD0/1 pin setting and Slave Address

CAD1 pin	CAD0 pin	Slave Address
0	0	64H
0	1	65H
1	0	66H
1	1	Switch Mode

When the first one byte data including the Slave address is transmitted after a Start condition, the device, which is specified as the communicator by the Slave address on bus, selected.

After transmitting the Slave address, the device that has the corresponding device address will execute a command after transmitting an Acknowledge signal. The 8-bit (Least Significant bit-LSB) of the first one byte is the R/W bit.

When the R/W bit is set to "1", a READ command is executed. When the R/W bit is set to "0", a WRITE command is executed.

MSB LSB

1	1	0	0	1	CAD1	CAD0	R/W

Figure 12.4. Slave Address