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AK9752
Ultra-small IR Sensor IC with I²C I/F

1. General Description

The AK9752 is a very low power and ultra-small infrared-ray (IR) sensor module. It is composed of a quantum IR sensor and an integrated circuit (IC) for signal processing. The IR sensor's offset variation is calibrated at shipment. An integral analog-to-digital converter provides 16-bits data outputs. The AK9752 is applied for detecting human presence.

2. Features

☐ Quantum-type IR sensor

☐ Integrated Temperature sensor: -30 ~ 85ºC output on I²C bus

☐ 16-bits Digital outputs to I²C bus

☐ Integrated Digital filter:
- IR sensor: Cut-off frequency 2.5Hz, 0.9Hz, 0.45Hz
- Temperature sensor: Cut-off frequency 2.5Hz, 0.9Hz, 0.45Hz, 0.22Hz

☐ I²C interface:
Standard mode (100kHz) supported in case of external pull-up voltage VDD ~ 3.63V
Fast mode (400kHz) supported in case of external pull-up voltage VDD ~ 1.95V

☐ Interrupt Function
INTN pin can be used as a read-trigger or an interrupt request of signal level monitoring.

☐ Low Voltage Operation: 1.65 ~ 1.95V

☐ Low Current Consumption: 100μA (Max.) in case of 10Hz output (Continuous mode)
10μA (Typ.) in case of 1Hz output (Single shot mode)

☐ Ultra-small and Thin Package: 6-pin SON
2.2mm x 2.2mm x t0.6mm

3. Table of Contents

4. Block Diagram and Functions

4.1. Block Diagram

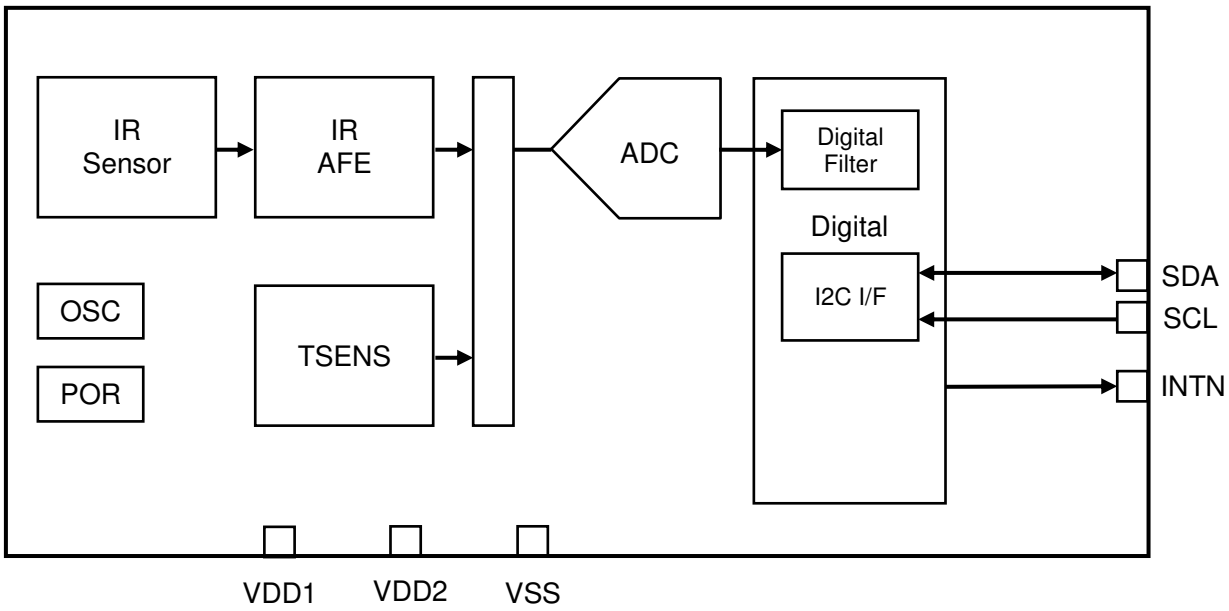


Figure 4.1 AK9752 Block Diagram

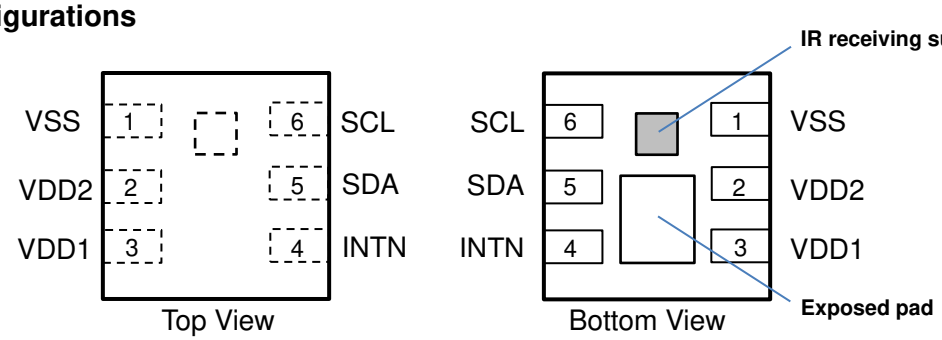
4.2. Functions

Table 4.1 Functions

Block	Function
IR Sensor	IR sensor element.
OSC	Built-in Oscillator.
TSENS	Built-in Temperature sensor.
IR AFE	Converting current from the IR sensor element into voltage signal. Also cancelling offset of the sensor signal.
ADC	Convert analog outputs of IR AFE and TSENS into digital signals.
Digital Filter	Digital filter (LPF) for ADC output. Cut-off frequency (Fc) is selectable.
I^2C I/F	Interface to external host MCU. SCL and SDA pins are provided for I^2C Interface. Standard mode (100kHz) is supported in case of external pull-up voltage VDD ~ 3.63V. Fast mode (400kHz) is supported in case of external pull-up voltage VDD ~ 1.95V.
POR	Power on reset circuit.

5. Pin Configurations and Functions

5.1. Pin Configurations



Note: Exposed pad internally connects to VSS pin.

Figure 5.1 Pin Configurations

5.2. Functions

Table 5.1 Functions

Pin No.	Name	I/O	Function
1	VSS	-	Ground Pin.
2	VDD2	-	Power Supply Pin. Connect together with VDD1 line on a board. (VDD2=VDD1=VDD)
3	VDD1	-	Power Supply Pin. Connect together with VDD2 line on a board. (VDD1=VDD2=VDD)
4	INTN	O	Interrupt Pin. It goes to “L” in the following cases. (1) ADC output is ready to be read. (2) IR output or Temperature Sensor output exceeds the specified threshold levels. INTN pin is an open drain output (N-type transistor), and connected to a power line of 1.65V ~ 3.63V through a pull-up resistor.
5	SDA	I/O	I^2C Data In/Output Pin. A bidirectional pin which is used to transmit data into and out of the device. It is composed of a signal input and an open drain output (N-type transistor). SDA pin is connected to the following power line through a pull-up resistor. VDD ~ 3.63V at Standard mode (100kHz) VDD ~ 1.95V at Fast mode (400kHz) Refer to the note in “17. Recommended External Circuits”
6	SCL	I	I^2C Clock Input Pin. Signal processing is executed at the rising and falling edge of SCL clock. SCL pin is connected to the following power line through a pull-up resistor. VDD ~ 3.63V at Standard mode (100kHz) VDD ~ 1.95V at Fast mode (400kHz) Refer to the note in “17. Recommended External Circuits”

6. Absolute Maximum Ratings

(VSS= 0V)

Parameter		Symbol	Min.	Max.	Unit
Power Supply	VDD1 pin, VDD2 pin	VDD	-0.3	2.5	V
Input Current	All pins	Iin	-10	10	mA
Output Current	All pins	Iout	-10	10	mA
Input Voltage	SDA pin, SCL pin, INTN pin	Vin	-0.3	4.5	V
Storage Temperature		Tst	-40	85	ºC

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS= 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply	VDD	1.65	1.8	1.95	V
Operating Temperature	Ta	-30		85	ºC

8. Power Supply Conditions

(Unless otherwise specified, VDD1=VDD2=VDD= 1.65 ~ 1.95V, Ta= -30 ~ 85ºC)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Power Supply Rise Time (* 1, * 2)	Time until VDD is set to the operating voltage from 0.2V.	VDD1 pin, VDD2 pin	PSUP			50	ms
Power-on Reset Time (* 1, * 2)	Time until AK9752 becomes Stand-by Mode after PSUP.	VDD1 pin, VDD2 pin	PORT			100	µs
Shutdown Voltage (* 2, * 3)	Shutdown Voltage for POR re-starting.	VDD1 pin, VDD2 pin	SDV			0.2	V
Power Supply Interval Time (* 1, * 2, * 3)	Voltage retention time below SDV for POR re-starting.	VDD1 pin, VDD2 pin	PSINT	100			µs

Notes:
* 1. Reference data only, not tested.
* 2. Power-on Reset circuit detects the rising edge of VDD, resets the internal circuit, and initializes the registers. After Power-on reset, Stand-by Mode is selected.
* 3. The condition that POR surely works at the power-up the power-up again after power supply goes down. Unless this condition is satisfied, the reset may not be correctly performed.

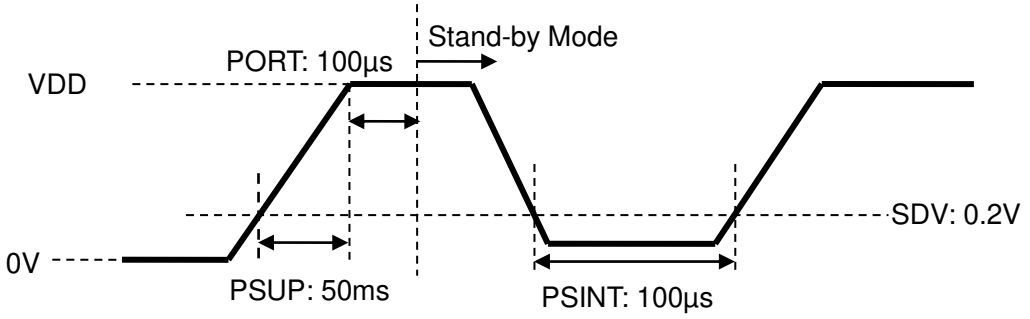


Figure 8.1. Power Supply Conditions

9. Electrical Characteristics

9.1. Analog Characteristics

(Unless otherwise specified, VDD1=VDD2=VDD= 1.65 ~ 1.95V, Ta= -30 ~ 85ºC)

Parameter		Symbol	Min.	Typ.	Max.	Unit
IR output resolution				16		bit
IR offset code (* 4)	・Temperature difference between object and sensor is zero.	SO0	-40	0	40	Code
IR output code (* 4)	・Object: Cavity Blackbody Φ22.2mm, 500K, Distance 10cm ・Ambient temperature Ta= 25ºC	SO1		13100		Code
Temperature sensor output resolution				16		bit
Temperature sensor Output code (* 4, * 5)	Ta= -30 ºC	TO		-27726		Code
	Ta= 25 ºC		-2016	0	2016	
	Ta= 85 ºC			30247		
Temperature sensor Sensitivity		TOS		0.0019837		ºC/Code
Averaged current consumption	Stand-by Mode MODE [1:0] = “00”	IDD0		1	10	μA
	Continuous Mode MODE [1:0] = “01”	IDD1			100	μA
	Single shot Mode (1Hz cycle) MODE [1:0] = “10”	IDD2		10		μA

Note:
* 4. 2’s complement
* 5. Linear to internal temperature (excluding noise)

9.2. Digital Characteristics

9.2.1. DC Characteristics

(Unless otherwise specified, VDD1=VDD2=VDD= 1.65 ~ 1.95V, Ta= -30 ~ 85ºC)

Parameter			Symbol	Min.	Typ.	Max.	Unit
High level input Voltage (* 6)		SCL pin, SDA pin	VIH1	70%VDD			V
Low level input Voltage (* 7)		SCL pin, SDA pin	VIL1			30%VDD	V
Input current	Vin=VSS / VDD	All pins	IIN	-10		10	μA
Hysteresis Input Voltage (* 8)		SCL pin, SDA pin	VHS	10%VDD			V
Low level output Voltage	IOL= 3mA	SDA pin	VOL			20%VDD	V
	IOL=300μA	INTN pin					

Note:
* 6. Max. 1.95V at Fast Mode, Max. 3.63V at Standard Mode
* 7. Refer to the note in “17. Recommended External Circuits”
* 8. Reference data only, not tested.

9.2.2. AC Characteristics (1): Standard Mode (100 kHz)

(Unless otherwise specified, VDD1=VDD2=VDD= 1.65 ~ 1.95V, Ta= -30 ~ 85°C)

External pull-up voltage: VDD ~ 3.63V

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCL frequency		fSCL			100	kHz
SDA bus idle time to the next command input		fBUF	4.7			µs
Start condition Hold time		tHD:STA	4.0			µs
Clock Low period		tLOW	4.7			µs
Clock High period		tHIGH	4.0			µs
Start condition set-up time		tSU:STA	4.7			µs
Data hold time		tHD:DAT	0			µs
Data set-up time		tSU:DAT	250			ns
Rise time SDA, SCL (* 9)	SDA pin, SCL pin	tR			1.0	µs
Fall time SDA, SCL (* 9)	SDA pin, SCL pin	tF			0.3	µs
Stop condition set-up time		tSU:STO	4.0			µs

Note:

* 9. Reference data only, not tested.

9.2.3. AC Characteristics (2): Fast Mode (400 kHz)

(Unless otherwise specified, VDD1=VDD2=VDD = 1.65 ~ 1.95V, Ta= -30 ~ 85°C)

External pull-up voltage: VDD ~ 1.95V

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCL frequency		fSCL			400	kHz
Noise suppression time		tSP			50	ns
SDA bus idle time to the next command input		fBUF	1.3			µs
Start condition Hold time		tHD:STA	0.6			µs
Clock Low period		tLOW	1.3			µs
Clock High period		tHIGH	0.6			µs
Start condition set-up time		tSU:STA	0.6			µs
Data hold time		tHD:DAT	0			µs
Data set-up time		tSU:DAT	100			ns
Rise time SDA, SCL (* 10)	SDA pin, SCL pin	tR			0.3	µs
Fall time SDA, SCL (* 10)	SDA pin, SCL pin	tF			0.3	µs
Stop condition set-up time		tSU:STO	0.6			µs

Note:

* 10. Reference data only, not tested.

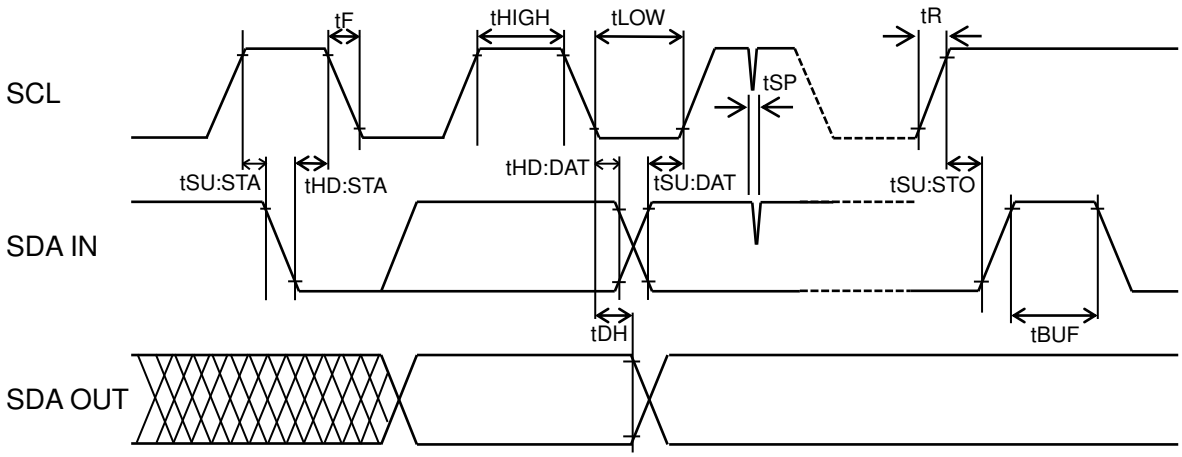


Figure 9.1 Bus Timing

9.2.4. AC Characteristics (3): INTN

(Unless otherwise specified, VDD1=VDD2=VDD= 1.65 ~ 1.95V, Ta= -30 ~ 85°C)

External pull-up voltage: VDD ~ 3.63V

Parameter		Symbol	Min.	Typ.	Max.	Unit
Rise time (* 11, * 12)	INTN pin	tR			2	µs
Fall time (* 11, * 12)	INTN pin	tF			0.25	µs

Note:

* 11. Reference data only, not tested.

* 12. The case that the load circuit of Figure 9.2 is connected.

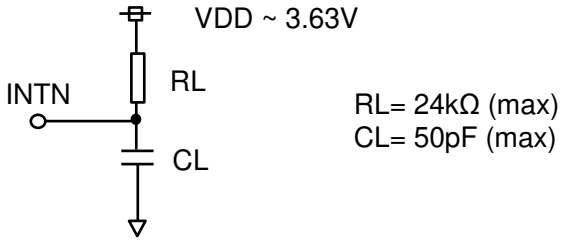


Figure 9.2. INTN load circuit

10. Functional Descriptions

10.1. Power Supply States

When VDD1 and VDD2 turn on from the state of VDD1= VDD2= OFF(0V), Power-on Reset(POR) automatically operates, all registers will be initialized, and the AK9752 will be set to Stand-by Mode.

Table 10.1. Power Supply States and Functions

State	VDD pin	I^2C	INTN pin	Analog Circuit	IDD
1	OFF(0V)	Disable	Unfixed	Power Down	Not specified
2	1.65V - 1.95V	Enable	“H” (* 13)	Power Down except POR circuit	< 10μA

Note:
* 13. “H” level by a pull-up resistor.

10.2. Reset functions

AK9752 is initialized in the following conditions,

(1) Power-on Reset(POR)
When VDD1, VDD2 turns ON, Power-on Reset (POR) resets AK9752 until VDD reaches the operating voltage.
After POR, all registers are set to initial values, and Stand-by Mode is selected.
Accessing registers should be performed after POR.

(2) Software Reset
AK9752 is reset by writing software reset register.
An acknowledge signal will return, and AK9752 becomes the same state as after POR.

10.3. Operating Mode

AK9752 is assumed to operate with connecting to Host MCU.

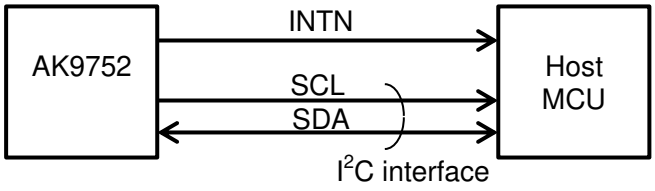


Figure 10.1 Example of use (Connection diagram)

AK9752 and Host MCU should be connected with SCL and SDA (I^2C interface). The operating control and the data readout of AK9752 can be available through the I2C interface. The slave address is 64H.
INTN output can be used as interrupt control signal.
Refer to Recommended External Circuits (Figure 17.1) for details.

There are three operating modes.

(1) Stand-by Mode
(2) Continuous Mode
(3) Single shot Mode

10.4. Descriptions for each Operating Mode

10.4.1. Stand-by Mode (MODE [1:0] = “00”)

AK9752 goes to Stand-by Mode by resetting(POR or Software RST) or setting the operating mode setting register. All circuits are powered down except for POR circuit. All registers can be accessed in this mode.
Parameters and measurement data in registers are retained, and INTN is set to the initial state in this mode.

10.4.2. Continuous Mode (MODE [1:0] = “01”)

When Continuous Mode (MODE [1:0] = “01”) is selected, the measurement is automatically repeated at the period of 100ms(typ.). The read-out registers will be updated every after completion of a measurement.
This mode is terminated by setting Stand-by Mode (MODE [1:0] = “00”).
When MODE [1:0] is changed during a measurement, the measurement is interrupted. Then the last data is retained in the registers.
It is possible to write the threshold setting register and the interrupt setting register during this mode.

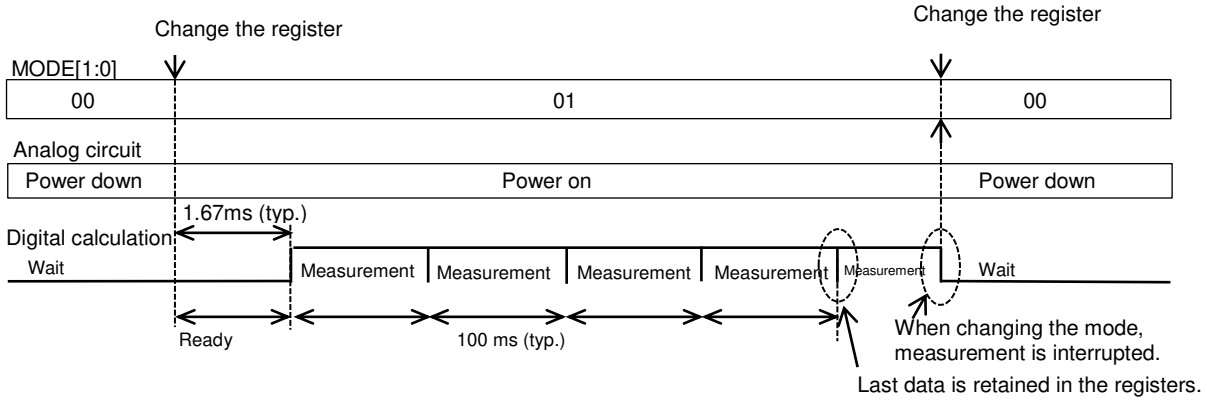


Figure 10.2. Continuous Mode

10.4.3. Single Shot Mode (MODE [1:0] = “10”)

When AK9752 is set to Single shot Mode (MODE[1:0] = “10”), measurement is done one time, and the measurement data is stored to the read-out registers. AK9752 becomes automatically powered down except for POR circuit after completion of the measurement. MODE[1:0] changes to “00”.
The digital filter of ADC is invalid in this mode.

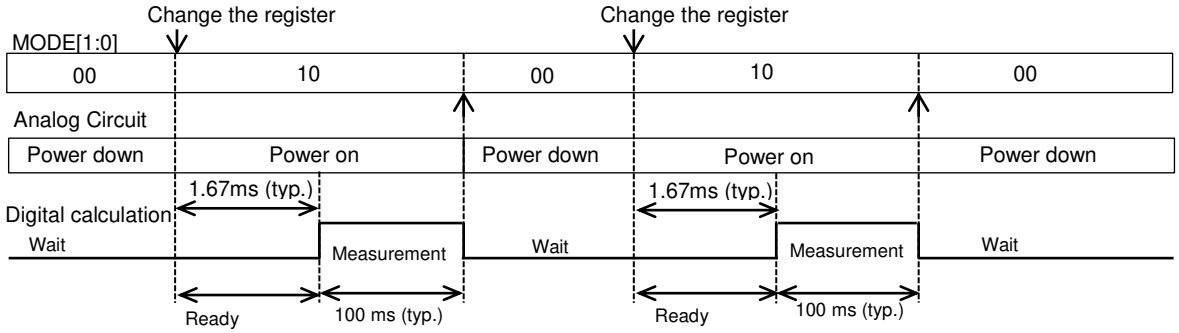


Figure 10.3. Single shot Mode

10.5. Read Measurement Data

When measurement data is stored and updated in the read-out register, DRDY bit of ST1 register changes to “1”. This state is called “Data Ready”.
It can be also set up so that INTN outputs “L”, when the DRDY changes to “1”, by setting the interrupt setting register INTEN.
By the either above ways, it can be confirmed whether Data Ready or not.
The read-out procedure is detailed as follows. (Single shot Mode is used as an example.)

10.5.1. Normal Read-out Procedure

(1) Read out ST1 register
DRDY: DRDY bit shows whether the state is “Data Ready” or not.
DRDY = “0” means “No Data Ready”.
DRDY = “1” means “Data Ready”.
It is recommended that measurement data is read out when DRDY = “1”.

(2) Read out INTCAUSE register
Interrupt factors can be found out by reading out INTCAUSE register.
Refer to 13. Registers Functional Descriptions for details.
When starting reading-out of INTCAUSE register, measurement data are transferred to read-out registers and retained. (Data protection)
INTN returns to “Hi-Z” after reading out INTCAUSE register.

(3) Read out measurement data

(4) Read out ST2 resister (Required Operation)
AK9752 recognizes that a data read-out has finished by read out the ST2 registers. Because read-out registers are protected while reading out, data is not updated. Data protection of the read-out registers is released by reading out the ST2 register. The ST2 register must be read out after accessing read-out registers.
DOR: DOR bit shows whether there are any data which had not been read out before initiating the current read.
DOR= “0” means that there are no data which had not been read out before initiating the current read.
DOR= “1” means that there are data which had not been read out before initiating the current read.
DRDY and DOR changes to “0” after reading out ST2 register.

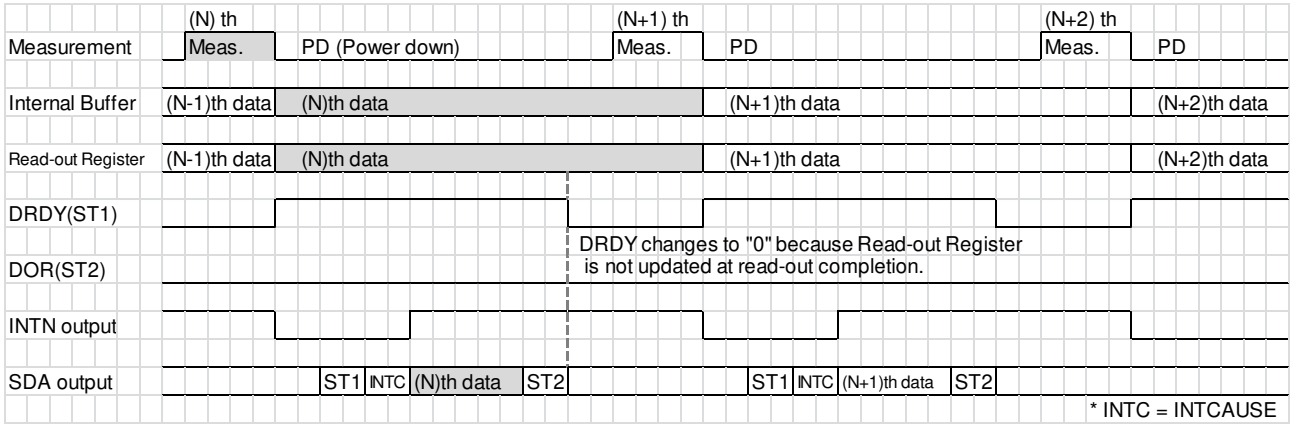


Figure 10.4. Normal Read-out Procedure

10.5.2. Read-out Data during a measurement Period

The read-out registers retain the previous data during a measurement period, so the data can be read out during the measurement period. When data is read out during the measurement period, the previous data is read out.

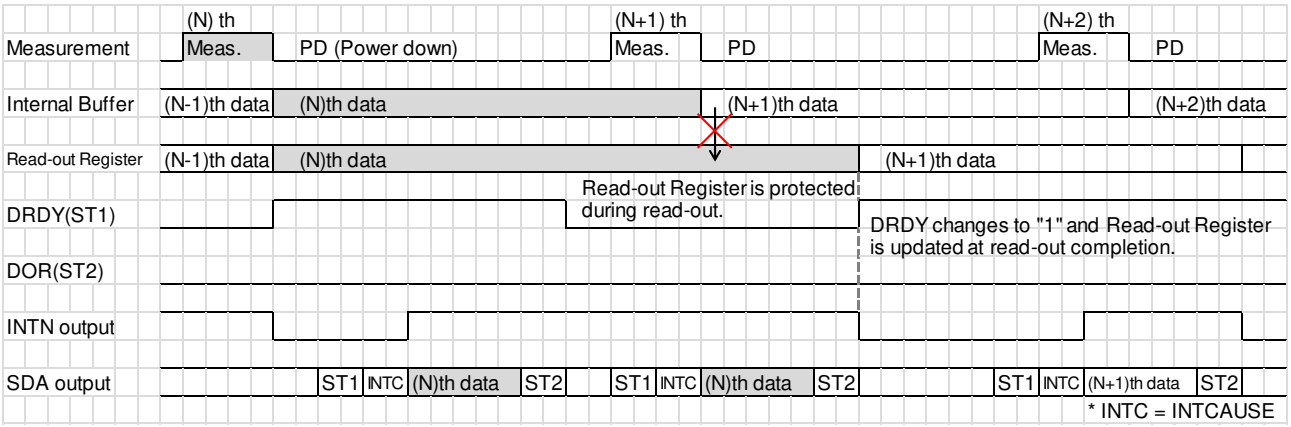


Figure 10.5. Read-out during a measurement period

10.5.3. Skipping Data

When (N)th data is not read out between the end points of (N+1)th measurement, DRDY is held until measurement data is read out. Because the Nth data was skipped, DOR changes to “1” at the completion of (N+1)th measurement.

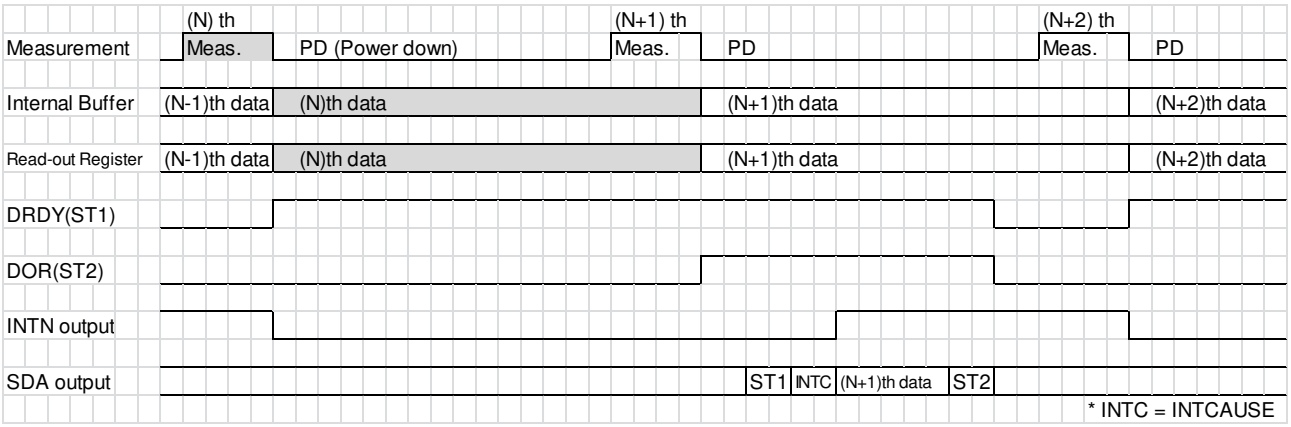


Figure 10.6. Data Skipping

When a data read-out starts after Nth measurement, and when it is not completed until the end of (N+1)th measurement, the read-out registers are protected to read out the data normally.
In this case, (N+1)th data can be read out by re-reading out before (N+2)th measurement completion.

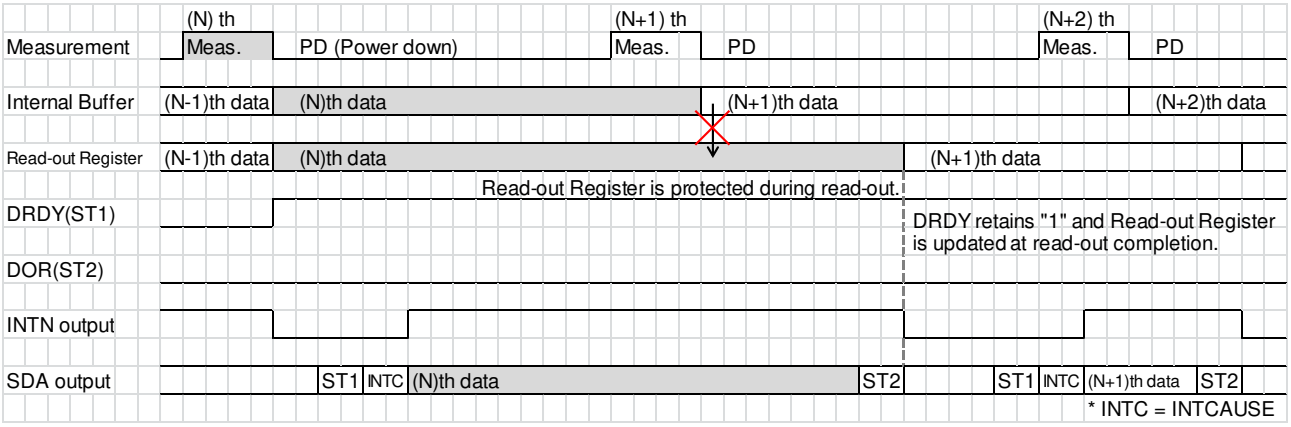


Figure 10.7. Measurement Completion during read-out data (one measurement)

When (N+1)th and (N+2)th measurement are completed during (N)th data read-out, (N+1)th data is skipped and DOR changes to “1” after (N+2)th measurement.
DOR returns to “0” when the next read-out.

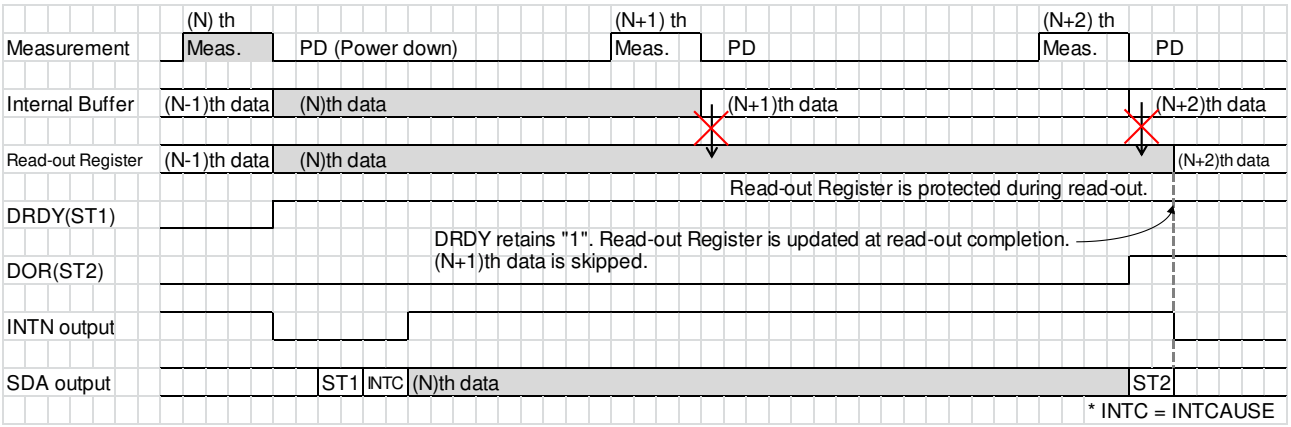


Figure 10.8. Measurement Completion during read-out data (twice measurement)

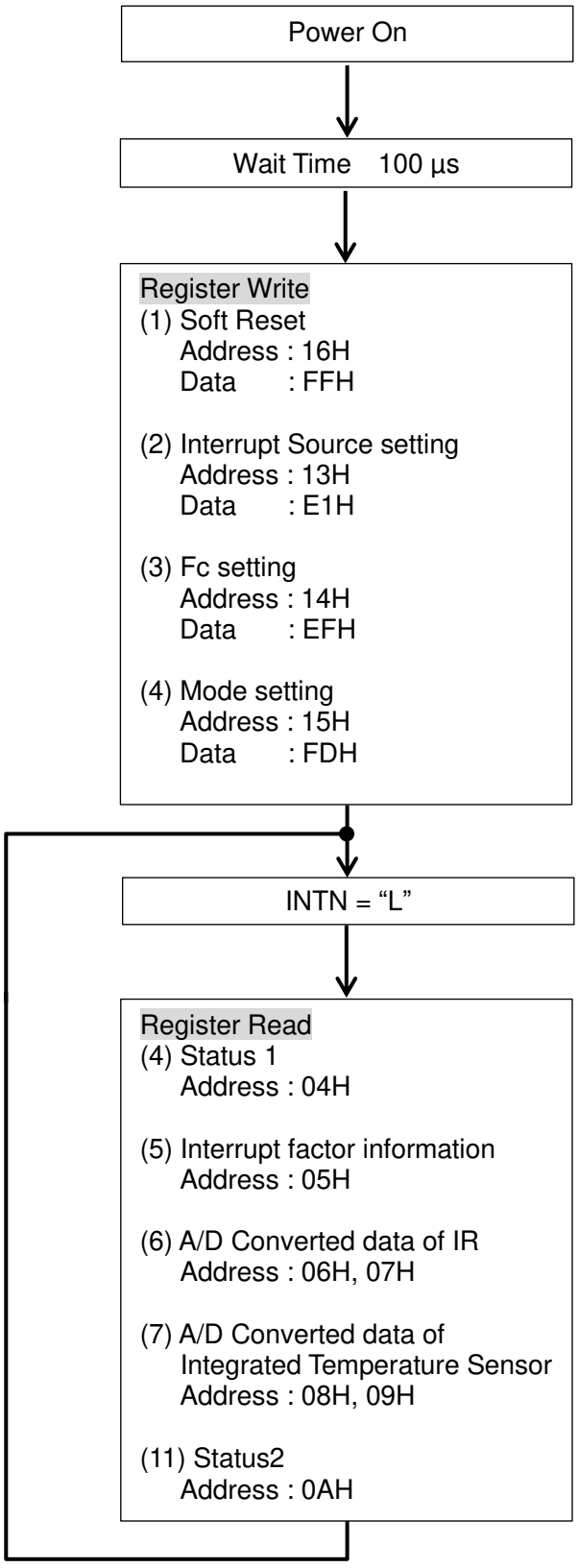
10.5.4. End Operation

Select Stand-by Mode (MODE[1:0] = “00”) to quit the Continuous Mode.

10.5.5. Example of Read-out Procedure

Example of read-out procedure of AK9752 is shown in the following.
The below settings are assumed.

- Continuous Mode
- Cut-off frequency of Digital Filter Fc=0.45Hz
- Data ready interrupt setting is enable. → INTN output turns to “L”(Active) after completion of data ready.


Power On
Wait Time 100 µs
Register Write
(1) Soft Reset
Address : 16H
Data : FFH
(2) Interrupt Source setting
Address : 13H
Data : E1H
(3) Fc setting
Address : 14H
Data : EFH
(4) Mode setting
Address : 15H
Data : FDH
INTN = “L”
Register Read
(4) Status 1
Address : 04H
(5) Interrupt factor information
Address : 05H
(6) A/D Converted data of IR
Address : 06H, 07H
(7) A/D Converted data of
Integrated Temperature Sensor
Address : 08H, 09H
(11) Status2
Address : 0AH

11. Serial Interface

The I^2C bus interface of the AK9752 supports Standard Mode (Max. 100kHz). Fast Mode (Max. 400kHz) is also supported in case that an external pull-up voltage is VDD ~ 1.95V.

11.1. Data Transfer

Access AK9752 through the I^2C bus after POR.
Initially the Start Condition should be input to access the AK9752 through the bus. Next, send a one byte slave address, which includes the device address. The AK9752 compares the slave address, and if these addresses match, the AK9752 generates an acknowledge signal and executes a read / write command. The Stop Condition should be input after executing a command.

11.1.1. Changing state of the SDA line

The SDA line state should be changed only while the SCL line is “L”. The SDA line state must be maintained while the SCL line is “H”. The SDA line state can be changed while the SCL line is “H”, only when a Start Condition or a Stop Condition is input.

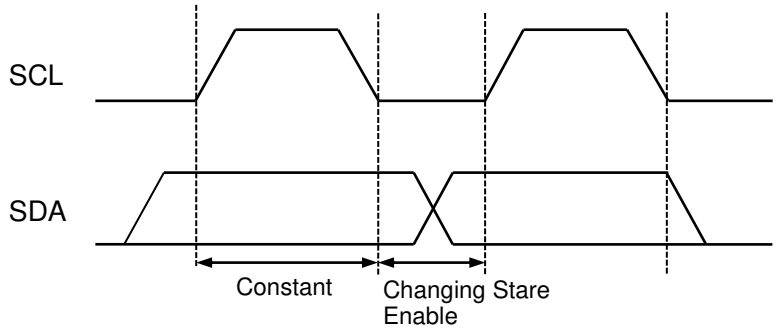


Figure 11.1.Changing state of SDA line

11.1.2. Start / Stop Conditions

A Start Condition is generated when the SDA line state is changed from “H” to “L” while the SCL line is “H”. All command start from a Start Condition.
A Stop condition is generated when the SDA line state is changed from “L” to “H” while the SCL line is “H”. All command end after a Stop Condition.

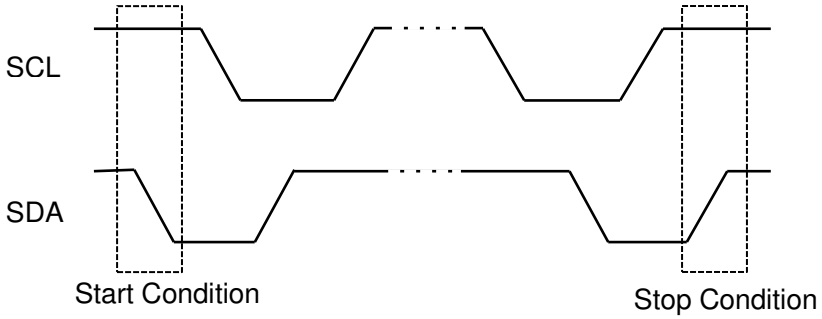


Figure 11.2. Start / Stop Conditions

11.1.3. Acknowledge

The device transmitting data will release the SDA line after transmitting one byte of data (SDA line state is “H”). The device receiving data will pull the SDA line to “L” during the next clock. This operation is called “Acknowledge”. The Acknowledge signal can be used to indicate successful data transfers.

The AK9752 will output an acknowledge signal after receiving a Start Condition and the slave address.

The AK9752 will output an acknowledge signal after receiving each byte, when the write instruction is transmitted.

The AK9752 will transmit the data stored in the selected address after outputting an acknowledge signal, when a read instruction is transmitted. Then the AK9752 will monitor the SDA line after releasing the SDA line. If the master device generates an Acknowledge instead of Stop Condition, the AK9752 transmits an 8-bit data stored in the next address. When the Acknowledge is not generated, transmitting data is terminated.

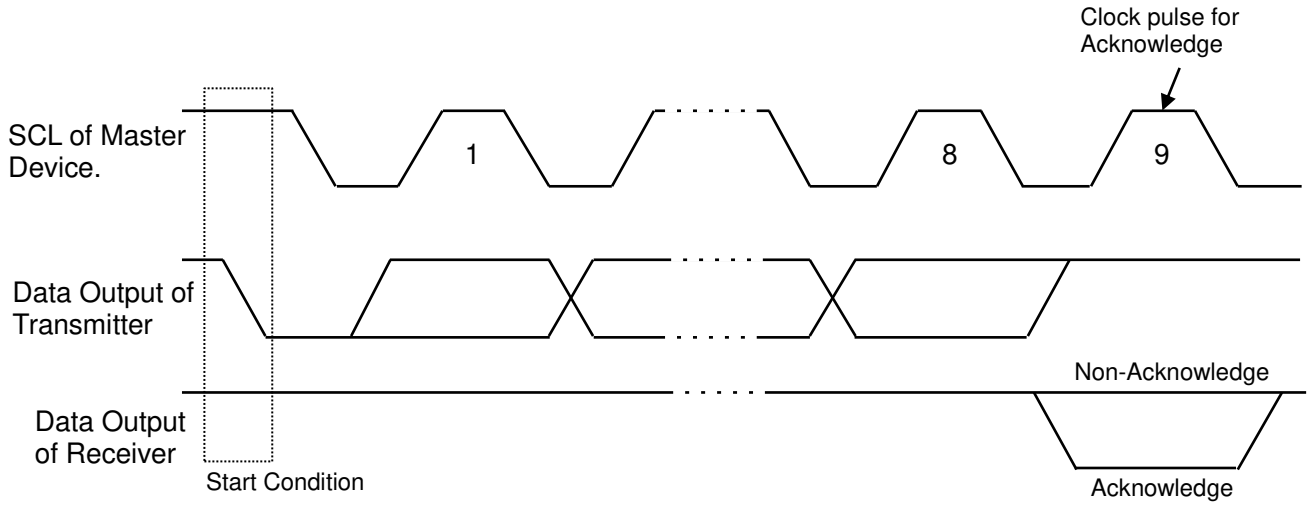


Figure 11.3. Acknowledge

11.1.4. Slave Address

The slave address of the AK9752 is fixed to 64H.

When the first one byte data including the slave address is transmitted after a Start Condition, the device, which is specified as the communicator by the slave address on bus, is selected.

After transmitting the slave address, the device that has the corresponding device address will execute a command after transmitting an Acknowledge signal. The 8-bit (Least Significant bit-LSB) of the first one byte is the R/W bit.

When the R/W bit is set to “1”, a read command is executed. When the R/W bit is set to “0”, a write command is executed.

MSB							LSB
1	1	0	0	1	0	0	R/W

Figure 11.4. Slave Address

11.1.5. Write Command

When the R/W bit set to “0”, the AK9752 executes a write operation. The AK9752 will output an Acknowledge signal and receive the second byte, after receiving a Start Condition and first one byte (slave address) in a write operation. The second byte has an MSB-first configuration, and specifies the address of the internal control register.

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0

Figure 11.5. Register Address

The AK9752 will generate an Acknowledge and receive the third byte after receiving the second byte (Register Address).

The data after the third byte are the control data. The control data consists of 8-bit and has an MSB-first configuration. The AK9752 generates an Acknowledge for each byte received. The data transfer is terminated by a Stop Condition, generated by the master device.

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

Figure11.6. Control data

Two or more bytes can be written at once. The AK9752 generates an Acknowledge and receives the next data after receiving the third byte (Control Data). When the following data is transmitted without a Stop Condition, after transmitting one byte, the internal address counter is automatically incremented, and data is written in the next address.
The automatic address increment works for the registers which set threshold of IR, threshold of Temperature Sensor, interrupt source, cut-off frequency of digital filter, and operation mode (0BH~15H). The address counter returns to address 0BH after reaching address 15H.

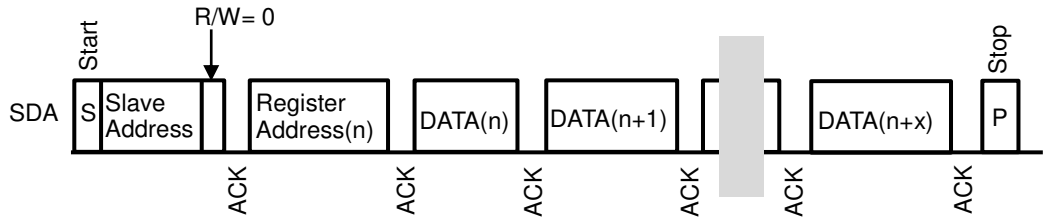


Figure 11.7. Write Operation

11.1.6. Read Command

When the R/W bit is set to “1”, the AK9752 executes a read operation. When the AK9752 transmits data from the specified address, the master device generates an Acknowledge instead of a Stop Condition and the next address data can be read out.
This automatic address increment works for the registers which store ST1, interrupt factor information, IR measurement data, Temperature Sensor measurement data, ST2(04H~0AH) and thresholds of IR, thresholds of Temperature Sensor, interrupt factor setting, cut-off frequency of digital filter, and operation mode(0BH~15H).
The address counter returns to address 04H after reaching address 0AH.
The address counter returns to address 0BH after reaching address 15H.
The AK9752 supports both current address read and random address read.

(1) Current Address Read

The AK9752 has an integrated address counter. The data specified by the counter is read out in the current address read operation. The internal address counter retains the next address which is accessed at last. For example, when the address which was accessed last is “n”, the data of address “n+1” is read out by the current address read instruction.
The AK9752 will generate an Acknowledge after receiving the slave address for a read command (R/W bit = “1”) in the current address read operation. Then the AK9752 will start to transmit the data specified by the internal address counter at the next clock, and will increment the internal address counter by one. When the AK9752 generates a Stop Condition instead of an Acknowledge after transmitting the one byte data, a read out operation is terminated.

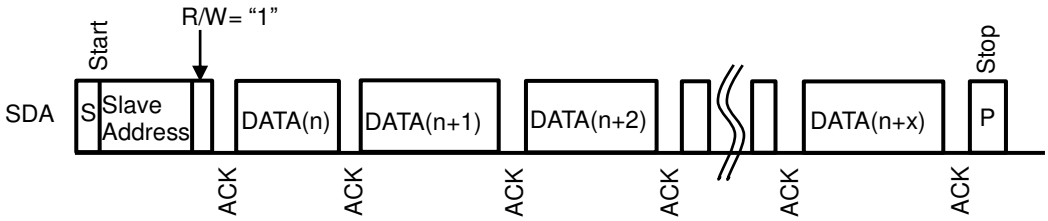


Figure 11.8. Current Address Read

(2) Random Read

Data from an arbitrary address can be read out by a random read operation. A random read requires the input of a dummy write instruction before the input of the slave address of a read instruction (R/W bit = “1”). To execute a random read, first generate a Start Condition, then input the slave address for a write instruction (R/W bit = “0”) and a read address, sequentially.
After the AK9752 generates an Acknowledge in response to this address input, generate a Start Condition and the slave address for a read instruction (R/W bit = “1”) again. The AK9752 generates an Acknowledge in response to the input of this slave address. Next, the AK9752 output the data at the specified address, then increments the internal address counter by one.
When a Stop Condition from the master device is generated in generated instead of an Acknowledge after the AK9752 outputs data, Read operation stops.

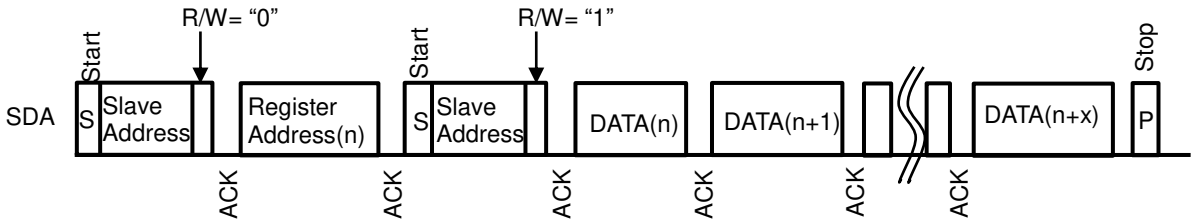


Figure 11.9. Random Read

12. Memory Map

Table 12.1. Register Map

Name	Address	Soft Reset	R/W	Data	
				Contents	bit
WIA1	00H	Disable	R	Company Code	8
WIA2	01H	Disable	R	Device ID	8
INFO1	02H	Disable	R	Information	8
INFO2	03H	Disable	R	Information	8
ST1	04H	Enable	R	Status 1	1
INTCAUSE	05H	Enable	R	Interrupt Factor Information	5
IR	06H	Enable	R	IR A/D Converted data (lower 8-bit)	8
IR	07H	Enable	R	IR A/D Converted data (upper 8-bit)	8
TMP	08H	Enable	R	Integrated Temperature Sensor data (lower 8-bit)	8
TMP	09H	Enable	R	Integrated Temperature Sensor data (upper 8-bit)	8
ST2	0AH	Enable	R	Status 2	1
THIRH	0BH	Enable	R/W	IR Upper Threshold level (lower 8-bit)	8
THIRH	0CH	Enable	R/W	IR Upper Threshold level (upper 8-bit)	8
THIRL	0DH	Enable	R/W	IR lower Threshold level (lower 8-bit)	8
THIRL	0EH	Enable	R/W	IR lower Threshold level (upper 8-bit)	8
THTMPH	0FH	Enable	R/W	Integrated Temperature Sensor Upper Threshold level (lower 8-bit)	8
THTMPH	10H	Enable	R/W	Integrated Temperature Sensor Upper Threshold level (upper 8-bit)	8
THTMPL	11H	Enable	R/W	Integrated Temperature Sensor Lower Threshold level (lower 8-bit)	8
THTMPL	12H	Enable	R/W	Integrated Temperature Sensor Lower Threshold level (upper 8-bit)	8
INTEN	13H	Enable	R/W	Interrupt Factor Setting	5
CNTL1	14H	Enable	R/W	Cut-off Frequency (Fc) Setting	5
CNTL2	15H	Enable	R/W	Operating Mode Setting	2
CNTL3	16H	Enable	R/W	Soft Reset	1

13. Registers Functional Descriptions

Table 13.1. Register Detail Map

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	WIA1	0	1	0	0	1	0	0	0
01H	WIA2	0	0	0	1	0	1	0	0
02H	INFO1	0	0	0	0	0	0	0	0
03H	INFO2	0	0	0	0	0	0	0	0
04H	ST1	1	1	1	1	1	1	1	DRDY
05H	INTCAUSE	1	1	1	IRH	IRL	TMPH	TMPL	DR
06H	IR	IR[7]	IR[6]	IR[5]	IR[4]	IR[3]	IR[2]	IR[1]	IR[0]
07H	IR	IR[15]	IR[14]	IR[13]	IR[12]	IR[11]	IR[10]	IR[9]	IR[8]
08H	TMP	TMP[7]	TMP[6]	TMP[5]	TMP[4]	TMP[3]	TMP[2]	TMP[1]	TMP[0]
09H	TMP	TMP[15]	TMP[14]	TMP[13]	TMP[12]	TMP[11]	TMP[10]	TMP[9]	TMP[8]
0AH	ST2	1	1	1	1	1	1	1	DOR
0BH	THIRH	THIRH[7]	THIRH[6]	THIRH[5]	THIRH[4]	THIRH[3]	THIRH[2]	THIRH[1]	THIRH[0]
0CH	THIRH	THIRH[15]	THIRH[14]	THIRH[13]	THIRH[12]	THIRH[11]	THIRH[10]	THIRH[9]	THIRH[8]
0DH	THIRL	THIRL[7]	THIRL[6]	THIRL[5]	THIRL[4]	THIRL[3]	THIRL[2]	THIRL[1]	THIRL[0]
0EH	THIRL	THIRL[15]	THIRL[14]	THIRL[13]	THIRL[12]	THIRL[11]	THIRL[10]	THIRL[9]	THIRL[8]
0FH	THTMPH	THTMPH[7]	THTMPH[6]	THTMPH[5]	THTMPH[4]	THTMPH[3]	THTMPH[2]	THTMPH[1]	THTMPH[0]
10H	THTMPH	THTMPH[15]	THTMPH[14]	THTMPH[13]	THTMPH[12]	THTMPH[11]	THTMPH[10]	THTMPH[9]	THTMPH[8]
11H	THTMPL	THTMPL[7]	THTMPL[6]	THTMPL[5]	THTMPL[4]	THTMPL[3]	THTMPL[2]	THTMPL[1]	THTMPL[0]
12H	THTMPL	THTMPL[15]	THTMPL[14]	THTMPL[13]	THTMPL[12]	THTMPL[11]	THTMPL[10]	THTMPL[9]	THTMPL[8]
13H	INTEN	1	1	1	IRHI	IRLI	TMPHI	TMPLI	DRI
14H	CNTL1	1	1	1	FCTMP[2]	FCTMP[1]	FCTMP[0]	FCIR[1]	FCIR[0]
15H	CNTL2	1	1	1	1	1	1	MODE[1]	MODE[0]
16H	CNTL3	1	1	1	1	1	1	1	SRST

[Functional Descriptions]

1). WIA1: Company Code (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	WIA1	0	1	0	0	1	0	0	0

One Byte fixed code as Company code of AKM.(48H)

2). WIA2: Device ID (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	WIA2	0	0	0	1	0	1	0	0

One Byte fixed code as AKM device ID. (14H)

3). INFO1: Information1 (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	INFO1	0	0	0	0	0	0	0	0

INFO1 [7:0]: Information for AKM use only.

4). INFO2: Information2 (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	INFO2	0	0	0	0	0	0	0	0

INFO2 [7:0]: Reserve

5). ST1: Status1 (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	ST1	1	1	1	1	1	1	1	DRDY
Reset		1	1	1	1	1	1	1	0

DRDY: Data Ready
"0": Normal State
"1": Data Ready
The DRDY changes to "1", when measurement data is ready to be read. This bit returns to "0", when ST2 register is read out.

6). INTCAUSE: Interrupt factor Information (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	INTCAUSE	1	1	1	IRH	IRL	TMPH	TMPL	DR
Reset		1	1	1	0	0	0	0	0

When the correspondent bit in the Interrupt Factor Setting register (INTEN) is enabled, the interrupt to the Host MCU is available. When an interruption happens, the interrupt factor is confirmed by reading out this INTCAUSE register.
INTN pin returns to “Hi-Z” when INCAUSE register is read out.

IRH: Relation between IR sensor output and the upper threshold
“0”: IR sensor does not cross the upper threshold upward.
“1”: IR sensor crosses the upper threshold upward.
In case that IRHI is set to “1” in INTEN register, IRH changes to “1” when IR sensor output IR[15:0] crosses the upper threshold THIRH[15:0] upward. Otherwise, IRH retains "0".

IRL: Relation between IR sensor output and the lower threshold
“0”: IR sensor does not cross the lower threshold downward.
“1”: IR sensor crosses the lower threshold downward.
In case that IRLI is set to “1” in INTEN register, IRL changes to “1” when IR sensor output IR[15:0] crosses the lower threshold THIRL[15:0] downward. Otherwise, IRL retains "0".

TMPH: Relation between Temperature sensor output and the upper threshold
“0”: Temperature sensor does not cross the upper threshold upward.
“1”: Temperature sensor crosses the upper threshold upward.
In case that TMPHI is set to “1” in INTEN register, TMPH changes to “1” when Temperature sensor output TMP[15:0] crosses the upper threshold THTMPH[15:0] upward. Otherwise, TMPH retains "0".

TMPL: Relation between Temperature sensor output and the lower threshold
“0”: Temperature sensor does not cross the lower threshold downward.
“1”: Temperature sensor crosses the lower threshold downward.
In case that TMPLI is set to “1” in INTEN register, TMPL changes to “1” when Temperature sensor output TMP[15:0] crosses the lower threshold THTMPL[15:0] downward. Otherwise, TMPL retains "0".

DR: Data Ready
“0”: Normal State
“1”: Data Ready
DR changes to “1” when measurement data is ready to be read out with DRI is set to “1”.

7). IR: Measurement data of IR Sensor (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	IR	IR[7]	IR[6]	IR[5]	IR[4]	IR[3]	IR[2]	IR[1]	IR[0]
07H	IR	IR[15]	IR[14]	IR[13]	IR[12]	IR[11]	IR[10]	IR[9]	IR[8]
Reset		0	0	0	0	0	0	0	0

Measurement data of IR Sensor
IR[7:0]: Lower 8-bit of output data
IR[15:8]: Upper 8-bit of output data
16-bit data is stored in 2's compliment format.

Table 13.2. Measurement data of IR Sensor

Measurement data of IR Sensor [15:0]			Output current of IR Sensor	Unit
2's compliment	Hex	Decimal		
0111 1111 1111 1111	7FFF	32767	15000 or more	pA
⋮	⋮	⋮	⋮	
0010 0111 0001 0000	2710	10000	4578	
⋮	⋮	⋮	⋮	
0000 0011 1110 1000	03E8	1000	457.8	
⋮	⋮	⋮	⋮	
0000 0000 0110 0100	0064	100	45.78	
⋮	⋮	⋮	⋮	
0000 0000 0000 0001	0001	1	0.4578	
0000 0000 0000 0000	0000	0	0	
1111 1111 1111 1111	FFFF	-1	-0.4578	
⋮	⋮	⋮	⋮	
1111 1111 1001 1100	FF9C	-100	-45.78	
⋮	⋮	⋮	⋮	
1111 1100 0001 1000	FC18	-1000	-457.8	
⋮	⋮	⋮	⋮	
1101 1000 1111 0000	D8F0	-10000	-4578	
⋮	⋮	⋮	⋮	
1000 0000 0000 0000	8001	-32767	-15000 or less	

Output current of IR Sensor (pA) = 0.4578 × Measurement data of IR Sensor (Decimal)

8). TMP: Measurement data of Temperature Sensor (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	TMP	TMP[7]	TMP[6]	TMP[5]	TMP[4]	TMP[3]	TMP[2]	TMP[1]	TMP[0]
09H	TMP	TMP[15]	TMP[14]	TMP[13]	TMP[12]	TMP[11]	TMP[10]	TMP[9]	TMP[8]
Reset		0	0	0	0	0	0	0	0

Measurement data of Integrated Temperature Sensor
TMP[7:0]: Lower 8-bit of output data
TMP[15:8]: Upper 8-bit of output data
16-bit data is stored in 2's compliment format.

Table 13.3. Measurement data of Temperature Sensor

Measurement data of Temperature Sensor [15:0]			Temperature	Unit
2's compliment	Hex	Decimal		
0111 1111 1111 1111	7FFF	32767	90 or more	ºC
⋮	⋮	⋮	⋮	
0011 0001 0101 0010	3152	12626	50	
⋮	⋮	⋮	⋮	
0000 0000 0000 0001	0001	1	25.00198	
0000 0000 0000 0000	0000	0	25	
1111 1111 1111 1111	FFFF	-1	24.99802	
⋮	⋮	⋮	⋮	
1001 0011 0111 1110	937E	-27778	-30	
⋮	⋮	⋮	⋮	
1011 1001 1000 0000	8001	-32767	-40 or less	

Indicated value of Temperature Sensor (ºC) =
0.0019837 × Measurement data of Temperature Sensor (Decimal) + 25

9). ST2: Status 2 (Read Only Register)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	ST2								DOR
Reset		1	1	1	1	1	1	1	0

Note:
ST2 register must be read out after reading out measurement data. Otherwise, measurement data would not be updated.

DOR: Data Overrun
"0": Normal State
"1": Data Overrun
DOR changes to "1" when data skipping happens, and returns to "0" after reading out ST2 register.