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DUAL EPAD® PRECISION HIGH SLEW RATE CMOS OPERATIONAL AMPLIFIER

KEY FEATURES

- **Factory pre-trimmed V_{OS}**
- **V_{OS}=25μV @ I_{OS}=0.01pA**
- **5V/μs slew rate**
- **EPAD (Electrically Programmable Analog Device)**
- **User programmable V_{OS} trimmer**
- **Rail-to-rail input/output**
- **Compatible with standard EPAD Programmer**
- **Each amplifier V_{OS} can be trimmed to a different V_{OS} level**
- **High precision through in-system circuit precision trimming**
- **Reduces or eliminates V_{OS}, PSRR, CMRR and TCV_{OS} errors**
- **System level "calibration" capability**
- **Low voltage operation**

BENEFITS

- Ready-to-use off-the-shelf standard part
- Custom automated trimming optional
- Remote controlled automated trimming
- In-System Programming capability
- No external components
- No internal clocking noise source
- Simple and cost effective
- Small package size
- Extremely small total functional volume size
- Low system implementation cost

GENERAL DESCRIPTION

The ALD2724E/ALD2724 is a dual monolithic operational amplifier with MOSFET input that has rail-to-rail input and output voltage ranges. The input voltage range and output voltage range are very close to the positive and negative power supply voltages. Typically the input voltage can be beyond positive power supply voltage V+ or the negative power supply voltage V- by up to 300mV. The output voltage swings to within 60mV of either positive or negative power supply voltages at rated load.

With high impedance load, the output voltage of the ALD2724E/ALD2724 approaches within 1mV of the power supply rails. This device is designed as an alternative to the popular J-FET input operational amplifier in applications where lower operating voltages, such as 9V battery or ±3.25V to ±5V power supplies are being used. The ALD2724E/ALD2724 offers high slew rate of 5.0V/μs.

The rail-to-rail input and output feature of the ALD2724E/ALD2724 expands signal voltage range for a given operating supply voltage and allows numerous analog serial stages to be implemented without losing operating voltage margin. The output stage is designed to drive up to 10mA into 400pF capacitive and 1.5KΩ resistive loads at unity gain and up to 4000pF at a gain of 5. Short circuit protection to either ground or the power supply rails is at approximately 15mA clamp current. Due to complementary output stage design, the output can source and sink 10mA into a load with symmetrical drive and is ideally suited for applications where push-pull voltage drive is desired.

APPLICATIONS

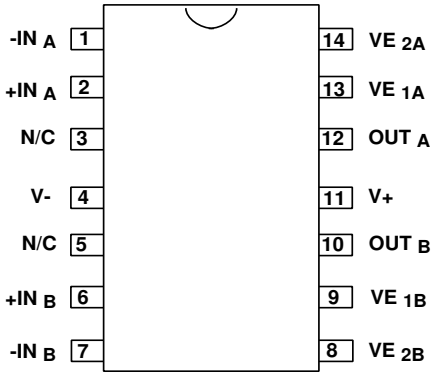
- Sensor interface circuits
- Transducer biasing circuits
- Capacitive and charge integration circuits
- Biochemical probe interface
- Signal conditioning
- Portable instruments
- High source impedance electrode amplifiers
- Precision Sample and Hold amplifiers
- Precision current to voltage converter
- Error correction circuits
- Sensor compensation circuits
- Precision gain amplifiers
- Periodic In-system calibration
- System output level shifter

ORDERING INFORMATION

Operating Temperature Range		
0°C to +70°C	0°C to +70°C	-55°C to +125°C
14-Pin Small Outline Package (SOIC)	14-Pin Plastic Dip Package	14-Pin CERDIP Package
ALD2724ESB ALD2724SB	ALD2724EPB ALD2724PB	ALD2724EDB ALD2724DB

* Contact factory for high temperature versions.

PIN CONFIGURATION



TOP VIEW
SB, PB, DB PACKAGES

* N/C Pins are internally connected. Do not connect externally.

FUNCTIONAL DESCRIPTION

The ALD2724E/ALD2724 uses EPADs as in-circuit elements for trimming of offset voltage bias characteristics. Each ALD2724E/ALD2724 has a pair of EPAD-based circuits connected such that one circuit is used to adjust V_{OS} in one direction and the other circuit is used to adjust V_{OS} in the other direction. While each of the EPAD devices is a monotonically adjustable programmable device, the V_{OS} of the ALD2724E can be adjusted many times in both directions. Once programmed, the set V_{OS} levels are stored permanently, even when the device power is removed.

Functional Description of ALD2724E

The ALD2724E is pre-programmed at the factory under standard operating conditions for minimum equivalent input offset voltage. It also has a guaranteed offset voltage program range, which is ideal for applications that require electrical offset voltage programming.

The ALD2724E is an operational amplifier that can be trimmed with user application-specific programming or in-system programming conditions. User application-specific circuit programming refers to the situation where the Total Input Offset Voltage of the ALD2724E can be trimmed with the actual intended operating conditions.

For example, an application circuit may have +5V and -5V power supplies, and the operational amplifier input is biased at +1V, and an average operating temperature at +85°C. The circuit can be wired up to these conditions within an environmental chamber with the ALD2724E inserted into a test socket connected to this circuit while it is being electrically trimmed. Any error in V_{OS} due to these bias conditions can be automatically zeroed out. The Total V_{OS} error is now limited only by the adjustable range and the stability of V_{OS}, and the input noise voltage of the operational amplifier. Therefore, this Total V_{OS} error now includes V_{OS} as V_{OS} is traditionally specified; plus the V_{OS} error contributions from PSRR, CMRR, TCV_{OS}, and noise. Typically this total V_{OS} error (V_{OST}) is approximately ±25μV for the ALD2724E.

In-System Programming refers to the condition where the EPAD adjustment is made after the ALD2724E has been inserted into a circuit board. In this case, the circuit design must provide for the ALD2724E to operate in normal mode and in programming mode. One of the benefits of in-system programming is that not only is the ALD2724E offset voltage from operating bias conditions accounted for, any residual errors introduced by other circuit components, such as resistor or sensor induced voltage errors, can also be corrected. In this way, the “in-system” circuit output can be adjusted to a desired level, eliminating the need for another trimming function.

Functional Description of ALD2724

The ALD2724 is pre-programmed at the factory under standard operating conditions for minimum equivalent input offset voltage. The ALD2724 offers similar programmable features as the ALD2724E, but with a more limited offset voltage program range. In is intended for standard operational amplifier applications, where little or no electrical porggramming by the user is necessary.

USER PROGRAMMABLE V_{OS} FEATURE

Each ALD2724E/ALD2724 has four additional pins, compared to a conventional dual operational amplifier which has eight pins. These four additional pins are named VE1A, VE2A for op amp A and VE1B, VE2B for op amp B. Each of these pins VE1A, VE2A, VE1B, VE2B (represented by VExx) are connected to a separate, internal offset bias circuit. VExx pins have initial internal bias voltage values of approximately 1V to 2V. The voltage on these pins can be programmed using the ALD E100 EPAD Programmer and the appropriate Adapter Module. The useful programming range of voltages on VExx pins are 1V to 4V.

VExx pins are programming pins, used during electrical programming mode to inject charge into the internal EPADs. Increasing voltage on VE1A/VE1B decreases the offset voltage whereas increasing voltage on VE2A/VE2B increases the offset voltage of op amp A and op amp B, respectively. The injected charge is then permanently stored. After programming, VExx pins must be left open in order for these voltages to remain at the programmed levels.

During programming, voltages on VExx pins are increased incrementally to program the offset voltage of the operational amplifier to the desired V_{OS}. Note that desired V_{OS} can be any value within the offset voltage programmable ranges, and can be equal zero, a positive value or a negative value. This V_{OS} value can also be reprogrammed to a different value at a later time, provided that the useful VE1x or VE2x programming voltage range has not been exceeded. VExx pins can also serve as capacitively coupled input pins.

Internally, VE1 and VE2 are programmed and connected differentially. Temperature drift effects between the two internal offset bias circuits cancel each other and introduce less net temperature drift coefficient change than offset voltage trimming techniques such as offset adjustment with an external trimmer potentiometer.

While programming, V+, VE1 and VE2 pins may be alternately pulsed with 12V (approximately) pulses generated by the EPAD Programmer. In-system programming requires the ALD2724E application circuit to accommodate these programming pulses. This can be accomplished by adding resistors at certain appropriate circuit nodes. For more information, see Application Note AN1700.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V+ 10.6V
Differential input voltage range -0.3V to V+ +0.3V
Power dissipation 600 mW
Operating temperature range SB, PB packages 0°C to +70°C
DB package -55°C to +125°C
Storage temperature range -65°C to +150°C
Lead temperature, 10 seconds +260°C
CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C V_S = ±5.0V unless otherwise specified

Parameter	Symbol	2724E Min	2724E Typ	2724E Max	2724 Min	2724 Typ	2724 Max	Unit	Test Conditions
Supply Voltage	V_S V+	±3.25 6.5		±5.0 10.0	±3.25 6.5		±5.0 10.0	V V	Dual Supply Single Supply
Initial Input Offset Voltage[1]	$V_{OS\,i}$		25	100		40	150	µV	$R_S \le 100K\Omega$
Offset Voltage Program Range [2]	ΔV_{OS}	±5	±7		±0.5	±2		mV	
Programmed Input Offset Voltage Error [3]	V_{OS}		25	100		40	150	µV	At user specified target offset voltage
Total Input Offset Voltage [4]	V_{OST}		25	100		40	150	µV	At user specified target offset voltage
Input Offset Current [5]	I_{OS}		0.01	10 240		0.01	10 240	pA pA	T_A = 25°C 0°C ≤ T_A ≤ +70°C
Input Bias Current [5]	I_B		0.01	10 240		0.01	10 240	pA pA	T_A = 25°C 0°C ≤ T_A ≤ +70°C
Input Voltage Range [6]	V_{IR}	-0.3 -2.8		5.3 +2.8	-0.3 -2.8		5.3 +2.8	V V	V+ = +5V V_S = ±2.5V
Input Resistance	R_{IN}		10^{14}			10^{14}		Ω	
Input Offset Voltage Drift [7]	TCV_{OS}		5			5		µV/°C	$R_S \le 100K\Omega$
Initial Power Supply Rejection Ratio [8]	$PSRR_i$		85			85		dB	$R_S \le 100K\Omega$
Initial Common Mode Rejection Ratio [8]	$CMRR_i$		90			90		dB	$R_S \le 100K\Omega$
Large Signal Voltage Gain	A_V		150			150		V/mV V/mV	R_L =10KΩ 0°C ≤ T_A ≤ +70°C
Output Voltage Range	V_O low V_O high	4.99	-4.998 4.998	-4.99	4.99	-4.998 4.998	-4.99	V V	R_L =1MΩ V =5V 0°C ≤ T_A ≤ +70°C
	V_O low V_O high	4.90	-4.96 4.95	-4.90	4.90	-4.96 4.95	-4.90	V V	R_L =100KΩ 0°C ≤ T_A ≤ +70°C
Output Short Circuit Current	I_{SC}		15			15		mA	

* NOTES 1 through 9, see section titled "Definitions and Design Notes".

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

T_A = 25°C V_S = ±5.0V unless otherwise specified

Parameter	Symbol	2724E			2724			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Supply Current	I_S		5.0	6.5		5.0	6.5	mA	V_{IN} = 0V No Load
Power Dissipation	P_D			65			65	mW	V_S = ±2.5V
Input Capacitance	C_{IN}		1			1		pF	
Maximum Load Capacitance	C_L		400 4000			400 4000		pF pF	Gain = 1 Gain = 5
Equivalent Input Noise Voltage	e_n		26			26		nV/√Hz	f = 1KHz
Equivalent Input Noise Current	i_n		0.6			0.6		fA/√Hz	f =10Hz
Bandwidth	B_W		2.1			2.1		MHz	
Slew Rate	S_R		5.0			5.0		V/µs	A_V = +1 R_L = 2KΩ
Rise time	t_r		0.1			0.1		µs	R_L = 2KΩ
Overshoot Factor			15			15		%	R_L=2KΩ C_L=100pF
Settling Time	t_S		2			2		µs	0.1% A_V = -1 R_L= 5KΩ C_L = 50pF
Channel Separation	CS		140			140		dB	A_V = 100

T_A = 25°C V_S = ±5.0V unless otherwise specified

Parameter	Symbol	2724E			2724			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Average Long Term Input Offset Voltage Stability [9]	$\frac{\Delta V_{OS}}{\Delta \text{ time}}$		0.02			0.02		µV/ 1000 hrs	
Initial VE Voltage	$VE1_i$, $VE2_i$		1.4			2.5		V	
Programmable Change of VE Range	ΔVE1, ΔVE2	1.5	2.0			0.5		V	
Programmed VE Voltage Error	e(VE1-VE2)		0.1			0.1		%	
VE Pin Leakage Current	i_{eb}		-5			-5		µA	

* NOTES 1 through 9, see section titled "Definitions and Design Notes".

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

$V_S = \pm 5.0V$ $-55°C \leq T_A \leq +125°C$ unless otherwise specified

Parameter	Symbol	2724E			2724			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Initial Input offset Voltage	$V_{OS\,i}$		0.7			0.7		mV	$R_S \leq 100K\Omega$
Input Offset Current	I_{OS}			2.0			2.0	nA	
Input Bias Current	I_B			2.0			2.0	nA	
Initial Power Supply Rejection Ratio [8]	$PSRR_i$		85			85		dB	$R_S \leq 100K\Omega$
Initial Common Mode Rejection Ratio [8]	$CMRR_i$		97			97		dB	$R_S \leq 100K\Omega$
Large Signal Voltage Gain	A_V	10	25		10	25		V/mV	$R_L = 10K\Omega$
Output Voltage Range	V_O low V_O high	 4.8	-4.9 4.9	-4.8	 4.8	-4.9 4.9	-4.8	V V	$R_L = 10K\Omega$

DEFINITIONS AND DESIGN NOTES:

1. Initial Input Offset Voltage is the initial offset voltage of the ALD2724E/ALD2724 operational amplifier when shipped from the factory. The device has been pre-programmed and tested for programmability.

2. Offset Voltage Program Range is the range of adjustment of user specified target offset voltage. This is typically an adjustment in either the positive or the negative direction of the input offset voltage from an initial input offset voltage. The input offset programming pins, VE1A/VE1B or VE2A/VE2B, change the input offset voltage in the negative or positive direction, for each of the amplifiers, A or B respectively. User specified target offset voltage can be any offset voltage within this programming range.

3. Programmed Input Offset Voltage Error is the final offset voltage error after programming when the Input Offset Voltage is at target Offset Voltage. This parameter is sample tested.

4. Total Input Offset Voltage is the same as Programmed Input Offset Voltage, corrected for system offset voltage error. Usually this is an all inclusive system offset voltage, which also includes offset voltage contributions from input offset voltage, PSRR, CMRR, TCV_{OS} and noise. It can also include errors introduced by external components, at a system level. Programmed Input Offset Voltage and Total Input Offset Voltage is not necessarily zero offset voltage, but an offset voltage set to compensate for other system errors as well. This parameter is sample tested.

5. The Input Offset and Bias Currents are essentially input protection diode reverse bias leakage currents. This low input bias current assures that the analog signal from the source will not be distorted by it. For applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

6. Input Voltage Range is determined by two parallel complementary input stages that are summed internally, each stage having a separate input offset voltage. While Total Input Offset Voltage can be trimmed to a desired target value, it is essential to note that this trimming occurs at only one user selected input bias voltage. Depending on the selected input bias voltage relative to the power supply voltages, offset voltage trimming may affect one or both input stages. For the ALD2724E/ALD2724, the switching point between the two stages occurs at approximately 1.5V above negative supply voltage.

7. Input Offset Voltage Drift is the average change in Total Input Offset Voltage as a function of ambient temperature. This parameter is sample tested.

8. Initial PSRR and initial CMRR specifications are provided as reference information. After programming, error contribution to the offset voltage from PSRR and CMRR is set to zero under the specific power supply and common mode conditions, and becomes part of the Programmed Input Offset Voltage Error.

9. Average Long Term Input Offset Voltage Stability is based on input offset voltage shift through operating life test at 125°C extrapolated to T_A = 25°C, assuming activation energy of 1.0eV. This parameter is sample tested.

ADDITIONAL DESIGN NOTES:

A. The ALD2724E/ALD2724 is internally compensated for unity gain stability using a novel scheme which produces a single pole role off in the gain characteristics while providing more than 70 degrees of phase margin at unity gain frequency. A unity gain buffer using the ALD2724E/ALD2724 will typically drive 400pF of external load capacitance.

B. The ALD2724E/ALD2724 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail-to-rail input common mode voltage range. The switching point between the two differential stages is 1.5V above negative supply voltage. For applications such as inverting amplifiers or non-inverting amplifiers with a gain larger than 2.5 (5V operation), the common mode voltage does not make excursions below this switching point. However, this switching does take place if the operational amplifier is connected as a rail-to-rail unity gain buffer and the design must allow for input offset voltage variations.

C. The output stage consists of class AB complementary output drivers. The oscillation resistant feature, combined with the rail-to-rail input and output feature, makes the ALD2724E/ALD2724 an effective analog signal buffer for high source impedance sensors, transducers, and other circuit networks.

D. The ALD2724E/ALD2724 has static discharge protection. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. The user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages not to exceed 0.3V of the power supply voltage levels.

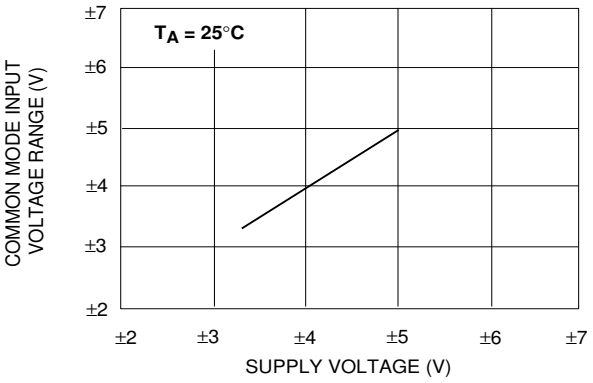
E. VExx are high impedance terminals, as the internal bias currents are set very low to a few microamperes to conserve power. For some applications, these terminals may need to be shielded from external coupling sources. For example, digital signals running nearby may cause unwanted offset voltage fluctuations. Care during the printed circuit board layout, to place ground traces around these pins and to isolate them from digital lines, will generally eliminate such coupling effects. In addition, optional decoupling capacitors of 1000pF or greater value can be added to VExx terminals.

F. The ALD2724E/ALD2724 is designed for use in low voltage, micropower circuits. The maximum operating voltage during normal operation should remain below 10V at all times. Care should be taken to insure that the application in which the device is used does not experience any positive or negative transient voltages that will cause any of the terminal voltages to exceed this limit.

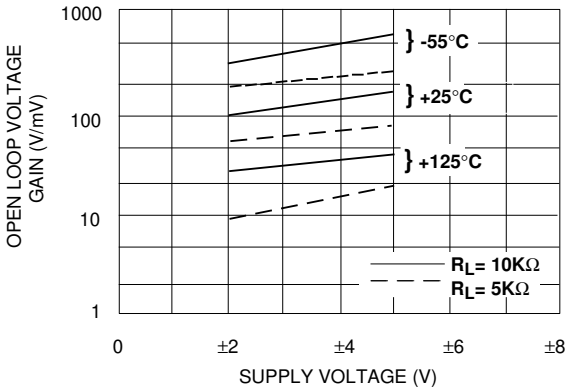
G. All inputs or unused pins except VExx pins should be connected to a supply voltage such as Ground so that they do not become floating pins, since input impedance at these pins is very high. If any of these pins are left undefined, they may cause unwanted oscillation or intermittent excessive current drain. As these devices are built with CMOS technology, normal operating and storage temperature limits, ESD and latchup handling precautions pertaining to CMOS device handling should be observed.

TYPICAL PERFORMANCE CHARACTERISTICS

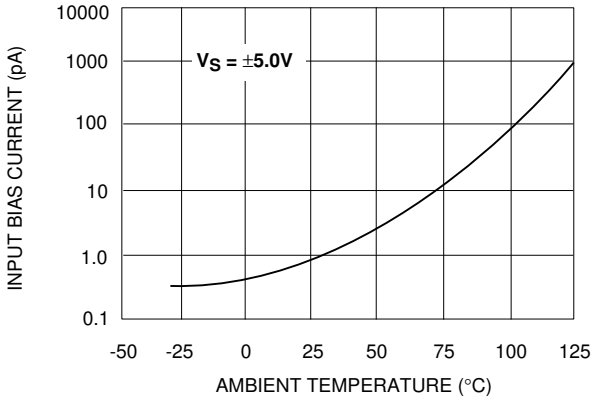
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



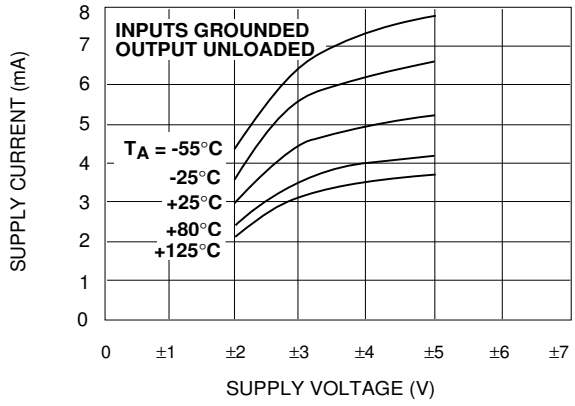
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



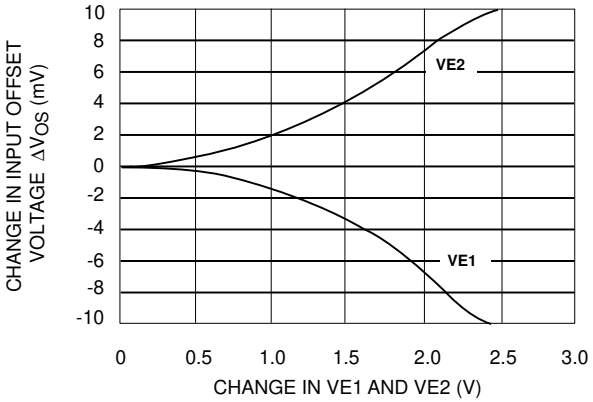
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



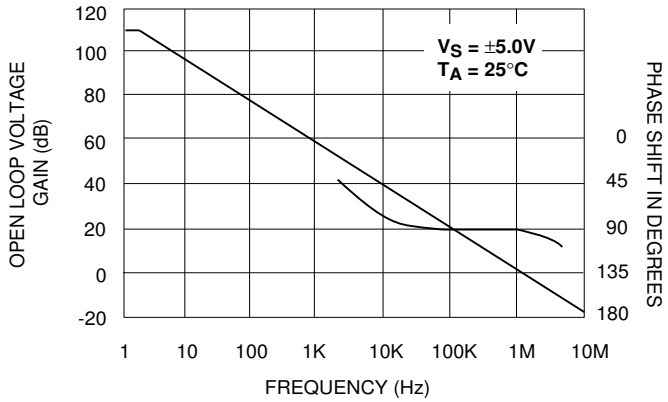
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



ADJUSTMENT IN INPUT OFFSET VOLTAGE AS A FUNCTION OF CHANGE IN VE1 AND VE2

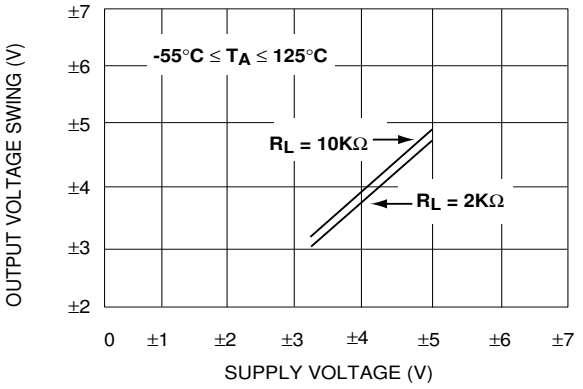


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

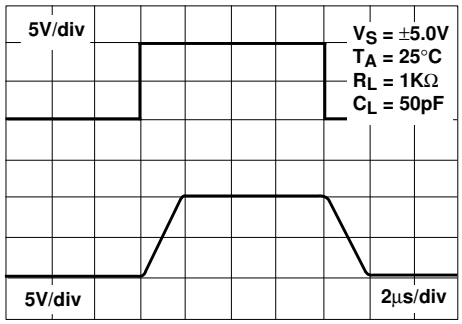


TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

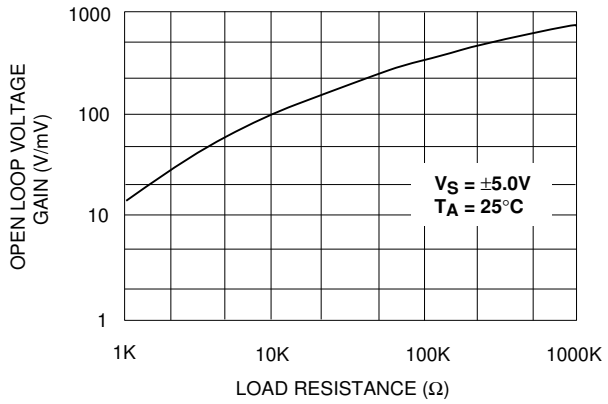
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



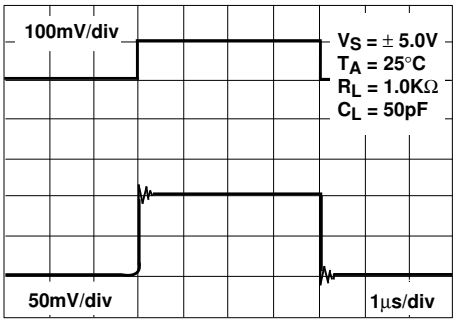
LARGE - SIGNAL TRANSIENT RESPONSE



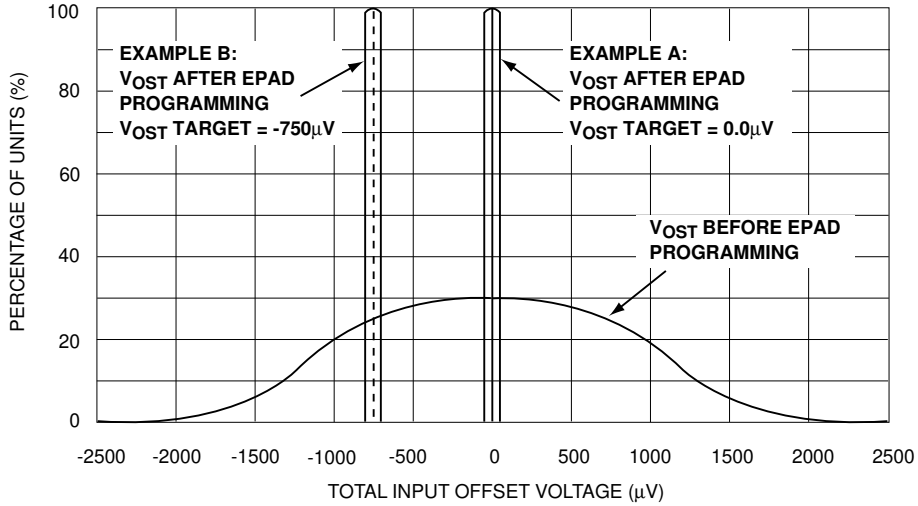
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



SMALL - SIGNAL TRANSIENT RESPONSE

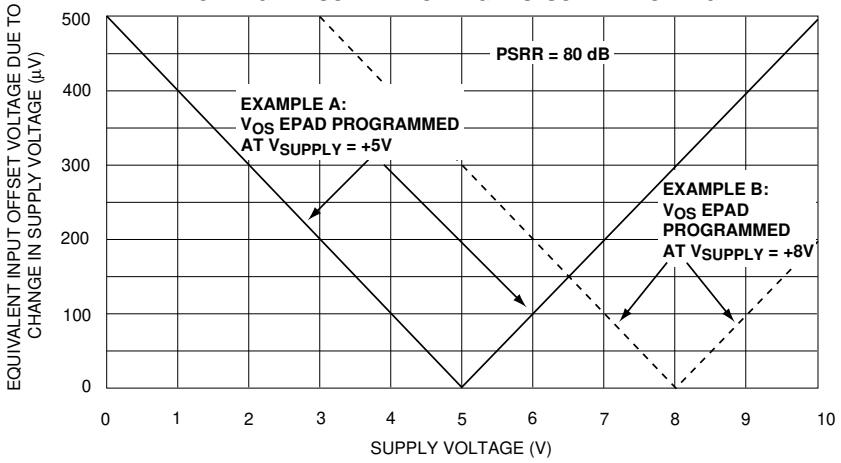


DISTRIBUTION OF TOTAL INPUT OFFSET VOLTAGE BEFORE AND AFTER EPAD PROGRAMMING

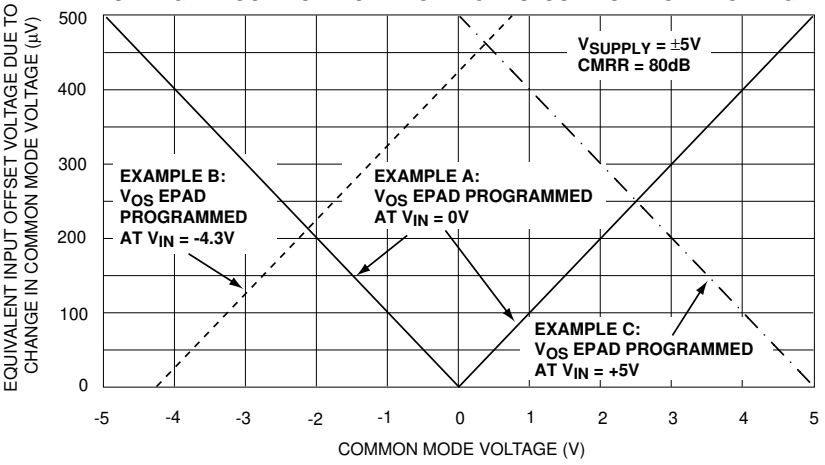


TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

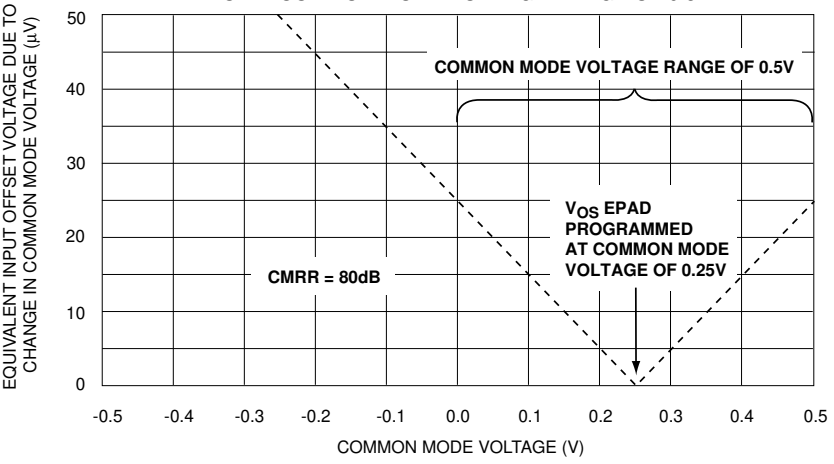
TWO EXAMPLES OF EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN SUPPLY VOLTAGE vs. SUPPLY VOLTAGE



THREE EXAMPLES OF EQUIVALENT INPUT OFFSET VOLTAGE DUE TO CHANGE IN COMMON MODE VOLTAGE vs. COMMON MODE VOLTAGE



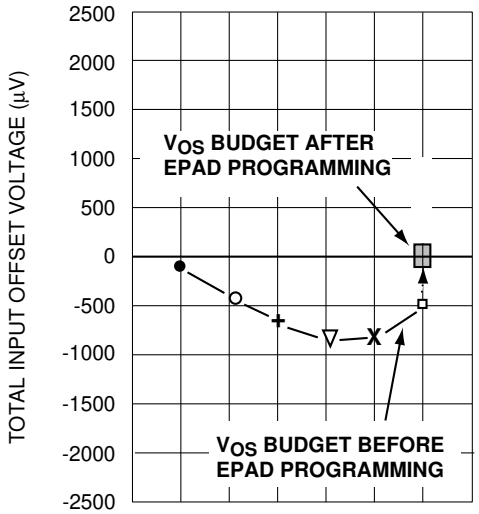
EXAMPLE OF MINIMIZING EQUIVALENT INPUT OFFSET VOLTAGE FOR A COMMON MODE VOLTAGE RANGE OF 0.5V



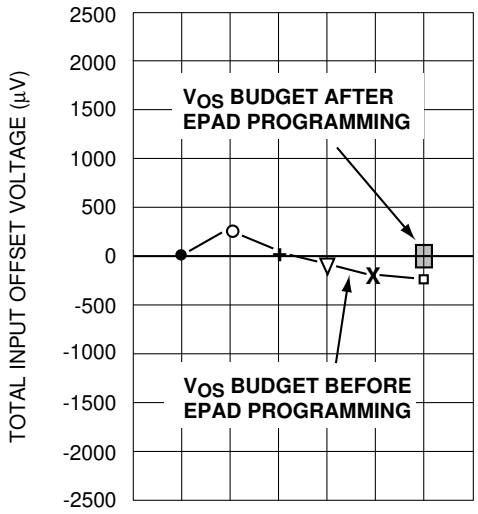
TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

APPLICATION SPECIFIC / IN-SYSTEM PROGRAMMING

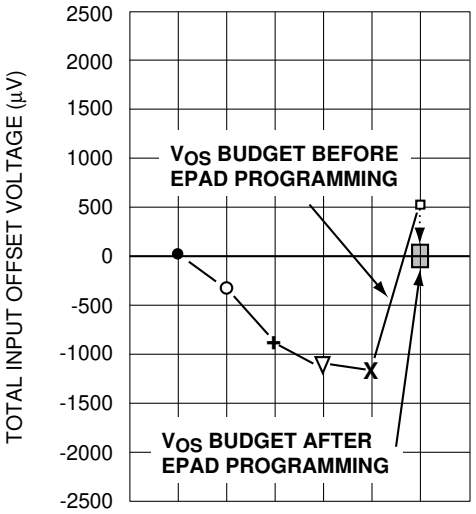
Examples of applications where accumulated total input offset voltage from various contributing sources is minimized under different sets of user-specified operating conditions



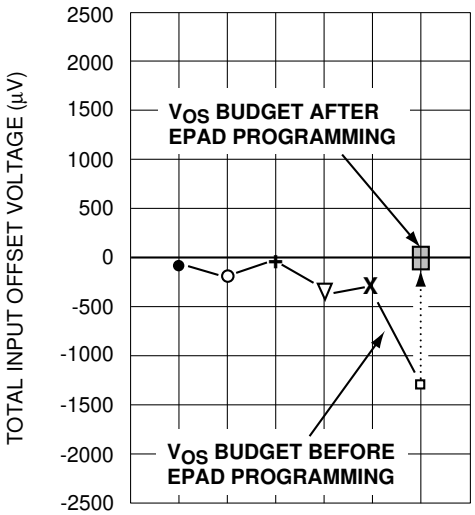
EXAMPLE A



EXAMPLE B



EXAMPLE C

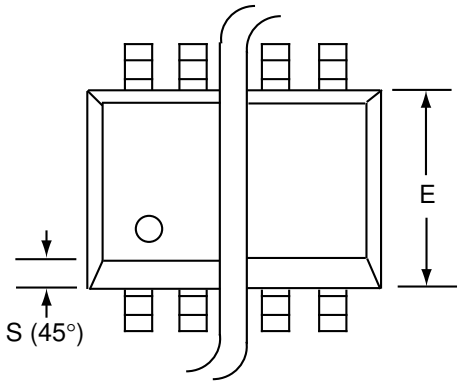


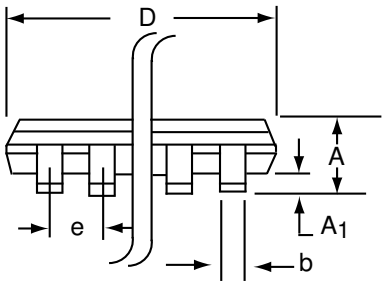
EXAMPLE D

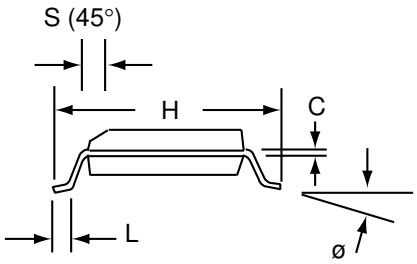
- ● Device input V_{OS}
- ○ PSRR equivalent V_{OS}
- \+ CMRR equivalent V_{OS}
- ▽ T_A equivalent V_{OS}
- X Noise equivalent V_{OS}
- ▫ External Error equivalent V_{OS}
- ▮ Total Input V_{OS} after EPAD Programming

SOIC-14 PACKAGE DRAWING

14 Pin Plastic SOIC Package



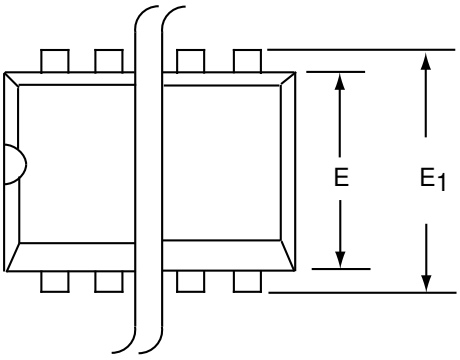


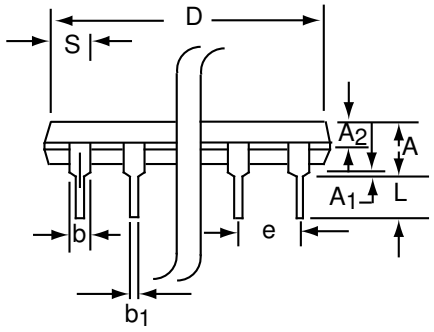


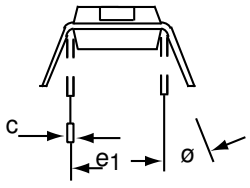
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-14	8.55	8.75	0.336	0.345
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-14 PACKAGE DRAWING

14 Pin Plastic DIP Package



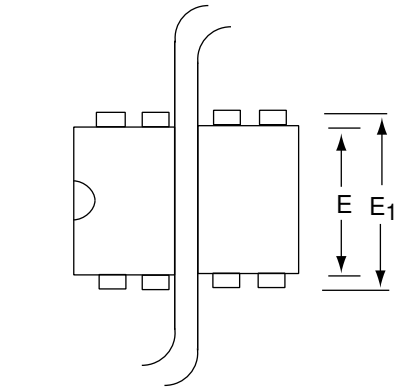


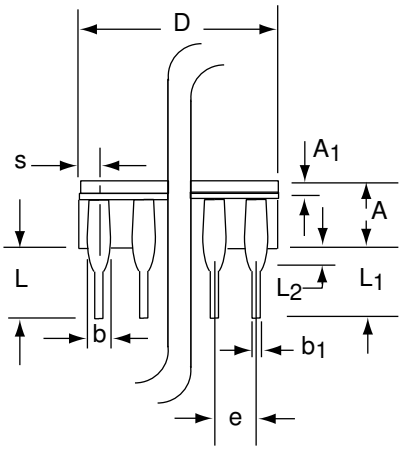


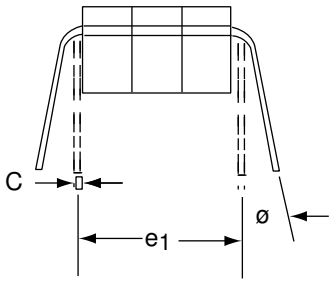
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-14	17.27	19.30	0.680	0.760
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-14	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°

CERDIP-14 PACKAGE DRAWING

14 Pin CERDIP Package







Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A_1	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b_1	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-14	--	19.94	--	0.785
E	5.59	7.87	0.220	0.310
E_1	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	--	0.125	--
L_2	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°