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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





**QUAD PRECISION CMOS VOLTAGE COMPARATOR WITH PUSH-PULL DRIVER**

**GENERAL DESCRIPTION**

The ALD4302A/ALD4302 is a monolithic high performance quad voltage comparator built with advanced silicon gate CMOS technology. It features very high typical input impedance of  $10^{12}\Omega$ ; low input bias current of 10pA; fast response time of 120ns; very low power dissipation of 150µA per comparator; and single (+5V) or dual ( $\pm 5V$ ) power supply operation.

The input voltage range includes ground, making this comparator ideal for single supply low level signal detection with high source impedance. The outputs can source and sink current, allowing application flexibility, and can be used in either wired-OR connection without pull up resistor or push-pull configuration. The ALD4302A/ALD4302 can be used in wired-OR connections with other open drain circuits such as the ALD2301 and ALD2303 voltage comparators.

The ALD4302A/ALD4302 is ideal for a great variety of precision voltage comparator applications, especially low level signal detection circuits requiring low standby power, yet retaining high output current capability.

**FEATURES**

- Guaranteed to drive 200Ω loads
- Fanout of 30LS TTL loads
- Low supply current of 150µA each comparator
- Extremely low input bias currents -- typically 10pA
- Virtually eliminates source impedance effects
- Low operating supply voltage of 4V to 10V
- Single (+5V) and dual supply ( $\pm 5V$ ) operation
- High speed for both large and small signals - 120ns for TTL inputs and 400ns for 5mV overdrive
- CMOS, NMOS and TTL compatible
- Push-pull outputs
- High output sinking current -- typically 60mA
- Low supply current spikes
- High gain -- 100V/mV

**ORDERING INFORMATION ("L" suffix for lead free version)**

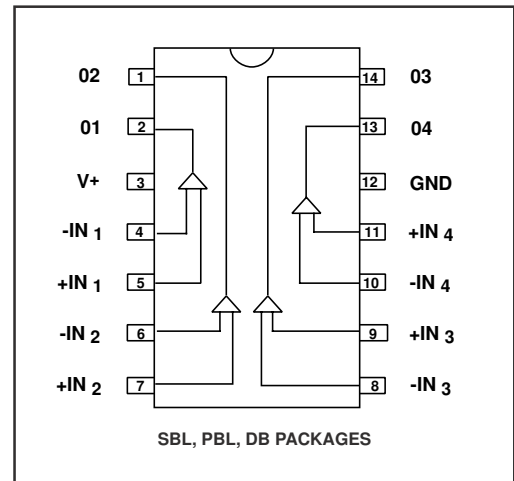
Operating Temperature Range *		
0°C to +70°C	0°C to +70°C	-55°C to +125°C
14-Pin Small Outline Package (SOIC)	14-Pin Plastic Dip Package	14-Pin CERDIP Package
ALD4302ASBL	ALD4302APBL	ALD4302ADB
ALD4302SBL	ALD4302PBL	ALD4302DB

\* Contact factory for leaded (non-RoHS) or high temperature versions.

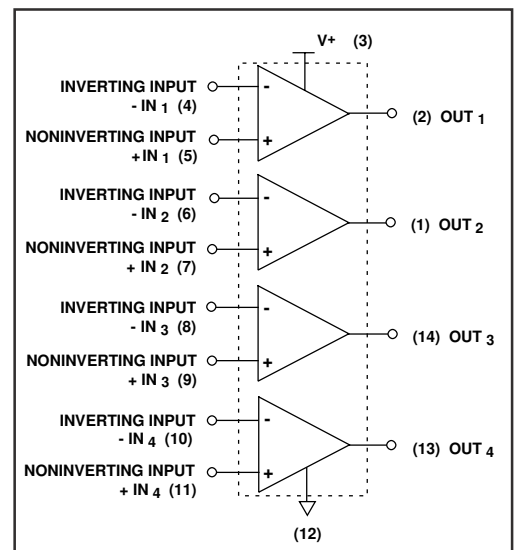
**APPLICATIONS**

- MOSFET driver
- High source impedance voltage comparison circuits
- Multiple limit window comparator
- Power supply voltage monitor
- Photo-detector sensor circuit
- High speed LED driver
- Oscillators
- Battery operated instruments
- Remote signal detection
- Multiple relay drivers

**PIN CONFIGURATION**



**BLOCK DIAGRAM**



## ABSOLUTE MAXIMUM RATINGS

Supply voltage, $V_+$	_____	10.6V	
Differential input voltage range	_____	-0.3V to $V_+$ +0.3V	
Power dissipation	_____	600 mW	
Operating temperature range	SBL, PBL packages	_____	0°C to +70°C
	DB package	_____	-55°C to +125°C
Storage temperature range	_____	-65°C to +150°C	
Lead temperature, 10 seconds	_____	+260°C	

## OPERATING ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$   $V_+ = +5\text{V}$  unless otherwise specified

Parameter	Symbol	4302A			4302			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Supply Voltage	$V_S$	$\pm 2$		$\pm 5$	$\pm 2$		$\pm 5$	V	Dual Supply Single Supply
	$V_+$	4		10	4		10	V	
Supply Current	$I_S$		600	1000		600	1000	$\mu\text{A}$	$R_{LOAD} = \infty$
Voltage Gain	$A_{VD}$	30	100		30	100		V/mV	$R_{LOAD} \geq 15\text{K}\Omega$
Input Offset Voltage	$V_{OS}$			5			10	mV	$R_{LOAD} = 1.5\text{K}\Omega$
Input Offset Current <sup>1</sup>	$I_{OS}$		10	200 800		10	200 800	pA	
Input Bias Current <sup>1</sup>	$I_B$		10	200 1000		10	200 1000	pA	0°C $\leq T_A \leq 70^\circ\text{C}$
Common Mode Input Voltage Range <sup>2</sup>	$V_{ICR}$	-0.3		$V_+ - 1.5$	-0.3		$V_+ - 1.5$	V	0°C $\leq T_A \leq 70^\circ\text{C}$
Low Level Output Voltage	$V_{OL}$		0.18	0.4		0.18	0.4	V	$I_{SINK} = 12\text{mA}$ $V_{INPUT} = 1\text{V}$ Differential
Low Level Output Current	$I_{OL}$	24	60		24	60		mA	$V_{OL} = 1.0\text{V}$
High Level Output Voltage	$V_{OH}$	3.5	4.5		3.5	4.5		V	$I_{OH} = -2\text{mA}$
Response Time <sup>2</sup>	$t_{RP}$		400			400		ns	$R_L = 5.1\text{K}\Omega$ $C_L = 15\text{pF}$ 100mV Input Step/5mV Overdrive
			120			120		ns	$R_L = 5.1\text{K}\Omega$ $C_L = 15\text{pF}$ TTL- Level Input Step

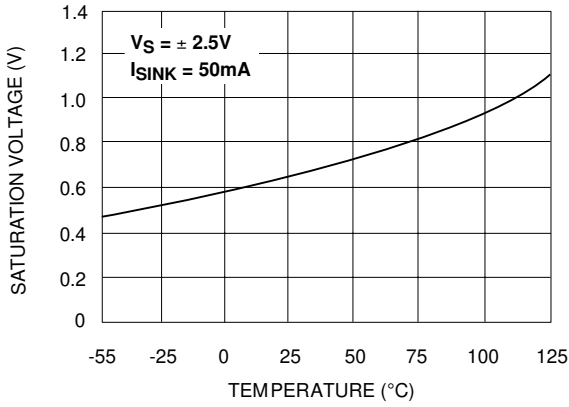
Notes: <sup>1</sup> Consists of junction leakage currents

<sup>2</sup> Sample tested parameters

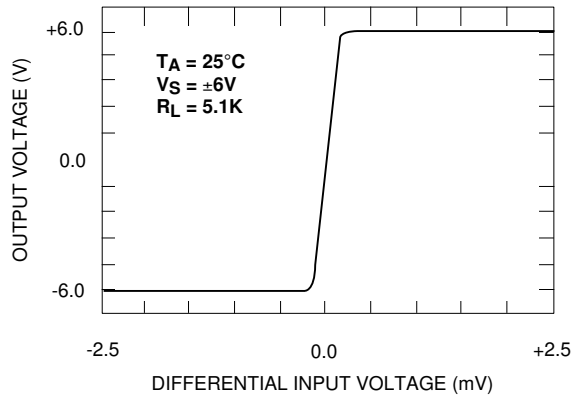


# TYPICAL PERFORMANCE CHARACTERISTICS

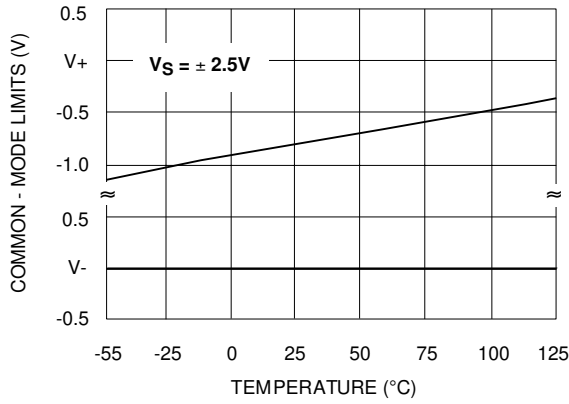
**SATURATION VOLTAGE vs. TEMPERATURE**



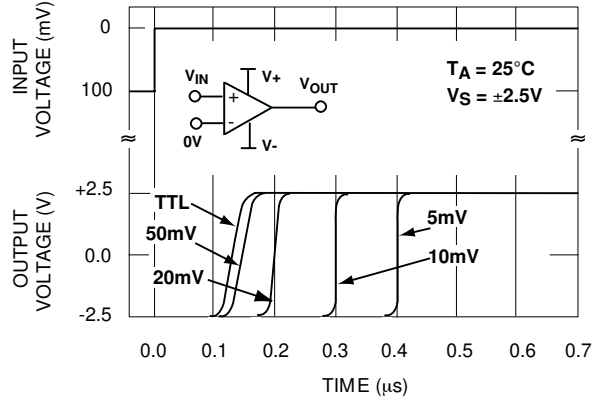
**TRANSFER FUNCTION**



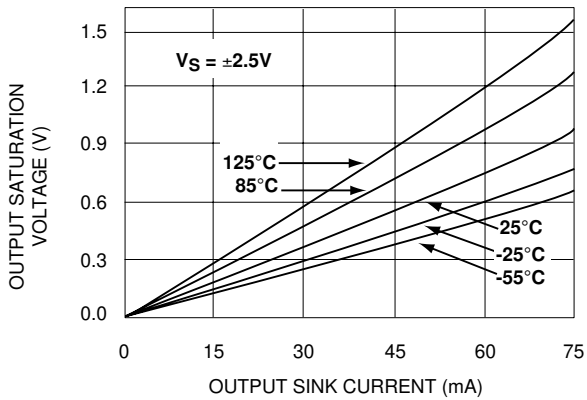
**COMMON - MODE VOLTAGE REFERRED TO SUPPLY VOLTAGE**



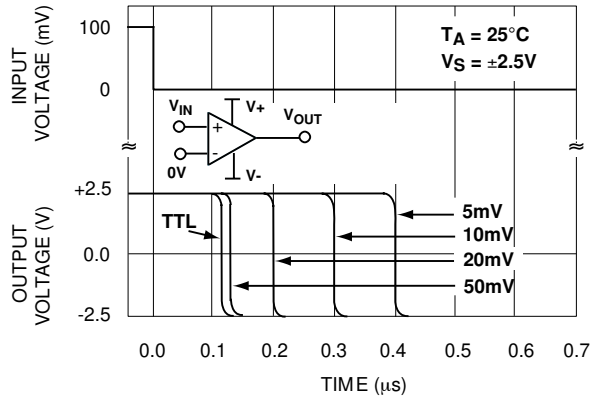
**RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES**



**SATURATION VOLTAGE vs. SINK CURRENT**

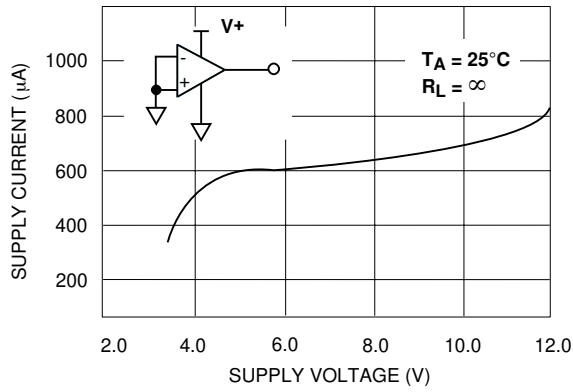


**RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES**

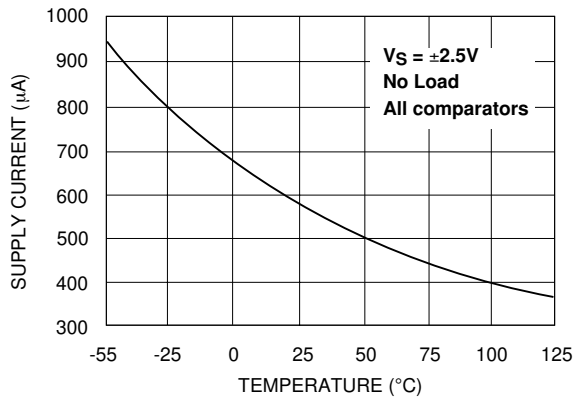


## TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

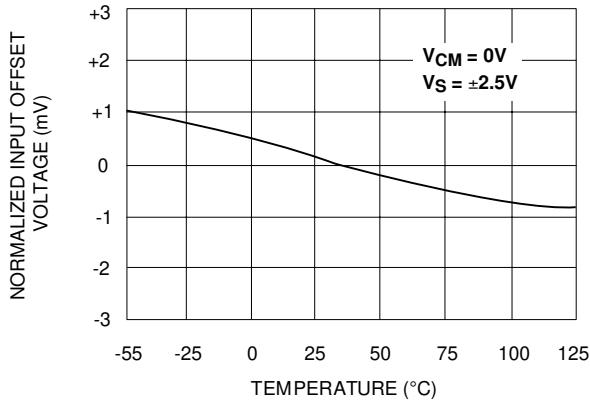
**TOTAL SUPPLY CURRENT vs. TOTAL SUPPLY VOLTAGE**



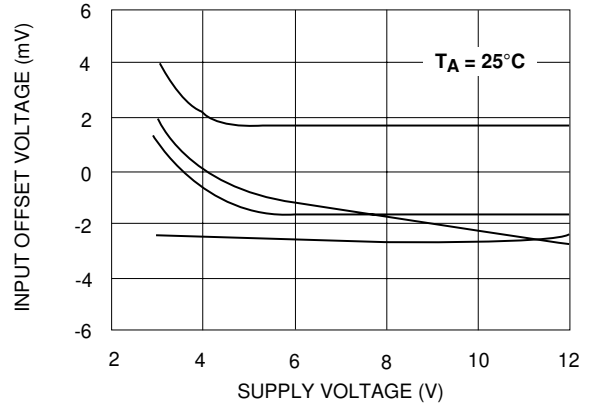
**SUPPLY CURRENT vs. TEMPERATURE**



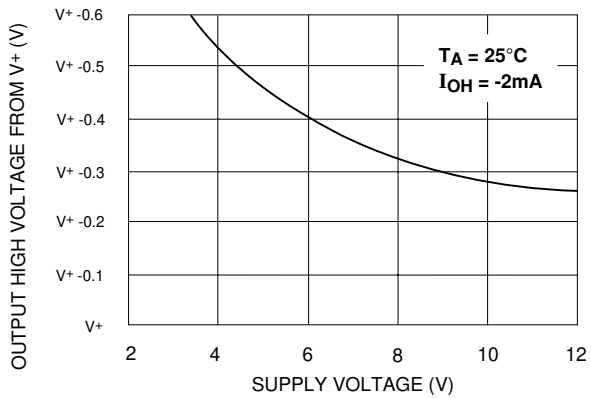
**NORMALIZED INPUT OFFSET VOLTAGE vs. TEMPERATURE**



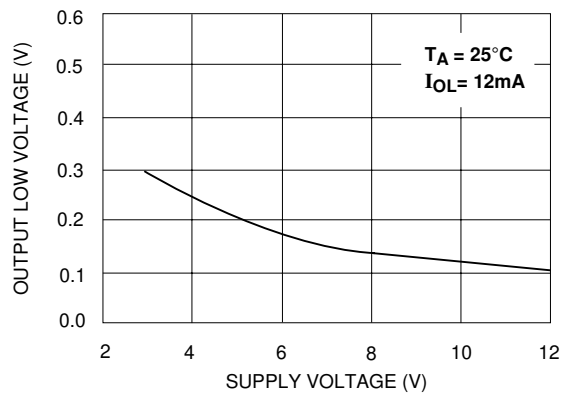
**INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE REPRESENTATIVE SAMPLES**



**OUTPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE**

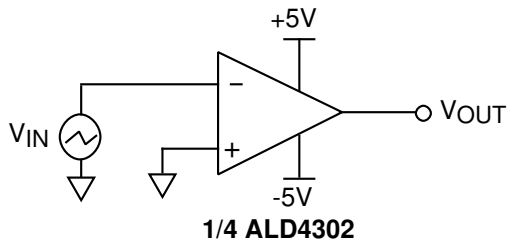


**OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE**

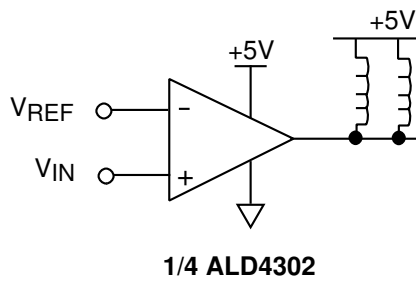


## TYPICAL APPLICATIONS

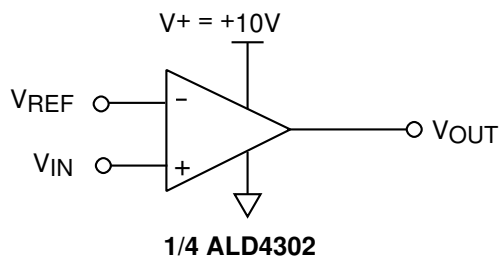
ZERO CROSSING DETECTOR



MULTIPLE RELAY DRIVE



VOLTAGE LEVEL TRANSLATOR

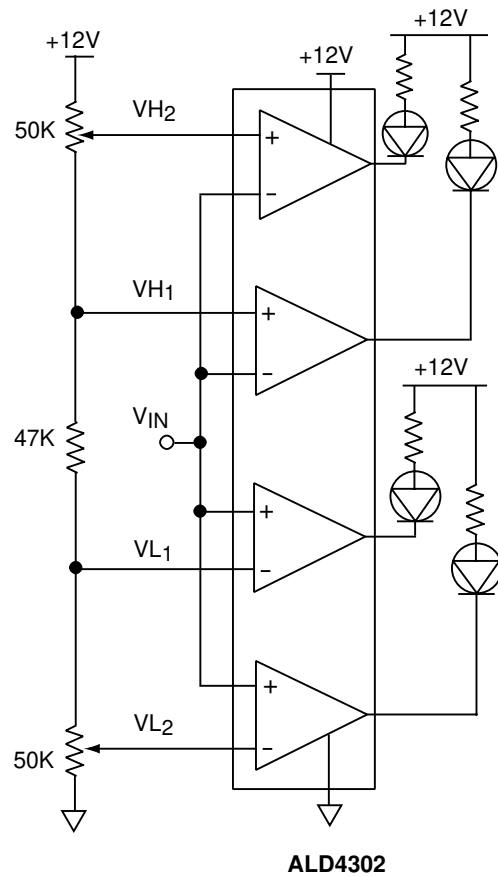


$V_{REF} = 1.4V$  for TTL input

$V_{REF} = \frac{V^+}{2}$  for CMOS input

Output  $V_{OUT}$  swings from rail- to- rail

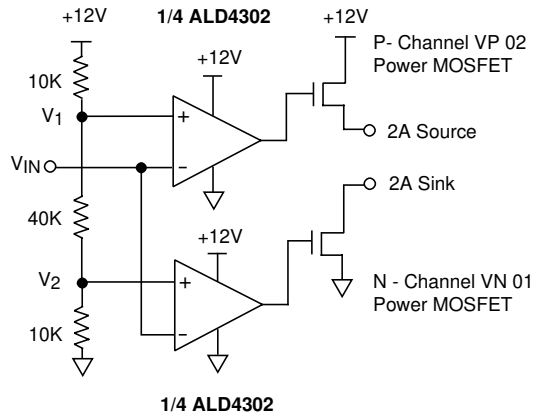
DOUBLE DUAL LIMIT WINDOW COMPARATOR



VL1 and VH1 first limit window send warning.  
VL2 and VH2 second limit window execute  
system cutoff.

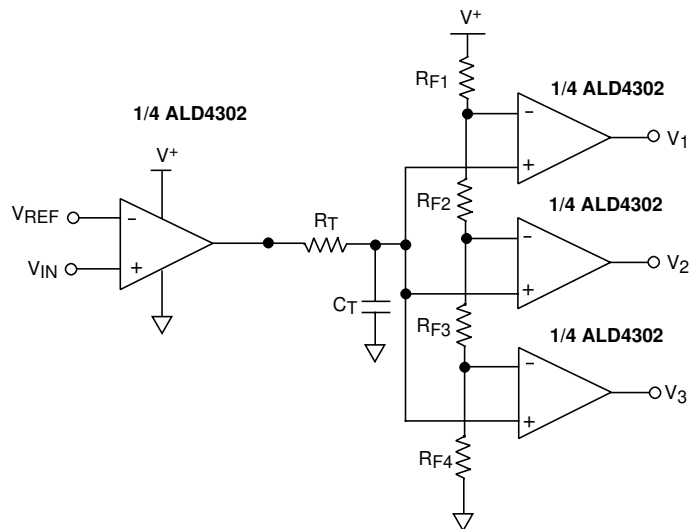
## TYPICAL APPLICATIONS (cont'd)

### PUSH-PULL COMPLEMENTARY POWER MOSFET DRIVER



This circuit eliminates crossover current in the complementary power transistors. The outputs can be used to source and sink different loads or tied together to provide push-pull drive.

### TIME DELAY GENERATOR

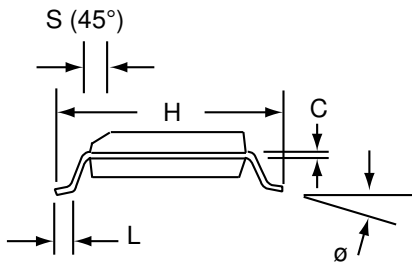
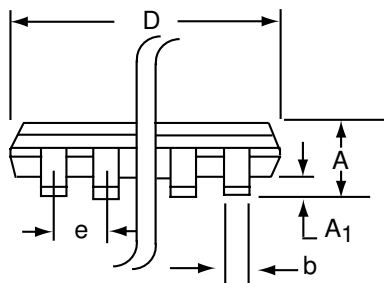
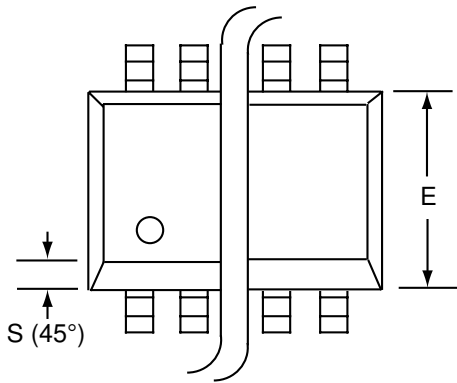


#### Design & Operating Notes:

1. As each output sources up to 10mA in the output high state, the output stage of a wired-OR low output circuit must be able to sink this current and still provide desired output voltage levels. For TTL output levels, this consideration limits the number to a maximum of three ALD4302 outputs wired-OR together.
2. In order to minimize stray oscillation, all unused inputs must be tied to ground.
3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. These currents are a function of ambient temperature, and would have to be considered in applications where very high source impedance or high accuracy are involved.
4. The high output sinking current of 60mA for each output offers flexibility in many applications, as a separate buffer or driver would not be necessary to drive the intended load. However, as the circuit normally operates close to ambient temperature due to its very low power consumption, thermal effects caused by large output current transients must be considered in certain applications.

# SOIC-14 PACKAGE DRAWING

## 14 Pin Plastic SOIC Package

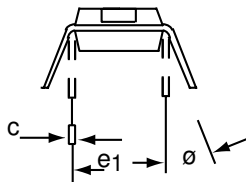
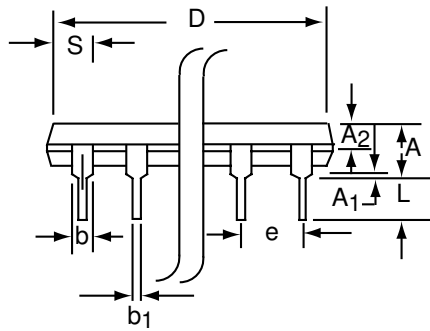
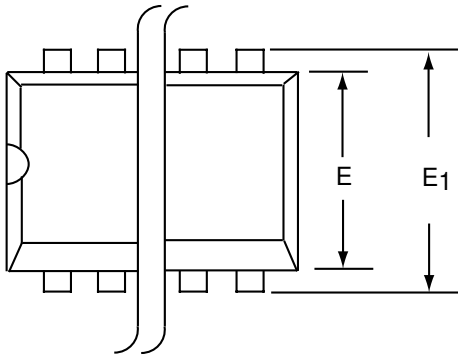


Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-14	8.55	8.75	0.336	0.345
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020



# OPDIP-14 PACKAGE DRAWING

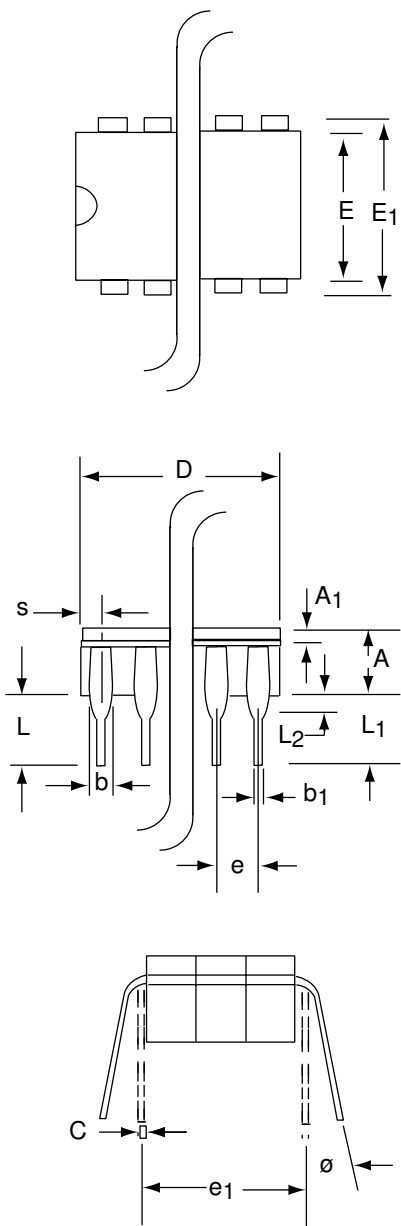
## 14 Pin Plastic DIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A <sub>1</sub>	0.38	1.27	0.015	0.050
A <sub>2</sub>	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b <sub>1</sub>	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-14	17.27	19.30	0.680	0.760
E	5.59	7.11	0.220	0.280
E <sub>1</sub>	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e <sub>1</sub>	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-14	1.02	2.03	0.040	0.080
θ	0°	15°	0°	15°

# CERDIP-14 PACKAGE DRAWING

## 14 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
<b>A</b>	3.55	5.08	0.140	0.200
<b>A<sub>1</sub></b>	1.27	2.16	0.050	0.085
<b>b</b>	0.97	1.65	0.038	0.065
<b>b<sub>1</sub></b>	0.36	0.58	0.014	0.023
<b>C</b>	0.20	0.38	0.008	0.015
<b>D-14</b>	--	19.94	--	0.785
<b>E</b>	5.59	7.87	0.220	0.310
<b>E<sub>1</sub></b>	7.73	8.26	0.290	0.325
<b>e</b>	2.54 BSC		0.100 BSC	
<b>e<sub>1</sub></b>	7.62 BSC		0.300 BSC	
<b>L</b>	3.81	5.08	0.150	0.200
<b>L<sub>1</sub></b>	3.18	--	0.125	--
<b>L<sub>2</sub></b>	0.38	1.78	0.015	0.070
<b>S</b>	--	2.49	--	0.098
<b>Ø</b>	0°	15°	0°	15°