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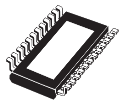
ALED1642GW

16 channel LED driver with error detection, current gain control and 12/16-bit PWM brightness control for automotive applications

Datasheet - production data



TSSOP24 (exposed pad)

Features

- AECQ100 qualification
- 16 constant current output channels
- Output current: from 3 mA to 40 mA
- Current programmable through external resistor
- 7-bit global current gain adjustment in two ranges
- 12/16-bit PWM grayscale brightness control
- Programmable output turn-on/off time
- Error detection mode (both open and shorted-LED)
- Programmable shorted-LED detection thresholds
- Auto power saving/auto-wakeup
- Selectable SDO synchronization on the CLK falling edge
- Gradual output delay (selectable)
- Supply voltage: 3 V to 5.5 V
- Thermal shutdown and overtemperature alert
- Up to 30 MHz 4-wires interface
- 20 V current generator rated voltage

Applications

- Full color/monochrome displays
- Dashboard (backlighting led indicators)
- Automotive Interior lighting

Description

The ALED1642GW is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The ALED1642GW guarantees 20 V output driving capability allowing the user to connect several LEDs in series. In the output stage, sixteen regulated current sources provide from 3 mA to 40 mA constant current to drive the LEDs. The current is programmed through an external resistor and can be adjusted by a 7-bit current gain register in two subranges. The brightness can be adjusted separately for each channel through 12/16-bit grayscale control.

Programmable turn-on and turn-off time (four different values available) improves the low noise generation performance of the system.

Open/short error detection mode is available in the ALED1642GW. The auto power-shutdown and auto power-on features (selectable) allow the device to save power without external intervention.

Thermal management includes an overtemperature data alert and output thermal shutdown (170 °C). The high clock frequency is up to 30 MHz and it makes the device suitable for high data rate transmission. A selectable gradual output delay reduces the inrush current, whereas the selectable SDO synchronization feature works when the device is used in daisy-chain configuration. The supply voltage range is between 3 V and 5.5 V.

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1 Pin description

Figure 1. TSSOP24EP pinout

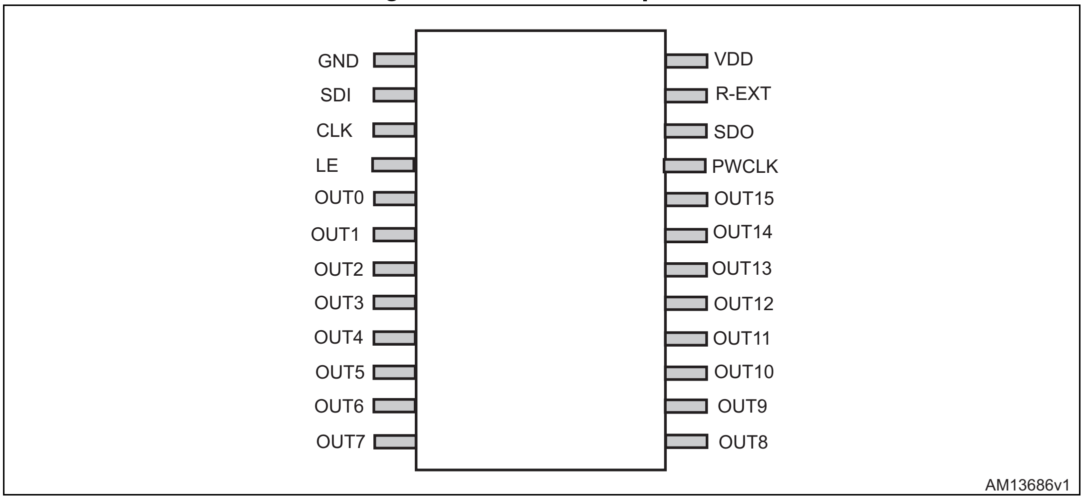


Table 1. Pin description

TSSOP24EP	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT0-OUT15	Output terminals
21	PWCLK	Clock input for PWM counter
22	SDO	Serial data output terminal
23	R-EXT	Terminal for external resistor for constant current programming
24	VDD	Supply voltage terminal

2 Absolute maximum ratings

Stressing the device above the ratings listed in the *Table 2* may cause the device permanent damage. Operating under conditions above those indicated in the operating section is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_{OUT}	Output voltage	-0.5 to 20	V
I_{OUT}	Output current	50	mA
V_i	Input voltage	-0.4 to V_{DD} +0.4	V
I_{GND}	GND terminal current	1400	mA
ESD	Electrostatic discharge protection HBM human body model	±2	kV

3 Thermal characteristics

Table 3. Thermal characteristics

Symbol	Parameter		Value	Unit
T_a	Operative free-air temperature range(1)		-40 to +150	°C
T_{OPR}	Operative junction temperature range		-40 to +150	
T_{STG}	Storage ambient temperature range		-55 to +150	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	TSSOP24EP(2)	37.5	°C/W

1. This data must be considered in adequate power dissipation conditions, the junction temperature must be maintained below 150 °C.
2. The exposed pad should be soldered directly to the PCB to get the thermal benefits. The exposed pad can be attached to a metal land electrically isolated or connected to ground.

4 Electrical characteristics

V_{DD} = 3.3 V, T_j = - 40 to 125 °C, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3		5.5	V
V_{OUT}	Output voltage	Out 0 - out 15	-	-	19	
V_{IH}	Input voltage		$0.7xV_{DD}$	-	V_{DD}	
V_{IL}			GND	-	$0.3xV_{DD}$	
V_{OL}	Serial data output voltage (SDO)	V_{DD}= 3 to 5.5 V I = +/- 1 mA	-	-	0.4	
V_{OH}			V_{DD} -0.4	-	-	
I_{Oleak}	Output leakage current	V_{OUT} = 19 V, all outputs OFF	-	-	0.5	µA
V_{uvlo}	UVLO threshold (rising)			2.7	2.9	V
	UVLO threshold (falling)		2.2	2.3		
Hy_{uvlo}	UVLO hysteresis			400		mV

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ΔI_{OL1}	Output current precision channel-to-channel (all outputs ON)(1)(2)	V_{OUT} = 0.1 V; (I_{OUT} = 3 mA) R_{EXT} = 11 kΩ CFG-0…CFG-5= "000000" CFG-6 = "0"	-	-	±4	%
ΔI_{OL2}		V_{OUT} = 0.5 V; (I_{OUT} = 20 mA) R_{EXT} = 11 kΩ CFG-0…CFG-5 = "011010" CFG-6 = "1"	-	-	±3	
ΔI_{OL3}		V_{OUT} = 0.8 V; (I_{OUT} = 36 mA) R_{EXT} = 11 kΩ CFG-0…CFG-5 = "111111" CFG-6 = "1"	-	-	±3	
ΔI_{OL2a}	Output current precision device-to-device (all outputs ON)(1)	V_{OUT} = 0.5 V; (I_{OUT} = 20 mA) R_{EXT}=1 1 kΩ CFG-0…CFG-5 = "011010" CFG-6 = "1"	-	-	±6	%
$\%/dV_{OUT}$	Output current vs. output voltage regulation (3)	V_{OUT} from 1 V to 3 V; (I_{OUT} = 36 mA) R_{EXT} = 11 kΩ CFG-0…CFG-5 = "111111" CFG-6 = "1"	-	±0.1	-	%/V
$\%/dV_{DD}$	Output current vs. supply voltage regulation(4)	V_{DD} from 3 V to 5.5 V V_{OUT} = 0.8 V; (I_{OUT} = 36 mA) R_{EXT} = 11 kΩ CFG-0…CFG-5 = "111111" CFG-6 = "1"	-	±1	-	
Rup	Pull-up resistor for PWCLK pin		400	500	650	KΩ
Rdw	Pull-down resistor for LE pin		400	500	650	
I_{DD}(OFF1)	Supply current (OFF)	R_{EXT} = 11 kΩ OUT 0 to 15 = OFF CFG = default	-	-	6	mA
I_{DD}(ON1)	Supply current (ON)	R_{EXT} = 11 kΩ; I_{OUT} = 20 mA OUT 0 to 15 = ON CFG-0…CFG-5 = "011010" CFG-6 = "1"	-		8	
I_{DD}(ON2)		R_{EXT} = 11 kΩ; I_{OUT} = 36 mA OUT 0 to 15 = ON CFG-0…CFG-5 = "111111" CFG-6 = "1"	-		10	
I_{DD} (auto OFF)	Supply current (auto OFF)	R_{EXT}= 11 kΩ; OUT 0 to 15 = OFF CFG-0…CFG-5 = "111111" CFG-6 = "1"	-	200	500	µA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{flg}	Thermal flag			150		°C
T_{sd}	Thermal shutdown(5)			170		°C
$T_{sd\text{-}hy}$	Thermal shutdown hysteresis(5)			15	20	°C

1. Tested with just one output loaded.
2. (Ioutn - Ioutavg1-15)/ Ioutavg1-15) x 100.
3. $$\Delta(\%/V) = \frac{(Ioutn @ Voutn = 3.0V) - (Ioutn @ Voutn = 1.0V)}{(Ioutn @ Voutn = 1.0V)} \times \frac{100}{3-1}$$
4. $$\Delta(\%/V) = \frac{(Ioutn @ Vdd = 5.5V) - (Ioutn @ Vdd = 3.0V)}{(Ioutn @ Vdd = 3.0V)} \times \frac{100}{5.5-3}$$
5. Not tested, guaranteed by design.

Figure 2. Typical chip-to-chip accuracy

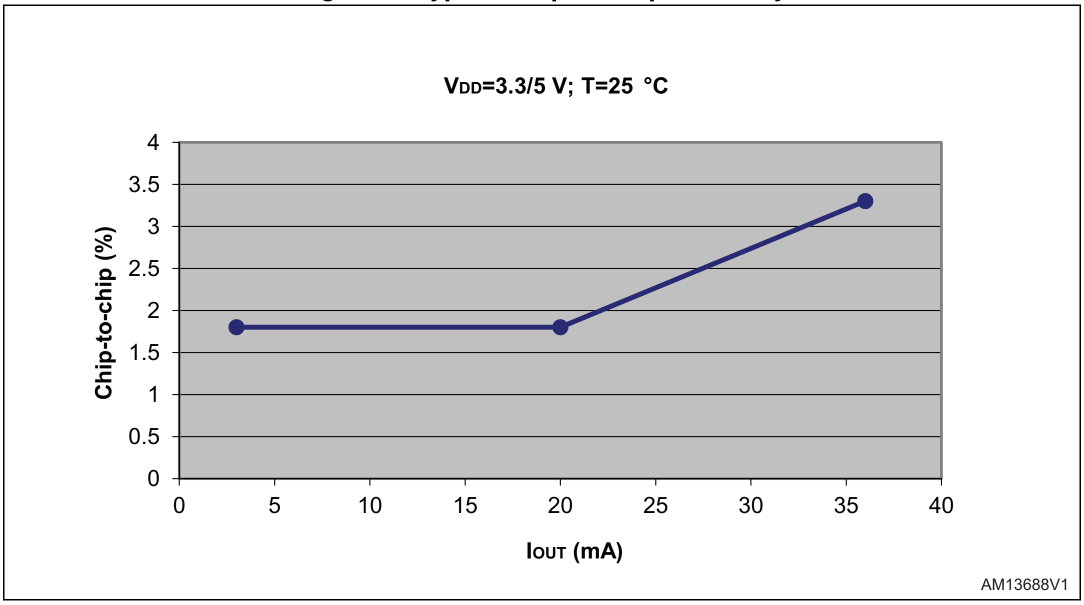
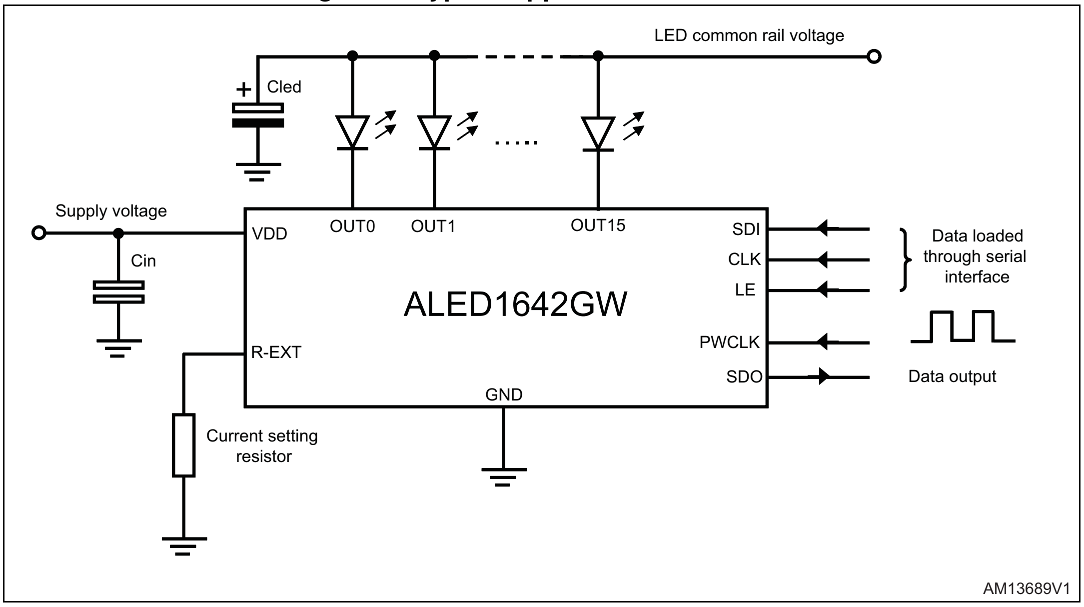


Figure 3. Typical application schematic



5 Switching characteristics

V_{DD} = 3.3 V, T_j = 25 °C, unless otherwise specified.

Table 5. Switching characteristics[1][2]

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{clk}	Clock frequency	Cascade operation	-	-	30	MHz
f_{pwclk}	PWclock frequency		-	-	30	
$tr_{(SDO)}$	SDO rise time	R_{EXT}= 11 kΩ; I_{OUT} = 20 mA V_{OUT} = 0.8 V VIH = V_{DD}; VIL = GND RL = 3.3 KΩ; CL = 10 pF CFG-0…CFG-5 = “011010” CFG-6 = “1”	-	5	-	ns
$tf_{(SDO)}$	SDO fall time		-	5	-	
tPLHLE	LE - OUTn[3]; Propagation delay time (“L to “H”)	R_{EXT} = 11 kΩ; I_{OUT} = 20 mA V_{OUT} = 0.8 V VIH = V_{DD}; VIL = GND RL = 50 Ω; CL = 10 pF CFG-0…CFG-5 = “011010” CFG-6 = “1”	-	200	-	
tPLH	CLK - SDO CFG-13 = ‘0’; Propagation delay time (“L to “H”)		8	15	25	
tPHLLE	LE - OUTn[3]; Propagation delay time (“H” to “L”)		-	100	-	
tPHL	CLK - SDO CFG-13 = ‘0’; Propagation delay time (“H” to “L”)		8	15	25	
tw(CLK)	CLK; Pulse width		20	-	-	
t_W(PWCLK)	PWCLK; Pulse width		20	-	-	
tw(L)	LE; Pulse width		20	-	-	
t_{gr-d}	Gradual delay ch-to-ch			10		
$t_{su(L)}$	Setup time for LE		5	-	-	
$t_{h(L)}$	Hold time for LE		5	-	-	
$t_{su(D)}$	Setup time for SDI		5	-	-	
$t_{h(D)}$	Hold time for SDI		10	-	-	
tclkr[4]	Maximum CLK rise time		-	-	5	µs
tclkf[4]	Maximum CLK fall time		-	-	5	
I_{out-ov}	Output current turn-on overshoot	V_{OUT} = 0.6 to 3 V CL = 10 pF; I_{OUT} = 3 to 36 mA	-	-	10	%
t_{n-err}	Normal error detection minimum output ON time		-	-	1	µs

Table 5. Switching characteristics(1)(2)

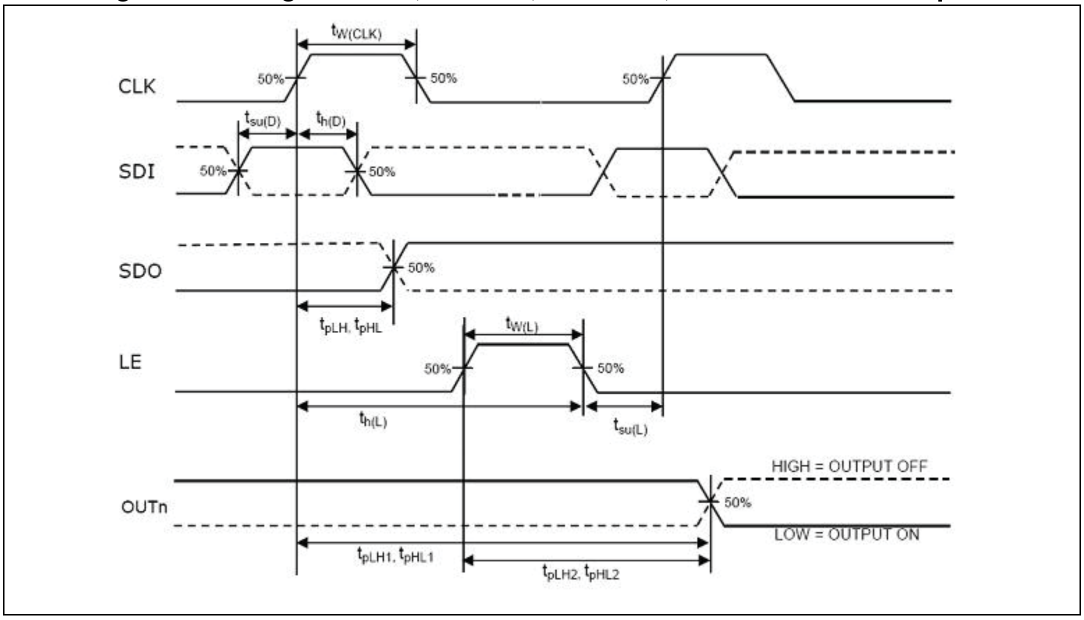
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{shutdown}$	Auto power shutdown time (auto OFF)	From LE falling edge to R_{EXT} voltage reference at -10%	-	100	-	ns
t_{wakeup}	Auto-wakeup	From LE falling edge to R_{EXT} voltage reference at 90%	-	3	-	µs

1. All table limits are guaranteed by design.
2. Not tested in production.
3. CFG -11= 0 and CFG -12 = 0 (output tr = 30 ns; output tf = 20 ns); CFG-14=1 (no output gradual delay).
4. If devices are connected in cascade and tclkr or tclkf is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

Table 6. Programmable T_{ON}/T_{OFF} (output rise and fall time)

Configuration bits (CFG-12 - CFG-11)	Conditions	Typ. (20% to 80%)		Unit
		Turn-on	Turn-off	
0 - 0	R_{EXT} = 11 kΩ; I_{OUT} = 20 mA V_{OUT} = 0.8 V VIH= V_{DD}; VIL= GND RL = 50 Ω; CL=10pF CFG-0...CFG-5=“011010” CFG-6 = “1”	30 ns	20 ns	ns
0 - 1		100 ns	40 ns	
1 - 0		140 ns	80 ns	
1 - 1		180 ns	150 ns	

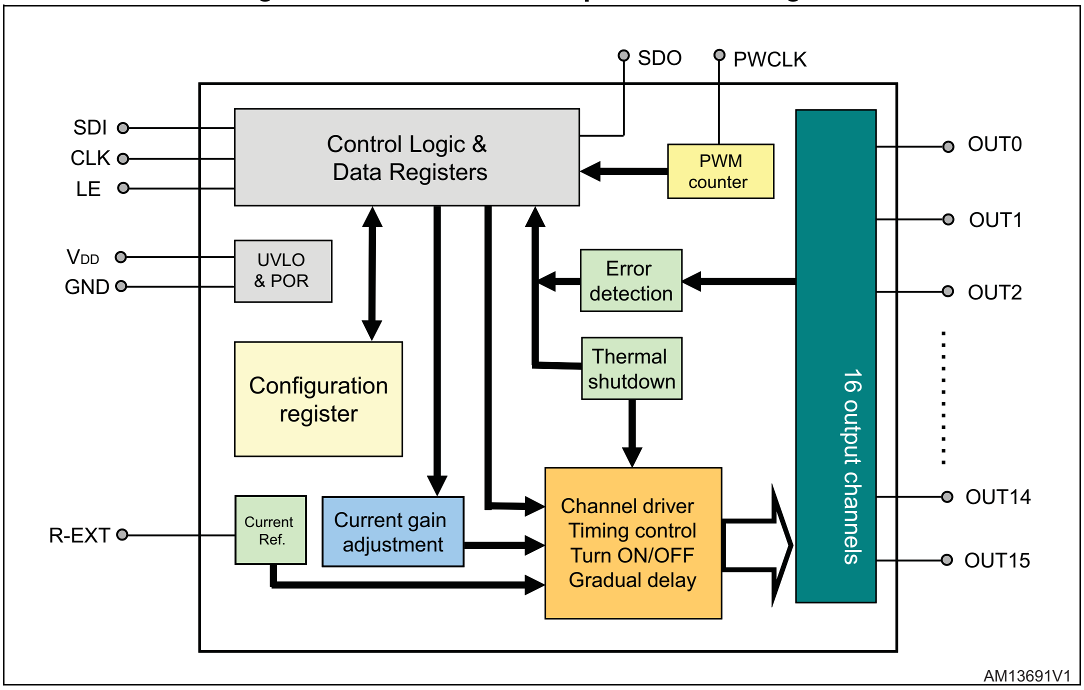
Figure 4. Timing for clock, serial in, serial out, latch enable and outputs



The correct sampling of the data depends on the stability of the data at SDI on the rising edge of the clock signal and it is assured by a proper data setup and hold time ($t_{SU(D)}$ and $t_{h(D)}$), as shown in *Figure 4*. The same figure shows the propagation delay from CLK to SDO (t_{PLH}/t_{PHL}). *Figure 4* describes also the minimum duration of CLK, LE pulses ($t_{W(CLK)}$) and $t_{W(L)}$ respectively and the propagation delay from LE to OUT_n (t_{PLHLE} and t_{PHLLE}) in the hypothesis that all channels have already been enabled by PWM counter.

6 Simplified internal block diagram

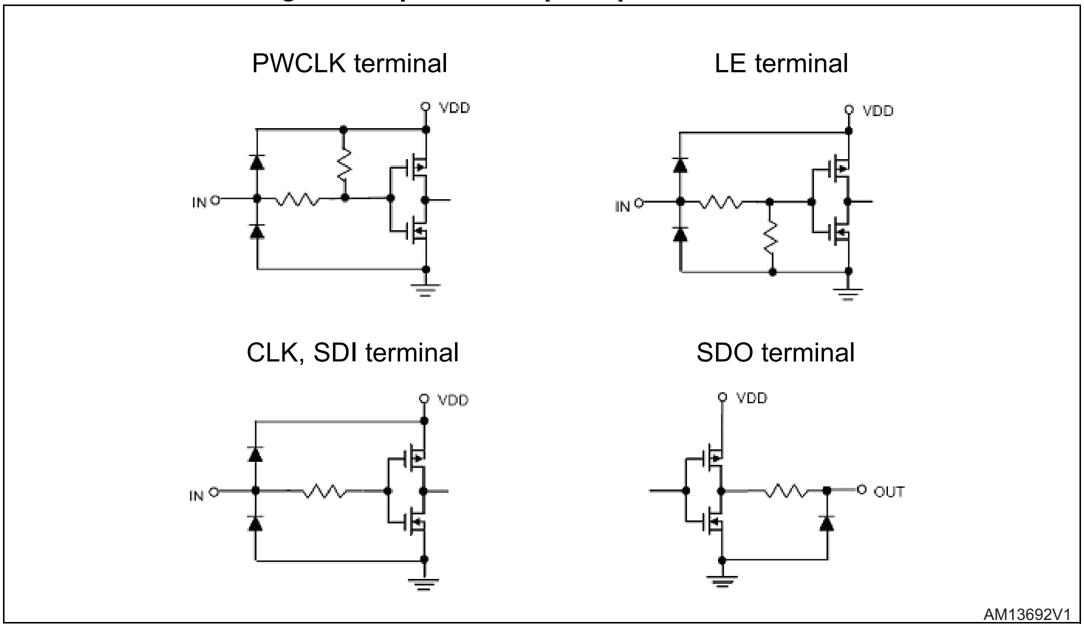
Figure 5. ALED1642GW simplified block diagram



6.1 Equivalent circuits of inputs and outputs

LE and PWCLK input terminals have pull-down and pull-up connection respectively. CLK and SDI must be connected to the external circuit to fix the logic level.

Figure 6. Input and output equivalent circuits



7 Digital blocks

The data input arrives through the serial Interface at each CLK rising edge. The LE signal is used to latch the loaded data and also to address data loading to the appropriate register, thermal flag reading and error detection. The access to the different registers or functions of the device (configuration register, brightness register or current gain, error detection, etc.) is achieved by using different digital keys, defined as a number of CLK pulses during which the LE signal is asserted. The available digital keys are listed in *Table 7* and *Figure 7*. A typical channel data input is shown in *Figure 8*.

Table 7. Digital key summary

Number	# CLK rising edge when the LE is “1”	Command description
1	1 – 2	Write switch (to turn on/off output channels)
2	3 – 4	Brightness data latch
3	5 – 6	Brightness global latch
4	7	Write configuration register
5	8	Read configuration register
6	9	Start open error detection mode
7	10	Start short error detection mode
8	11	Start combined error detection mode
9	12	End error detection mode
10	13	Thermal error reading
11	14	Reserved
12	15	Reserved

Figure 7. Digital keys

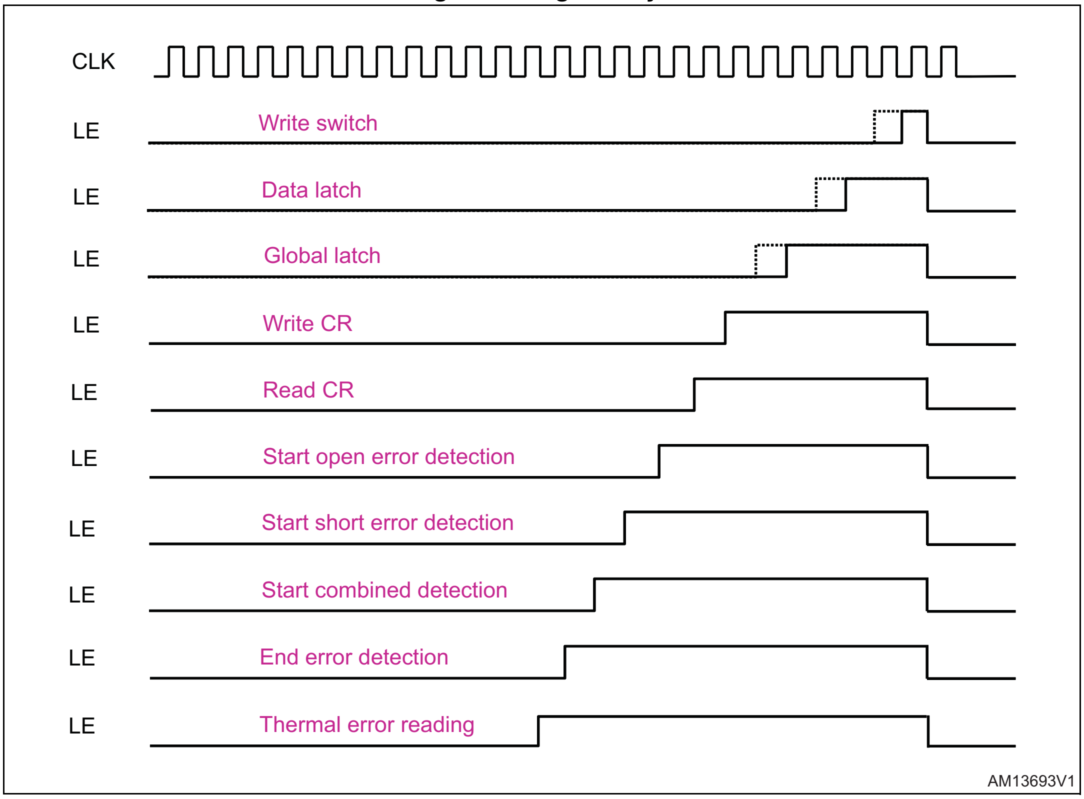
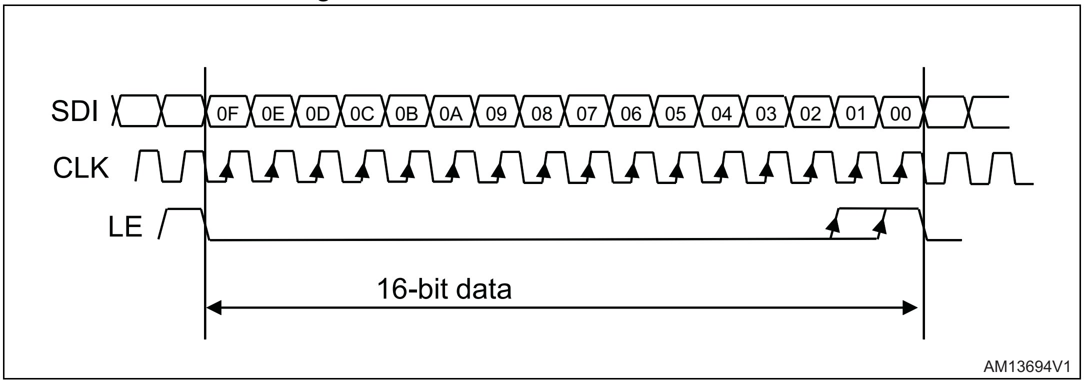


Figure 8. Channel data and write switch



8 Configuration register

The configuration register is used to enable or disable some device features, to program some parameters and to change other settings. The access to this register (read or write) is managed to find a description for each bit as described in *Table 8*. The default value of the configuration register (when the device is switched on or after a reset) is "0" for all bits. To change anything in the configuration register, a 16-bit digital word must be sent (CFG - 0 represents LSB, CFG -15 the MSB).

Table 8. Configuration register

<table>
<tr><th>Bit</th><th>Definition</th><th>R/W</th><th colspan="5">Description</th><th>Default</th></tr>
<tr><td>CFG-0</td><td rowspan="6">Current gain adjustment</td><td rowspan="6">R/W</td><td colspan="5" rowspan="6">6-bit DAC allows adjusting the device output current in 64 steps for each range (defined by CFG-6)</td><td>0</td></tr>
<tr><td>CFG-1</td><td>0</td></tr>
<tr><td>CFG-2</td><td>0</td></tr>
<tr><td>CFG-3</td><td>0</td></tr>
<tr><td>CFG-4</td><td>0</td></tr>
<tr><td>CFG-5</td><td>0</td></tr>
<tr><td>CFG-6</td><td>Current range</td><td>R/W</td><td colspan="5">"0" low current range
"1" high current range</td><td>0</td></tr>
<tr><td>CFG-7</td><td>Error detection mode</td><td>R/W</td><td colspan="5">"0" normal mode
"1" reserved mode</td><td>0</td></tr>
<tr><td rowspan="3">CFG-8</td><td rowspan="5">Shorted-LED detection thresholds</td><td rowspan="3">R/W</td><td colspan="2" rowspan="5">Programmable output shorted-LED detection thresholds</td><td>CFG-9</td><td>CFG-8</td><td>Th. volt.</td><td rowspan="3">0</td></tr>
<tr><td>0</td><td>0</td><td>1.8 V</td></tr>
<tr><td>0</td><td>1</td><td>2.5 V</td></tr>
<tr><td rowspan="2">CFG-9</td><td rowspan="2">R/W</td><td>1</td><td>0</td><td>3 V</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td>1</td><td>3.5 V</td></tr>
<tr><td>CFG-10</td><td>Auto OFF shutdown</td><td>R/W</td><td colspan="5">"0" device always ON
"1" auto power shutdown active (auto OFF)</td><td>0</td></tr>
<tr><td rowspan="3">CFG-11</td><td rowspan="5">Output turn-on/off time</td><td rowspan="3">R/W</td><td rowspan="5">Programmable output rise and fall time (20% to 80%)</td><td>CFG-12</td><td>CFG-11</td><td>Turn-on</td><td>Turn-off</td><td rowspan="3">0</td></tr>
<tr><td>0</td><td>0</td><td>30 ns</td><td>20 ns</td></tr>
<tr><td>0</td><td>1</td><td>100 ns</td><td>40 ns</td></tr>
<tr><td rowspan="2">CFG-12</td><td rowspan="2">R/W</td><td>1</td><td>0</td><td>140 ns</td><td>80 ns</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td>1</td><td>180 ns</td><td>150 ns</td></tr>
<tr><td>CFG-13</td><td>SDO delay</td><td>R/W</td><td colspan="5">If "0" no delay is present on SDO
If "1" the data are shifted out and they are synchronized with the falling edge of the CLK signal</td><td>0</td></tr>
</table>

Table 8. Configuration register (continued)

Bit	Definition	R/W	Description	Default
CFG-14	Gradual output delay	R/W	"0" a progressive delay is applied to output (10 ns per channel) "1" no delay is applied to output	0
CFG-15	12/16 PWM counter	R/W	"0" to select 16-bit brightness register (65536 grayscale rightness steps). "1" to select 12-bit brightness register (4096 grayscale brightness steps)	0

8.1 Gain control (from CFG 0 to 5) and current ranges (CFG- 6)

The LED current can be programmed using an external resistor connected to GND from R_{EXT} pin and can be fixed using the dedicated bits of the configuration register (from CFG - 0 to CFG - 5 bits define the gain, while CFG - 6 bit defines the current range within the which the gain can be adjusted). The device can regulate the current up to 36 mA and down to 0.5 mA. The accuracy of the LED current depends on the selected range and it is guaranteed in the ranges indicated in the static electrical characteristics only (see *Table 3* and *9*). When the device is switched on, the selected current range and the resistor connected to the R_{EXT} pin fix the default LED current:

$$I_{OL\_default} = \frac{V_{REF}}{R_{EXT}} \cdot K$$

Where V_{REF}=1.23 V is the voltage of the R_{EXT} pin and K is the mirroring current ratio, whose value depends on the selected current range:

- K = 28 with low current range selected (CFG - 6 = "0")
- K = 80 with high current range selected (CFG - 6 = "1")

The relation between the programmed current and the current gain settings is the following:

$$I_{OL} = (I_{OL\_default} + G \cdot \Delta I_{step})$$

where G is the current gain value (decimal value) defined by the dedicated bits of the current gain register. The current gain is managed by 6-bits of the configuration register (CFG - 0 to CFG - 5, CFG - 0 is LSB and CFG - 5 is MSB) and can be adjusted within two ranges (selectable through the bit CFG - 6) over 64 steps. The width of each step depends on the default current ($I_{ol\_default}$) as well as the selected R_{EXT}. Finally, each step is as follows:

$$\Delta I_{step} = \frac{I_{OL\_default}}{21}$$

The *Table 9* shows an example of the current setting with an external resistance (R_{EXT}) = 11 KΩ:

Table 9. Example of current ranges

	R_{EXT} [KΩ]	CFG-6	CFG-0 to CFG-5	LED current(1) [mA]	Accuracy
Low range	11	0	000000	3.1 mA	± 4% ch-to-ch
	11	0	111111	12.5 mA	-
High range	11	1	000000	8.9 mA	
	11	1	011010	20 mA	± 3% ch-to-ch

1. The indicated values may be slightly different on the current device.

The *Table 10* shows an example of current setting and gain control with R_{EXT} = 11 kΩ, see also *Figure 9*.

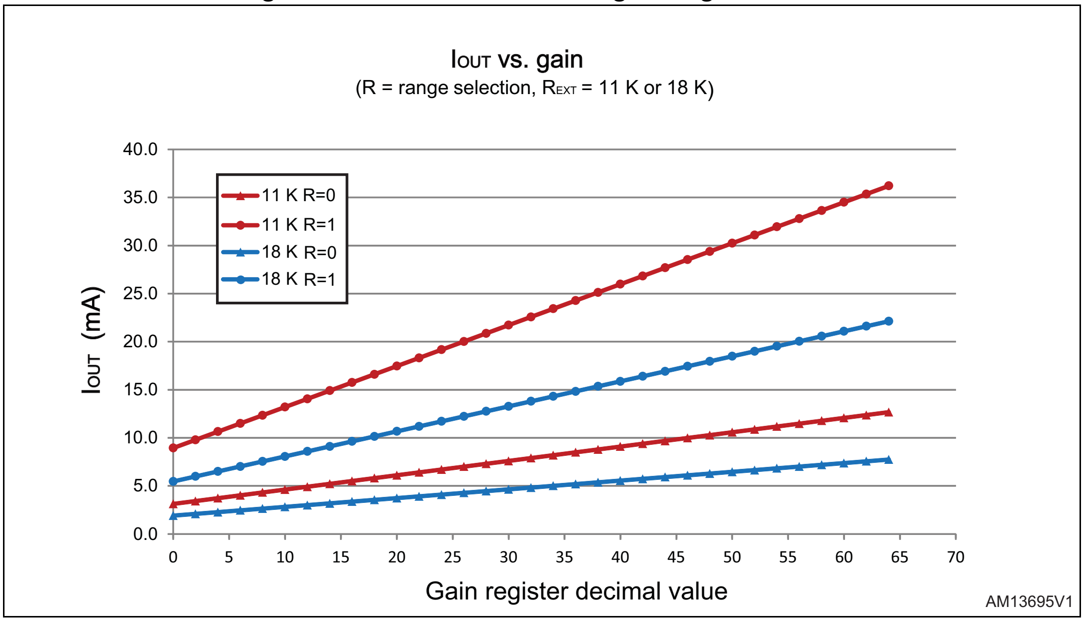
Table 10. Gain steps for the current range selected by R_{EXT} = 11 kΩ

	CFG-6	CFG(0 to 5)	LED current (1) [mA]
Low range	0	000000	3.131
	0	000001	3.280
	…	…	…
	0	111111	12.524
High range	1	000000	8.945
	1	000001	9.371
	…	…	…
	1	111111	35.782

1. The indicated values may be slightly different on the current device.

The external programming resistance must be connected as close as possible to the related device pins (R_{EXT} and GND) to reduce as minimum as possible the routing length and prevent reference noise injection and electromagnetic interferences. Moreover, a direct connection to the device GND pin reduces the possible output current variation when the total device ground current changes (load effect).

Figure 9. Channel current vs. gain register value



8.2 Error detection mode (CFG-7)

Stopping the normal activity of the display and turning on all driver channels allows the error detection to be performed and failed LED or display defects to be checked.

The error detection is active when the CFG -7 bit of the configuration register is "0". The diagnostics is performed as shown in *Figure 10*:

- The LED has to be selected turning on the relative channel on the switch register (powering on or off the output channels); the brightness register value for this channel cannot be zero.
- The normal error detection has to be selected in the configuration register (CFG-7= "0"). The appropriate digital key to choose the type of detection (open, short or combined) must be sent (see *Table 7*).
- After the error detection starts, the channel under testing has to be turned on at least 1 µs (the LED is at the nominal current). Please note that, the output power-on depends on PWCLK signal and in several applications this signal is not synchronized with the serial interface clock (CLK pin). Therefore, to be sure that, between the detection start and the detection end, the output power-on is 1 µs and moreover, that last power-on, in the interval, starts at least 0.5 µs before the detection end pattern (see *Figure 11*), it is suggested that the error detection should be performed just after the device startup (brightness counter reset) with all channels ON, before applying PWCLK signal..
- The result of the detection ("0" indicates a fault condition) is shifted out from SDO in 16 clock pulses after the "detection end command" is provided, first output bit represents channel 15 (error data can be read in a way similar to configuration register data reading as shown on *Figure 12*, *13*, *14* and *15*).

Figure 10. Error detection action sequence

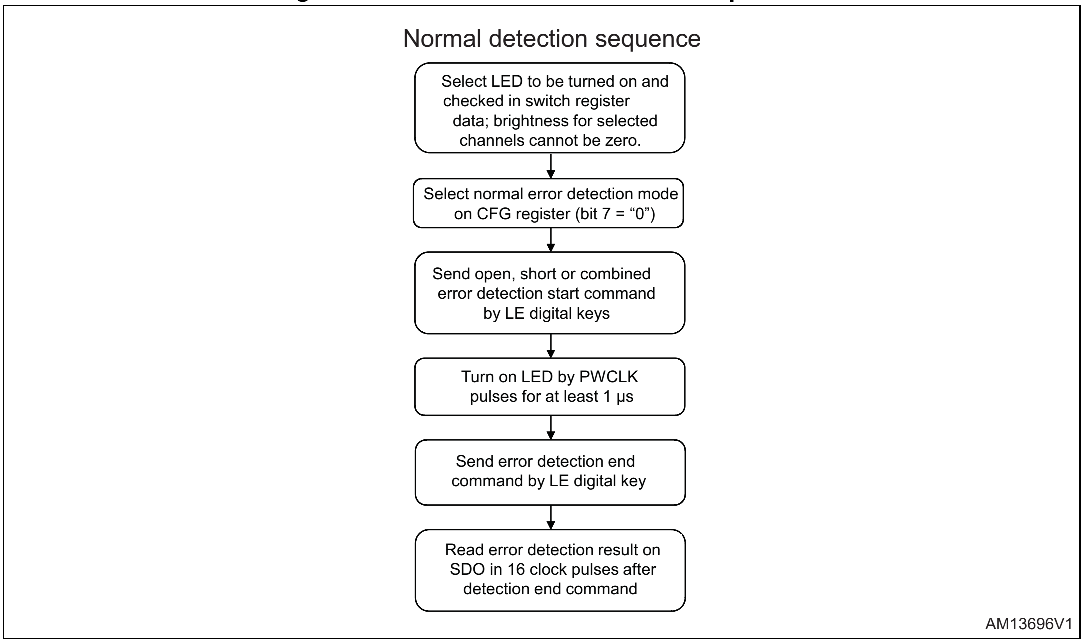


Figure 11. Error detection power-on timing

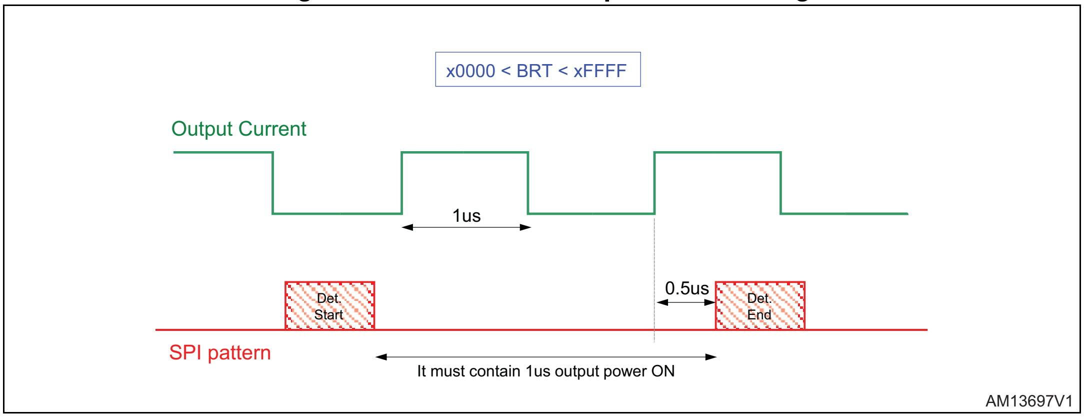


Figure 12. Configuration register reading sequence

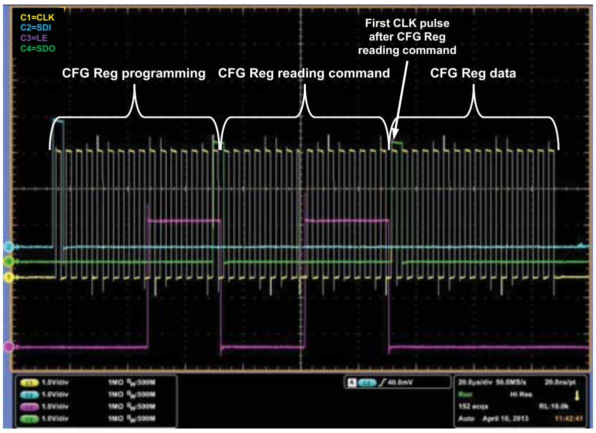


Figure 13. Configuration register reading sequence (zoom)

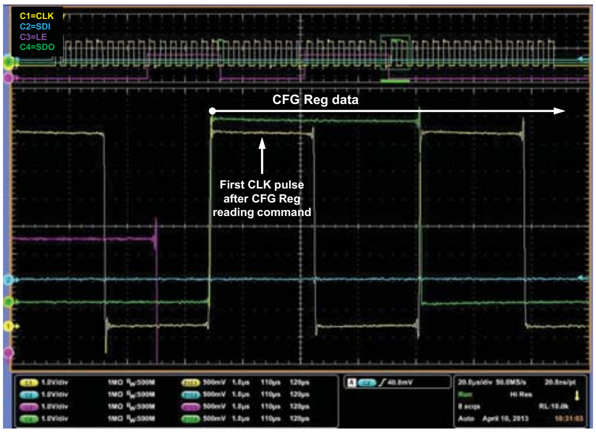


Figure 14. Configuration register reading sequence - SDO delay actives

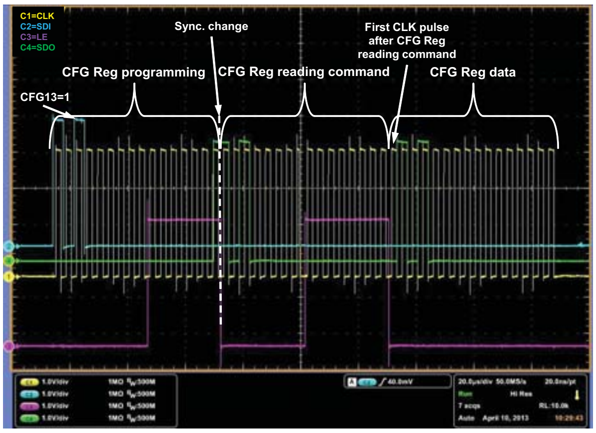
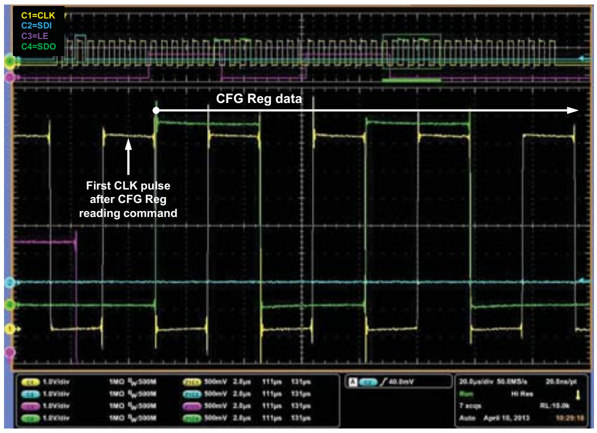


Figure 15. Configuration register reading sequence - SDO delay actives (zoom)



8.3 Error detection conditions

During the error detection phases for each channel, the following checks have to be performed:

- The output current in open detection mode (digital key: 9 CLK rising edges when LE is "1")
- The output voltage in short detection (digital key: 10 CLK rising edges when LE is "1")
- Both parameters (output voltage and current) in combined error detection mode (digital key: 11 CLK rising edges when LE is "1").

The thresholds for the error diagnostics are listed in *Table 11*:

Table 11. Diagnostic thresholds

Error detection modes		Checked malfunction	CFG-9	CFG-8	Thresholds (V)		
					Min.	Typ.	Max.
Open detection	Combined mode	Open line or output short to GND	x	x	-	$I_{OUT} \leq 0.5 \times I_{OUT}$ programmed	-
Short detection		Short on LED or short to V-LED	0	0	1.15	$V_{OUT} \geq 1.8$	2.05
			0	1	2.25	$V_{OUT} \geq 2.5$	2.75
			1	0	2.75	$V_{OUT} \geq 3.0$	3.25
			1	1	3.25	$V_{OUT} \geq 3.5$	3.80

8.4 Auto-wakeup/auto power shutdown (CFG-10)

This feature reduces the power consumption when all outputs are OFF. It is active when the CFG -10 bit of configuration register is "1". The auto power shutdown (auto OFF) starts when the data latched is "0" for all channels, and device is active again (wakeup) at the first latched data string including at least one bit = "1" (at least one channel ON). Timings for shutdown and wakeup are present in the dynamics feature table. While the auto power shutdown is active, the device ignores any other command except the channel power-on.

8.5 Programmable turn-on/turn-off time (CFG-11/12)

The device gives the possibility to program the turn-on and turn-off time of the current generators. Four different values can be selected using CFG -12 and CFG-11 bits of the configuration register (see *Table 8*) to fit the application requirements: 30/20 ns (00), 100/40 ns (01), 140/80 ns (10) and 180/150 ns (11). The selected value refers to T_{ON} (current rise time) and T_{OFF} (current fall time).