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ALPHA RF Transceiver

Features

- FM Transceiver Module
- Low cost, high performance
- Fast PLL lock time
- Wakeup timer
- 2.2V – 3.8V power supply
- Low power consumption
- 10MHz crystal for PLL timing
- Clock and reset signal output for external MCU use
- 16 bit RX Data FIFO
- SPI interface
- Internal data filtering and clock recover
- Digital signal strength indicator (DRSSI)
- Programmable TX frequency deviation (from 15 to 240 KHz)
- Programmable receiver bandwidth (from 67 to 400 kHz)
- Standby current less than 0.3uA
- Two 8 bit TX data registers
- High data rate (up to 115.2 kbps with internal demodulator, with external RC filter highest data rate is 256 kbps)
- Operates from -45 to +85OC

Applications

- Wireless Security Systems
- Car Alarms
- Remote Gate Controls
- Remote Sensing
- Data Capture
- Sensor Reporting

Introduction

The Alpha Modules are extremely cost effective but high performance radio modules. Supplied in a miniature Surface mount package this Transceiver module can Transmit/Receive at up to 115Kbps at a maximum of 300m.

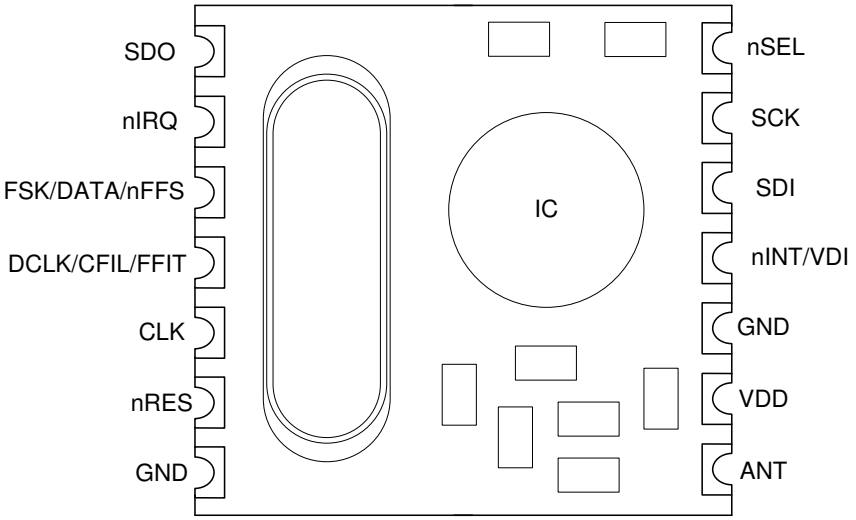
Operating at 2.2-3.6V, the module monitors its battery voltage and can sleep with very low standby current. The module can wake intermittently and provide direct control outputs to a microcontroller making it ideally suited to battery applications.

These Modules will suit one to one multi-node wireless links in applications including car and building security, POS and inventory tracking, remote process monitoring.

Ordering Information

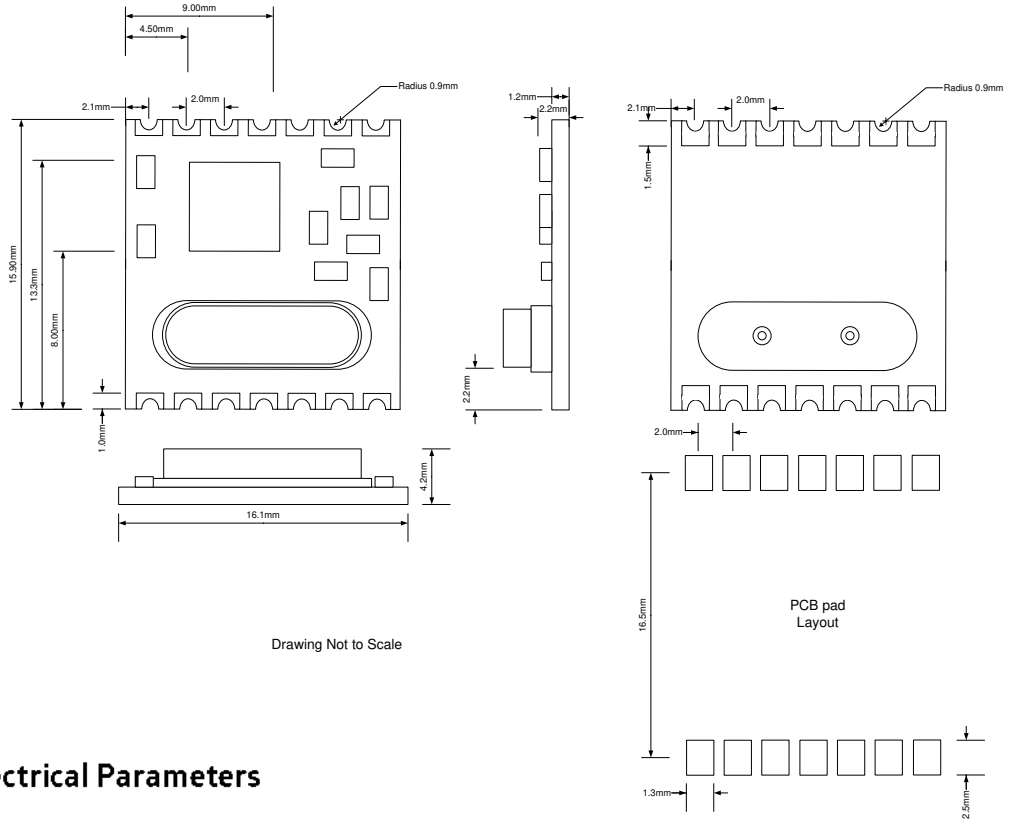
Part Number	Description
ALPHA-TRX433S	FM Transceiver Module, pre-set to 433MHz
ALPHA-TRX868S	FM Transceiver Module, pre-set to 868MHz
ALPHA-TRX915S	FM Transceiver Module, pre-set to 915MHz

Pin Description



PIN	Definition	Type	Function
11	nINT/VDI	DI/ DO	Interrupt input (active low)/Valid data indicator
9	VDD	S	Positive power supply
12	SDI	DI	SPI data input
13	SCK	DI	SPI clock input
8	ANT	IN	Antenna Connection
1	SDO	DO	Serial data output with bus hold
2	nIRQ	DO	Interrupts request output（active low）
3	FSK/DATA/nFFS	DI/DO/DI	Transmit FSK data input/ Received data output (FIFO not used)/ FIFO select
4	DCLK/CFIL/FFIT	DO/AIO/DO	Clock output (no FIFO)/ external filter capacitor(analog mode)/ FIFO interrupts(active high) when FIFO level set to 1, FIFO empty interruption can be achieved
5	CLK	DO	Clock output for external microcontroller
6	nRES	DIO	Reset Input (active low）
7, 10	GND	S	Power ground
14	nSEL	DI	Chip select (active low)

Mechanical Dimensions



Drawing Not to Scale

PCB pad Layout

Electrical Parameters

Maximum (not in working mode)

Symbol	Parameter	Minimum	Maximum	Unit
V_{dd}	Positive power supply	-0.5	6.0	V
V_{in}	All pin input level	-0.5	Vdd+0.5	V
I_{in}	Input current except power	-25	25	mA
ESD	Human body model		1000	V
T_{st}	Storage temperature	-55	125	°C
T_{ld}	Soldering temperature(10s)		260	°C

Recommended working range

Symbol	Parameter	Minimum	Maximum	Unit
V_{dd}	Positive power supply	2.2	3.8	V
T_{op}	Working temperature	-40	85	°C

DC Characteristics

Test Conditions: T_{op} 27°C V_{cc} = 3.3V

Symbol	Parameter	Remark	Minimum	Typical	Maximum	Unit
$I_{dd\_TX\_0}$	Supply current (TX mode, P_{out} = 0dBm)	433MHz band 868MHz band 915MHz band		15 **16** 17		mA
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, P_{out} = P_{max})	433MHz band 868MHz band 915MHz band		22 23 24	26 27 28	mA
I_{dd_RX}	Supply current (RX mode)	433MHz band 868MHz band 915MHz band		11 12 13	13 14 15	mA
I_x	Stand by current	Crystal and base band on		3.0	3.5	mA
I_{pd}	Sleep mode current	All blocks off		0.3		uA
I_{lb}	Low battery detection			0.5	1.7	uA
V_{lb}	Low battery step	0.1V per step	2.2		5.3	V
V_{lba}	Low battery detection accuracy			75		mV
V_{il}	Low level input				0.3*V_{dd}	V
V_{ih}	High level input		0.7*V_{dd}			V
I_{il}	Leakage current	V_{il}=0V	-1		1	uA
I_{ih}	Leakage current	V_{ih}=V_{dd} V_{dd}=5.4V	-1		1	uA
V_{ol}	Low level output	I_{ol}=2mA			0.4	V
V_{oh}	High level output	I_{oh}=-2mA	V_{dd}-0.4			V

AC Characteristics

PLL Parameters

Symbol	Parameter	Remark	Min	Typical	Max	Unit
f_{ref}	PLL frequency		9	10	11	MHz
t_{lock}	PLL lock time	After 10MHz step hopping, frequency error <10 kHz		30		us
T_{stP}	PLL Start up time	With running crystal oscillator		200	300	us
f_{LO}	frequency (10MHz crystal used)	433 MHz band 2.5KHz steps 868 MHz band 5KHz steps 915 MHz band 7.5KHz steps	430.24 860.48 900.72		439.75 879.51 929.27	MHz

AC Characteristics

Receiver

Symbol	Parameter	Remark	Min	Typical	Max	Unit
BW	Receiver bandwidth	Mode 1 Mode2 Mode 3 Mode 4 Mode 5 Mode 6	60 120 180 240 300 360	67 134 200 270 350 400	75 150 225 300 375 450	KHz
BR	FSK bit rate	With internal digital demodulator	0.6		115.2	kbps
BRA	FSK bit rate	With external RC filter			256	kbps
AFC_{range}	AFC working range	df_{FSK} FSK deviation in the received signal		0.8* df_{FSK}		
P_{min}	Receiver Sensitivity	BER 10-3, BW=67 kHz, BR=1.2 kbps, 868 MHz Band		-110		dBm
$IIP3_{inh}$	Input IP3	In band interferers in high bands (868 MHz, 915 MHz)		-21		dBm
$IIP3_{outh}$	Input IP3	Out of band interferers | f-fo | > 4 MHz		-18		dBm
$IIP3_{inl}$	IIP3 (LNA –6 dB gain)	In band interferers in low band (433 MHz)		-15		dBm
$IIP3_{outl}$	IIP3 (LNA –6 dB gain)	Out of band interferers | f-fo | > 4 MHz		-12		dBm
P_{max}	Maximum Power Input	LNA High Gain	0			dBm
C_{in}	RF Input Capacitance			1		pF
RS_A	RSSI accuracy			±6		dB
RS_{Rs}	RSSI range			46		dB
C_{ARSSI}	ARSSI filter		1			nF
RS_{STEP}	RSSI programmable step			6		dB
RS_{RESP}	DRSSI response time	RSSI output high after valid , CARRSI=5nF		500		us
P_{sp}	Receiver Spurious emission				-60	dBm

AC Characteristics (Transmitter)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{out}	Open Collector output DC	Programmable	0.5		6	mA
P_{max_50}	Max. output power delivered to 50 Ohm load over a suitable matching network	In 433MHz band		7		dBm
		In 868MHz / 915MHz band		5		
P_{max_ant}	Max. EIRP with suitable selected PCB antenna	In 433 MHz band with monopole antenna with matching network		7		dBm
		In 868 MHz / 915 MHz bands		7		
P_{out}	Typical output power	Selectable in 2.5dB steps	P_{max} - 17.5		P_{max}	dBm
P_{sp}	Spurious emission $f-f_{sp} > 1$ MHz	At max power 50 ohm load			-55	dBc
		With PCB antenna			-60	
P_{harm}	Harmonic suppression	At max power 50 ohm load			-35	dBc
		With PCB antenna			-42	dBc
C_o	Output capacitance (set by the automatic antenna tuning circuit)	In 433MHz band In 868 and 915MHz bands	2 2.1	2.6 2.7	3.2 3.3	pf
Q_o	Quality factor of the output capacitance	In 433MHz band In 868 and 915MHz bands	13 8	15 10	17 12	
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier			-75 -85	dbc/HZ
BR	FSK bit rate	Via internal TX data register			172	kbps
BRA	FSK bit rate	TX data connected to the FSK input			256	
df_{fsk}	FSK frequency deviation	Programmable in 15 kHz steps	15		240	kHz

AC Characteristic (Turn-on/Turnaround timings)

Symbol	Parameter	Remark	Min	Typical	Max	Unit
T_{st}	Crystal oscillator startup time	Crystal ESR < 100			5	ms
$T_{tx\_rx\_XTAL\_ON}$	Transmitter - Receiver turnover time	Synthesizer off, crystal oscillator on		450		us
$T_{rx\_tx\_XTAL\_ON}$	Receiver - Transmitter turnover time	Synthesizer off, crystal oscillator on		350		us
$T_{tx\_rx\_SYNT\_ON}$	Transmitter - Receiver turnover time	Synthesizer on, crystal oscillator on		425		us
$T_{rx\_tx\_SYNT\_ON}$	Receiver - Transmitter turnover time	Synthesizer on, crystal oscillator on		300		us
C_{xl}	Crystal load capacitance	Programmable in 0.5 pF steps, tolerance+/- 10%	8.5		16	pf
t_{POR}	Internal POR timeout	After V_{dd} has reached 90% of final value			100	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.96		1.05	ms
$C_{in, D}$	Digital input apacitance				2	pf
$t_{r, f}$	Digital output rise/fall time	15pF pure capacitive load			10	ns

Programming Guide

Brief Description

ALPHA-TRX supports a command interface to setup frequency, deviation, output power and also data rate. There is no need to change any hardware when using frequency-hopping applications.

Commands to the transmitter are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16- bit command). Bits having no influence (don't care) are indicated with X. Special care must be taken when the microcontroller's builtin hardware serial port is used. If the port cannot be switched to 16-bit mode then a separate I/O line should be used to control the nSEL pin to ensure the low level during the whole duration of the command or a software serial control interface should be implemented. The Power-On Reset (POR) circuit sets default values in all control and command registers. The receiver will generate an interrupt request (IT) for the microcontroller - by pulling the nIRQ pin low - on the following events:

- The TX register is ready to receive the next byte (RGIT)
- The RX FIFO has received the preprogrammed amount of bits (FFIT)
- Power-on reset (POR)
- RX FIFO overflow (FFOV) / TX register underrun (RGUR)
- Wake-up timer timeout (WKUP)
- Negative pulse on the interrupt input pin nINT (EXT)
- Supply voltage below the preprogrammed value is detected (LBD)

FFIT and FFOV are applicable when the RX FIFO is enabled. RGIT and RGUR are applicable only when the TX register is enabled. To identify the source of the IT, the status bits should be read out.

Symbol	Parameter	Min value (ns)
t_{CH}	Clock high time	25
t_{CL}	Clock time low	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Select high time 25 t DS Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{DD}	Data delay time	10

Control Commands

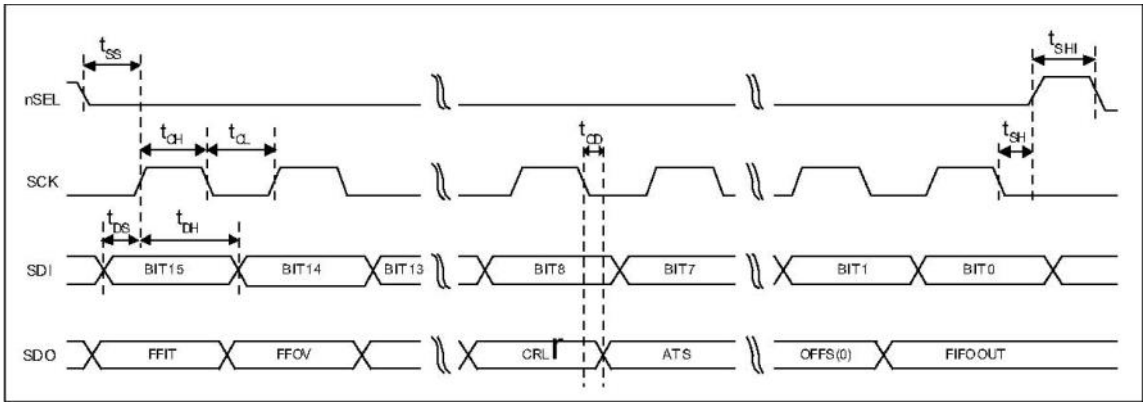
	Control Command	Related Parameter/Functions	Related control bits
1	Configuration Setting Command	Frequency band, crystal oscillator load capacitance, RX FIFO and TX register enable	*el, ef, b1* to *b0, x3* to *x0*
2	Power Management Command	Receiver/Transmitter mode change, synthesizer, crystal oscillator, PA, wake-up timer, clock output enable	*er, ebb, et, es, ex, eb, ew, dc*
3	Frequency Setting Command	Frequency of the local oscillator/carrier signal	*f11* to *f0*
4	Data Rate Command	Bit rate	*cs, r6* to *r0*
5	Receiver Control Command	Function of pin 16, Valid Data Indicator, baseband bandwidth, LNA gain, digital RSSI threshold	*p16, d1* to *d0, i2* to *i0, g1* to *g0, r2* to *r0*
6	Data Filter Command	Data filter type, clock recovery parameters	*al, ml, s, f2* to *f0*
7	FIFO and Reset Mode Command	Data FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable, POR sensitivity	*f3* to *f0, sp, ff, al, dr*
8	Synchron Pattern Command	Synchron pattern	*b7* to *b0*
9	Receiver FIFO Read Command	RX FIFO read	
10	AFC Command	AFC parameters	*a1* to *a0, rl1* to *rl0, st, fi, oe, en*
11	TX Configuration Control Command	Modulation parameters, output power	*mp, m3* to *m0, p2* to *p0*
12	PLL Setting Command	CLK out buffer speed, dithering, PLL bandwidth	*ob1* to *ob0, ddit, dly, bw0*
13	Transmitter Register Write Command	TX data register write	*t7* to *t0*
14	Wake-Up Timer Command	Wake-up time period	*r4* to *r0, m7* to *m0*
15	Low Duty-Cycle Command	Enable and set low duty-cycle mode	*d6* to *d0, en*
16	Low Battery Detector and Microcontroller Clock Divider Command	LBD voltage and microcontroller clock division ratio	*d2* to *d0, v3* to *v0*
17	Status Read Command	Status bit readout	

In general, setting the given bit to one will activate the related function. In the following tables, the POR column shows the default values of the command registers after power-on.

Control register Values

	Control Register	Power on Reset Value
1	Configuration Setting Command	8008h
2	Power Management Command	8208h
3	Frequency Setting Command	A680h
4	Data Rate Command	C623h
5	Receiver Control Command	9080h
6	Data Filter Command	C22Ch
7	FIFO and Reset Mode Command	CA80h
8	Synchron Pattern Command	CED4h
9	Receiver FIFO Read Command	B000h
10	AFC Command	C4F7h
11	TX Configuration Control Command	9800h
12	PLL Setting Command	CC77h
13	Transmitter Register Write Command	B8AAh
14	Wake-Up Timer Command	E196h
15	Low Duty-Cycle Command	C80Eh
16	Low Battery Detector and Microcontroller Clock Divider Command	C000h
17	Status Read Command	0000h

Commands
Timing Diagram



Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	0	0	el	ef	b1	b0	x3	x2	x1	x0	8008h

e l: Enable TX register
e f: Enable RX FIFO buffer

b1	b0	Band[MHz]
0	0	Reserved
0	1	433
1	0	868
1	1	915

x3..x0: select crystal load capacitor

x3	x2	x1	x0	Load capacitor [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
1	1	1	0	15.5
1	1	1	1	16.0

Power Management Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	1	0	er	ebb	et	es	ex	eb	ew	dc	8208h

er: Enable receiver
ebb: Enable base band block
et: Enable transmitter
es: Enable synthesizer
ex: Enable crystal oscillator
eb: Enable low battery detector
ew: Enable wake-up timer
dc: Disable clock output of CLK pin

Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

f11..f0: Set operation frequency:
433band: Fc=430+F*0.0025 MHz
868band: Fc=860+F*0.0050 MHz
915band: Fc=900+F*0.0075 MHz
Fc is carrier frequency and F is the frequency parameter. 36≤F≤3903

Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	cs	r6	r5	r4	r3	r2	r1	r0	C623h

r6..r0: Set data rate:
BR=10000000/29/（R+1）/（1+cs*7）

Receiver Control Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	0	P16	d1	d0	i2	i1	i0	g1	g0	r2	r1	r0	9080h

P16: select function of pin16

P16	
0	Interrupt input
1	VDI output

i2..i0:select baseband bandwidth

I2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved

d1..d0: select VDI response time

d1	d0	Response
0	0	Fast
0	1	Medium
1	0	Slow
1	1	Always on

g1..g0: select LNA gain

g1	g0	LNA gain (dBm)
0	0	0
0	1	-6
1	0	-14
1	1	-20

r2..r0: select DRSSI threshold

r2	r1	r0	RSSIsetth [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	Reserved
1	0	1	Reserved

The actual DRSSI threshold is related to LNA setup: SSIth = RSSIsetth + GLNA.

Data Filter Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	al	ml	1	s	1	f2	f1	f0	C22Ch

al: Enable clock recovery auto-lock
ml: Enable clock recovery fast mode
s: select data filter type

s	Filter type
0	Digital filter
1	Analog RC filter

f1..f0: Set DQD threshold

FIFO and Reset Mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	1	0	f3	f2	f1	f0	sp	al	ff	dr	CA80h

f3..f0: Set FIFO interrupt level
sp: Select the length of the synchron pattern:

sp	Byte1	Byte0 (POR)	Synchron Pattern (Byte1+Byte0)
0	2Dh	D4h	2DD4h
1	Not used	D4h	D4h

al: select FIFO fill start condition

al	Condition
0	Sync-word
1	Always

ff: Enable FIFO fill
dr: Disable hi sensitivity reset mode

Synchron Pattern Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	b7	b6	b5	b4	b3	b2	b1	b0	CED4h

This command is used to reprogram the synchronic pattern;

Receiver FIFO Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	B000h

This command is used to read FIFO data when FFIT interrupt generated. FIFO data output starts at 8th SCK period.

AFC Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	a1	a0	rl1	rl0	st	fi	oe	en	C4F7h

If crystal oscillator, synthesizer and power amplifier are auto-controlled, this command will close power amplifier and synthesizer immediately, then stop crystal oscillator after S periods of CLK signal

a1..a0: select AFC auto-mode:

a1	a0	
0	0	Controlled by MCU
0	1	Run once at power on
1	0	Keep offset when VDI hi
1	1	Keeps independently from VDI

rl1..rl0: select range limit

r1	r0	Range (fres)
0	0	No restriction
0	1	+15/-16
1	0	+7/-8
1	1	+3-4

freq

315，433band: 2.5kHz
868band: 5kHz
915band: 7.5kHz

st: st goes hi will store offset into output register
fi: Enable AFC hi accuracy mode
oe: Enable AFC output register
en: Enable AFC function

TX Configuration Control Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	1	0	0	mp	m3	m2	m1	m0	0	p2	p1	p0	9800h

m: select modulation polarity
m2..m0: select frequency deviation:

m3	m2	m1	m0	Frequency Deviation [kHz]
0	0	0	0	15
0	0	0	1	30
0	0	1	0	45
0	0	1	1	60
0	1	0	0	75
0	1	0	1	90
0	1	1	0	105
0	1	1	1	120
1	0	0	0	135
1	0	0	1	150
1	0	1	0	165
1	0	1	1	180
1	1	0	0	195
1	1	0	1	210
1	1	1	0	225
1	1	1	1	240

p2..p0: select output power

p2	p1	p0	Output power [dBm]
0	0	0	0
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-18
1	0	1	-21

PLL Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	0	ob1	ob0	lpx	ddy	ddit	1	bw0	CC67h

ob1-ob0: Microcontroller output clock buffer rise and fall time control.

ob1	ob0	Selected uC CLK frequency
0	0	5 or 10 MHz (recommended)
0	1	3.3 MHz
1	X	2.5 MHz or less

lpx: select low power mode of the crystal oscillator.

lpx	Crystal start-up time (typ)	Power consumption (typ)
0	1 ms	620 uA
1	2 ms	460 uA

ddy: phase detector delay enable.
ddi: disables the dithering in the PLL loop.
bw1-bw0: select PLL bandwidth

bw0	Max bit rate [kbps]	Phase noise at 1MHz offset [dBc/Hz]
0	86.2	-107
1	256	-102

Transmitter Register Write Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	1	0	0	0	t7	t6	t5	t4	t3	t2	t1	t0	B8AAh

This command is use to write a data byte to RF12 and then RF12 transmit it

Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up period is determined by:
Twake-up = M * 2R [ms]

Low Duty-Cycle Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	d6	d5	d4	d3	d2	d1	d0	en	C80Eh

d6..d0: Set duty cycle
D.C.= (D * 2 +1) / M *100%

En: Enable low duty cycle mode

Low Battery Detector and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d2	d1	d0	0	v3	v2	v1	v0	C000h

d2..d0: select frequency of CLK pin

d2	d1	d0	Clock Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

CLK signal is derive form crystal oscillator and it can be applied to MCU clock in to save a second crystal.
If not used, please set bit "dc" to disable CLK output

To integrate the load capacitor internal can not only save cost, but also adjust reference frequency by software

v3..v0: Set threshold voltage of Low battery detector： Vlb=2.2+V*0.1 [V]

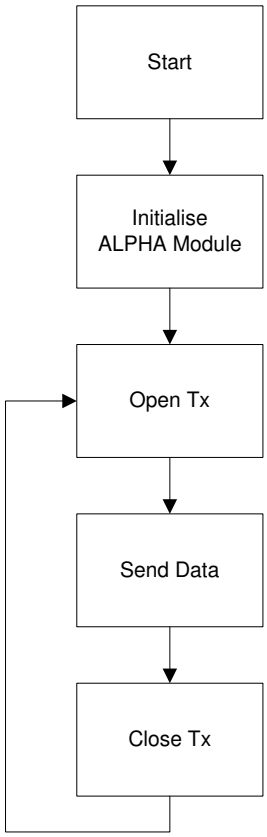
Status Read Command

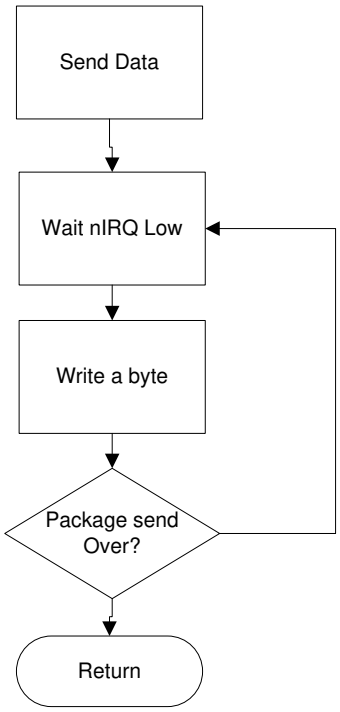
bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-

Bit	
15	TX ready for next byte or FIFO received data status
14	Power on reset status
13	TX Register under run or RX FIFO Overflow status
12	Wakeup timer overflow status
11	Interrupt on external source status
10	Low battery detect status
9	FIFO empty status
8	Antenna tuning signal strength
7	Received signal strength indicator
6	Data Quality Detector status
5	Clock Recovery Locked status
4	Toggling in each AFC cycle
3	Measured Offset Frequency Sign Value 1='+', 0='-'
2	Measured offset Frequency value (3 bits)
1	Measured offset Frequency value (3 bits)
0	Measured offset Frequency value (3 bits)

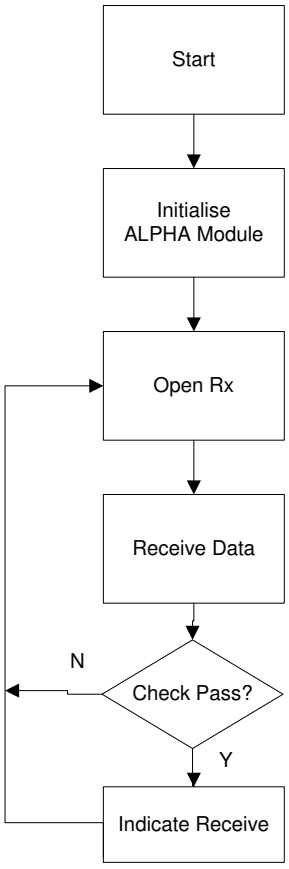
This command starts with a 0 and be used to read internal status register. Data output starts at 8th SCK period.

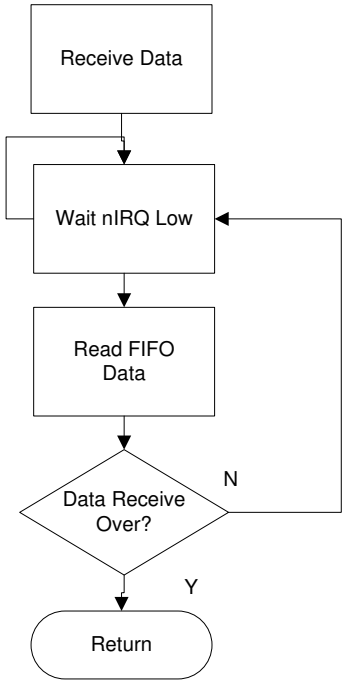
Transmitter Operation Flow





Receiver Operation Flow





After Initialisation, open FIFO receive mode and wait for nIRQ low, only then can the MCU read received and stored data in FIFO.
For the next received package please reset FIFO

RF Solutions Ltd. Recycling Notice
Meets the following EC Directives:

DO NOT
Discard with normal waste, please recycle.

ROHS Directive 2002/95/EC
Specifies certain limits for hazardous substances.

WEEE Directive 2002/96/EC
Waste electrical & electronic equipment. This product must be disposed of through a licensed WEEE collection point. RF Solutions Ltd., fulfills its WEEE obligations by membership of an approved compliance scheme.

Waste Batteries and Accumulators Directive 2006/66/EC
Where batteries are fitted, before recycling the product, the batteries must be removed and disposed of at a licensed collection point.

Environment Agency producer registration number:
WEE/JB0104WV.

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