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# AMIS-30511

# Micro-Stepping Motor Driver

**ON Semiconductor®**

**http://onsemi.com**

### Introduction

The AMIS−30511 is a micro−stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and a SPI interface with an external microcontroller. The AMIS−30511 contains a current−translation table and takes the next micro−step depending on the clock signal on the "NXT" input pin and the status of the "DIR" (=direction) register or input pin. The chip provides a so−called "speed and load angle" output. This allows the creation of stall detection algorithms, step loss detection, and control loops based on load−angle to adjust torque and speed. It is using a proprietary PWM algorithm for reliable current control.

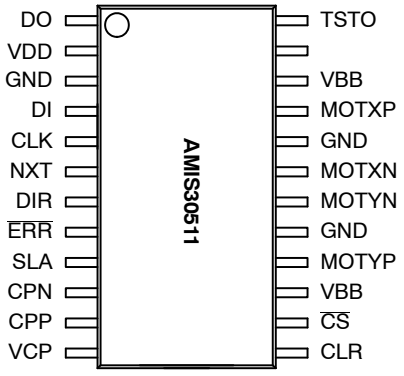
The AMIS−30511 is implemented in I2T100 technology, enabling both high−voltage analog circuitry and digital functionality on the same chip. The chip is fully compatible with the automotive voltage requirements.

The AMIS−30511 is ideally suited for general−purpose stepper motor applications in the automotive, industrial, medical, and marine environment.

### Key Features

- Dual H−Bridge for 2−phase Stepper Motors
- Programmable Peak−current up to 800 mA Using a 5−bit Current DAC
- On−chip Current Translator
- SPI Interface
- Speed and Load Angle Output
- Seven Step Modes from Full−step up to 32 Micro−steps
- Fully Integrated Current−sense
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Low EMC PWM with Selectable Voltage Slopes
- Active Fly−back Diodes
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Compatible with 3.3 V Microcontrollers, 5 V Tolerant Inputs
- −40°C to 125°C Temperature Range at 800 mA Peak Current

### PIN ASSIGNMENT




(Top View)

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| AMIS30511 | SOIC 24 | Tape & Reel |

**Table of Contents**



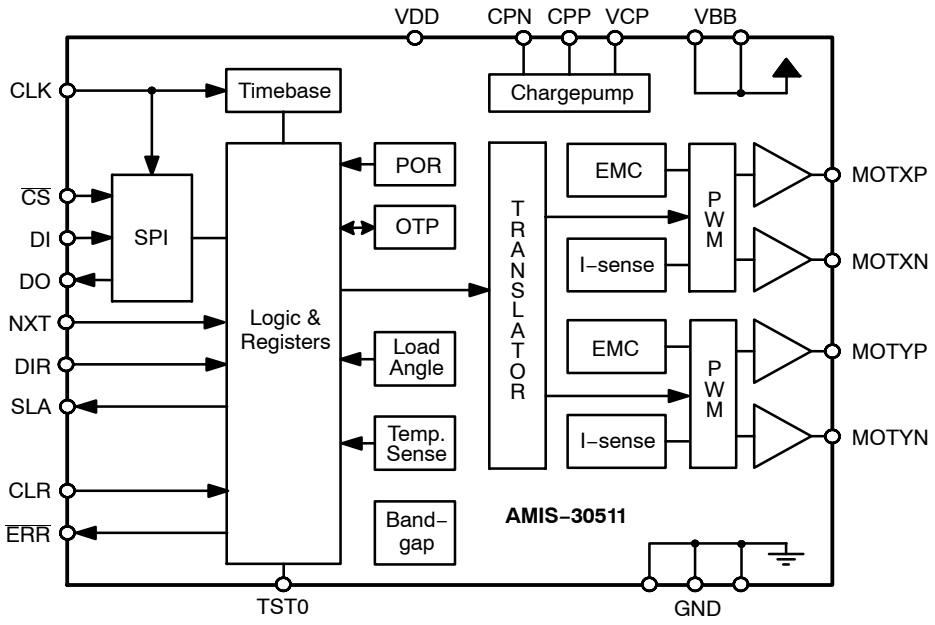



**Figure 1. Block Diagram**

**Table 1. Pin List and Descriptions**

| Name | Pin | Description |
|---|---|---|
| DO | 1 | SPI data output (open drain) |
| VDD | 2 | Logic Supply Input (needs external decoupling capacitor) |
| GND | 3 | Ground |
| DI | 4 | SPI data in |
| CLK | 5 | SPI clock input |
| NXT | 6 | Next micro−step input |
| DIR | 7 | Direction input |
| $\overline{ERR}$ | 8 | Error Output (open drain) |
| SLA | 9 | Speed Load Angle Output |
| CPN | 10 | Negative connection of charge pump capacitor |
| CPP | 11 | Positive connection of charge pump capacitor |
| VCP | 12 | Charge−pump filter−capacitor |
| CLR | 13 | “Clear” = Chip Reset input |
| $\overline{CS}$ | 14 | SPI chip select input |
| VBB | 15 | High Voltage Supply Input |
| MOTYP | 16 | Negative end of phase Y coil output |
| GND | 17 | Ground |
| MOTYN | 18 | Positive end of phase Y coil output |
| MOTXN | 19 | Positive end of phase X coil output |
| GND | 20 | Ground |
| MOTXP | 21 | Negative end of phase X coil output |
| VBB | 22 | High Voltage Supply Input |
| / | 23 | No Function (to be left open in normal operation) |
| TST0 | 24 | Test pin (to be tied to ground in normal operation) input |

**Table 2. Absolute Maximum Ratings**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{BB}$ | Analog DC supply voltage (Note 1) | −0.3 | +40 | V |
| $V_{DD}$ | Logic supply voltage | −0.3 | +7.0 | V |
| Tstrg | Storage temperature | −55 | +160 | °C |
| Tamb | Ambient temperature under bias | −50 | +150 | °C |
| $V_{ESD}$ | Electrostatic discharges on component level (Note 2) | −2 | +2 | kV |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. For limited time < 0.5 s.
2. Human body model (100 pF via 1.5 kΩ, according to JEDEC EIA−JESD22−A114−B).

**Table 3. Recommended Operating Conditions**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{BB}$ | Analog DC supply | +6 | +30 | V |
| $V_{DD}$ | Logic supply voltage | 4.75 | 5.25 | V |
| $T_a$ | Ambient temperature $V_{BB} \leq +18$ | −40 | +125 | °C |
| $T_a$ | Ambient temperature $V_{BB} \leq +30$ | −40 | +85 | °C |
| $T_j$ | Junction temperature | | +160 | °C |

NOTE: Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

**Table 4. DC Parameters** (The DC parameters are given for $V_{BB}$ and temperature in their operating ranges unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.)

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **SUPPLY INPUTS** | | | | | | | |
| $V_{BB}$ | VBB | Nominal operating supply range | | 6 | | 30 | V |
| $I_{BB}$ | | Total current consumption | Unloaded outputs | | | 8 | mA |
| $V_{DD}$ | VDD | Logic supply voltage | | 4.75 | 5 | 5.25 | V |
| $I_{DDD}$ | | Dynamic current (Note 3) | | | | 18 | mA |
| $I_{DDS}$ | | Sleep current (Note 4) | | | | 250 | μA |
| **POWER−ON−RESET (POR)** | | | | | | | |
| $V_{DDH}$ | VDD | Internal POR comparator threshold | VDD rising | 4.0 | 4.25 | 4.4 | V |
| $V_{DDL}$ | | Internal POR comparator threshold | VDD falling | | 3.68 | | V |
| **MOTORDRIVER** | | | | | | | |
| $I_{MDmax,Peak}$ | MOTXP MOTXN MOTYP MOTYN | Max current through motor coil in normal operation | | | 800 | | mA |
| $I_{MDmax,RMS}$ | | Max RMS current through coil in normal operation | | | 400 | | mA |
| $I_{MDabs}$ | | Absolute error on coil current | | −10 | | 10 | % |
| $I_{MDrel}$ | | Error on current ratio $I_{coilx}$ / $I_{coily}$ | | −7 | | 7 | % |
| $I_{SET\_TC}$ | | Temperature coefficient of coil current set−level, CUR[4:0] = 0 ..31 | −40°C ≤ $T_j$ ≤ 160°C | | −240 | | ppm/°C |
| $R_{HS}$ | | On−resistance high−side driver, CUR[4:0] = 0...31 | $V_{bb}$ = 12 V, $T_j$ = 27°C | | 0.45 | 0.56 | Ω |
| | | | $V_{bb}$ = 12 V, $T_j$ = 160°C | | 0.94 | 1.25 | Ω |
| $R_{LS3}$ | | On−resistance low−side driver, CUR[4:0] = 23...31 | $V_{bb}$ = 12 V, $T_j$ = 27°C | | 0.45 | 0.56 | Ω |
| | | | $V_{bb}$ = 12 V, $T_j$ = 160°C | | 0.94 | 1.25 | Ω |
| $R_{LS2}$ | | On−resistance low−side driver, CUR[4:0] = 16...22 | $V_{bb}$ = 12 V, $T_j$ = 27°C | | 0.90 | 1.2 | Ω |
| | | | $V_{bb}$ = 12 V, $T_j$ = 160°C | | 1.9 | 2.5 | Ω |
| $R_{LS1}$ | | On−resistance low−side driver, CUR[4:0] = 9...15 | $V_{bb}$ = 12 V, $T_j$ = 27°C | | 1.8 | 2.3 | Ω |
| | | | $V_{bb}$ = 12 V, $T_j$ = 160°C | | 3.8 | 5.0 | Ω |
| $R_{LS0}$ | | On−resistance low−side driver, CUR[4:0] = 0...8 | $V_{bb}$ = 12 V, $T_j$ = 27°C | | 3.6 | 4.5 | Ω |
| | | | $V_{bb}$ = 12 V, $T_j$ = 160°C | | 7.5 | 10 | Ω |
| $I_{Mpd}$ | | Pull−down current | HiZ mode | | 0.5 | | mA |
| **DIGITAL INPUTS** | | | | | | | |
| $I_{leak}$ | DI, CLK NXT, DIR CLR, CSB | Input leakage (Note 5) | Tj = 160°C | | | 1 | μA |
| $V_{IL}$ | | Logic low threshold | | 0 | | 0.65 | V |
| $V_{IH}$ | | Logic high threshold | | 2.20 | | $V_{DD}$ | V |
| $R_{pd\_CLR}$ | CLR | Internal pull−down resistor | | 120 | | 300 | kΩ |
| $R_{pd\_TST}$ | TST0 | Internal pull−down resistor | | 3 | | 9 | kΩ |

3. Current with oscillator running and all analogue cells active. All outputs unloaded, no floating inputs
4. Current with all analogue cells in power down. Logic is powered but no clocks running. All outputs unloaded, no floating inputs
5. Not valid for pins with internal pull−down resistor
6. Thermal shutdown and low temperature warning are derived from thermal warning.
7. No more than 100 cumulated hours in life time above $Tt_w$

**Table 4. DC Parameters** (The DC parameters are given for $V_{BB}$ and temperature in their operating ranges unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.)

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **DIGITAL OUTPUTS** | | | | | | | |
| $V_{OL}$ | DO, ERRB | Logic Low level open drain | IOL = 5 mA | | | 0.5 | V |
| **THERMAL WARNING AND SHUTDOWN** | | | | | | | |
| $T_{tw}$ | | Thermal warning | | 138 | 145 | 152 | °C |
| $T_{tsd}$ (Notes 6,7) | | Thermal shutdown | | | $T_{tw}$ + 20 | | °C |
| **CHARGE PUMP** | | | | | | | |
| $V_{cp}$ | VCP | Output voltage | 6 V < $V_{BB}$ < 15 V | | 2 * $V_{BB}$ − 2.5 | | V |
| | | | 15 V < $V_{BB}$ < 30 V | $V_{BB}$+11 | $V_{BB}$+12.8 | $V_{BB}$+15 | V |
| $C_{buffer}$ | | External buffer capacitor | | 180 | 220 | 470 | nF |
| $C_{pump}$ | CPP CPN | External pump capacitor | | 180 | 220 | 470 | nF |
| **SPEED AND LOAD ANGLE OUTPUT** | | | | | | | |
| $V_{out}$ | SLA | Output voltage range | | 0.5 | | 4.5 | V |
| $V_{off}$ | | Output offset the SLA pin | 0.2 V < Vsla < Vdd − 0,2 V | -25 | | 25 | mV |
| $R_{out}$ | | Output resistance SLA pin | | | | 1 | kΩ |
| $C_{load}$ | | Load capacitance SLA pin | | | | 50 | pF |
| $G_{sla}$ | | Gain of SLA pin = $V_{BEMF}$ / $V_{COIL}$ | SLAG=0<br>SLAG=1 | | 0,5<br>0,25 | | |

3. Current with oscillator running and all analogue cells active. All outputs unloaded, no floating inputs
4. Current with all analogue cells in power down. Logic is powered but no clocks running. All outputs unloaded, no floating inputs
5. Not valid for pins with internal pull−down resistor
6. Thermal shutdown and low temperature warning are derived from thermal warning.
7. No more than 100 cumulated hours in life time above $Tt_w$

**Table 5. AC Parameters** (The AC parameters are given for $V_{BB}$ and temperature in their operating ranges.)

| Symbol | Pin(s) | Parameter | Remark/Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Internal Oscillator** | | | | | | | |
| $f_{osc}$ | | Frequency of internal oscillator | | 3.6 | 4 | 4.4 | MHz |
| **MOTORDRIVER** | | | | | | | |
| $f_{PWM}$ | MOTxx | PWM frequency | Frequency depends only on internal oscillator | 20.8 | 22.8 | 24.8 | kHz |
| | | Double PWM frequency | | 41.6 | 45.6 | 49.6 | kHz |
| $f_j$ | | PWM Jitter frequency | | | | | Hz |
| $f_d$ | | PWM Jitter depth | | | | | % $f_{PWM}$ |
| $Tb_{rise}$ | MOTxx | turn−on voltage slope, 10% to 90% $I_{MD}$ = 800 mA | EMC[1:0] = 00 | | 150 | | V/μs |
| | | | EMC[1:0] = 01 | | 100 | | V/μs |
| | | | EMC[1:0] = 10 | | 50 | | V/μs |
| | | | EMC[1:0] = 11 | | 25 | | V/μs |
| $Tb_{fall}$ | MOTxx | turn−off voltage slope, 90% to 10% $I_{MD}$ = 800 mA | EMC[1:0] = 00 | | 150 | | V/μs |
| | | | EMC[1:0] = 01 | | 100 | | V/μs |
| | | | EMC[1:0] = 10 | | 50 | | V/μs |
| | | | EMC[1:0] = 11 | | 25 | | V/μs |
| **DIGITAL OUTPUTS** | | | | | | | |
| $T_{H2L}$ | DO ERRB | Output fall−time from $V_{inH}$ to $V_{inL}$ | Capacitive load 400 pF and pull−up resistor of 1.5 kΩ | | | 50 | ns |
| **CHARGE PUMP** | | | | | | | |
| $f_{CP}$ | CPN CPP | Charge pump frequency | | | 250 | | kHz |
| $T_{CPU}$ | MOTxx | Start−up time of charge pump | Spec external components | | | | |
| **CLR FUNCTION** | | | | | | | |
| $T_{CLR}$ | CLR | Hard reset duration time | | 20 | – | 90 | μs |
| **NXT FUNCTION** | | | | | | | |
| $t_{NXT\_HI}$ | NXT | NXT minimum, high pulse width | See Figure 2 | 2 | | | μs |
| $t_{NXT\_LO}$ | | NXT minimum, low pulse width | See Figure 2 | 2 | | | μs |
| $t_{DIR\_SET}$ | | NXT hold time, following change of DIR | See Figure 2 | 0.5 | | | μs |
| $t_{DIR\_HOLD}$ | | NXT hold time, before change of DIR | See Figure 2 | 0.5 | | | μs |

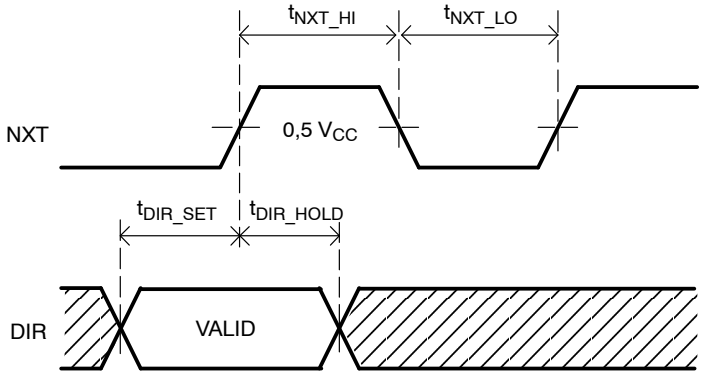



**Figure 2. NXT−input Timing Diagram**

**Table 6. Timing Parameters**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{CLK}$ | SPI clock period | 1 | | | μs |
| $t_{CLK\_HIGH}$ | SPI clock high time | 100 | | | ns |
| $t_{CLK\_LOW}$ | SPI clock low time | 100 | | | ns |
| $t_{SET\_DI}$ | DI set up time, valid data before rising edge of CLK | 50 | | | ns |
| $t_{HOLD\_DI}$ | DI hold time, hold data after rising edge of CLK | 50 | | | ns |
| $t_{CSB\_HIGH}$ | CSB high time | 2.5 | | | μs |
| $t_{SET\_CSB}$ | CSB set up time, CSB low before rising edge of CLK | 100 | | | ns |
| $t_{SET\_CLK}$ | CLK set up time, CLK low before rising edge of CSB | 100 | | | ns |

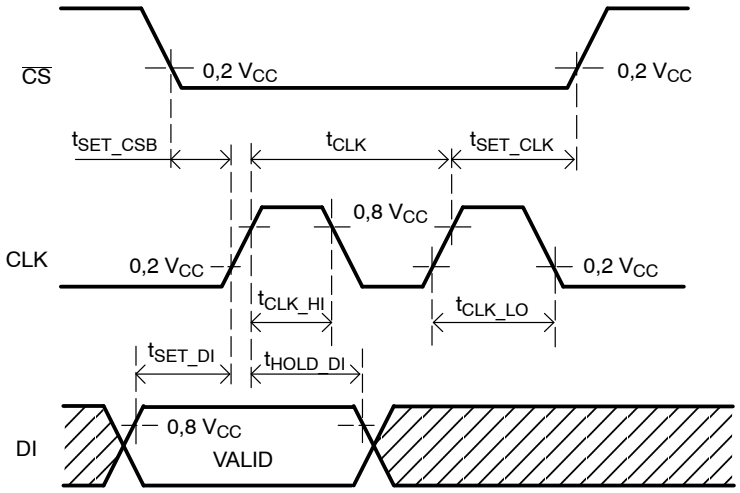



**Figure 3. SPI Timing**

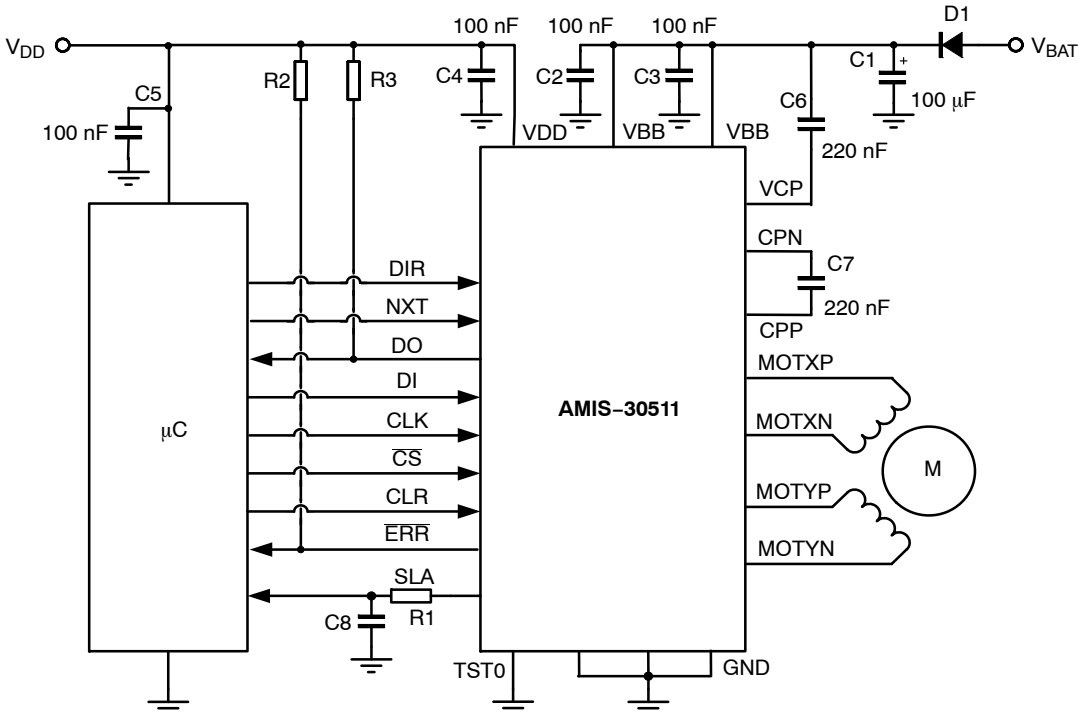



**Figure 4. Typical Application Schematic**

**Table 7. External Components List and Description**

| Component | Function | Typ. Value | Tolerance | Unit |
|---|---|---|---|---|
| $C_1$ | $V_{BB}$ buffer capacitor (Note 8) | 100 | −20 +80% | µF |
| $C_2$, $C_3$ | $V_{BB}$ decoupling block capacitor | 100 | −20 +80% | nF |
| $C_4$ | $V_{DD}$ buffer capacitor | 220 | ±20% | nF |
| $C_5$ | $V_{DD}$ buffer capacitor | 100 | ±20% | nF |
| $C_6$ | Charge pump buffer capacitor | 220 | ±20% | nF |
| $C_7$ | Charge pump pumping capacitor | 220 | ±20% | nF |
| $C_8$ | Low pass filter SLA | 1 | ±20% | nF |
| $R_1$ | Low pass filter SLA | 5.6 | ±1% | kΩ |
| $R_2$, $R_3$ | Pull up resistor | 4.7 | ±1% | kΩ |
| $D_1$ | Optional reverse protection diode | e.g. 1N4003 | | |

8. Low ESR < 1 Ohm.

## Functional Description

### H−Bridge Drivers

A full H−bridge is integrated for each of the two stator windings. Each H−bridge consists of two low−side and two high−side N−type MOSFET switches. Writing logic ‘0’ in bit <MOTEN> disables all drivers (high−impedance). Writing logic ‘1’ in this bit enables both bridges and current can flow in the motor stator windings.

In order to avoid large currents through the H−bridge switches, it is guaranteed that the top− and bottom−switches of the same half−bridge are never conductive simultaneously (interlock delay).

A two−stage protection against shorts on motor lines is implemented. In a first stage, the current in the driver is limited. Secondly, when excessive voltage is sensed across the transistor, the transistor is switched−off.

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. The output slope is defined by the gate−drain capacitance of output transistor and the (limited) current that drives the gate. There are two trimming bits for slope control (Table 23: SPI Control Parameter Overview EMC[1:0]).

The power transistors are equipped with so−called “active diodes”: when a current is forced through the transistor switch in the reverse direction, i.e. from source to drain, then the transistor is switched on. This ensures that most of the current flows through the channel of the transistor instead of through the inherent parasitic drain−bulk diode of the transistor.

Depending on the desired current range and the micro−step position at hand, the Rdson of the low−side transistors will be adapted such that excellent current−sense accuracy is maintained. The Rdson of the high−side transistors remain unchanged, see Table 4: DC Parameters for more details.

### PWM Current Control

A PWM comparator compares continuously the actual winding current with the requested current and feeds back the information to a digital regulation loop. This loop then generates a PWM signal, which turns on/off the H−bridge switches. The switching points of the PWM duty−cycle are synchronized to the on−chip PWM clock. The frequency of the PWM controller can be doubled and an artificial jitter can be added (Table 12: SPI Control Register 1). The PWM frequency will not vary with changes in the supply voltage. Also variations in motor−speed or load−conditions of the motor have no effect. There are no external components required to adjust the PWM frequency.

### Automatic Forward and Slow−Fast Decay

The PWM generation is in steady−state using a combination of forward and slow−decay. The absence of fast−decay in this mode, guarantees the lowest possible current−ripple “by design”. For transients to lower current levels, fast−decay is automatically activated to allow high−speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

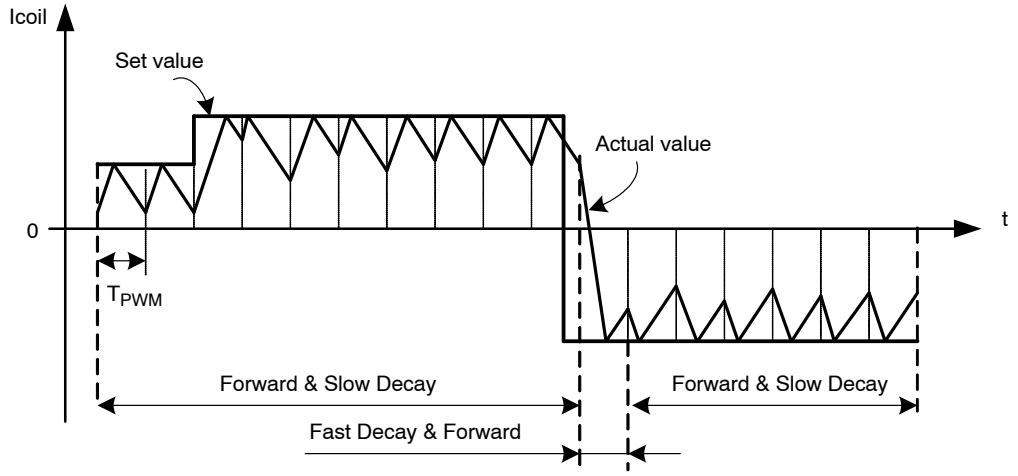



**Figure 5. Forward and Slow/Fast Decay PWM**

In case the supply voltage is lower than 2*Bemf, then the duty cycle of the PWM is adapted automatically to >50% to maintain the requested average current in the coils. This process is completely automatic and requires no additional parameters for operation. The over−all current−ripple is divided by two if PWM frequency is doubled (Table 12: SPI Control Register 1).

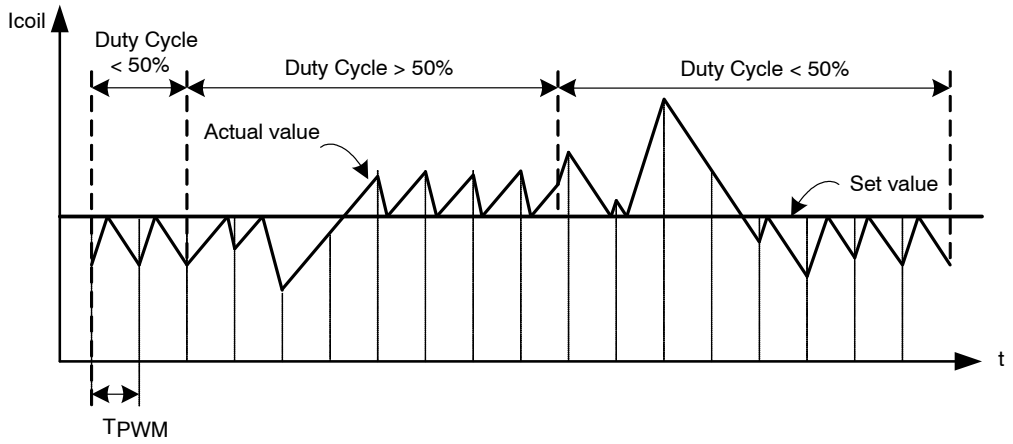



**Figure 6. Automatic Duty Cycle Adaptation**

## Step Translator

### Step Mode

The step translator provides the control of the motor by means of SPI register Stepmode: SM[2:0], SPI register DIRCNTRL, and input pins DIR and NXT. It is translating consecutive steps in corresponding currents in both motor coils for a given step mode.

One out of seven possible stepping modes can be selected through SPI−bits SM[2:0] (Table 24: SPI Control Parameter Overview SM[2:0]) After power−on or hard reset, the coil−current translator is set to the default 1/32 micro−stepping at position '0'. Upon changing the step mode, the translator jumps to position 0* of the corresponding stepping mode. When remaining in the same step mode, subsequent translator positions are all in the same column and increased or decreased with 1. Table 9 lists the output current versus the translator position.

As shown in Figure 7 the output current−pairs can be projected approximately on a circle in the $(I_x,I_y)$ plane. There is, however, one exception: uncompensated half step. In this step mode the currents are not regulated to a fraction of Imax but are in all intermediate steps regulated at 100 percent. In the $(I_x,I_y)$ plane the current−pairs are projected on a square. Table 8 lists the output current versus the translator position for this case.

**Table 8. Square Translator Table for Full Step and Uncompensated Half Step**

| | Stepmode ( SM[2:0] ) | | % of Imax | |
|---|---|---|---|---|
| | 101 | 110 | | |
| MSP[6:0] | Uncompensated Half−Step | Full Step | Coil x | Coil y |
| 000 0000 | 0* | − | 0 | 100 |
| 001 0000 | 1 | 1 | 100 | 100 |
| 010 0000 | 2 | − | 100 | 0 |
| 011 0000 | 3 | 2 | 100 | −100 |
| 100 0000 | 4 | − | 0 | −100 |
| 101 0000 | 5 | 3 | −100 | −100 |
| 110 0000 | 6 | − | −100 | 0 |
| 111 0000 | 7 | 0* | −100 | 100 |

**Table 9. Circular Translator Table**

| | Stepmode ( SM[2:0] ) | | | | | % of Imax | |
|---|---|---|---|---|---|---|---|
| | 000 | 001 | 010 | 011 | 100 | | |
| MSP[6:0] | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | Coil x | Coil y |
| 000 0000 | ‘0’ | 0* | 0* | 0* | 0* | 0 | 100 |
| 000 0001 | 1 | – | – | – | – | 3.5 | 98.8 |
| 000 0010 | 2 | 1 | – | – | – | 8.1 | 97.7 |
| 000 0011 | 3 | – | – | – | – | 12.7 | 96.5 |
| 000 0100 | 4 | 2 | 1 | – | – | 17.4 | 95.3 |
| 000 0101 | 5 | – | – | – | – | 22.1 | 94.1 |
| 000 0110 | 6 | 3 | – | – | – | 26.7 | 93 |
| 000 0111 | 7 | – | – | – | – | 31.4 | 91.8 |
| 000 1000 | 8 | 4 | 2 | 1 | – | 34.9 | 89.5 |
| 000 1001 | 9 | – | – | – | – | 38.3 | 87.2 |
| 000 1010 | 10 | 5 | – | – | – | 43 | 84.9 |
| 000 1011 | 11 | – | – | – | – | 46.5 | 82.6 |
| 000 1100 | 12 | 6 | 3 | – | – | 50 | 79 |
| 000 1101 | 13 | – | – | – | – | 54.6 | 75.5 |
| 000 1110 | 14 | 7 | – | – | – | 58.1 | 72.1 |
| 000 1111 | 15 | – | – | – | – | 61.6 | 68.6 |
| 001 0000 | 16 | 8 | 4 | 2 | 1 | 65.1 | 65.1 |
| 001 0001 | 17 | – | – | – | – | 68.6 | 61.6 |
| 001 0010 | 18 | 9 | – | – | – | 72.1 | 58.1 |
| 001 0011 | 19 | – | – | – | – | 75.5 | 54.6 |
| 001 0100 | 20 | 10 | 5 | – | – | 79 | 50 |
| 001 0101 | 21 | – | – | – | – | 82.6 | 46.5 |
| 001 0110 | 22 | 11 | – | – | – | 84.9 | 43 |
| 001 0111 | 23 | – | – | – | – | 87.2 | 38.3 |
| 001 1000 | 24 | 12 | 6 | 3 | – | 89.5 | 34.9 |
| 001 1001 | 25 | – | – | – | – | 91.8 | 31.4 |
| 001 1010 | 26 | 13 | – | – | – | 93 | 26.7 |
| 001 1011 | 27 | – | – | – | – | 94.1 | 22.1 |
| 001 1100 | 28 | 14 | 7 | – | – | 95.3 | 17.4 |
| 001 1101 | 29 | – | – | – | – | 96.5 | 12.7 |
| 001 1110 | 30 | 15 | – | – | – | 97.7 | 8.1 |
| 001 1111 | 31 | – | – | – | – | 98.8 | 3.5 |
| 010 0000 | 32 | 16 | 8 | 4 | 2 | 100 | 0 |
| 010 0001 | 33 | – | – | – | – | 98.8 | −3.5 |
| 010 0010 | 34 | 17 | – | – | – | 97.7 | −8.1 |
| 010 0011 | 35 | – | – | – | – | 96.5 | −12.7 |
| 010 0100 | 36 | 18 | 9 | – | – | 95.3 | −17.4 |
| 010 0101 | 37 | – | – | – | – | 94.1 | −22.1 |
| 010 0110 | 38 | 19 | – | – | – | 93 | −26.7 |
| 010 0111 | 39 | – | – | – | – | 91.8 | −31.4 |
| 010 1000 | 40 | 20 | 10 | 5 | – | 89.5 | −34.9 |
| 010 1001 | 41 | – | – | – | – | 87.2 | −38.3 |
| 010 1010 | 42 | 21 | – | – | – | 84.9 | −43 |

**Table 9. Circular Translator Table**

| | Stepmode ( SM[2:0] ) | | | | | % of Imax | |
|---|---|---|---|---|---|---|---|
| | 000 | 001 | 010 | 011 | 100 | | |
| MSP[6:0] | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | Coil x | Coil y |
| 010 1011 | 43 | – | – | – | – | 82.6 | −46.5 |
| 010 1100 | 44 | 22 | 11 | – | – | 79 | −50 |
| 010 1101 | 45 | – | – | – | – | 75.5 | −54.6 |
| 010 1110 | 46 | 23 | – | – | – | 72.1 | −58.1 |
| 010 1111 | 47 | – | – | – | – | 68.6 | −61.6 |
| 011 0000 | 48 | 24 | 12 | 6 | 3 | 65.1 | −65.1 |
| 011 0001 | 49 | – | – | – | – | 61.6 | −68.6 |
| 011 0010 | 50 | 25 | – | – | – | 58.1 | −72.1 |
| 011 0011 | 51 | – | – | – | – | 54.6 | −75.5 |
| 011 0100 | 52 | 26 | 13 | – | – | 50 | −79 |
| 011 0101 | 53 | – | – | – | – | 46.5 | −82.6 |
| 011 0110 | 54 | 27 | – | – | – | 43 | −84.9 |
| 011 0111 | 55 | – | – | – | – | 38.3 | −87.2 |
| 011 1000 | 56 | 28 | 14 | 7 | – | 34.9 | −89.5 |
| 011 1001 | 57 | – | – | – | – | 31.4 | −91.8 |
| 011 1010 | 58 | 29 | – | – | – | 26.7 | −93 |
| 011 1011 | 59 | – | – | – | – | 22.1 | −94.1 |
| 011 1100 | 60 | 30 | 15 | – | – | 17.4 | −95.3 |
| 011 1101 | 61 | – | – | – | – | 12.7 | −96.5 |
| 011 1110 | 62 | 31 | – | – | – | 8.1 | −97.7 |
| 011 1111 | 63 | – | – | – | – | 3.5 | −98.8 |
| 100 0000 | 64 | 32 | 16 | 8 | 4 | 0 | −100 |
| 100 0001 | 65 | – | – | – | – | −3.5 | −98.8 |
| 100 0010 | 66 | 33 | – | – | – | −8.1 | −97.7 |
| 100 0011 | 67 | – | – | – | – | −12.7 | −96.5 |
| 100 0100 | 68 | 34 | 17 | – | – | −17.4 | −95.3 |
| 100 0101 | 69 | – | – | – | – | −22.1 | −94.1 |
| 100 0110 | 70 | 35 | – | – | – | −26.7 | −93 |
| 100 0111 | 71 | – | – | – | – | −31.4 | −91.8 |
| 100 1000 | 72 | 36 | 18 | 9 | – | −34.9 | −89.5 |
| 100 1001 | 73 | – | – | – | – | −38.3 | −87.2 |
| 100 1010 | 74 | 37 | – | – | – | −43 | −84.9 |
| 100 1011 | 75 | – | – | – | – | −46.5 | −82.6 |
| 100 1100 | 76 | 38 | 19 | – | – | −50 | −79 |
| 100 1101 | 77 | – | – | – | – | −54.6 | −75.5 |
| 100 1110 | 78 | 39 | – | – | – | −58.1 | −72.1 |
| 100 1111 | 79 | – | – | – | – | −61.6 | −68.6 |
| 101 0000 | 80 | 40 | 20 | 10 | 5 | −65.1 | −65.1 |
| 101 0001 | 81 | – | – | – | – | −68.6 | −61.6 |
| 101 0010 | 82 | 41 | – | – | – | −72.1 | −58.1 |
| 101 0011 | 83 | – | – | – | – | −75.5 | −54.6 |
| 101 0100 | 84 | 42 | 21 | – | – | −79 | −50 |
| 101 0101 | 85 | – | – | – | – | −82.6 | −46.5 |

**Table 9. Circular Translator Table**

| | Stepmode ( SM[2:0] ) | | | | | % of Imax | |
|---|---|---|---|---|---|---|---|
| | 000 | 001 | 010 | 011 | 100 | | |
| MSP[6:0] | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | Coil x | Coil y |
| 101 0110 | 86 | 43 | – | – | – | −84.9 | −43 |
| 101 0111 | 87 | – | – | – | – | −87.2 | −38.3 |
| 101 1000 | 88 | 44 | 22 | 11 | – | −89.5 | −34.9 |
| 101 1001 | 89 | – | – | – | – | −91.8 | −31.4 |
| 101 1010 | 90 | 45 | – | – | – | −93 | −26.7 |
| 101 1011 | 91 | – | – | – | – | −94.1 | −22.1 |
| 101 1100 | 92 | 46 | 23 | – | – | −95.3 | −17.4 |
| 101 1101 | 93 | – | – | – | – | −96.5 | −12.7 |
| 101 1110 | 94 | 47 | – | – | – | −97.7 | −8.1 |
| 101 1111 | 95 | – | – | – | – | −98.8 | −3.5 |
| 110 0000 | 96 | 48 | 24 | 12 | 6 | −100 | 0 |
| 110 0001 | 97 | – | – | – | – | −98.8 | 3.5 |
| 110 0010 | 98 | 49 | – | – | – | −97.7 | 8.1 |
| 110 0011 | 99 | – | – | – | – | −96.5 | 12.7 |
| 110 0100 | 100 | 50 | 25 | – | – | −95.3 | 17.4 |
| 110 0101 | 101 | – | – | – | – | −94.1 | 22.1 |
| 110 0110 | 102 | 51 | – | – | – | −93 | 26.7 |
| 110 0111 | 103 | – | – | – | – | −91.8 | 31.4 |
| 110 1000 | 104 | 52 | 26 | 13 | – | −89.5 | 34.9 |
| 110 1001 | 105 | – | – | – | – | −87.2 | 38.3 |
| 110 1010 | 106 | 53 | – | – | – | −84.9 | 43 |
| 110 1011 | 107 | – | – | – | – | −82.6 | 46.5 |
| 110 1100 | 108 | 54 | 27 | – | – | −79 | 50 |
| 110 1101 | 109 | – | – | – | – | −75.5 | 54.6 |
| 110 1110 | 110 | 55 | – | – | – | −72.1 | 58.1 |
| 110 1111 | 111 | – | – | – | – | −68.6 | 61.6 |
| 111 0000 | 112 | 56 | 28 | 14 | 7 | −65.1 | 65.1 |
| 111 0001 | 113 | – | – | – | – | −61.6 | 68.6 |
| 111 0010 | 114 | 57 | – | – | – | −58.1 | 72.1 |
| 111 0011 | 115 | – | – | – | – | −54.6 | 75.5 |
| 111 0100 | 116 | 58 | 29 | – | – | −50 | 79 |
| 111 0101 | 117 | – | – | – | – | −46.5 | 82.6 |
| 111 0110 | 118 | 59 | – | – | – | −43 | 84.9 |
| 111 0111 | 119 | – | – | – | – | −38.3 | 87.2 |
| 111 1000 | 120 | 60 | 30 | 15 | – | −34.9 | 89.5 |
| 111 1001 | 121 | – | – | – | – | −31.4 | 91.8 |
| 111 1010 | 122 | 61 | – | – | – | −26.7 | 93 |
| 111 1011 | 123 | – | – | – | – | −22.1 | 94.1 |
| 111 1100 | 124 | 62 | 31 | – | – | −17.4 | 95.3 |
| 111 1101 | 125 | – | – | – | – | −12.7 | 96.5 |
| 111 1110 | 126 | 63 | – | – | – | −8.1 | 97.7 |
| 111 1111 | 127 | – | – | – | – | −3.5 | 98.8 |

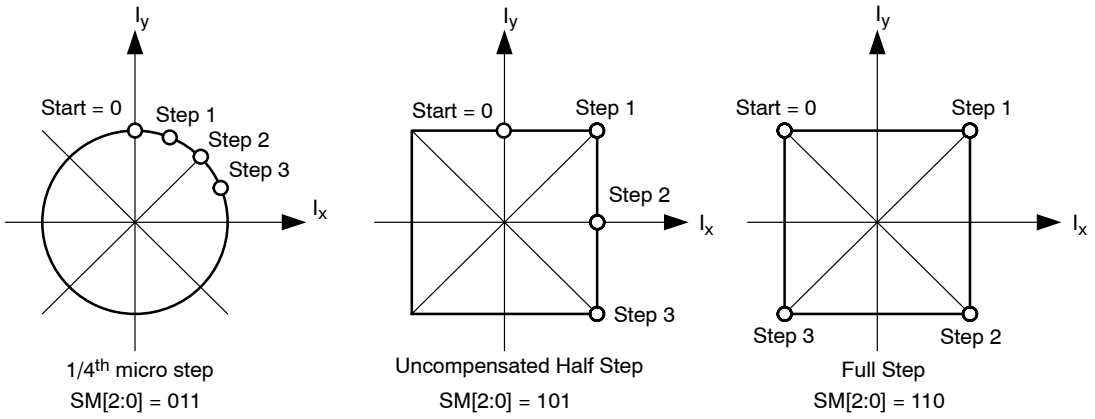



**Figure 7. Translator Table: Circular and Square**

### Direction

The direction of rotation is selected by means of following combination of the DIR input pin and the SPI−controlled direction bit <DIRCTRL>. (Table 12: SPI Control Register 1)

### NXT Input

Changes on the NXT input will move the motor current one step up/down in the translator table. Depending on the NXT−polarity bit <NXTP> (Table 12: SPI Control Register 1), the next step is initiated either on the rising edge or the falling edge of the NXT input.

### Translator Position

The translator position can be read in Table 28: SPI Status Register 3. This is a 7−bit number equivalent to the 1/32th micro−step from Table 9: Circular Translator Table. The translator position is updated immediately following a NXT trigger.

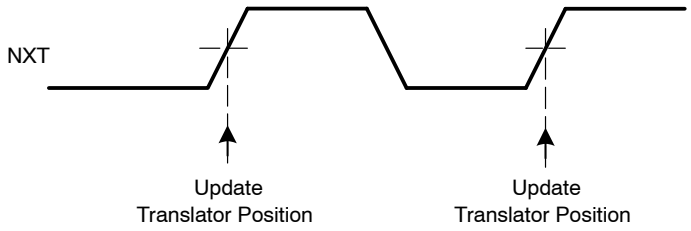


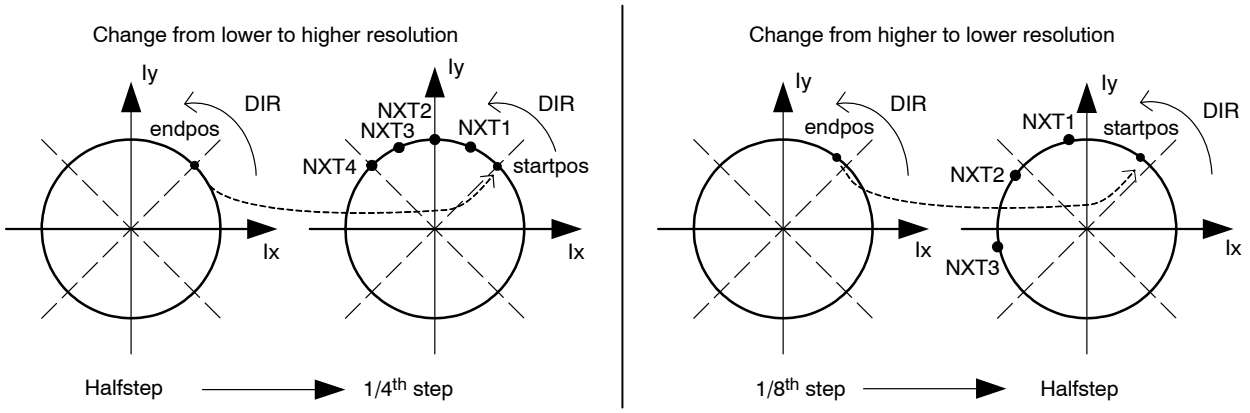

**Figure 8. Translator Position Timing Diagram**

### Synchronization of Step Mode and NXT Input

When step mode is re−programmed to another resolution (Table 11: SPI Control Register 0), then this is put in effect immediately upon the first arriving “NXT” input. If the micro−stepping resolution is increased (see Figure 9) then the coil currents will be regulated to the nearest micro−step, according to the fixed grid of the increased resolution. If however the micro−stepping resolution is decreased, then it is possible to introduce an offset (or phase shift) in the micro−step translator table.

If the step resolution is decreased at a translator table position that is shared both by the old and new resolution setting, then the offset is zero and micro−stepping proceeds according to the translator table.

If the translator position is not shared both by the old and new resolution setting, then the micro−stepping proceeds with an offset relative to the translator table (See Figure 8 right hand side).




Left: Change from lower to higher resolution. The left−hand side depicts the ending half−step position during which a new step mode resolution was programmed. The right−hand side diagram shows the effect of subsequent NXT commands on the micro−step position.

Right: Change from higher to lower resolution. The left−hand side depicts the ending micro−step position during which a new step mode resolution was programmed. The right−hand side diagram shows the effect of subsequent NXT commands on the half−step position.

**Figure 9. NXT−Step Mode Synchronization**

NOTE: It is advised to reduce the micro−stepping resolution only at micro−step positions that overlap with desired micro−step positions of the new resolution.

### Programmable Peak−Current

The amplitude of the current waveform in the motor coils (coil peak current = Imax) is adjusted by means of an SPI parameter “CUR[4:0]” (Table 11: SPI Control Register 0). Whenever this parameter is changed, the coil−currents will be updated immediately at the next PWM period. The impedance of the bottom drivers is adapted with the current range: See Table 4: DC Parameters.

**Table 10. Programmable Peak Current CUR[4:0]**

| Current Range | CUR[4:0] Index | Current (mA) | Current Range | CUR[4:0] Index | Current (mA) |
|---|---|---|---|---|---|
| 0 | 0 | 15 | 2 | 16 | 181 |
| | 1 | 30 | | 17 | 200 |
| | 2 | 45 | | 18 | 221 |
| | 3 | 50 | | 19 | 244 |
| | 4 | 55 | | 20 | 269 |
| | 5 | 61 | | 21 | 297 |
| | 6 | 67 | | 22 | 328 |
| | 7 | 74 | 3 | 23 | 362 |
| | 8 | 82 | | 24 | 400 |
| 1 | 9 | 91 | | 25 | 441 |
| | 10 | 100 | | 26 | 487 |
| | 11 | 110 | | 27 | 538 |
| | 12 | 122 | | 28 | 594 |
| | 13 | 135 | | 29 | 656 |
| | 14 | 149 | | 30 | 724 |
| | 15 | 164 | | 31 | 800 |

NOTE: Changing the current over different current ranges might lead to false over current triggering.

### Speed and Load Angle Output

The SLA−pin provides an output voltage that indicates the level of the Back−e.m.f. voltage of the motor. This Back−e.m.f. voltage is sampled during every so−called “coil current zero crossings”. Per coil, two zero−current positions exist per electrical period, yielding in total four zero−current observation points per electrical period.

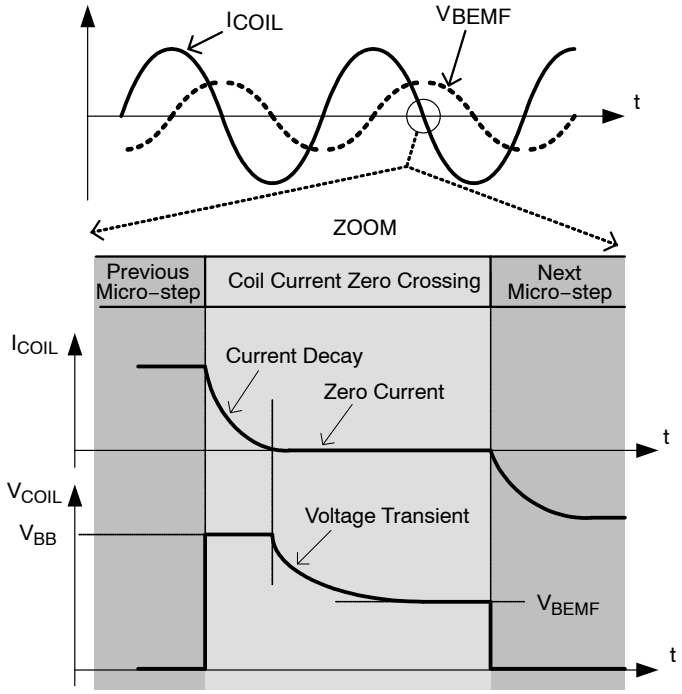



**Figure 10. Principle of Bemf Measurement**

Because of the relatively high recirculation currents in the coil during current decay, the coil voltage $V_{COIL}$ shows a transient behavior. As this transient is not always desired in application software, two operating modes can be selected by means of the bit <SLAT> (see “SLA−transparency” in Table 13: SPI Control Register 2). The SLA pin shows in “transparent mode” full visibility of the voltage transient behavior. This allows a sanity−check of the speed−setting versus motor operation and characteristics and supply voltage levels. If the bit “SLAT” is cleared, then only the voltage samples at the end of each coil current zero crossing are visible on the SLA−pin. Because the transient behavior of the coil voltage is not visible any more, this mode generates smoother Back e.m.f. input for post−processing, e.g. by software.

In order to bring the sampled Back e.m.f. to a descent output level (0 to 5 V), the sampled coil voltage $V_{COIL}$ is divided by 2 or by 4. This divider is set through an SPI bit <SLAG>. (Table 13: SPI Control Register 2)

The following drawing illustrates the operation of the SLA−pin and the transparency−bit. “PWMsh” and “Icoil=0” are internal signals that define together with SLAT the sampling and hold moments of the coil voltage.

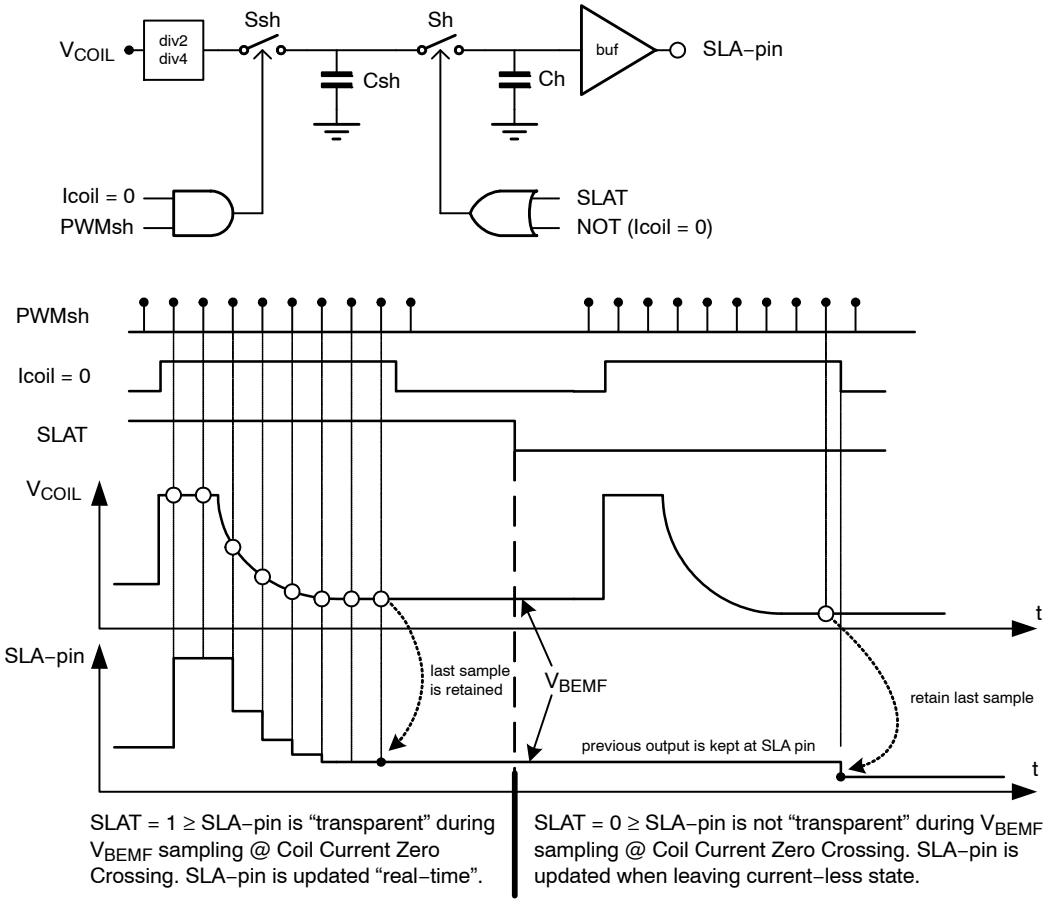



**Figure 11. Timing Diagram of SLA−pin**

## Warning, Error Detection and Diagnostics Feedback

### Thermal Warning and Shutdown

When junction temperature rises above TTW, the thermal warning bit <TW> is set (Table 25: SPI Status Register 0). If junction temperature increases above thermal shutdown level, then the circuit goes in “thermal shutdown” mode (<TSD>) and all driver transistors are disabled (high impedance) (Table 27: SPI Status Register 2). The conditions to reset flag <TSD> is to be at a temperature lower than TTW and to clear the <TSD> flag by reading it using any SPI read command.

### Over−Current Detection

The over−current detection circuit monitors the load current in each activated output stage. If the load current exceeds the over−current detection threshold, then the over−current flag is set and the drivers are switched off to reduce the power dissipation and to protect the integrated circuit. Each driver transistor has an individual detection bit in the Table 26: SPI Status Register 1 and Table 27: SPI Status Register 2 (<OVCXij> and <OVCYij>). Error condition is latched and the microcontroller needs to clean the status bits to reactivate the drivers.

NOTE: Successive reading the SPI Status Registers 1 and 2 in case of a short circuit condition, may lead to damage to the drivers.

### Open Coil Detection

Open coil detection is based on the observation of 100 percent duty cycle of the PWM regulator. If in a coil 100 percent duty cycle is detected for longer than 200ms then the related driver transistors are disabled (high−impedance) and an appropriate bit in the SPI status register is set (<OPENX> or <OPENY>). (Table 25: SPI Status Register 0).

### Charge Pump Failure

The charge pump is an important circuit that guarantees low Rdson for all drivers, especially for low supply voltages. If supply voltage is too low or external components are not properly connected to guarantee Rdson of the drivers, then the bit <CPFAIL> is set in the Table 25: SPI Status Register 0. Also after power−on−reset the charge pump voltage will need some time to exceed the required threshold. During that time <CPFAIL> will be set to “1”.

### Error Output

This is a digital output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = <TW> OR <TSD> OR <OVCXij> OR <OVCYij> OR <OPENi> OR <CPFAIL>

### CLR pin (=Hard Reset)

Logic 0 on CLR pin allows normal operation of the chip. To reset the complete digital inside AMIS−30511, the input CLR needs to be pulled to logic 1 during minimum time given by $T_{CLR}$. (Table 5: AC Parameters) This reset function clears all internal registers without the need of a power−cycle. The operation of all analog circuits is depending on the reset state of the digital, charge pump remains active. Logic 0 on CLR pin resumes normal operation again.

### Sleep Mode

The bit <SLP> in Table 13: SPI Control Register 2 is provided to enter a so−called “sleep mode”. This mode allows reduction of current−consumption when the motor is not in operation. The effect of sleep mode is as follows:

- The drivers are put in HiZ
- All analog circuits are disabled and in low−power mode
- All internal registers are maintaining their logic content
- NXT and DIR inputs are forbidden
- SPI communication remains possible (slight current increase during SPI communication)
- Reset of chip is possible through CLR pin
- Oscillator and digital clocks are silent, except during SPI communication

Normal operation is resumed after writing logic ‘0’ to bit <SLP>. A start−up time is needed for the charge pump to stabilize. After this time, NXT commands can be issued.

## SPI Interface

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with AMIS−30511. The implemented SPI block is designed to interface directly with numerous micro−controllers from several manufacturers. AMIS−30511 acts always as a Slave and can't initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

### SPI Transfer Format and Pin Signal

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI). DO signal is the output from the Slave (AMIS−30511), and DI signal is the output from the Master. A chip select line (CSB) allows individual selection of a Slave SPI device in a multiple−slave system. The CSB line is active low. If AMIS−30511 is not selected, DO is pulled up with the external pull up resistor. Since AMIS−30511 operates as a Slave in MODE 0 (CPOL = 0; CPHA = 0) it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation. The SPI clock idles low between the transferred bytes.

The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.

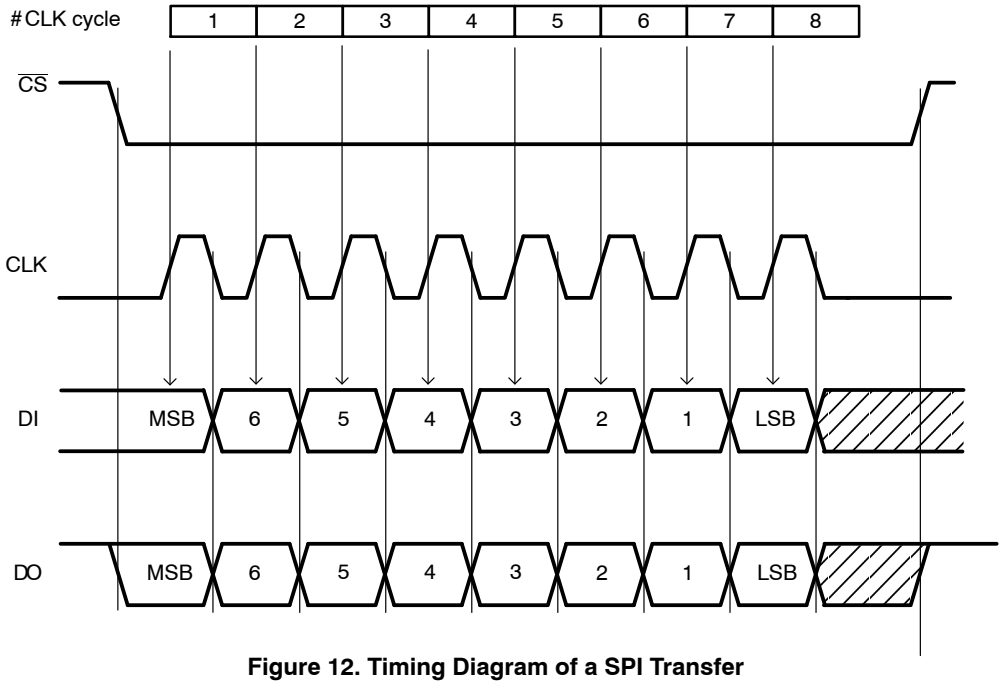



**Figure 12. Timing Diagram of a SPI Transfer**

NOTE: At the falling edge of the eight clock pulse the data−out shift register is updated with the content of the addressed internal SPI register. The internal SPI registers are updated at the first rising edge of the AMIS−30511 system clock when CSB = High

### Transfer Packet:

Serial data transfer is assumed to follow MSB first rule. The transfer packet contains one or more bytes.

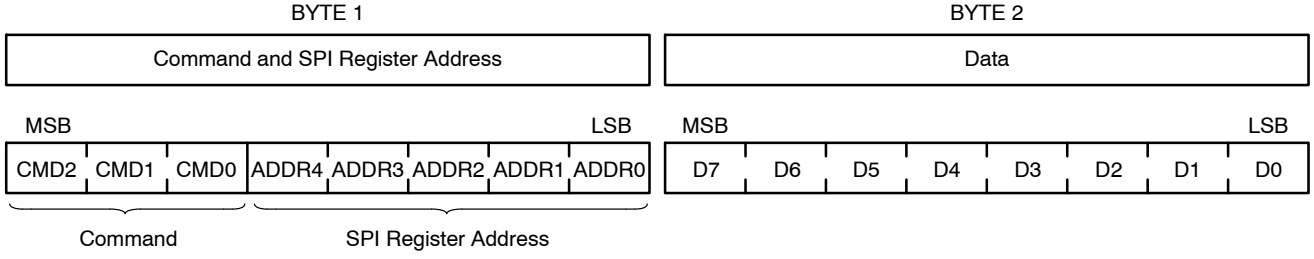



**Figure 13. SPI Transfer Packet**

Byte 1 contains the Command and the SPI Register Address and indicates to AMIS−30511 the chosen type of operation and addressed register. Byte 2 contains data, or sent from the Master in a WRITE operation, or received from AMIS−30511 in a READ operation.

2 command types can be distinguished in the communication between master and AMIS−30511:

- READ **from** SPI Register with address ADDR[4:0]: **CMD2** = “0”
- WRITE **to** SPI Register with address ADDR[4:0]: **CMD2** = “1”

**READ Operation**

If the Master wants to read data from Status or Control Registers, it initiates the communication by sending a READ command. This READ command contains the address of the SPI register to be read out. At the falling edge of the eight clock pulse the data−out shift register is updated with the content of the corresponding internal SPI register. In the next 8−bit clock pulse train this data is shifted out via DO pin. At the same time the data shifted in from DI (Master) should be interpreted as the following successive command or is dummy data.

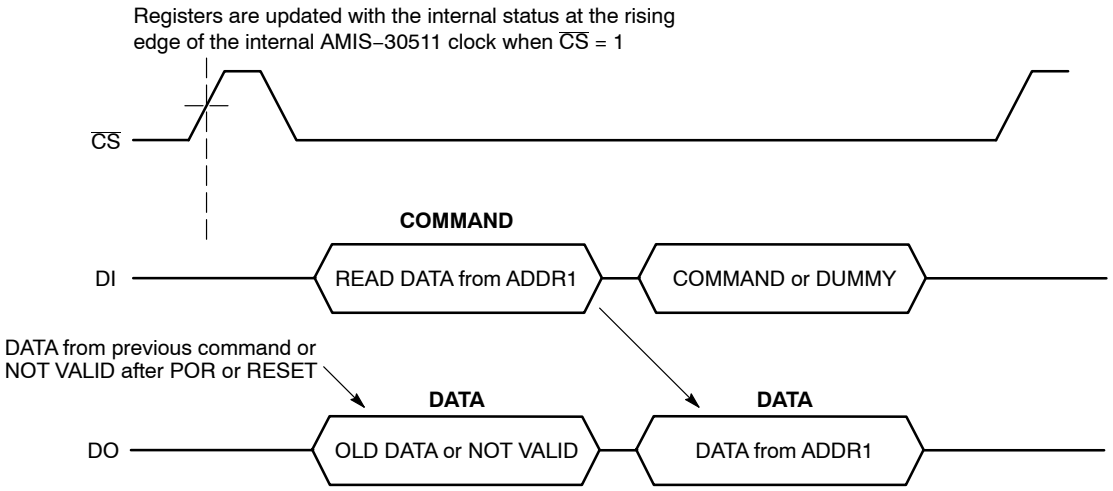



**Figure 14. Single READ operation where DATA from SPI register with Address 1 is read by the Master**

All 4 Status Registers (see SPI Registers) contain 7 data bits and a parity check bit. The most significant bit (D7) represents a parity of D[6:0]. If the number of logical ones in D[6:0] is odd, the parity bit D7 equals “1”. If the number of logical ones in D[6:0] is even then the parity bit D7 equals “0”. This simple mechanism protects against noise and increases the consistency of the transmitted data. If a parity check error occurs it is recommended to initiate an additional READ command to obtain the status again.

Also the Control Registers can be read out following the same routine. Control Registers don’t have a parity check.

The CSB line is active low and may remain low between successive READ commands as illustrated in Figure 14. There is however one exception. In case an error condition is latched in one of Status Registers (see SPI Registers) the ERRB pin is activated. (See 9.6.5. Error Output). This signal flags a problem to the external microcontroller. By reading the Status Registers information about the root cause of the problem can be determined. After this READ operation the Status Registers are cleared. Because the Status Registers and ERRB pin (see SPI Registers) are only updated by the internal system clock when the CSB line is high, the Master should force CSB high immediately after the READ operation. For the same reason it is recommended to keep the CSB line high always when the SPI bus is idle.

**WRITE Operation**

If the Master wants to write data to a Control Register it initiates the communication by sending a WRITE command. This contains the address of the SPI register to write to. The command is followed with a data byte. This incoming data will be stored in the corresponding Control Register after CSB goes from low to high! AMIS−30511 responds on every incoming byte by shifting out via DO the data stored in the last received address.

It is important that the writing action (command − address and data) to the Control Register is exactly 16 bits long. If more or less bits are transmitted the complete transfer packet is ignored.

A WRITE command executed for a read−only register (e.g. Status Registers) will not affect the addressed register and the device operation.

Because after a power−on−reset the initial address is unknown the data shifted out via DO is not valid.

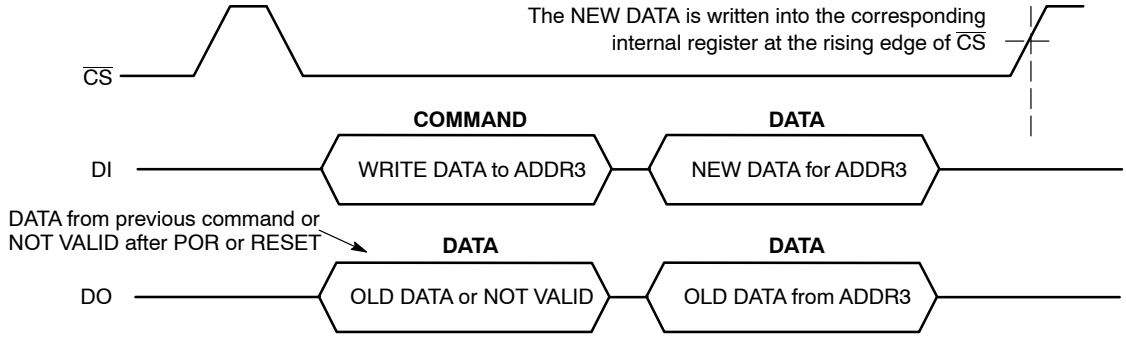



**Figure 15. Single WRITE Operation where DATA from the Master is Written in SPI Register with Address 3**

**Examples of Combined READ and WRITE Operations**

In the following examples successive READ and WRITE operations are combined. In Figure 13 the Master first reads the status from Register at ADDR4 and at ADDR5 followed by writing a control byte in Control Register at ADDR2. Note that during the write command (in Figure 3) the old data of the pointed register is returned at the moment the new data is shifted in:

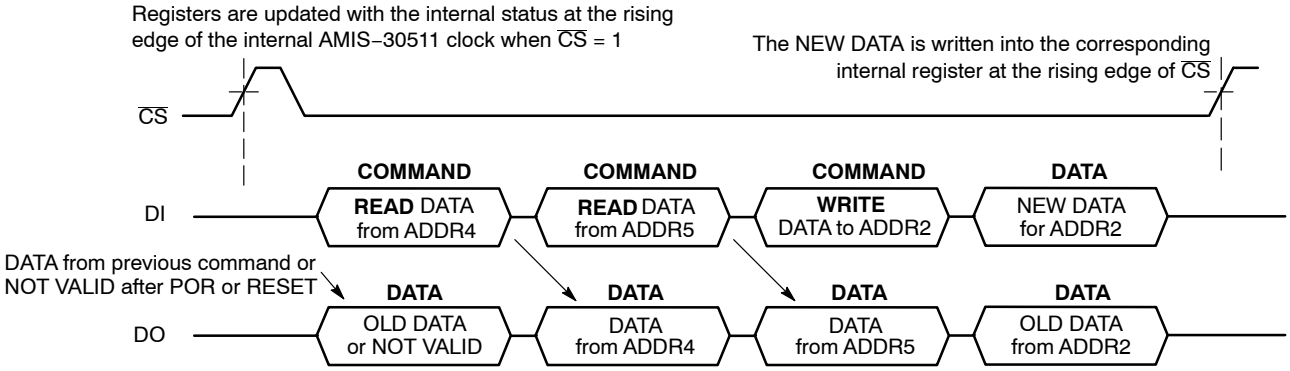



**Figure 16. 2 Successive READ Commands Followed by a WRITE Command**

After the write operation the Master could initiate a read back command in order to verify the data correctly written as illustrated in Figure 14. During reception of the READ command the old data is returned for a second time. Only after receiving the READ command the new data is transmitted. This rule also applies when the master device wants to initiate an SPI transfer to read the Status Registers. Because the internal system clock updates the Status Registers only when CSB line is high, the first read out byte might represent old status information.

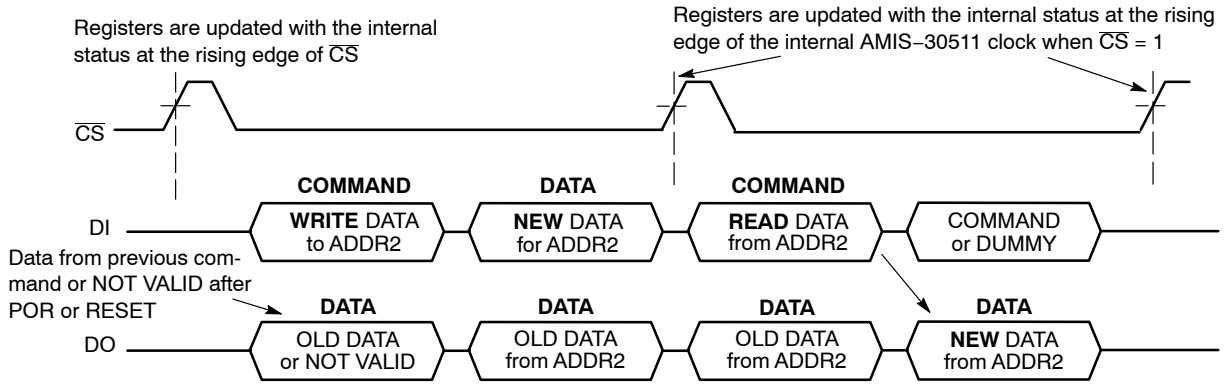



**Figure 17. A WRITE Operation where DATA from the Master is Written in SPI Register with Address 2 Followed by a READ Back Operation to Confirm a Correct WRITE Operation**

NOTE: The internal data−out shift buffer of AMIS−30511 is updated with the content of the selected SPI register only at the last (every eight) falling edge of the CLK signal (see SPI Transfer Format and Pin Signals). As a result, new data for transmission cannot be written to the shift buffer at the beginning of the transfer packet and the first byte shifted out might represent old data.

### SPI Control Registers

All SPI control registers have Read/Write access and default to “0” after power−on or hard reset.

**Table 11. SPI Control Register 0**

| Control Register 0 (CR0) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Structure | | | | | | | |
| Address | Content | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 01h | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | SM[2:0] | | | CUR[4:0] | | | | |

Where:

| | |
|---|---|
| R/W | Read and Write access |
| Reset: | Status after power−On or hard reset |
| SM[2:0]: | Step mode |
| CUR[4:0]: | Current amplitude |

**Table 12. SPI Control Register 1**

| Control Register 1 (CR1) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Structure | | | | | | | |
| Address | Content | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 02h | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | DIRCTRL | NXTP | – | – | PWMF | PWMJ | EMC[1:0] | |

Where:

| | |
|---|---|
| R/W | Read and Write access |
| Reset: | Status after power−on or hard reset |
| DIRCTRL | Direction control |
| NXTP | NEXT polarity |
| PWMF | PWM frequency |
| PWMJ | PWM jitter |
| EMC[1:0] | EMC slope control |

**Table 13. SPI Control Register 2**

| Control Register 2 (CR2) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Structure | | | | | | | |
| Address | Content | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 03h | Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | MOTEN | SLP | SLAG | SLAT | – | – | – | – |

Where:

| | |
|---|---|
| R/W | Read and Write access |
| Reset: | Status after power−On or hard reset |
| MOTEN | Motor enable |
| SLP | Sleep |
| SLAG | Speed load angle gain |
| SLAT | Speed load angle transparency |

**Table 14. SPI Control Parameter Overview SLAT**

| Symbol | Description | Status | Behaviour |
|---|---|---|---|
| SLAT | Speed Load Angle Transparency bit | <SLAT> = 0 | SLA is transparent |
| | | <SLAT> = 1 | SLA is NOT transparent |

**Table 15. SPI Control Parameter Overview SLAG**

| Symbol | Description | Status | Value |
|---|---|---|---|
| SLAG | Speed Load Angle Gain setting | <SLAG> = 0 | Gain = 0.5 |
| | | <SLAG> = 1 | Gain = 0.25 |

**Table 16. SPI Control Parameter Overview PWMF**

| Symbol | Description | Status | Value |
|---|---|---|---|
| PWMF | Enables doubling of the PWM frequency | <PWMF> = 0 | $f_{PWM}$ = 22.8 kHz |
| | | <PWMF> = 1 | $f_{PWM}$ = 45.6 kHz |

**Table 17. SPI Control Parameter Overview PWMJ**

| Symbol | Description | Status | Behaviour |
|---|---|---|---|
| PWMJ | Enables jittery PWM | <PWMJ> = 0 | Jitter disabled |
| | | <PWMJ> = 1 | Jitter enabled |

**Table 18. SPI Control Parameter Overview SLP**

| Symbol | Description | Status | Behaviour |
|---|---|---|---|
| SLP | Enables sleep mode | <SLP> = 0 | Active mode |
| | | <SLP> = 1 | Sleep mode |

**Table 19. SPI Control Parameter Overview MOTEN**

| Symbol | Description | Status | Value |
|---|---|---|---|
| MOTEN | Activates the motor driver outputs | <MOTEN> = 0 | Drivers disabled |
| | | <MOTEN> = 1 | Drivers enabled |

**Table 20. SPI Control Parameter Overview DIRCTRL**

| Symbol | Description | Status | | Value |
|---|---|---|---|---|
| DIRCTRL | Controls the direction of rotation (in combination with logic level on input DIR) | <DIR> = 0 | <DIRCTRL> = 0 | CW motion |
| | | | <DIRCTRL> = 1 | CCW motion |
| | | <DIR> = 1 | <DIRCTRL> = 0 | CCW motion |
| | | | <DIRCTRL> = 1 | CW motion |

**Table 21. SPI Control Parameter Overview NXTP**

| Symbol | Description | Status | Value |
|---|---|---|---|
| NXTP | Selects if NXT triggers on rising or falling edge | <NXTP> = 0 | Trigger on rising edge |
| | | <NXTP> = 1 | Trigger on falling edge |

CUR[4:0] Selects IMCmax peak. This is the peak or amplitude of the regulated current waveform in the motor coils.

**Table 22. SPI Control Parameter Overview CUR[4:0]**

| Index | CUR[4:0] | | | | | Current (mA) | Index | CUR[4:0] | | | | | Current (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 15 | 10 | 1 | 0 | 0 | 0 | 0 | 181 |
| 1 | 0 | 0 | 0 | 0 | 1 | 30 | 11 | 1 | 0 | 0 | 0 | 1 | 200 |
| 2 | 0 | 0 | 0 | 1 | 0 | 45 | 12 | 1 | 0 | 0 | 1 | 0 | 221 |
| 3 | 0 | 0 | 0 | 1 | 1 | 50 | 13 | 1 | 0 | 0 | 1 | 1 | 244 |
| 4 | 0 | 0 | 1 | 0 | 0 | 55 | 14 | 1 | 0 | 1 | 0 | 0 | 269 |
| 5 | 0 | 0 | 1 | 0 | 1 | 61 | 15 | 1 | 0 | 1 | 0 | 1 | 297 |
| 6 | 0 | 0 | 1 | 1 | 0 | 67 | 16 | 1 | 0 | 1 | 1 | 0 | 328 |
| 7 | 0 | 0 | 1 | 1 | 1 | 74 | 17 | 1 | 0 | 1 | 1 | 1 | 362 |
| 8 | 0 | 1 | 0 | 0 | 0 | 82 | 18 | 1 | 1 | 0 | 0 | 0 | 400 |
| 9 | 0 | 1 | 0 | 0 | 1 | 91 | 19 | 1 | 1 | 0 | 0 | 1 | 441 |
| A | 0 | 1 | 0 | 1 | 0 | 100 | 1A | 1 | 1 | 0 | 1 | 0 | 487 |
| B | 0 | 1 | 0 | 1 | 1 | 110 | 1B | 1 | 1 | 0 | 1 | 1 | 538 |
| C | 0 | 1 | 1 | 0 | 0 | 122 | 1C | 1 | 1 | 1 | 0 | 0 | 594 |
| D | 0 | 1 | 1 | 0 | 1 | 135 | 1D | 1 | 1 | 1 | 0 | 1 | 656 |
| E | 0 | 1 | 1 | 1 | 0 | 149 | 1E | 1 | 1 | 1 | 1 | 0 | 724 |
| F | 0 | 1 | 1 | 1 | 1 | 164 | 1F | 1 | 1 | 1 | 1 | 1 | 800 |

EMC[1:0] Adjusts the dV/dt of the PWM voltage slopes on the motor pins.

**Table 23. SPI Control Parameter Overview EMC[1:0]**

| Index | EMC[1:0] | | Slope (V/μs) | Remark |
|---|---|---|---|---|
| 0 | 0 | 0 | 150 | Turn−on and turn−off voltage slope 10% to 90% |
| 1 | 0 | 1 | 100 | ” |
| 2 | 1 | 0 | 50 | ” |
| 3 | 1 | 1 | 25 | ” |

SM[2:0] Selects the micro−stepping mode.

**Table 24. SPI Control Parameter Overview SM[2:0]**

| Index | SM[2:0] | | | Step Mode | Remark |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1/32 | Micro−step |
| 1 | 0 | 0 | 1 | 1/16 | Micro−step |
| 2 | 0 | 1 | 0 | 1/8 | Micro−step |
| 3 | 0 | 1 | 1 | 1/4 | Micro−step |
| 4 | 1 | 0 | 0 | 1/2 | Uncompensated half−step |
| 5 | 1 | 0 | 1 | 1/2 | Compensated half−step |
| 6 | 1 | 1 | 0 | Full | Full step |
| 7 | 1 | 1 | 1 | N/A | For future use |

### SPI Status Register Description

All four SPI status registers have Read Access and are default to “0” after power−on or hard reset.

**Table 25. Status Register 0 (SR0)**

| Address | | Structure | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 04h | Content | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | Access | R | R | R | R | R | R | R | R |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | PAR | TW | CPfail | − | OPENX | OPENY | − | − |

Where:

| | |
|---|---|
| R | Read only mode access |
| Reset | Status after power−on or hard reset |
| PAR | Parity check |
| TW | Thermal warning |
| Cpfail | Charge pump failure |
| OPENX | Open Coil X detected |
| OPENY | Open Coil Y detected |
| Remark: | Data is **not** latched |

**Table 26. Status Register 1 (SR1)**

| Address | | Structure | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 05h | Content | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | Access | R | R | R | R | R | R | R | R |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | PAR | OVCXPT | OVCXPB | OVCXNT | OVCXNB | − | − | − |

Where:

| | |
|---|---|
| R | Read only mode access |
| Reset | Status after power−on or hard reset |
| PAR | Parity check |
| OVXPT | Over−current detected on X H−bridge: MOTXP terminal, top transistor |
| OVXPB | Over−current detected on X H−bridge: MOTXP terminal, bottom transistor |
| OVXNT | Over−current detected on X H−bridge: MOTXN terminal, top transistor |
| OVXNB | Over−current detected on X H−bridge: MOTXN terminal, bottom transistor |
| Remark: | Data is latched |

**Table 27. SPI Status Register 2 (SR2)**

| Address | | Structure | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 06h | Content | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| | Access | R | R | R | R | R | R | R | R |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Data | PAR | OVCYPT | OVCYPB | OVCYYNT | OVCYNB | TSD | − | − |

Where:

| | |
|---|---|
| R | Read only mode access |
| Reset | Status after power−on or hard reset |
| PAR | Parity check |
| OVCYPT | Over−current detected on Y H−bridge: MOTYP terminal, top transistor |
| OVCYPB | Over−current detected on Y H−bridge: MOTYP terminal, bottom transistor |
| OVCYNT | Over−current detected on Y H−bridge: MOTYN terminal, top transistor |
| OVCYNB | Over−current detected on Y H−bridge: MOTYN terminal, bottom transistor |
| TSD | Thermal shutdown |
| Remark: | Data is latched |