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# AMIS-30523

*Product Preview*

# CAN Micro-Stepping Motor Driver

**Introduction**

The AMIS−30523 is a micro−stepping stepper motor driver for bipolar stepper motors with an embedded CAN transceiver.

The motor driver is connected through I/O pins and a SPI interface with an external microcontroller. It has an on−chip voltage regulator, reset−output and watchdog reset, able to supply peripheral devices. It contains a current−translation table and takes the next micro−step depending on the clock signal on the "NXT" input pin and the status of the "DIR" (=direction) register or input pin.

The CAN transceiver is the interface between a (CAN) protocol controller and the physical bus. It provides differential transmit capability to the bus and differential receive capability to the CAN controller. To cope with the long bus delay the communication speed needs to be low. The integrated transceiver allows low transmit data rates down 10 kbit/s or lower.

The AMIS−30523 is ideally suited for general−purpose stepper motor applications in the automotive, industrial, medical, and marine environment. With the on−chip voltage regulator and embedded CAN transceiver it further reduces the BOM for mechatronic stepper applications.

**Key Features**

***Motor Driver***

- Dual H−Bridge for 2−Phase Stepper Motors
- Programmable Peak−Current up to 1.2 A Continuous (1.6 A for a Short Time)*
- On−Chip Current Translator
- SPI Interface
- Seven Step Modes from Full Step up to 32 Micro−Steps
- PWM Current Control with Automatic Selection of Fast and Slow Decay and Fully Integrated Current−Sense
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Integrated 5 V Regulator to Supply External Microcontroller

***CAN Transceiver***

- Compatible with the ISO 11898 Standard
- Wide Range of Bus Communication Speed (0 up to 1 Mbit/s)
- Allows Low Transmit Data Rate in Networks Exceeding 1 km
- Extremely Low Current Standby Mode with Wake−up via the Bus
- Low EME: Common−Mode Choke is No Longer Required
- Differential Receiver with Wide common−mode range (± 35 V)
- Voltage Source via $V_{SPLIT}$ Pin for Stabilizing the Recessive Bus Level
- No Disturbance of the Bus Lines with an Un−Powered Node
- Logic Level Inputs Compatible with 3.3 V Devices
- These are Pb−Free Devices

*Output Current Level May be Limited by Ambient Temperature and Heat Sinking

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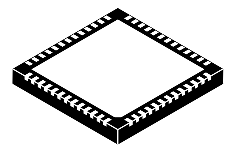

1 52

**QFN52, 8x8**
**CASE 485M**

**MARKING DIAGRAM**

1
AMIS30523
0C523−001
XXXXYZZ

| | |
|---|---|
| 0C523−001 | = Specific Device Code |
| XXXX | = Date Code |
| WL | = Wafer Lot |
| Y | = Assembly Location |
| ZZ | = Traceability Code |

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 34 of this data sheet.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

## BLOCK DIAGRAM

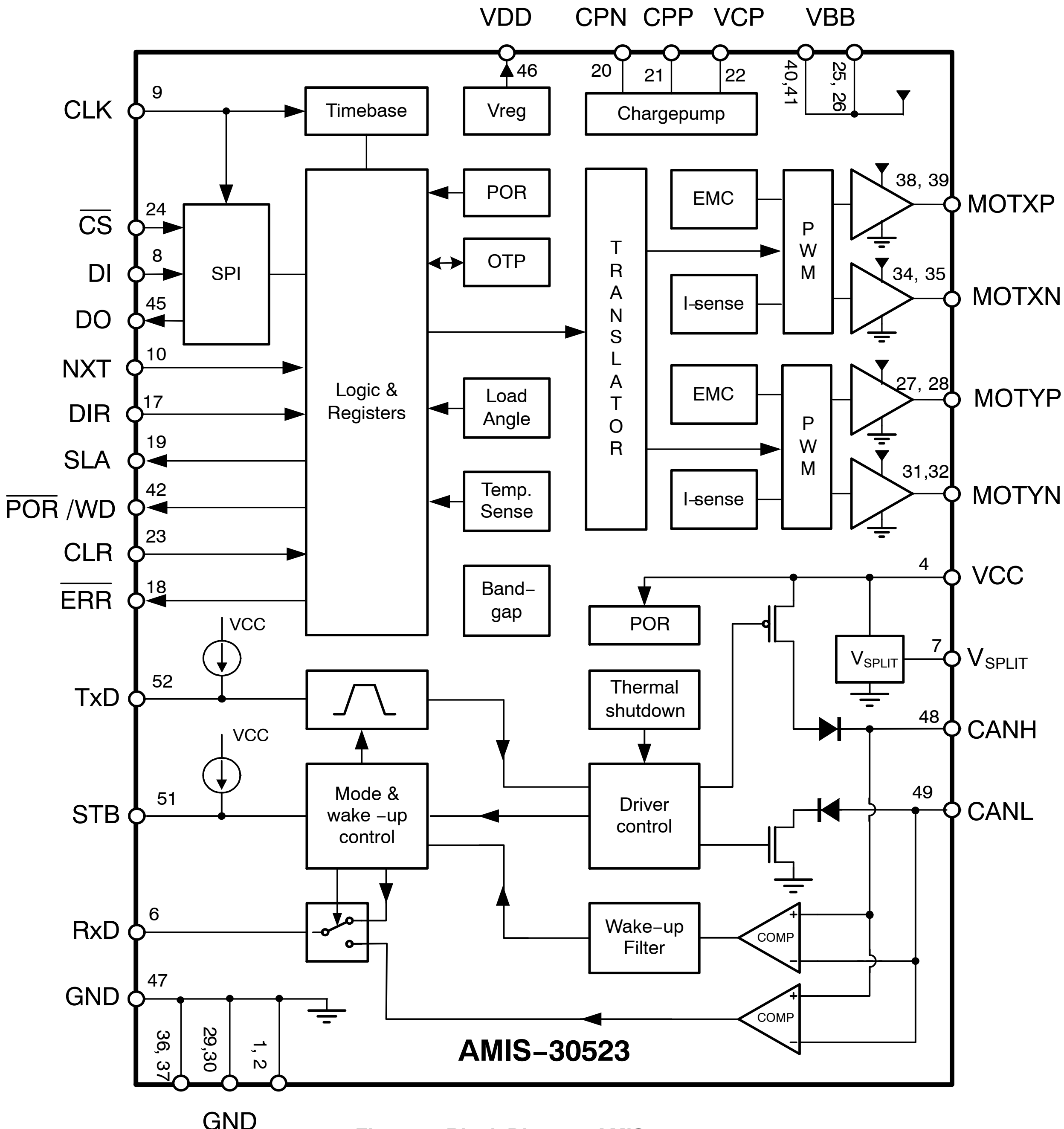


**Figure 1. Block Diagram AMIS−30523**

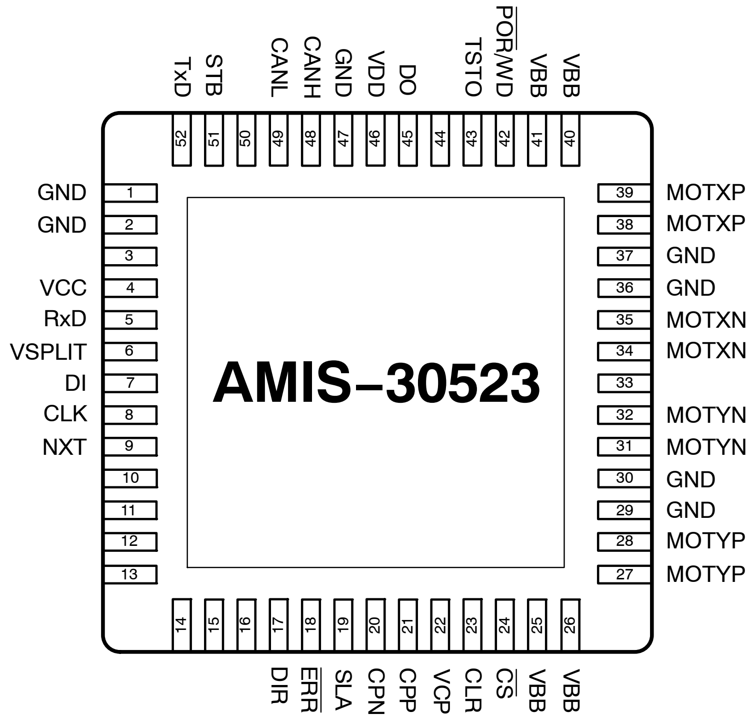


**Figure 2. Pin Out AMIS−30523**

**Table 1. PIN DESCRIPTION**

| Name | Pin | Description | Type | Equivalent Schematic |
|---|---|---|---|---|
| GND | 1, 2 | Ground | Supply | |
| / | 3 | No function (to be left open in normal operation) | | |
| VCC | 4 | CAN Supply voltage | Supply | |
| / | 5 | No function (to be left open in normal operation) | | |
| RXD | 6 | CAN Receive data output; dominant transmitter → low output | Digital Output | |
| VSPLIT | 7 | CAN common−mode stabilization output | Supply | |
| DI | 8 | SPI Data In | Digital Input | Type 2 |
| CLK | 9 | SPI Clock Input | Digital Input | Type 2 |
| NXT | 10 | Next micro−step input | Digital Input | Type 2 |
| / | 11 .. 16 | No function (to be left open in normal operation) | | |
| DIR | 17 | Direction input | Digital Input | Type 2 |
| ERRB | 18 | Error output (open drain) | Digital Output | Type 4 |
| SLA | 19 | Speed load angle output | Analog Output | Type 5 |
| CPN | 20 | Negative connection of charge pump capacitor | High Voltage | |
| CPP | 21 | Positive connection of charge pump capacitor | High Voltage | |
| VCP | 22 | Charge pump filter−capacitor | High Voltage | |
| CLR | 23 | “Clear” = chip reset input | Digital Input | Type 1 |
| CSB | 24 | SPI chip select input | Digital Input | Type 2 |
| VBB | 25, 26 | High voltage supply Input | Supply | Type 3 |
| MOTYP | 27, 28 | Negative end of phase Y coil output | Driver Output | |
| GND | 29, 30 | Ground, heat sink | Supply | |

**Table 1. PIN DESCRIPTION**

| Name | Pin | Description | Type | Equivalent Schematic |
|---|---|---|---|---|
| MOTYN | 31, 32 | Positive end of phase Y coil output | Driver Output | |
| / | 33 | No function (to be left open in normal operation) | | |
| MOTXN | 34, 35 | Positive end of phase X coil output | Driver Output | |
| GND | 36, 37 | Ground, heat sink | Supply | |
| MOTXP | 38, 39 | Negative end of phase X coil output | Driver Output | |
| VBB | 40, 41 | High voltage supply input | Supply | Type 3 |
| PORB/WD | 42 | Power−on−reset and watchdog reset output (open drain) | Digital Output | Type 2 |
| TST0 | 43 | Test pin input (to be tied to ground in normal operation) | Digital Input | |
| / | 44 | No function (to be left open in normal operation) | | |
| DO | 45 | SPI data output (open drain) | Digital Output | Type 4 |
| VDD | 46 | 5V Logic Supply Output (needs external decoupling capacitor) | Supply | Type 6 |
| GND | 47 | Ground | Supply | |
| CANH | 48 | High−level CAN bus line (high in dominant mode) | Analog Output | |
| CANL | 49 | Low−level CAN bus line (low in dominant mode) | Analog Output | |
| / | 50 | No function (to be left open in normal operation) | | |
| STB | 51 | CAN stand−by mode control input | Digital Input | |
| TXD | 52 | CAN transmit data input; low input → dominant driver; internal pull−up current | Digital Input | |

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{BB}$ | Analog DC supply voltage (Note 1) | −0.3 | +40 | V |
| $V_{CC}$ | CAN Supply voltage | −0.3 | +7 | V |
| $V_{CANH}$, $V_{CANL}$, $V_{SPLIT}$ | DC voltage CANH ,CANL and VSPLIT (Note 2) | −50 | +50 | V |
| $V_{TRANS}$ | Transient voltage CANH, CANL and VSPLIT (Note 3) | −300 | +300 | V |
| $T_{ST}$ | Storage temperature | −55 | +150 | °C |
| $T_J$ | Junction Temperature under bias (Note 4) | −40 | +170 | °C |
| $V_{ESD}$ | Electrostatic discharges on component level, All pins (Note 5) | −2 | +2 | kV |
| $V_{ESD}$ | Electrostatic discharges on component level, All pins (Note 7) | −500 | +500 | V |
| $V_{ESD}$ | Electrostatic discharges on CANH, CANL and VSPLIT (Note 6) | −6 | +6 | kV |
| $V_{ESD}$ | Electrostatic discharges on CANH and CANL (Note 7) | −500 | +500 | V |
| $V_{ESD}$ | Electrostatic discharges on component level, HiV pins (Note 6) | −6 | +6 | kV |
| Latch−up | Static latch−up at all pins | | 100 | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. For limited time < 0.5 s.
2. For $0 < V_{CC} < 5.25$ V unlimited time
3. Applied transient waveforms in accordance with ISO 7637 part 3, test pulses 1, 2, 3a, and 3b.
4. Circuit functionality not guaranteed.
5. Standardized Human body model (100 pF via 1.5 kΩ, according to JEDEC EIA−JESD22−A114−B).
6. Standardized human body model electrostatic discharge (ESD) pulses (100 pF via 1.5 kΩ) stressed pin to ground.
7. Standardized charged device model ESD pulses when tested according to ESD STM5.3.1−1999.

**Table 3. THERMAL RESISTANCE**

| Package | Thermal Resistance | | | Unit |
|---|---|---|---|---|
| | Junction−to−Exposed Pad ($Rth_{J-EP}$) | Junction−to−Ambient ($Rth_{J-A}$) | | |
| | | 1S0P Board | 2S2P Board | |
| QFN−52 | 0.95 | 60 | 30 | K/W |

## EQUIVALENT SCHEMATICS

Following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.

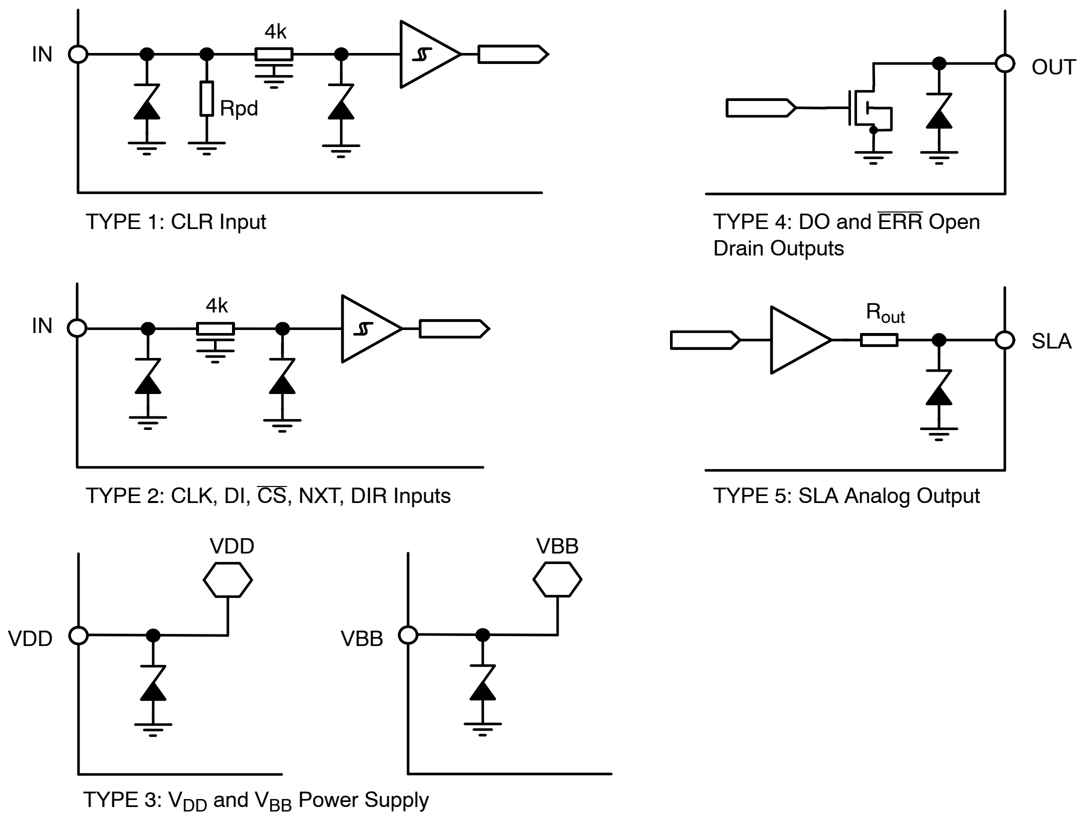


**Figure 3. In− and Output Equivalent Diagrams**

## PACKAGE THERMAL CHARACTERISTICS

The AMIS−30523 is available in a QFN−52 package. For cooling optimizations, the QFN has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer. Figure 4 gives an example for good power distribution solutions.

For precise thermal cooling calculations the major thermal resistances of the device are given. The thermal media to which the power of the devices has to be given are:

- Static environmental air (via the case)
- PCB board copper area (via the exposed pad)

The thermal resistances are presented in Table 5: DC Parameters Motor Driver.

The major thermal resistances of the device are the Rth from the junction to the ambient ($Rth_{J-A}$) and the overall Rth from the junction to exposed pad ($Rth_{J-EP}$). In Table 3 one can find the values for the $Rth_{J-A}$ and $Rth_{J-EP}$, simulated according to JESD−51:

The $Rth_{J-A}$ for 2S2P is simulated conform JEDEC JESD−51 as follows:

- A 4−layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
- Board thickness is 1.46 mm (FR4 PCB material)
- The 2 signal layers: 70 μm thick copper with an area of 5500 $mm^2$ copper and 20% conductivity

- The 2 power internal planes: 36 μm thick copper with an area of 5500 $mm^2$ copper and 90% conductivity

The $Rth_{J-A}$ for 1S0P is simulated conform JEDEC JESD−51 as follows:

- A 1−layer printed circuit board with a single power and signal layer
- Board thickness is 1.46 mm (FR4 PCB material)
- The layer has a thickness of 70 μm copper with an area of 5500 $mm^2$ copper and 20% conductivity

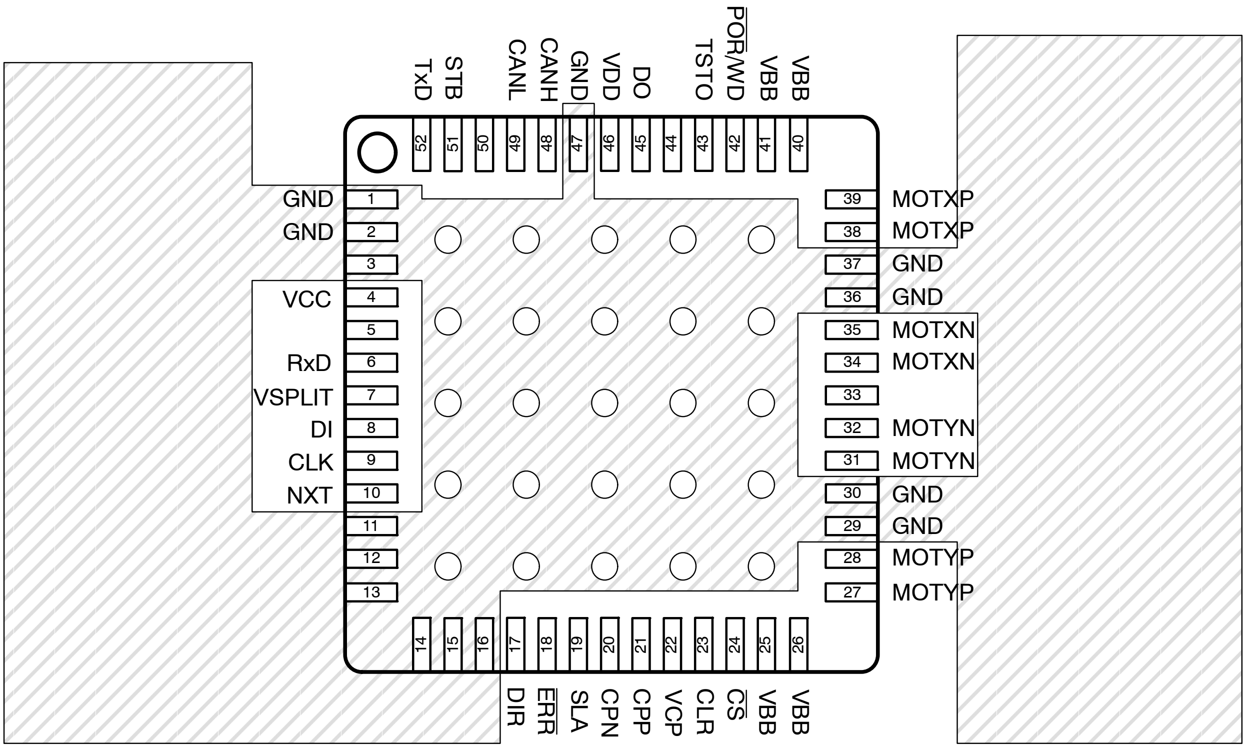


**Figure 4. Example of QFN−52 PCB Ground Plane Layout in Top View (preferred layout at top and bottom)**

## ELECTRICAL SPECIFICATION

### Recommend Operation Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

**Table 4. OPERATING RANGES**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{BB}$ | Motor Driver Analog DC supply | 6 | 30 | V |
| $V_{CC}$ | CAN transceiver DC supply | 4.75 | 5.25 | V |
| $T_J$ | Junction temperature (Note 8) | −40 | +172 | °C |

8. No more than 100 cumulative hours in life time above $T_{tw}$.

**Table 5. DC PARAMETERS MOTOR DRIVER**
(The DC Parameters are Given for $V_{BB}$ and Temperature in Their Operating Ranges Unless Otherwise Specified)
Convention: Currents Flowing in the Circuit are Defined as Positive.

| Symbol | Pin(s) | Parameter | Remark/ Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SUPPLY AND VOLTAGE REGULATOR** | | | | | | | |
| $V_{BB}$ | VBB | Nominal operating supply range | | 6 | | 30 | V |
| $I_{BB}$ | | Total internal current consumption | Unloaded outputs | | | 8 | mA |
| $I_{BBS}$ | | Sleep current in $V_{BB}$ (Note 9) | Unloaded outputs | | | 100 | μA |
| $V_{DD}$ | VDD | Regulated Output Voltage | | 4.50 | 5 | 5.50 | V |
| $I_{INT}$ | | Internal load current | Unloaded outputs | | | 8 | mA |
| $I_{LOAD}$ | | Max. Output Current (external and internal loads) | 6 V ≤ $V_{BB}$ < 8 V | 15 | | | mA |
| | | | 8 V ≤ $V_{BB}$ v 30 V | 40 | | | mA |
| $I_{DDLIM}$ | | Current limitation | Pin shorted to ground | | | 200 | mA |
| $I_{LOAD\_PD}$ | | Output current in Power Down | | 1 | | | mA |
| **POWER ON RESET (POR)** | | | | | | | |
| $V_{DDH}$ | VDD | Internal POR comparator threshold | VDD rising | 3.9 | 4.15 | 4.4 | V |
| $V_{DDL}$ | | Internal POR comparator threshold | VDD falling | | 3.80 | | V |
| $V_{DDHYS}$ | | Hysteresis between $V_{DDH}$ and $V_{DDL}$ | | 0.1 | 0.35 | 0.6 | V |
| **MOTORDRIVER** | | | | | | | |
| $I_{MDmax,Peak}$ | MOTXP MOTXN MOTYP MOTYN | Max current through motor coil in normal operation | | | 1600 | | mA |
| $I_{Mdmax,RMS}$ | | Max RMS current through coil in normal operation | | | 800 | | mA |
| $I_{Mdabs}$ | | Absolute error on coil current | | −10 | | 10 | % |
| $I_{Mdrel}$ | | Error on current ratio $I_{coilx}$ / $I_{coily}$ | | −7 | | 7 | % |
| $I_{SET\_TC1}$ | | Temperature coefficient of coil current set−level, CUR[4:0] = 0 ... 27 (Note 10) | −40 °C ≤ $T_J$ ≤ 160°C | | −240 | | ppm/K |
| $I_{SET\_TC2}$ | | Temperature coefficient of coil current set−level, CUR[4:0] = 28 ... 31 (Note 10) | −40 °C ≤ $T_J$ ≤ 160°C | | −490 | | ppm/K |
| $R_{HS}$ | | On−resistance high−side driver, CUR[4:0] = 0 ... 31 | $V_{BB}$ = 12 V, $T_J$ = 27°C | | 0.45 | 0.56 | Ω |
| | | | $V_{BB}$ = 12 V, $T_J$ = 160°C | | 0.94 | 1.25 | Ω |
| $R_{LS3}$ | | On−resistance low−side driver, CUR[4:0] = 23 ... 31 | $V_{BB}$ = 12 V, $T_J$ = 27°C | | 0.45 | 0.56 | Ω |
| | | | $V_{BB}$ = 12 V, $T_J$ = 160°C | | 0.94 | 1.25 | Ω |
| $R_{LS2}$ | | On−resistance low−side driver, CUR[4:0] = 16 ... 22 | $V_{BB}$ = 12 V, $T_J$ = 27°C | | 0.90 | 1.2 | Ω |
| | | | $V_{BB}$ = 12 V, $T_J$ = 160°C | | 1.9 | 2.5 | Ω |
| $R_{LS1}$ | | On−resistance low−side driver, CUR[4:0] = 9 ... 15 | $V_{BB}$ = 12 V, $T_J$ = 27°C | | 1.8 | 2.3 | Ω |
| | | | $V_{BB}$ = 12 V, $T_J$ = 160°C | | 3.8 | 5.0 | Ω |
| $R_{LS0}$ | | On−resistance low−side driver, CUR[4:0] = 0 ... 8 | $V_{BB}$ = 12 V, $T_J$ = 27°C | | 3.6 | 4.5 | Ω |
| | | | $V_{BB}$ = 12 V, $T_J$ = 160°C | | 7.5 | 10 | Ω |
| $I_{Mpd}$ | | Pull down current motor pins | HiZ mode | | 1 | | mA |

9. Characterization Data Only, not tested in production
10. The coil current at a given junction temperature is calculated as: $I_{coil}$ @ $T_J$ = $I_{coil}$ [1 + ($T_J$ − 125) x $I_{SET\_TCi}$ x $10^{-6}$].
See also paragraph Programmable Peak Current.
11. Not valid for pins with internal Pull Down resistor.
12. No more than 100 cumulated hours in life time above $T_{tw}$.
13. Thermal shutdown is derived from Thermal Warning.

**Table 5. DC PARAMETERS MOTOR DRIVER**

(The DC Parameters are Given for $V_{BB}$ and Temperature in Their Operating Ranges Unless Otherwise Specified)
Convention: Currents Flowing in the Circuit are Defined as Positive.

| Symbol | Pin(s) | Parameter | Remark/ Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS** | | | | | | | |
| $I_{leak}$ | DI, CLK NXT, DIR CLR, CSB | Input Leakage (Note 11) | $T_J$ = 160°C | | | 1 | μA |
| $V_{IL}$ | | Logic Low Threshold | | 0 | | 0.65 | V |
| $V_{IH}$ | | Logic High Threshold | | 2.20 | | $V_{DD}$ | V |
| $R_{pd\_CLR}$ | CLR | Internal Pull Down Resistor | | 120 | | 300 | kΩ |
| $R_{pd\_TST}$ | TST0 | Internal Pull Down Resistor | | 3 | | 9 | kΩ |
| **DIGITAL OUTPUTS** | | | | | | | |
| $V_{OL}$ | DO, ERRB, PORB/ WD | Logic Low level open drain | $I_{OL}$ = 5 mA | | | 0.3 | V |
| **THERMAL WARNING & SHUTDOWN** | | | | | | | |
| $T_{tw}$ | | Thermal Warning | | 138 | 145 | 152 | °C |
| $T_{tsd}$ | | Thermal shutdown (Notes 12 and 13) | | | $T_{tw}$ + 20 | | °C |
| **CHARGE PUMP** | | | | | | | |
| $V_{opCP}$ | VCP | Output voltage | 6 V< $V_{BB}$ < 15 V | | 2 * $V_{BB}$ – 2 | | V |
| | | | 15 V < $V_{BB}$ < 30 V | $V_{BB}$ + 9 | $V_{BB}$ + 11.5 | $V_{BB}$ + 16 | V |
| **PACKAGE THERMAL RESISTANCE VALUE** | | | | | | | |
| $Rth_{J-A}$ | QFN package | Thermal Resistance Junction−to−Ambient | Simulated Conform JEDEC JESD−51, (2S2P) | | 30 | | K/W |
| $Rth_{J-EP}$ | | Thermal Resistance Junction−to−Exposed Pad | | | 0.95 | | K/W |
| **SPEED AND LOAD ANGLE OUTPUT** | | | | | | | |
| $V_{out}$ | SLA | Output Voltage Range | | 0.2 | | $V_{DD}$ – 0.2 | V |
| $V_{off}$ | | Output Offset SLA pin | | −50 | | 50 | mV |
| $G_{sla}$ | | Gain of SLA Pin = $V_{BEMF}$ / $V_{COIL}$ | SLAG = 0 | | 0.5 | | |
| | | | SLAG = 1 | | 0.25 | | |
| $R_{out}$ | | Output Resistance SLA pin | (Note 9) | | 0.23 | 1 | kΩ |
| $C_{load}$ | | Load Capacitance SLA pin | (Note 9) | | | 50 | pF |

9. Characterization Data Only, not tested in production
10. The coil current at a given junction temperature is calculated as: $I_{coil}$ @ $T_J$ = $I_{coil}$ [1 + ($T_J$ – 125) x $I_{SET\_TCi}$ x $10^{-6}$]. See also paragraph Programmable Peak Current.
11. Not valid for pins with internal Pull Down resistor.
12. No more than 100 cumulated hours in life time above $T_{tw}$.
13. Thermal shutdown is derived from Thermal Warning.

**Table 6. AC PARAMETERS MOTOR DRIVER** (The AC Parameters are Given for $V_{BB}$ and Temperature in Their Operating Ranges)

| Symbol | Pin(s) | Parameter | Remark/ Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **INTERNAL OSCILLATOR** | | | | | | | |
| $f_{osc}$ | | Frequency of internal oscillator | | 3.6 | 4 | 4.4 | MHz |
| **MOTOR DRIVER** | | | | | | | |
| $f_{PWM}$ | MOTxx | PWM frequency | Frequency depends only on internal oscillator | 20.8 | 22.8 | 24.8 | kHz |
| | | Double PWM frequency | | 41.6 | 45.6 | 49.6 | kHz |
| $f_d$ | | PWM jitter Depth (Note 14) | | | 10 | | % $f_{PWM}$ |
| $tb_{rise}$ | MOTxx | Turn−on voltage slope, 10% to 90% | EMC[1:0] = 00 | | 150 | | V/μs |
| | | | EMC[1:0] = 01 | | 100 | | V/μs |
| | | | EMC[1:0] = 10 | | 50 | | V/μs |
| | | | EMC[1:0] = 11 | | 25 | | V/μs |
| $tb_{fall}$ | MOTxx | Turn−off voltage slope, 90% to 10% | EMC[1:0] = 00 | | 150 | | V/μs |
| | | | EMC[1:0] = 01 | | 100 | | V/μs |
| | | | EMC[1:0] = 10 | | 50 | | V/μs |
| | | | EMC[1:0] = 11 | | 25 | | V/μs |
| **DIGITAL OUTPUTS** | | | | | | | |
| $t_{H2L}$ | DO ERRB | Output fall−time from $V_{inH}$ to $V_{inL}$ (Note 14) | Capacitive load 400 pF and pull−up resistor of 1.5 kΩ | | | 50 | ns |
| **CHARGE PUMP** | | | | | | | |
| $f_{CP}$ | CPN CPP | Charge pump frequency | | | 250 | | kHz |
| $t_{CPU}$ | MOTxx | Start−up time of charge pump (Note 14) | Spec external components See Table 10 | | | 5 | ms |
| **CLR FUNCTION** | | | | | | | |
| $t_{CLR}$ | CLR | Hard reset duration time | | 100 | | | μs |
| **POWER−UP** | | | | | | | |
| $t_{PU}$ | PORB/ WD | Power−up time | $V_{BB}$ = 12 V, $I_{LOAD}$ = 50 mA, $C_{LOAD}$ = 220 nF | | | 110 | μs |
| $t_{POR}$ | | Reset duration | See Figure 22 | | | 100 | ms |
| $t_{RF}$ | | Reset filter time | See Figure 22 | 1 | | | μs |
| **WATCHDOG** | | | | | | | |
| $t_{WDTO}$ | PORB/ WD | Watchdog time out interval | See Figure 23 | 32 | | 512 | ms |
| $t_{WDPR}$ | | Prohibited watchdog acknowledge delay | See Figure 23 | | 2 | | ms |
| **NXT FUNCTION** | | | | | | | |
| $t_{NXT\_HI}$ | NXT | NXT Minimum, High Pulse Width | See Figure 5 | 2 | | | μs |
| $t_{NXT\_HI}$ | | NXT Minimum, Low Pulse Width | See Figure 5 | 2 | | | μs |
| $t_{DIR\_SET}$ | | NXT Hold Time, Following Change of DIR | See Figure 5 | | 2 | | μs |
| $t_{DIR\_HOLD}$ | | NXT Hold Time, Before Change of DIR | See Figure 5 | | 2 | | μs |

14. Characterization Data Only, not tested in production.

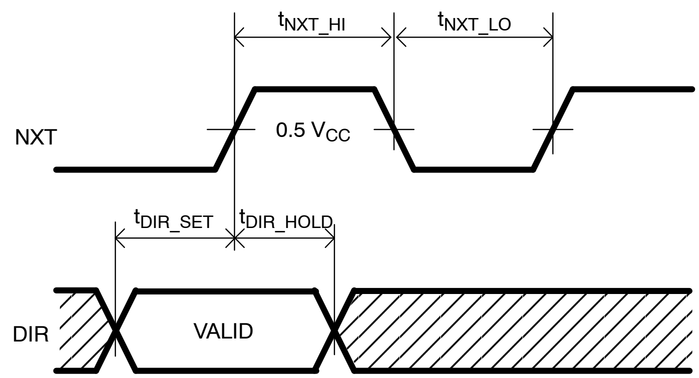


**Figure 5. NXT−Input Timing Diagram**

**Table 7. SPI TIMING PARAMETERS**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{CLK}$ | SPI clock period | 1 | | | μs |
| $t_{CLK\_HIGH}$ | SPI clock high time | 100 | | | ns |
| $t_{CLK\_LOW}$ | SPI clock low time | 100 | | | ns |
| $t_{SET\_DI}$ | DI set up time, valid data before rising edge of CLK | 50 | | | ns |
| $t_{HOLD\_DI}$ | DI hold time, hold data after rising edge of CLK | 50 | | | ns |
| $t_{CSB\_HIGH}$ | CSB high time | 2.5 | | | μs |
| $t_{SET\_CSB}$ | CSB set up time, CSB low before rising edge of CLK | 100 | | | ns |
| $t_{SET\_CLK}$ | CLK set up time, CLK low before rising edge of CSB | 100 | | | ns |

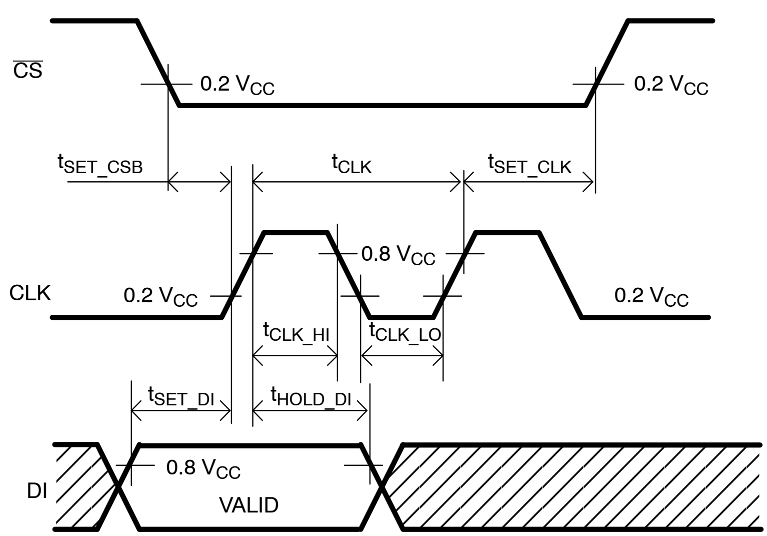


**Figure 6. SPI Timing**

**Table 8. DC PARAMETERS CAN TRANSCEIVER**
(The DC parameters are given for $V_{CC}$ and temperature in its operating range; $T_J$ = −40 to +150°C; $R_{LT}$ = 60 Ω unless otherwise specified) Convention: currents flowing in the circuit are defined as positive.

| Symbol | Pin(s) | Parameter | Remark / Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | | |
| $I_{CC}$ | VCC | Supply current | Dominant; $V_{TxD}$ = 0 V<br>Recessive; $V_{TxD}$ = $V_{CC}$ | | 45 | 65 | mA |
| $I_{CCS}$ | | Supply current in standby mode | $T_{J,max}$ = 100°C | | 4 | 8 | mA |
| **TRANSMITTER DATA INPUT** | | | | | | | |
| $V_{iH}$ | TXD | High−level input voltage | CAN bus output recessive | 2.0 | – | $V_{CC}$ + 0.3 | V |
| $V_{iL}$ | | Low−level input voltage | CAN bus output dominant | −0.3 | – | +0.8 | V |
| $I_{iH}$ | | High−level input current | $V_{TxD}$ = $V_{CC}$ | −5 | 0 | +5 | μA |
| $I_{iL}$ | | Low−level input current | $V_{TxD}$ = 0 V | −75 | −200 | −350 | μA |
| $C_i$ | | Input capacitance | (Note 15) | – | 5 | 10 | pF |
| **TRANSMITTER MODE SELECT** | | | | | | | |
| $V_{iH}$ | TXD | High−level input voltage | Standby mode | 2.0 | – | $V_{CC}$ + 0.3 | V |
| $V_{iL}$ | | Low−level input voltage | Normal mode | −0.3 | – | +0.8 | V |
| $I_{iH}$ | | High−level input current | $V_{STB}$ = $V_{CC}$ | −5 | 0 | +5 | μA |
| $I_{iL}$ | | Low−level input current | $V_{STB}$ = 0 V | −1 | −4 | −10 | μA |
| $C_i$ | | Input capacitance | (Note 15) | – | 5 | 10 | pF |
| **RECEIVER DATA OUTPUT** | | | | | | | |
| $V_{OH}$ | RXD | High−level output voltage | $I_{RXD}$ = −10 mA | 0.6 x $V_{CC}$ | | 0.75 x $V_{CC}$ | V |
| $V_{OL}$ | | Low−level output voltage | $I_{RXD}$ = 5 mA | | 0.25 | 0.45 | V |
| $I_{oh}$ | | High−level output current | $V_o$ = 0.7 x $V_{CC}$ | −5 | −10 | −15 | mA |
| $I_{ol}$ | | Low−level output current | $V_o$ = 0.3 x $V_{CC}$ | 5 | 10 | 15 | mA |
| $C_i$ | | Input capacitance | (Note 15) | – | 5 | 10 | pF |

15. Characterization Data Only, not tested in production.

### Table 8. DC PARAMETERS CAN TRANSCEIVER

(The DC parameters are given for $V_{CC}$ and temperature in its operating range; $T_J$ = −40 to +150°C; $R_{LT}$ = 60 Ω unless otherwise specified) Convention: currents flowing in the circuit are defined as positive.

| Symbol | Pin(s) | Parameter | Remark / Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **BUS LINES** | | | | | | | |
| $V_{o(reces)}$ (norm) | CANH CANL | Recessive bus voltage | $V_{TxD}$ = $V_{CC}$; no load normal mode | 2.0 | 2.5 | 3.0 | V |
| $V_{o(reces)}$ (stby) | | Recessive bus voltage | $V_{TxD}$ = $V_{CC}$; no load standby mode | −100 | 0 | 100 | mV |
| $I_{o(reces)}$ (CANH) | | Recessive output current at pin CANH | −35 V < $V_{CANH}$< +35 V; 0 V < $V_{CC}$ < 5.25 V | −2.5 | − | +2.5 | mA |
| $I_{o(reces)}$ (CANL) | | Recessive output current at pin CANL | −35 V <$V_{CANL}$ < +35 V; 0 V <$V_{CC}$ < 5.25 V | −2.5 | − | +2.5 | mA |
| $V_{o(dom)}$ (CANH) | | Dominant output voltage at pin CANH | $V_{TxD}$ = 0 V | 3.0 | 3.6 | 4.25 | V |
| $V_{o(dom)}$ (CANL) | | Dominant output voltage at pin CANL | $V_{TxD}$ = 0 V | 0. 5 | 1.4 | 1.75 | V |
| $V_{o(dif)}$ (bus_dom) | | Differential bus output voltage ($V_{CANH}$ − $V_{CANL}$) | $V_{TxD}$ = 0 V; dominant; 42.5 Ω < $R_{LT}$ < 60 Ω | 1.5 | 2.25 | 3.0 | V |
| $V_{o(dif)}$ (bus_rec) | | Differential bus output voltage ($V_{CANH}$ − $V_{CANL}$) | $V_{TxD}$ = $V_{CC}$; recessive; no load | −120 | 0 | +50 | mV |
| $I_{o(sc)}$ (CANH) | | Short circuit output current at pin CANH | $V_{CANH}$ = 0 V; $V_{TxD}$ = 0 V | −45 | −70 | −120 | mA |
| $I_{o(sc)}$ (CANL) | | Short circuit output current at pin CANL | $V_{CANL}$ = 36 V; $V_{TxD}$ = 0 V | 45 | 70 | 120 | mA |
| $V_{i(dif)\ (th)}$ | | Differential receiver threshold voltage (see Figure 8) | −5 V < $V_{CANL}$ < +12 V; −5 V < $V_{CANH}$ < +12 V; | 0.5 | 0.7 | 0.9 | V |
| $V_{ihcm(dif)\ (th)}$ | | Differential receiver threshold voltage for high common−mode (see Figure 8)) | −35 V < $V_{CANL}$ < +35 V; −35 V < $V_{CANH}$ < +35 V; | 0.40 | 0.7 | 1.00 | V |
| $V_{i(dif)\ (hys)}$ | | Differential receiver input voltage hysteresis (see Figure 8) | −35 V < $V_{CANL}$ < +35 V; −35 V < $V_{CANH}$ < +35 V; | 50 | 70 | 100 | mV |
| $R_{i(cm)}$ (CANH) | | Common−mode input resistance at pin CANH | | 15 | 26 | 37 | kΩ |
| $R_{i(cm)}$ (CANL) | | Common−mode input resistance at pin CANL | | 15 | 26 | 37 | kΩ |
| $R_{i(cm)\ (m)}$ | | Matching between pin CANH and pin CANL common mode input resistance | $V_{CANH}$ = $V_{CANL}$ | −3 | 0 | +3 | % |
| $R_{i(dif)}$ | | Differential input resistance | | 25 | 50 | 75 | kΩ |
| $C_{i(CANH)}$ | CANH CANL | Input capacitance at pin CANH | $V_{TxD}$ = $V_{CC}$; (Note 15) | | 7.5 | 20 | pF |
| $C_{i(CANL)}$ | | Input capacitance at pin CANL | $V_{TxD}$ = $V_{CC}$; (Note 15) | | 7.5 | 20 | pF |
| $C_{i(dif)}$ | | Differential input capacitance | $V_{TxD}$ = $V_{CC}$; (Note 15) | | 3.75 | 10 | pF |
| **COMMON−MODE STABILIZATION** | | | | | | | |
| $V_{SPLIT}$ | VSPLIT | Reference output voltage at pin $V_{SPLIT}$ | Normal mode; −500 μA < $I_{SPLIT}$ < 500 μA | 0.3 x $V_{CC}$ | − | 0.7 x $V_{CC}$ | |
| $I_{SPLIT(i)}$ | | $V_{SPLIT}$ leakage current | Stand−by mode | −5 | | +5 | μA |
| $I_{SPLIT(lim)}$ | | $V_{SPLIT}$ limitation current | Normal mode | −3 | | +3 | mA |
| **POWER ON RESET (POR)** | | | | | | | |
| PORL | | POR level | CANH, CANL, $V_{ref}$ in tri−state below POR level | 2.2 | 3.5 | 4.7 | V |

15. Characterization Data Only, not tested in production.

**Table 9. AC PARAMETER CAN TRANSCEIVER**
The AC parameters are given for $V_{CC}$ and temperature in its operating range; $T_J$ = −40 to +150°C; $R_{LT}$ = 60 Ω unless otherwise specified

| Symbol | Pin(s) | Parameter | Remark / Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **TIMING CHARACTERISTICS** | | | | | | | |
| $t_{d(TxD-BUSon)}$ | | Delay TXD to bus active | $C_l$ = 100 pF between CANH to CANL | 40 | 85 | 105 | ns |
| $t_{d(TxD-BUSoff)}$ | | Delay TXD to bus inactive | $C_l$ = 100 pF between CANH to CANL | 30 | 60 | 105 | ns |
| $t_{d(BUSon-RXD)}$ | | Delay bus active to RXD | $C_{rxd}$ = 15 pF | 25 | 55 | 105 | ns |
| $t_{d(BUSoff-RXD)}$ | | Delay bus inactive to RXD | $C_{rxd}$ = 15 pF | 40 | 100 | 105 | ns |
| $t_{pd(rec-dom)}$ | | Propagation delay TXD to RXD from recessive to dominant | $C_l$ = 100 pF between CANH to CANL | 90 | | 230 | ns |
| $t_{d(dom-rec)}$ | | Propagation delay TXD to RXD from dominant to recessive | $C_l$ = 100 pF between CANH to CANL | 90 | | 245 | ns |
| $t_{d(stb-nm)}$ | | Delay standby mode to normal mode | | 5 | 7.5 | 10 | μs |
| $t_{dbus}$ | | Dominant time for wake−up via bus | | 0.75 | 2.5 | 5 | μs |

16. Characterization Data Only, not tested in production

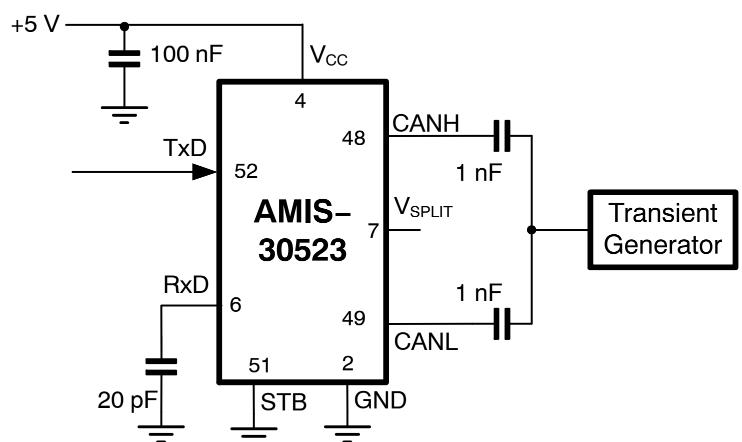


**Figure 7. Test Circuit for Transients**

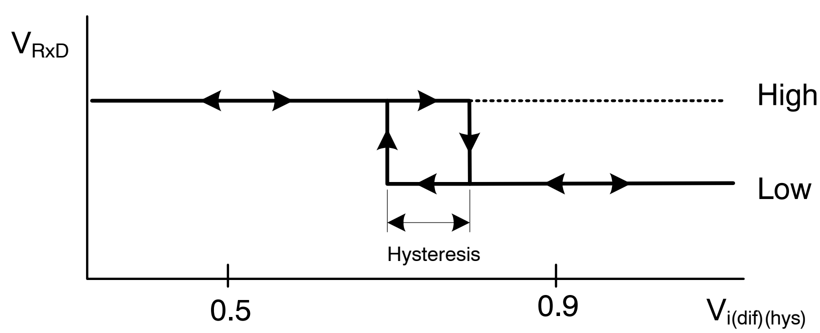


**Figure 8. Hysteresis of the Receiver**

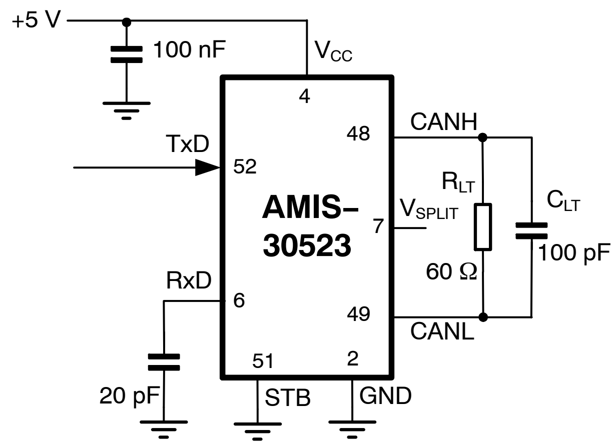


**Figure 9. Test Circuit for Timing Characteristics**

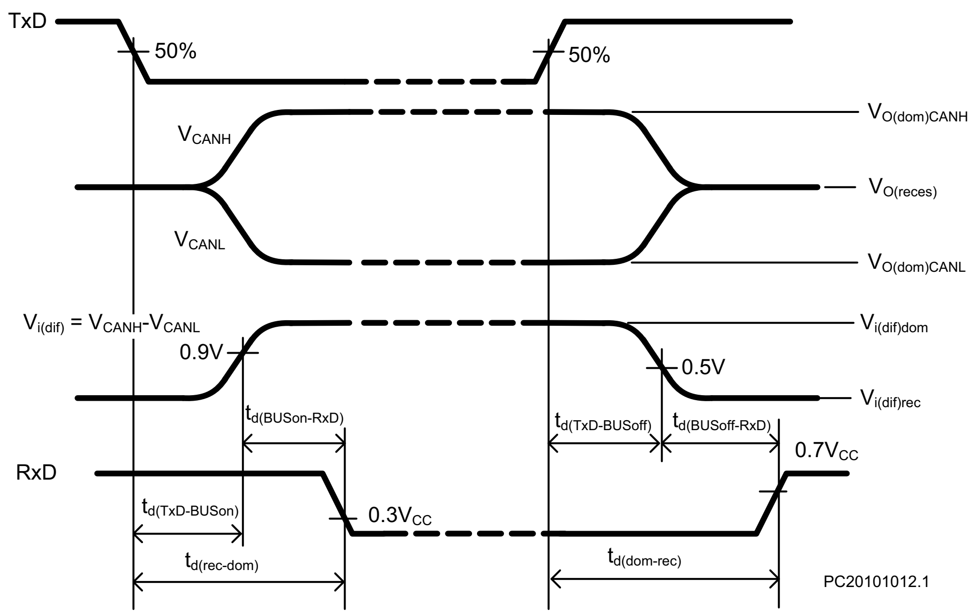


**Figure 10. Timing Diagram for AC Characteristics**

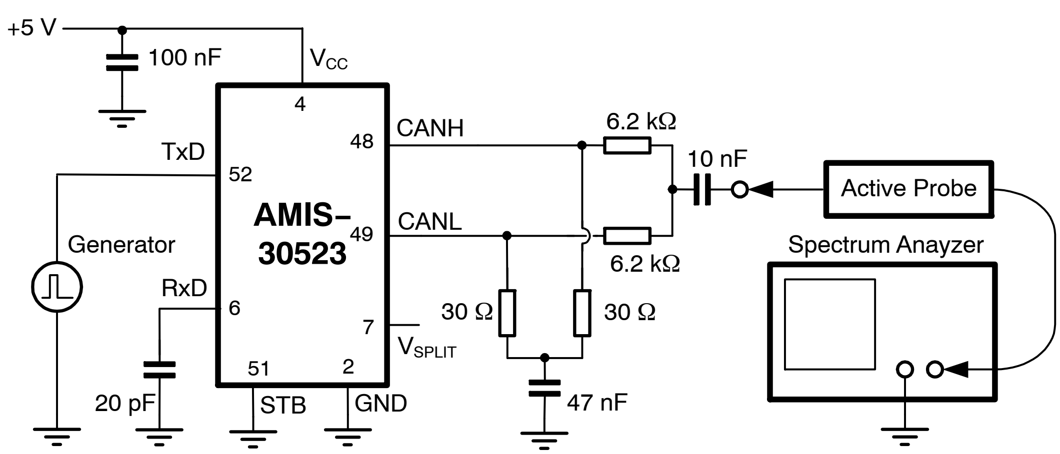


**Figure 11. Basic Test Set−up for EME**

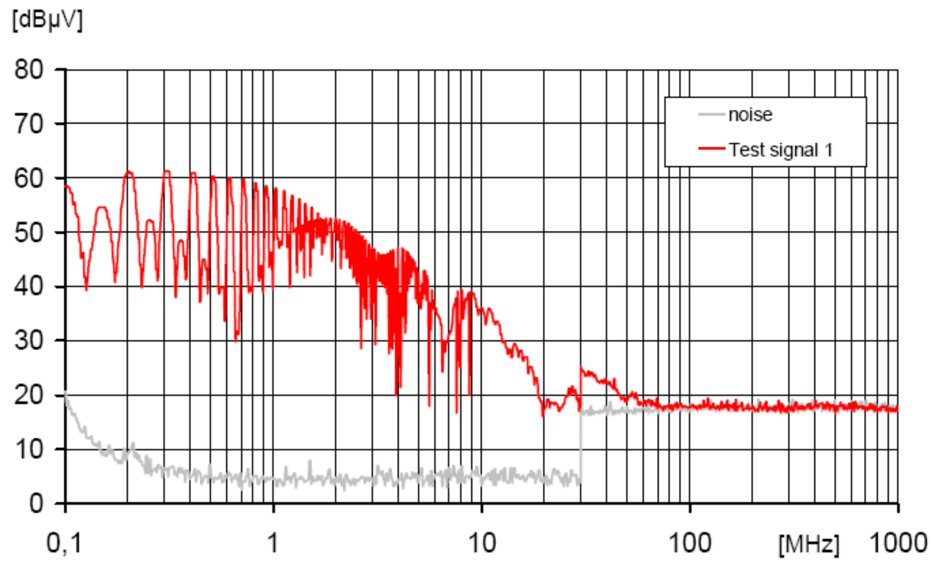


**Figure 12. EME Measurements**

## TYPICAL APPLICATION SCHEMATIC

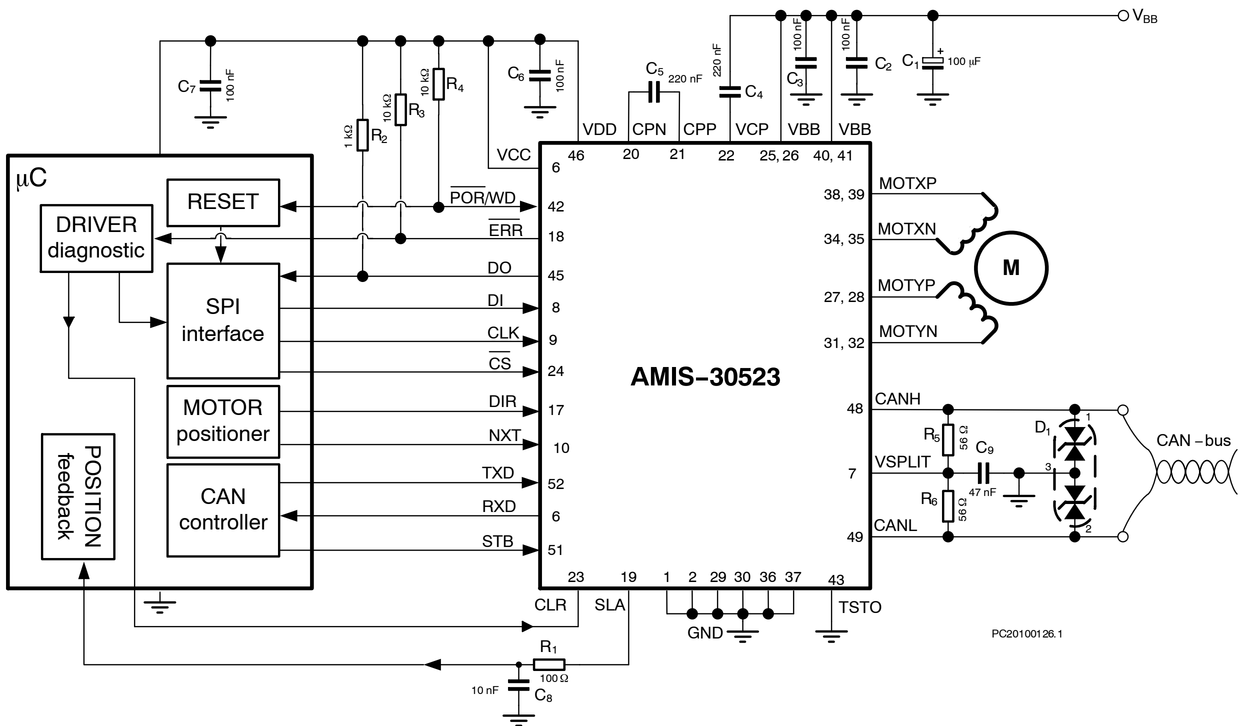


**Figure 13. Typical Application Schematic AMIS−30523**

### Table 10. EXTERNAL COMPONENTS LIST AND DESCRIPTION

| Component | Function | Typ Value | Tolerance | Unit |
|---|---|---|---|---|
| $C_1$ | $V_{BB}$ buffer capacitor (Note 17) | 100 | −20 +80% | μF |
| $C_2$, $C_3$ | $V_{BB}$ decoupling block capacitor | 100 | −20 +80% | nF |
| $C_4$ | Charge−pump pumping capacitor | 220 | ± 20% | nF |
| $C_5$ | Charge−pump buffer capacitor | 220 | ± 20% | nF |
| $C_6$, $C_7$ | $V_{DD}$ buffer capacitor | 100 | ± 20 % | nF |
| $C_8$ | Low pass filter SLA | 10 | ± 20% | nF |
| $C_9$ | VSPLIT decoupling capacitor | 47 | ± 20% | nF |
| $R_1$ | Low pass filter SLA | 100 | ± 1% | Ω |
| $R_2$ | Pull up resistor open drain DO output | 1 | ± 1% | kΩ |
| $R_3$, $R_4$ | Pull up resistor open drain output | 10 | ± 1% | kΩ |
| $R_5$, $R_6$ | CAN termination resistors | 56 | ± 1% | Ω |
| $D_1$ | CAN protection diode | NUP2105 | | |

17. Low ESR < 1 Ω.

## FUNCTIONAL DESCRIPTION MOTOR DRIVER

### Introduction

The AMIS−30523 is a micro−stepping stepper motor driver for bipolar stepper motors embedded with an integrated CAN transceiver.

The motor driver is connected through I/O pins and a SPI interface with an external microcontroller. It has an on−chip voltage regulator, reset−output and watchdog reset, able to supply peripheral devices. It contains a current−translation table and takes the next micro−step depending on the clock signal on the “NXT” input pin and the status of the “DIR” (=direction) register or input pin. A proprietary PWM algorithm is used for reliable current control. The motor driver provides a so−called “speed and load angle” output. This allows the creation of stall detection algorithms and control loops based on load−angle to adjust torque and speed.

### H−Bridge Drivers

A full H−bridge is integrated for each of the two stator windings. Each H−bridge consists of two low−side and two high−side N−type MOSFET switches. Writing logic ‘0’ in bit <MOTEN> disables all drivers (high−impedance). Writing logic ‘1’ in this bit enables both bridges and current can flow in the motor stator windings.

In order to avoid large currents through the H−bridge switches, it is guaranteed that the top− and bottom−switches of the same half−bridge are never conductive simultaneously (interlock delay).

A two−stage protection against shorts on motor lines is implemented. In a first stage, the current in the driver is limited. Secondly, when excessive voltage is sensed across the transistor, the transistor is switched off.

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. The output slope is defined by the gate−drain capacitance of output transistor and the (limited) current that drives the gate. There are two trimming bits for slope control (see Table 15 SPI Control Parameter Overview EMC[1:0]).

The power transistors are equipped with so−called “active diodes”: when a current is forced trough the transistor switch in the reverse direction, i.e. from source to drain, then the transistor is switched on. This ensures that most of the current flows through the channel of the transistor instead of through the inherent parasitic drain−bulk diode of the transistor.

Depending on the desired current range and the micro−step position at hand, the $R_{DS(on)}$ of the low−side transistors will be adapted such that excellent current−sense accuracy is maintained. The $R_{DS(on)}$ of the high−side transistors remain unchanged; see Table 5 DC Parameters Motor driver, for more details.

### PWM Current Control

A PWM comparator compares continuously the actual winding current with the requested current and feeds back the information to a digital regulation loop. This loop then generates a PWM signal, which turns on/off the H−bridge switches. The switching points of the PWM duty−cycle are synchronized to the on−chip PWM clock. The frequency of the PWM controller can be doubled and an artificial jitter can be added (see Table 15 SPI Control Parameter Overview PWMJ). The PWM frequency will not vary with changes in the supply voltage. Also variations in motor−speed or load−conditions of the motor have no effect. There are no external components required to adjust the PWM frequency.

### Automatic Forward and Slow−Fast Decay

The PWM generation is in steady−state using a combination of forward and slow−decay. The absence of fast−decay in this mode, guarantees the lowest possible current−ripple “by design”. For transients to lower current levels, fast−decay is automatically activated to allow high−speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

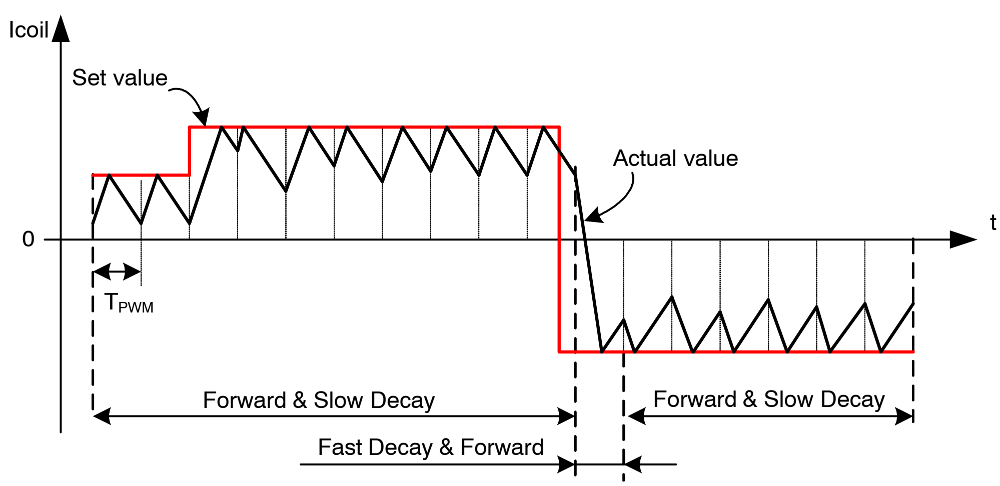


**Figure 14. Forward and Slow/Fast Decay PWM**

### Automatic Duty Cycle Adaptation

In case the supply voltage is lower than 2 * Bemf, then the duty cycle of the PWM is adapted automatically to >50% to maintain the requested average current in the coils. This process is completely automatic and requires no additional parameters for operation. The over−all current−ripple is divided by two if PWM frequency is doubled (see Table 15 SPI Control Parameter Overview PWMF)

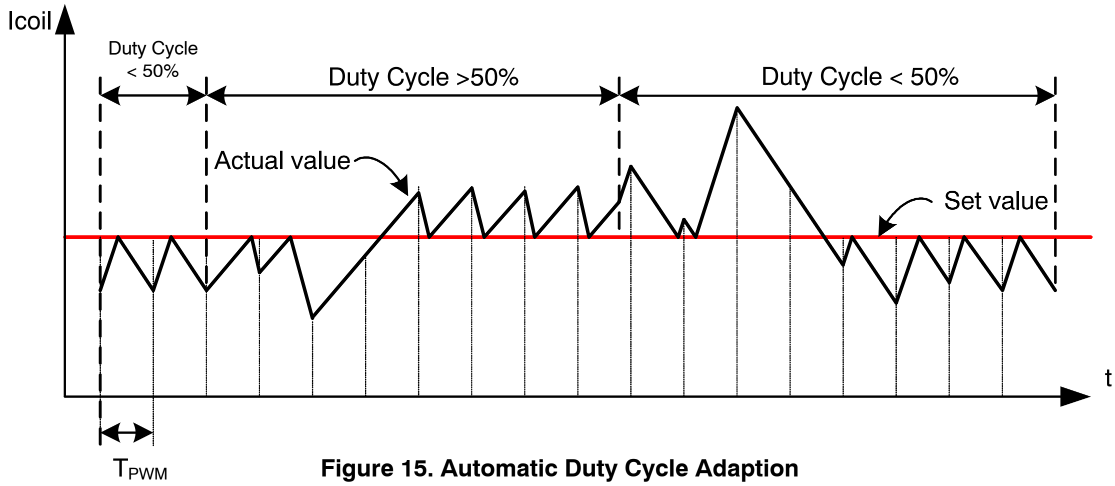


**Figure 15. Automatic Duty Cycle Adaption**

### Step Translator and Step Mode

The step translator provides the control of the motor by means of SPI register Stepmode: SM[2:0], SPI register DIRCNTRL and input pins DIR and NXT. It is translating consecutive steps in corresponding currents in both motor coils for a given step mode.

One out of seven possible stepping modes can be selected through SPI−bits SM[2:0] (see Table 15 SPI Control Parameter Overview ) After power−on or hard reset, the coil−current translator is set to the default 1/32 micro−stepping at position ‘0’. Upon changing the step mode, the translator jumps to position 0* of the corresponding stepping mode. When remaining in the same step mode, subsequent translator positions are all in the same column and increased or decreased with 1. Table 12 lists the output current vs. the translator position.

As shown in Figure 16 the output current−pairs can be projected approximately on a circle in the ($I_x$,$I_y$) plane. There are, however, two exceptions: uncompensated half step and full step. In these step modes the currents are not regulated to a fraction of $I_{max}$ but are in all intermediate steps regulated at 100%. In the ($I_x$,$I_y$) plane the current−pairs are projected on a square. Table 11 lists the output current vs. the translator position for these cases.

**Table 11. SQUARE TRANSLATOR TABLE FOR FULL STEP AND UNCOMPENSATED HALF STEP**

| MSP[6:0] | Stepmode ( SM[2:0] ) | | % of Imax | |
|---|---|---|---|---|
| | 101 | 110 | | |
| | Uncompensated Half−Step | Full Step | Coil x | Coil y |
| **000 0000** | **0** | – | 0 | 100 |
| 001 0000 | 1 | 1 | 100 | 100 |
| 010 0000 | 2 | – | 100 | 0 |
| 011 0000 | 3 | 2 | 100 | −100 |
| 100 0000 | 4 | – | 0 | −100 |
| 101 0000 | 5 | 3 | −100 | −100 |
| 110 0000 | 6 | – | −100 | 0 |
| 111 0000 | 7 | 0 | −100 | 100 |

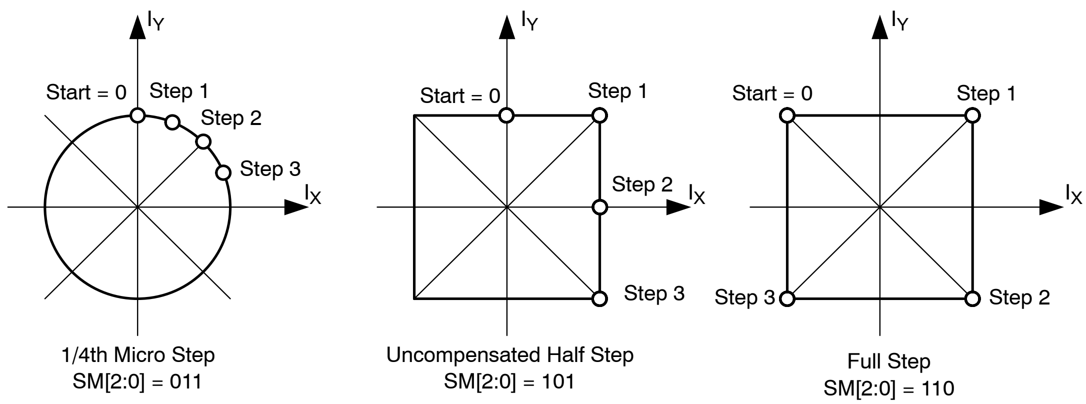


**Figure 16. Translator Table: Circular and Square**

**Table 12. CIRCULAR TRANSLATOR TABLE**

| | Stepmode (SM[2:0]) | | | | | % of $I_{max}$ | |
|---|---|---|---|---|---|---|---|
| | 000 | 001 | 010 | 011 | 100 | | |
| MSP[6:0] | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | Coil x | Coil y |
| 000 0000 | ‘0’ | 0* | 0* | 0* | 0* | 0 | 100 |
| 000 0001 | 1 | – | – | – | – | 3.5 | 98.8 |
| 000 0010 | 2 | 1 | – | – | – | 8.1 | 97.7 |
| 000 0011 | 3 | – | – | – | – | 12.7 | 96.5 |
| 000 0100 | 4 | 2 | 1 | – | – | 17.4 | 95.3 |
| 000 0101 | 5 | – | – | – | – | 22.1 | 94.1 |
| 000 0110 | 6 | 3 | – | – | – | 26.7 | 93 |
| 000 0111 | 7 | – | – | – | – | 31.4 | 91.8 |
| 000 1000 | 8 | 4 | 2 | 1 | – | 34.9 | 89.5 |
| 000 1001 | 9 | – | – | – | – | 38.3 | 87.2 |
| 000 1010 | 10 | 5 | – | – | – | 43 | 84.9 |
| 000 1011 | 11 | – | – | – | – | 46.5 | 82.6 |
| 000 1100 | 12 | 6 | 3 | – | – | 50 | 79 |
| 000 1101 | 13 | – | – | – | – | 54.6 | 75.5 |
| 000 1110 | 14 | 7 | – | – | – | 58.1 | 72.1 |
| 000 1111 | 15 | – | – | – | – | 61.6 | 68.6 |
| 001 0000 | 16 | 8 | 4 | 2 | 1 | 65.1 | 65.1 |
| 001 0001 | 17 | – | – | – | – | 68.6 | 61.6 |
| 001 0010 | 18 | 9 | – | – | – | 72.1 | 58.1 |
| 001 0011 | 19 | – | – | – | – | 75.5 | 54.6 |
| 001 0100 | 20 | 10 | 5 | – | – | 79 | 50 |
| 001 0101 | 21 | – | – | – | – | 82.6 | 46.5 |
| 001 0110 | 22 | 11 | – | – | – | 84.9 | 43 |
| 001 0111 | 23 | – | – | – | – | 87.2 | 38.3 |
| 001 1000 | 24 | 12 | 6 | 3 | – | 89.5 | 34.9 |
| 001 1001 | 25 | – | – | – | – | 91.8 | 31.4 |
| 001 1010 | 26 | 13 | – | – | – | 93 | 26.7 |
| 001 1011 | 27 | – | – | – | – | 94.1 | 22.1 |
| 001 1100 | 28 | 14 | 7 | – | – | 95.3 | 17.4 |
| 001 1101 | 29 | – | – | – | – | 96.5 | 12.7 |
| 001 1110 | 30 | 15 | – | – | – | 97.7 | 8.1 |
| 001 1111 | 31 | – | – | – | – | 98.8 | 3.5 |
| 010 0000 | 32 | 16 | 8 | 4 | 2 | 100 | 0 |
| 010 0001 | 33 | – | – | – | – | 98.8 | −3.5 |
| 010 0010 | 34 | 17 | – | – | – | 97.7 | −8.1 |
| 010 0011 | 35 | – | – | – | – | 96.5 | −12.7 |
| 010 0100 | 36 | 18 | 9 | – | – | 95.3 | −17.4 |
| 010 0101 | 37 | – | – | – | – | 94.1 | −22.1 |
| 010 0110 | 38 | 19 | – | – | – | 93 | −26.7 |
| 010 0111 | 39 | – | – | – | – | 91.8 | −31.4 |
| 010 1000 | 40 | 20 | 10 | 5 | – | 89.5 | −34.9 |
| 010 1001 | 41 | – | – | – | – | 87.2 | −38.3 |
| 010 1010 | 42 | 21 | – | – | – | 84.9 | −43 |
| 010 1011 | 43 | – | – | – | – | 82.6 | −46.5 |
| 010 1100 | 44 | 22 | 11 | – | – | 79 | −50 |
| 010 1101 | 45 | – | – | – | – | 75.5 | −54.6 |
| 010 1110 | 46 | 23 | – | – | – | 72.1 | −58.1 |
| 010 1111 | 47 | – | – | – | – | 68.6 | −61.6 |
| 011 0000 | 48 | 24 | 12 | 6 | 3 | 65.1 | −65.1 |
| 011 0001 | 49 | – | – | – | – | 61.6 | −68.6 |
| 011 0010 | 50 | 25 | – | – | – | 58.1 | −72.1 |
| 011 0011 | 51 | – | – | – | – | 54.6 | −75.5 |
| 011 0100 | 52 | 26 | 13 | – | – | 50 | −79 |
| 011 0101 | 53 | – | – | – | – | 46.5 | −82.6 |
| 011 0110 | 54 | 27 | – | – | – | 43 | −84.9 |
| 011 0111 | 55 | – | – | – | – | 38.3 | −87.2 |
| 011 1000 | 56 | 28 | 14 | 7 | – | 34.9 | −89.5 |
| 011 1001 | 57 | – | – | – | – | 31.4 | −91.8 |
| 011 1010 | 58 | 29 | – | – | – | 26.7 | −93 |
| 011 1011 | 59 | – | – | – | – | 22.1 | −94.1 |
| 011 1100 | 60 | 30 | 15 | – | – | 17.4 | −95.3 |
| 011 1101 | 61 | – | – | – | – | 12.7 | −96.5 |
| 011 1110 | 62 | 31 | – | – | – | 8.1 | −97.7 |
| 011 1111 | 63 | – | – | – | – | 3.5 | −98.8 |

**Table 12. CIRCULAR TRANSLATOR TABLE**

| MSP[6:0] | Stepmode ( SM[2:0] ) | | | | | % of Imax | |
|---|---|---|---|---|---|---|---|
| | 000 | 001 | 010 | 011 | 100 | | |
| | 1/32 | 1/16 | 1/8 | 1/4 | 1/2 | Coil x | Coil y |
| 100 0000 | 64 | 32 | 16 | 8 | 4 | 0 | −100 |
| 100 0001 | 65 | – | – | – | – | −3.5 | −98.8 |
| 100 0010 | 66 | 33 | – | – | – | −8.1 | −97.7 |
| 100 0011 | 67 | – | – | – | – | −12.7 | −96.5 |
| 100 0100 | 68 | 34 | 17 | – | – | −17.4 | −95.3 |
| 100 0101 | 69 | – | – | – | – | −22.1 | −94.1 |
| 100 0110 | 70 | 35 | – | – | – | −26.7 | −93 |
| 100 0111 | 71 | – | – | – | – | −31.4 | −91.8 |
| 100 1000 | 72 | 36 | 18 | 9 | – | −34.9 | −89.5 |
| 100 1001 | 73 | – | – | – | – | −38.3 | −87.2 |
| 100 1010 | 74 | 37 | – | – | – | −43 | −84.9 |
| 100 1011 | 75 | – | – | – | – | −46.5 | −82.6 |
| 100 1100 | 76 | 38 | 19 | – | – | −50 | −79 |
| 100 1101 | 77 | – | – | – | – | −54.6 | −75.5 |
| 100 1110 | 78 | 39 | – | – | – | −58.1 | −72.1 |
| 100 1111 | 79 | – | – | – | – | −61.6 | −68.6 |
| 101 0000 | 80 | 40 | 20 | 10 | 5 | −65.1 | −65.1 |
| 101 0001 | 81 | – | – | – | – | −68.6 | −61.6 |
| 101 0010 | 82 | 41 | – | – | – | −72.1 | −58.1 |
| 101 0011 | 83 | – | – | – | – | −75.5 | −54.6 |
| 101 0100 | 84 | 42 | 21 | – | – | −79 | −50 |
| 101 0101 | 85 | – | – | – | – | −82.6 | −46.5 |
| 101 0110 | 86 | 43 | – | – | – | −84.9 | −43 |
| 101 0111 | 87 | – | – | – | – | −87.2 | −38.3 |
| 101 1000 | 88 | 44 | 22 | 11 | – | −89.5 | −34.9 |
| 101 1001 | 89 | – | – | – | – | −91.8 | −31.4 |
| 101 1010 | 90 | 45 | – | – | – | −93 | −26.7 |
| 101 1011 | 91 | – | – | – | – | −94.1 | −22.1 |
| 101 1100 | 92 | 46 | 23 | – | – | −95.3 | −17.4 |
| 101 1101 | 93 | – | – | – | – | −96.5 | −12.7 |
| 101 1110 | 94 | 47 | – | – | – | −97.7 | −8.1 |
| 101 1111 | 95 | – | – | – | – | −98.8 | −3.5 |
| 110 0000 | 96 | 48 | 24 | 12 | 6 | −100 | 0 |
| 110 0001 | 97 | – | – | – | – | −98.8 | 3.5 |
| 110 0010 | 98 | 49 | – | – | – | −97.7 | 8.1 |
| 110 0011 | 99 | – | – | – | – | −96.5 | 12.7 |
| 110 0100 | 100 | 50 | 25 | – | – | −95.3 | 17.4 |
| 110 0101 | 101 | – | – | – | – | −94.1 | 22.1 |
| 110 0110 | 102 | 51 | – | – | – | −93 | 26.7 |
| 110 0111 | 103 | – | – | – | – | −91.8 | 31.4 |
| 110 1000 | 104 | 52 | 26 | 13 | – | −89.5 | 34.9 |
| 110 1001 | 105 | – | – | – | – | −87.2 | 38.3 |
| 110 1010 | 106 | 53 | – | – | – | −84.9 | 43 |
| 110 1011 | 107 | – | – | – | – | −82.6 | 46.5 |
| 110 1100 | 108 | 54 | 27 | – | – | −79 | 50 |
| 110 1101 | 109 | – | – | – | – | −75.5 | 54.6 |
| 110 1110 | 110 | 55 | – | – | – | −72.1 | 58.1 |
| 110 1111 | 111 | – | – | – | – | −68.6 | 61.6 |
| 111 0000 | 112 | 56 | 28 | 14 | 7 | −65.1 | 65.1 |
| 111 0001 | 113 | – | – | – | – | −61.6 | 68.6 |
| 111 0010 | 114 | 57 | – | – | – | −58.1 | 72.1 |
| 111 0011 | 115 | – | – | – | – | −54.6 | 75.5 |
| 111 0100 | 116 | 58 | 29 | – | – | −50 | 79 |
| 111 0101 | 117 | – | – | – | – | −46.5 | 82.6 |
| 111 0110 | 118 | 59 | – | – | – | −43 | 84.9 |
| 111 0111 | 119 | – | – | – | – | −38.3 | 87.2 |
| 111 1000 | 120 | 60 | 30 | 15 | – | −34.9 | 89.5 |
| 111 1001 | 121 | – | – | – | – | −31.4 | 91.8 |
| 111 1010 | 122 | 61 | – | – | – | −26.7 | 93 |
| 111 1011 | 123 | – | – | – | – | −22.1 | 94.1 |
| 111 1100 | 124 | 62 | 31 | – | – | −17.4 | 95.3 |
| 111 1101 | 125 | – | – | – | – | −12.7 | 96.5 |
| 111 1110 | 126 | 63 | – | – | – | −8.1 | 97.7 |
| 111 1111 | 127 | – | – | – | – | −3.5 | 98.8 |

### Direction

The direction of rotation is selected by means of following combination of the DIR input pin and the SPI−controlled direction bit <DIRCTRL>. (see Table 15 SPI Control Parameter Overview)

### NXT input

Changes on the NXT input will move the motor current one step up/down in the translator table (even when the motor is disabled). Depending on the NXT−polarity bit <NXTP> (see Table 15 SPI Control Parameter Overview), the next step is initiated either on the rising edge or the falling edge of the NXT input.

### Translator Position

The translator position MSP[6:0] can be read in SPI Status Register 3 (See Table 18 SPI Status Registers). This is a 7−bit number equivalent to the 1/32$^{th}$ micro−step from Table 12 "Circular Translator Table". The translator position is updated immediately following a NXT trigger.

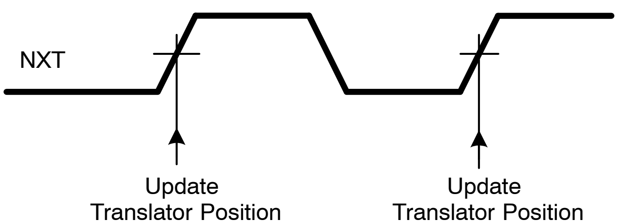


**Figure 17. Translator Position Timing Diagram**

### Synchronization of Step Mode and NXT Input

When step mode is re−programmed to another resolution (Figure 18), then this is put in effect immediately upon the first arriving "NXT" input. If the micro−stepping resolution is increased, the coil currents will be regulated to the nearest micro−step, according to the fixed grid of the increased resolution. If however the micro−stepping resolution is decreased, then it is possible to introduce an offset (or phase shift) in the micro−step translator table.

If the step resolution is decreased at a translator table position that is shared both by the old and new resolution setting, then the offset is zero and micro−stepping is proceeds according to the translator table.

If the translator position is **not** shared both by the old and new resolution setting, then the micro−stepping proceeds with an offset relative to the translator table (See Figure 18 right hand side).

More information can be found in application note AND8399/D.

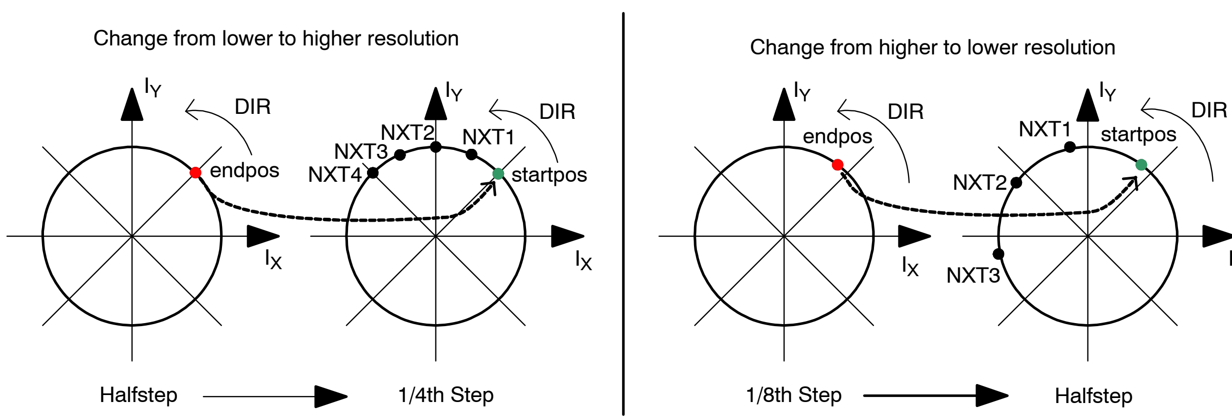


**Figure 18. NXT−Step−Mode Synchronization**

Left: change from lower to higher resolution. The left−hand side depicts the ending half−step position during which a new step mode resolution was programmed. The right−hand side diagram shows the effect of subsequent NXT commands on the micro−step position.

Right: change from higher to lower resolution. The left−hand side depicts the ending micro−step position during which a new step mode resolution was programmed. The right−hand side diagram shows the effect of subsequent NXT commands on the half−step position.

NOTE: It is advised to reduce the micro−stepping resolution only at micro−step positions that overlap with desired micro−step positions of the new resolution.

### Programmable Peak−Current

The amplitude of the current waveform in the motor coils (coil peak current = $I_{max}$) is adjusted by means of an SPI parameter "CUR[4:0]" (see Table 15 SPI Control Parameter Overview). Whenever this parameter is changed, the coil−currents will be updated immediately at the next PWM period. Figure 19 presents the Peak−Current and Current Ratings in conjunction to the Current setting CUR[4:0].

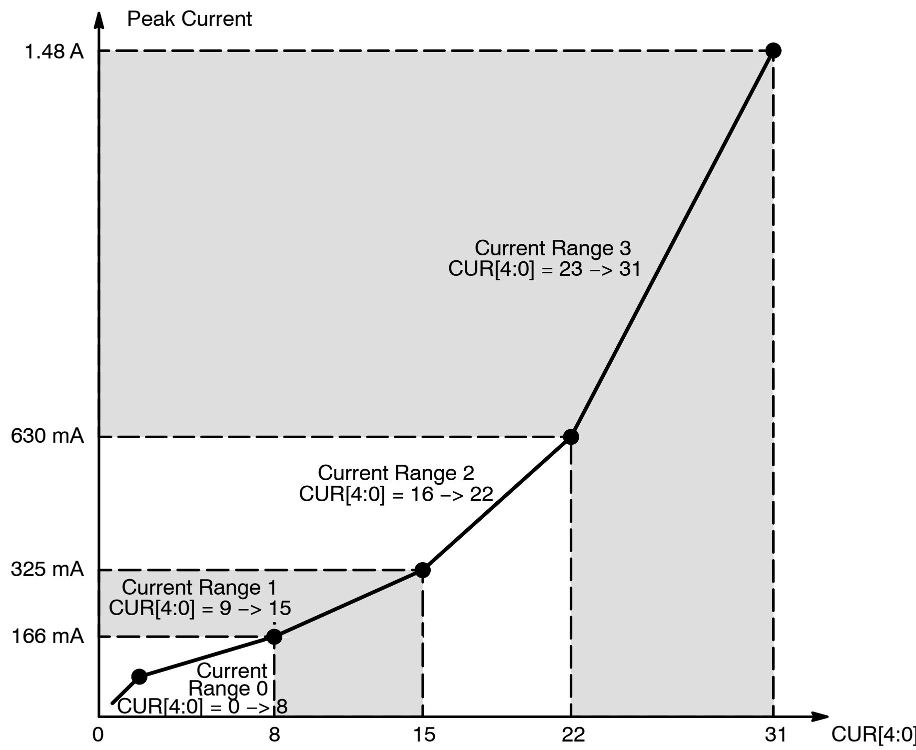


**Figure 19. Programmable Peak−Current Overview**

**Speed and Load Angle Output**

The SLA−pin provides an output voltage that indicates the level of the Back−e.m.f. voltage of the motor. This Back−e.m.f. voltage is sampled during every so−called ”coil current zero crossings”. Per coil, two zero−current positions exist per electrical period, yielding in total four zero−current observation points per electrical period.

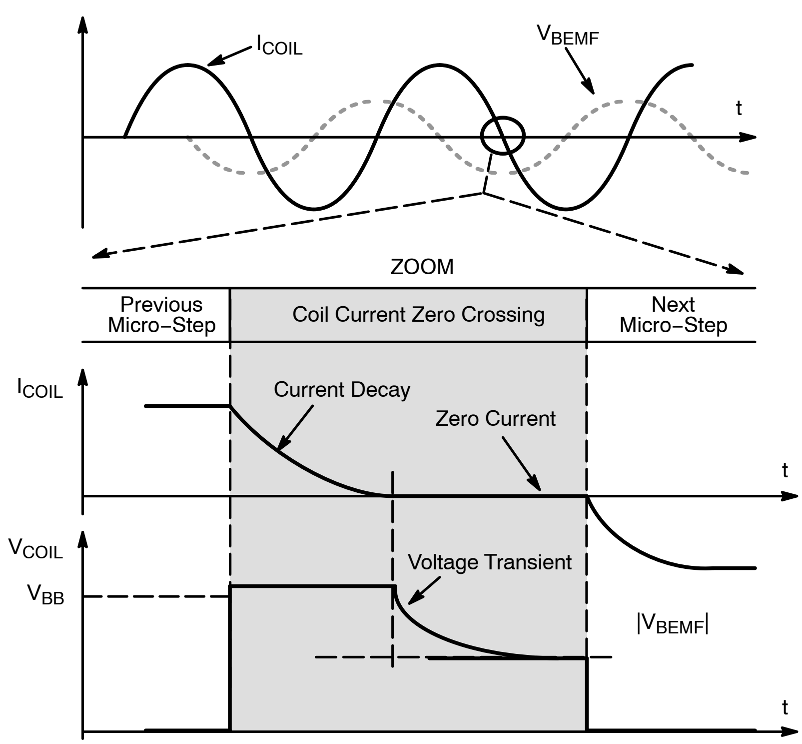


**Figure 20. Principle of Bemf Measurement**

Because of the relatively high recirculation currents in the coil during current decay, the coil voltage $V_{COIL}$ shows a transient behavior. As this transient is not always desired in application software, two operating modes can be selected by means of the bit <SLAT> (see “SLA−transparency” in Table 15 SPI Control Parameter Overview). The SLA pin shows in “transparent mode” full visibility of the voltage transient behavior. This allows a sanity−check of the speed−setting versus motor operation and characteristics and supply voltage levels. If the bit “SLAT” is cleared, then only the voltage samples at the end of each coil current zero crossing are visible on the SLA−pin. Because the transient behavior of the coil voltage is not visible anymore, this mode generates smoother Back e.m.f. input for post−processing, e.g. by software.

In order to bring the sampled Back e.m.f. to a descent output level (0 to 5 V), the sampled coil voltage $V_{COIL}$ is divided by 2 or by 4. This divider is set through an SPI bit <SLAG> (see Table 15 SPI Control Parameter Overview).

The following drawing illustrates the operation of the SLA−pin and the transparency−bit. “PWMsh” and “$I_{coil} = 0$” are internal signals that define together with SLAT the sampling and hold moments of the coil voltage.

More information can be found in application note AND8399/D.

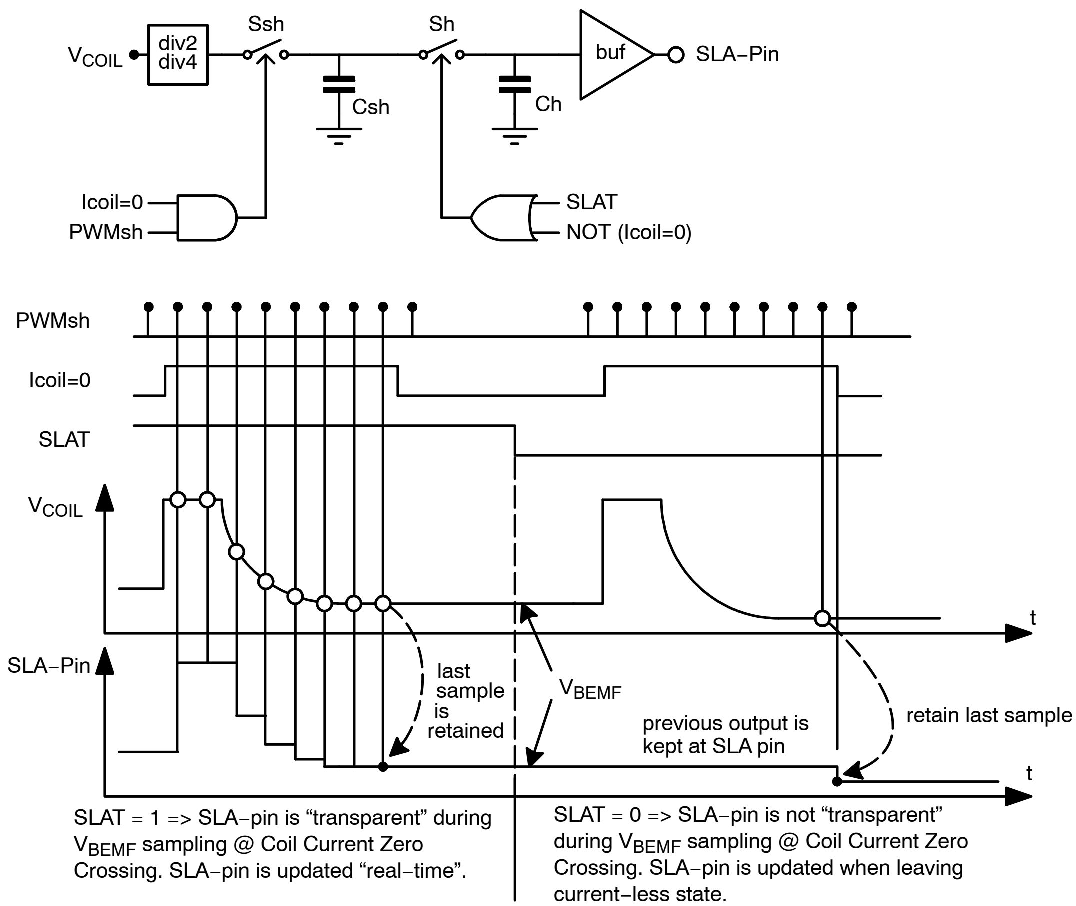


**Figure 21. Timing Diagram of SLA−Pin**

### Warning, Error Detection and Diagnostics Feedback

#### Thermal Warning and Shutdown

When junction temperature rises above $T_{TW}$, the thermal warning bit <TW> is set (Table 17 SPI Status registers Address SR0). If junction temperature increases above thermal shutdown level, then the circuit goes in “Thermal Shutdown” mode (<TSD>) and all driver transistors are disabled (high impedance) (see Table 17 SPI Status registers Address SR2). The conditions to reset flag <TSD> is to be at a temperature lower than $T_{TW}$ and to clear the <TSD> flag reading out Status Register 2.

#### Over−Current Detection

The over−current detection circuit monitors the load current in each activated output stage. If the load current exceeds the over−current detection threshold, then the over−current flag is set and the drivers are switched off to reduce the power dissipation and to protect the integrated circuit. Each driver transistor has an individual detection bit in (see Table 17 SPI Status registers Address SR1 and SR2: <OVCXij> and <OVCYij>). Error condition is latched and the microcontroller needs to clear the status bits (by reading Status Register 1 or 2) to reactivate the drivers.

**Note**: Successive reading the SPI StatusRegisters 1 and 2 in case of a short circuit condition, may lead to damage to the drivers

#### Open Coil/Current Not Reached Detection

Open coil detection is based on the observation of 100% duty cycle of the PWM regulator. If in a coil 100% duty cycle is detected for longer than 200 ms then the related driver transistors are disabled (high−impedance) and an appropriate bit in the SPI status register is set (<OPENX> or <OPENY>). (Table 17 SPI Status Register Address SR0)

When the resistance of a motor coil is very large and the supply voltage is low, it can happen that the motor driver is not able to deliver the requested current to the motor. Under these conditions the PWM controller duty cycle will be 100% and after 200 ms the error pin and <OPENX>, <OPENY> will flag this situation (motor current is kept alive). This feature can be used to test if the operating conditions (supply voltage, motor coil resistance) still allow reaching the requested coil−current or else the coil current should be reduced.

#### Charge Pump Failure

The charge pump is an important circuit that guarantees low $R_{DS(on)}$ for all drivers, especially for low supply voltages. If supply voltage is too low or external components are not properly connected to guarantee $R_{DS(on)}$ of the drivers, then the bit <CPFAIL> is set in Table 17. Also after POR the charge pump voltage will need some time to exceed the required threshold. During that time $t_{CPU}$ <CPFAIL> will be set to “1”.

#### Error Output

This is a digital output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = <TW> OR <TSD> OR <OVCXij> OR < OVCYij> OR <OPENi> OR <CPFAIL>

This open drain output can be wired OR−ed with error outputs other motor drivers.

#### Logic Supply Regulator

AMIS−30523 has an on−chip 5 V low−drop regulator with external capacitor to supply the digital part of the chip, some low−voltage analog blocks and external circuitry. The voltage level is derived from an internal bandgap reference. To calculate the available drive−current for external circuitry, the specified $I_{load}$ should be reduced with the consumption of internal circuitry (unloaded outputs) and the loads connected to logic outputs. See Table 5 DC parameters Motor Driver.

#### Power−On Reset (POR) Function

The open drain output pin PORB/WD provides an “active low” reset for external purposes. At power−up of AMIS−30523, this pin will be kept low for some time to reset for example an external microcontroller. A small analogue filter avoids resetting due to spikes or noise on the $V_{DD}$ supply.

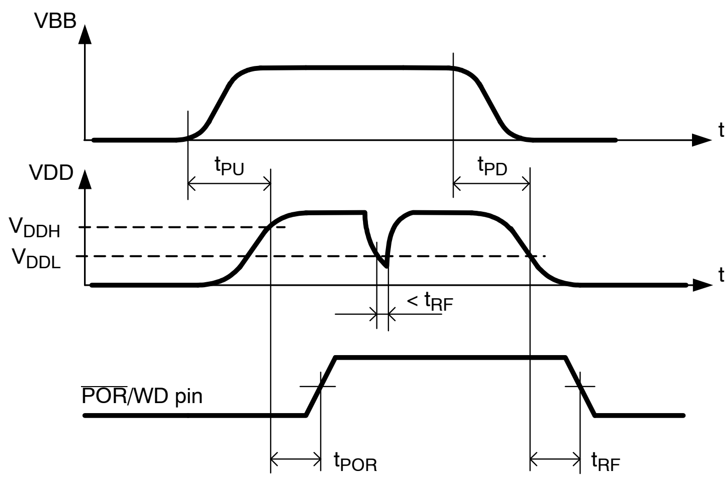


**Figure 22. Power−on−Reset Timing Diagram**