
Chipsmall
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采购部

AMIS−30621

Micro−Stepping Motor Driver

INTRODUCTION

The AMIS−30621 is a single−chip micro−stepping motor driver with position controller and control/diagnostic interface. It is ready to build dedicated mechatronics solutions connected remotely with a LIN master.

The chip receives positioning instructions through the bus and subsequently drives the motor coils to the desired position. The on−chip position controller is configurable (OTP or RAM) for different motor types, positioning ranges and parameters for speed, acceleration and deceleration. The AMIS−30621 acts as a slave on the LIN bus and the master can fetch specific status information like actual position, error flags, etc. from each individual slave node.

The chip is implemented in I2T100 technology, enabling both high voltage analog circuitry and digital functionality on the same chip. The AMIS−30621 is fully compatible with the automotive voltage requirements.

PRODUCT FEATURES

Motordriver

- Micro−Stepping Technology
- Peak Current Up to 800 mA
- Fixed Frequency PWM Current−Control
- Automatic Selection of Fast and Slow Decay Mode
- No External Fly−Back Diodes Required
- Compliant with 14 V Automotive Systems and Industrial Systems Up to 24 V

Controller with RAM and OTP Memory

- Position Controller
- Configurable Speeds and Acceleration
- Input to Connect Optional Motion Switch

LIN Interface

- Physical Layer Compliant to LIN rev. 2.0. Data−Link Layer Compatible with LIN Rev. 1.3 (Note 1)
- Field−Programmable Node Addresses
- Dynamically Allocated Identifiers
- Diagnostics and Status Information

Protection

- Overcurrent Protection
- Undervoltage Management
- Open−Circuit Detection
- High Temperature Warning and Management
- Low Temperature Flag
- LIN Bus Short−Circuit Protection to Supply and Ground
- Lost LIN Safe Operation

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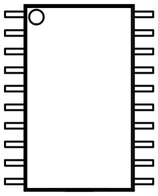
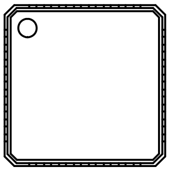


SOIC−20
3 & 7 SUFFIX
CASE 751AQ



NQFP−32
6 SUFFIX
CASE 560AA

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Power Saving

- Powerdown Supply Current < 50 μA
- 5 V Regulator with Wake−up on LIN Activity

EMI Compatibility

- LIN Bus Integrated Slope Control
- HV Outputs with Slope Control

- These are Pb−Free Devices

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1. Minor exceptions to the conformance of the data−link layer to LIN rev. 1.3.

APPLICATIONS

The AMIS−30621 is ideally suited for small positioning applications. Target markets include: automotive (headlamp alignment, HVAC, idle control, cruise control), industrial equipment (lighting, fluid control, labeling, process control, XYZ tables, robots...) and building automation (HVAC, surveillance, satellite dish, renewable energy systems). Suitable applications typically have multiple axes or require mechatronic solutions with the driver chip mounted directly on the motor.

Table 1. ORDERING INFORMATION

Part No.	Peak Current	UV*	Package	Shipping†
AMIS30621C6213G	800 mA	High	SOIC−20 (Pb−Free)	Tube / Tray
AMIS30621C6213RG	800 mA	High		Tape & Reel
AMIS30621C6216G	800 mA	Low	NQFP−32 (7 x 7 mm) (Pb−Free)	Tube / Tray
AMIS30621C6216RG	800 mA	Low		Tape & Reel
AMIS30621C6217G**	800 mA	Low	SOIC−20 (Pb−Free)	Tube / Tray
AMIS30621C6217RG**	800 mA	Low		Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*UV undervoltage lock out levels: see DC Parameters UV1 & UV2 (Stop Voltage thresholds).

** For prodcut versions AMIS30621C6217G and AMIS30621C6217RG the Ihold0 bit in OTP is programmed to ‘1’.

QUICK REFERENCE DATA

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{BB}, VHW2, VSWI	Supply voltage, Hardwired Address and SWI Pins	−0.3	+40 (Note 1)	V
V_{lin}	Bus input voltage	−40	+40	V
T_J	Junction temperature range (Note 2)	−50	+175	°C
T_{st}	Storage temperature	−55	+160	°C
V_{esd}	Human Body Model Electrostatic discharge voltage on LIN pin (Note 3)	−4	+4	kV
	Human Body Model Electrostatic discharge voltage on other pins (Note 3)	−2	+2	kV
	CDM Electrostatic discharge voltage on other pins (Note 4)	−500	+500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. For limited time: V_{BB} < 0.5 s, SWI and HW2 pins < 1.0 s.
2. The circuit functionality is not guaranteed.
3. Human Body Model according to MIL−STD−883 Method 3015.7, measured on SOIC devices, and according to AEC−Q100: EIA−JESD22−A114−B (100 pF via 1.5 kΩ) measured on NQFP device.
4. CDM according to EOS_ESD−DS5.3−1993 (draft)−socketed mode, measured on SOIC devices, and according to AEC−Q100: EIA−JESD22−A115−A measured on NQFP devices.

Table 3. OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
V_{BB}	Supply voltage	+6.5	+29	V
T_J	Operating temperature range (Note 5)	−40	+165	°C

5. Note that the thermal warning and shutdown will get active at the level specified in the “DC Parameters”. No more than 100 cumulated hours in life time above T_{tw}.

Table of Contents

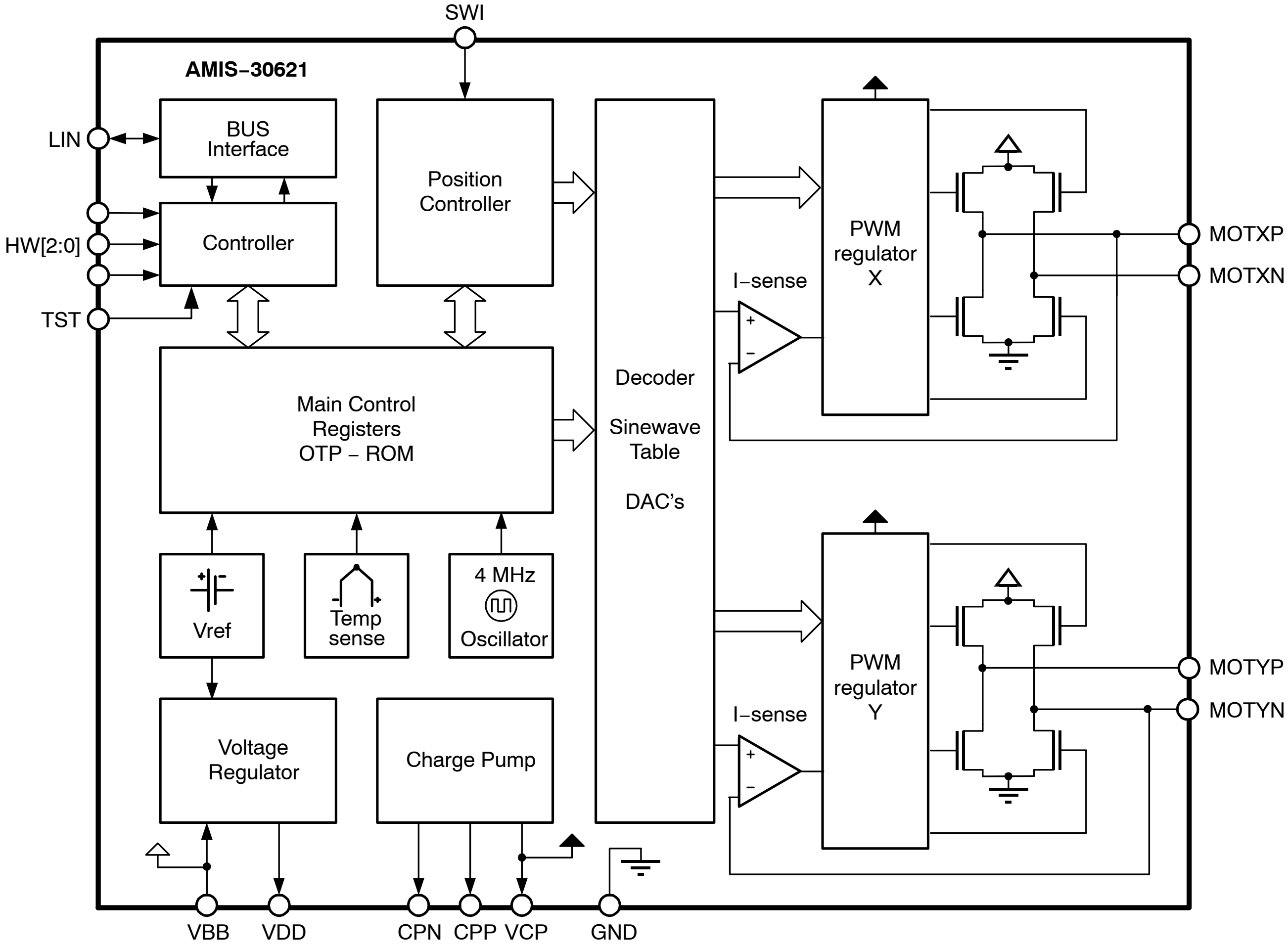


Figure 1. Block Diagram

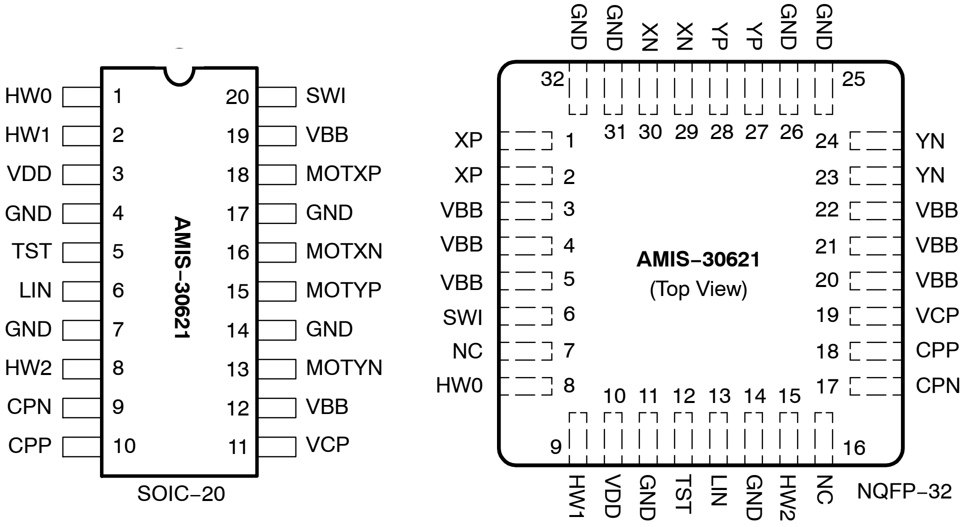


Figure 2. SOIC−20 and NQFP−32 Pin−out

Table 4. PIN DESCRIPTION

Pin Name	Pin Description		SOIC−20	NQFP−32
HW0	Bit 0 of LIN−ADD	To be Tied to GND or V_{DD}	1	8
HW1	Bit 1 of LIN−ADD		2	9
V_{DD}	Internal supply (needs external decoupling capacitor)		3	10
GND	Ground, heat sink		4,7,14,17	11, 14, 25, 26, 31, 32
TST	Test pin (to be tied to ground in normal operation)		5	12
LIN	LIN−bus connection		6	13
HW2	Bit 2 LIN−ADD		8	15
CPN	Negative connection of pump capacitor (charge pump)		9	17
CPP	Positive connection of pump−capacitor (charge pump)		10	18
VCP	Charge−pump filter−capacitor		11	19
V_{BB}	Battery voltage supply		12,19	3, 4, 5, 20, 21, 22
MOTYN	Negative end of phase Y coil		13	23, 24
MOTYP	Positive end of phase Y coil		15	27, 28
MOTXN	Negative end of phase X coil		16	29, 30
MOTXP	Positive end of phase X coil		18	1, 2
SWI	Switch input		20	6
NC	Not connected (to be tied to ground)			7, 16

PACKAGE THERMAL RESISTANCE

The AMIS−30621 is available in SOIC−20 and optimized NQFP32 packages. For cooling optimizations, the NQFP has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the head to the bottom layer. Figures 3 and 4 give examples for good power distribution solutions.

For precise thermal cooling calculations the major thermal resistances of the devices are given. The thermal media to which the power of the devices has to be given are:

- Static environmental air (via the case)
- PCB board copper area (via the device pins and exposed pad)

The thermal resistances are presented in Table 5: DC Parameters.

The major thermal resistances of the device are the Rth from the junction to the ambient (Rthja) and the overall Rth from the junction to the leads (Rthjp).

The NQFP device is designed to provide superior thermal performance. Using an exposed die pad on the bottom surface of the package, is mainly contributing to this performance. In order to take full advantage of the exposed pad, it is most important that the PCB has features to conduct heat away from the package. A thermal grounded pad with thermal vias can achieve this.

In below table, one can find the values for the Rthja and Rthjp, simulated according to the JESD−51standard:

Package	Rth Junction−to−Leads and Exposed Pad (Rthjp)	Rth Junction−to−Leads (Rthjp)	Rth Junction−to−Ambient Rthja 1S0P	Rth Junction−to−Ambient Rthja 2S2P
SOIC−20		19	62	39
NQFP−32	0.95		60	30

The Rthja for 2S2P is simulated conform to JESD−51 as follows:

- A 4−layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
- Board thickness is 1.46 mm (FR4 PCB material)
- The 2 signal layers: 70 μm thick copper with an area of 5500 mm^2 copper and 20% conductivity
- The 2 power internal planes: 36 μm thick copper with an area of 5500 mm^2 copper and 90% conductivity

The Rthja for 1S0P is simulated conform to JESD−51 as follows:

- A 1−layer printed circuit board with only 1 layer
- Board thickness is 1.46 mm (FR4 PCB material)
- The layer has a thickness of 70 μm copper with an area of 5500 mm^2 copper and 20% conductivity

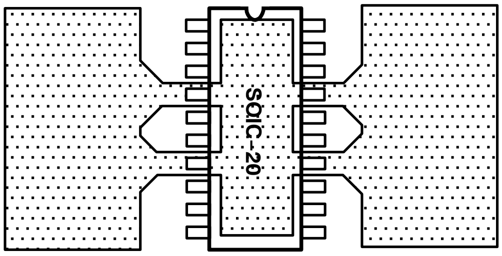


Figure 3. Example of SOIC−20 PCB Ground Plane Layout (Preferred Layout at Top and Bottom)

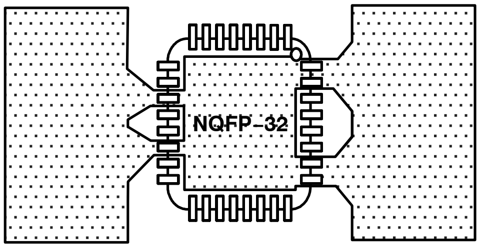


Figure 4. Example of NQFP−32 PCB Ground Plane Layout (Preferred Layout at Top and Bottom)

DC PARAMETERS

The DC parameters are guaranteed over temperature and V_{BB} in the operating range, unless otherwise specified. Convention: currents flowing into the circuit are defined as positive.

Table 5. DC PARAMETERS

Symbol	Pins	Parameter	Test Conditions	Min	Typ	Max	Unit
MOTORDRIVER							
$I_{MSmax,Peak}$	MOTXP MOTXN MOTYP MOTYN	Max current through motor coil in normal operation	V_{BB} = 14 V		800		mA
$I_{MSmax,RMS}$		Max RMS Current Through Coil in Normal Operation	V_{BB} = 14 V		570		mA
I_{MSabs}		Absolute Error on Coil Current (Note 6)	V_{BB} = 14 V	−10		10	%
I_{MSrel}		Matching of X and Y Coil Currents	V_{BB} = 14 V	−7	0	7	%
$R_{DS(on)}$		On Resistance for Each Motor Pin at I_{MSmax} (Note 7)	V_{BB} = 12 V, T_J = 50°C		0.50	1	Ω
			V_{BB} = 8 V, T_J = 50°C		0.55	1	Ω
			V_{BB} = 12 V, T_J = 150°C		0.70	1	Ω
			V_{BB} = 8 V, T_J = 150°C		0.85	1	Ω
I_{MSL}		Pull down current	HiZ Mode, V_{BB} = 7.7 V	0.4		2.2	mA
LIN TRANSMITTER							
I_{bus_off}	LIN	Dominant State, Driver Off	V_{bus} = 0 V, V_{BB} = 8 V and 18 V	−1			mA
I_{bus_off}		Recessive State, Driver Off	V_{bus} = V_{bat}, V_{BB} = 8 V and 18 V			20	μA
I_{bus_lim}		Current Limitation	V_{BB} = 8 V and 18 V	50	75	130	mA
R_{slave}		Pullup Resistance	V_{BB} = 8 V and 18 V	20	30	47	kΩ
LIN RECEIVER							
V_{bus_dom}	LIN	Receiver Dominant State	V_{BB} = 8 V and 18 V	0		0.4 * V_{BB}	V
V_{bus_rec}		Receiver Recessive State	V_{BB} = 8 V and 18 V	0.6 * V_{BB}		V_{BB}	V
V_{bus_hys}		Receiver Hysteresis	V_{BB} = 8 V and 18 V	0.05 * V_{BB}		0.175 * V_{BB}	V
THERMAL WARNING AND SHUTDOWN							
T_{tw}		Thermal warning		138	145	152	°C
T_{tsd}		Thermal shutdown (Notes 8 and 9)			T_{tw} + 10		°C
T_{low}		Low temperature warning (Note 9)			T_{tw} − 152		°C
SUPPLY AND VOLTAGE REGULATOR							
V_{BBOTP}	V_{BB}	Supply voltage for OTP zapping (Note 10)		9.0		10.0	V
UV_1		Stop voltage high threshold	Product versions with low UV; See Ordering Information	7.7	8.3	8.9	V
UV_2		Stop voltage low threshold		7.0	7.5	8.0	V
UV_1		Stop voltage high threshold	Product versions with high UV; See Ordering Information	8.8	9.3	9.8	V
UV_2		Stop voltage low threshold		8.1	8.5	8.9	V
I_{bat}		Total current consumption	Unloaded outputs V_{BB} = 29 V	1	3.50	10.0	mA
I_{bat_s}		Sleep mode current consumption	V_{BB} = 8 V and 18 V		40	100	μA
V_{DD}	V_{DD}	Regulated internal supply (Note 11)	8 V < V_{BB} < 29 V	4.75	5	5.25	V
$V_{DDReset}$		Digital supply reset level @ powerdown (Note 12)				4.5	V
I_{DDLim}		Current limitation	Pin shorted to ground V_{BB} = 14 V			40	mA

Table 5. DC PARAMETERS

Symbol	Pins	Parameter	Test Conditions	Min	Typ	Max	Unit
SWITCH INPUT AND HARDWIRE ADDRESS INPUT							
$Rt_{\_OFF}$	SWI HW2	Switch OPEN Resistance (Note 13)		10			kΩ
$Rt_{\_ON}$		Switch ON Resistance (Note 13)	Switch to GND or V_{BB}			2	kΩ
V_{BB_sw}		V_{BB} range for guaranteed operation of SWI and HW2		6		29	V
I_{lim_sw}		Current limitation	Short to GND or V_{bat} V_{BB} = 29 V			45	mA
HARDWIRED ADDRESS INPUTS AND TEST PIN							
V_{high}	HW0 HW1 TST	Input level high	V_{BB} = 14 V	0.7 * V_{DD}			V
V_{low}		Input level low	V_{BB} = 14 V			0.3 * V_{DD}	V
HW_{hyst}		Hysteresis	V_{BB} = 14 V	0.075 * V_{DD}			V
CHARGE PUMP							
V_{CP}	VCP	Output voltage	7 V < V_{BB} ≤ 14 V		2 * V_{BB} − 2.5		V
			14 V < V_{BB}	V_{BB} + 10		V_{BB} + 15	V
C_{buffer}		External buffer capacitor		220		470	nF
C_{pump}	CPP CPN	External pump capacitor		220		470	nF
PACKAGE THERMAL RESISTANCE VALUES							
Rth_{ja}	SO	Thermal resistance junction−to−ambient (2S2P)	Simulated conform JEDEC JES.D51		39		K/W
Rth_{jp}	SO	Thermal resistance junction−to−leads			19		K/W
Rth_{ja}	NQ	Thermal resistance junction−to−ambient (2S2P)			30		K/W
Rth_{jp}	NQ	Thermal resistance junction−to−leads and exposed pad			0.95		K/W

6. Tested in production for 800 mA, 400 mA, 200 mA and 100 mA current settings for both X and Y coil.
7. Based on characterization data.
8. No more than 100 cumulated hours in life time above T_{tw}.
9. Thermal shutdown and low temperature warning are derived from thermal warning. Guaranteed by design.
10. A buffer capacitor of minimum 100 μF is needed between V_{BB} and GND. Short connections to the power supply are recommended.
11. Pin V_{DD} must not be used for any external supply
12. The RAM content will not be altered above this voltage.
13. External resistance value seen from pin SWI or HW2, including 1 kΩ series resistor. For the switch OPEN, the maximum allowed leakage current is represented by a minimum resistance seen from the pin.

AC PARAMETERS

The AC parameters are guaranteed for temperature and V_{BB} in the operating range unless otherwise specified. The LIN transmitter and receiver physical layer parameters are compliant to LIN rev. 2.0 & 2.1.

Table 6. AC PARAMETERS

Symbol	Pins	Parameter	Test Conditions	Min	Typ	Max	Unit
POWERUP							
T_{pu}		Powerup Time	Guaranteed by Design			10	ms
INTERNAL OSCILLATOR							
f_{osc}		Frequency of Internal Oscillator	V_{BB} = 14 V	3.6	4.0	4.4	MHz
LIN TRANSMITTER CHARACTERISTICS ACCORDING TO LIN V2.0 & V2.1							
D1	LIN	Duty Cycle 1 = $t_{Bus\_rec(min)}$/ (2 x t_{Bit}); See Figure 5	THRec(max)= 0.744 x V_{BB} THDom(max)= 0.581 x V_{BB}; V_{BB} = 7.0 V...18 V; t_{Bit} = 50 μs	0.396			
D2		Duty Cycle 2 = $t_{Bus\_rec(max)}$/ (2 x t_{Bit}); See Figure 5	THRec(min)= 0.284 x V_{BB} THDom(min)= 0.422 x V_{BB}; V_{BB} = 7.6 V...18 V; t_{Bit} = 50 μs			0.581	
LIN RECEIVER CHARACTERISTICS ACCORDING TO LIN V2.0 & V2.1							
trx_pdr	LIN	Propagation delay bus dominant to RxD = Low	V_{BB} = 7.0 V & 18 V; See Figure 5			6	μs
trx_pdf		Propagation delay bus recessive to RxD = High	V_{BB} = 7.0 V & 18 V; See Figure 5			6	μs
trx_sym		Symmetry of receiver propagation delay	trx_pdr – trx_pdf	−2		+2	μs
SWITCH INPUT AND HARDWIRE ADDRESS INPUT							
T_{sw}	SWI HW2	Scan pulse period (Note 14)	V_{BB} = 14 V		1024		μs
T_{sw_on}		Scan pulse duration (Note 14)	V_{BB} = 14 V		64		μs
MOTORDRIVER							
F_{pwm}	MOTxx	PWM frequency (Note 14)		18	20	22.0	kHz
T_{brise}		Turn−on transient time	Between 10% and 90% V_{BB} = 14 V		150		ns
T_{bfall}		Turn−off transient time			140		ns
T_{stab}		Run current stabilization time (Note 14)			1/Vmin		s
CHARGE PUMP							
f_{CP}	CPN CPP	Charge pump frequency (Note 14)	V_{BB} = 14 V		250		kHz

14. Derived from the internal oscillator

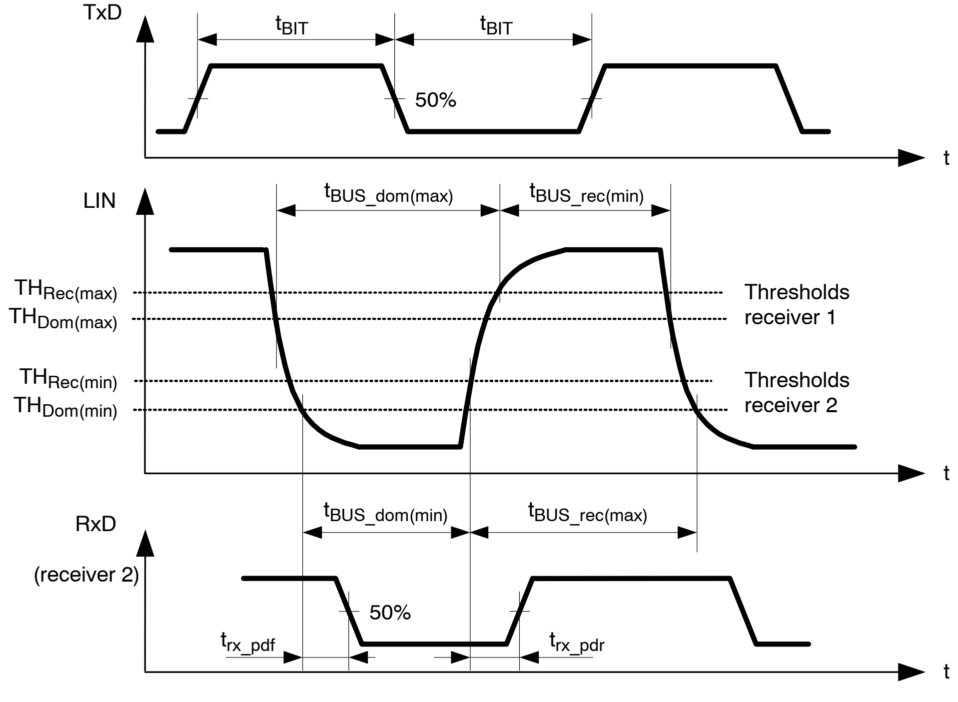


Figure 5. Timing Diagram for AC Characteristics According to LIN 2.0 & 2.1

TYPICAL APPLICATION

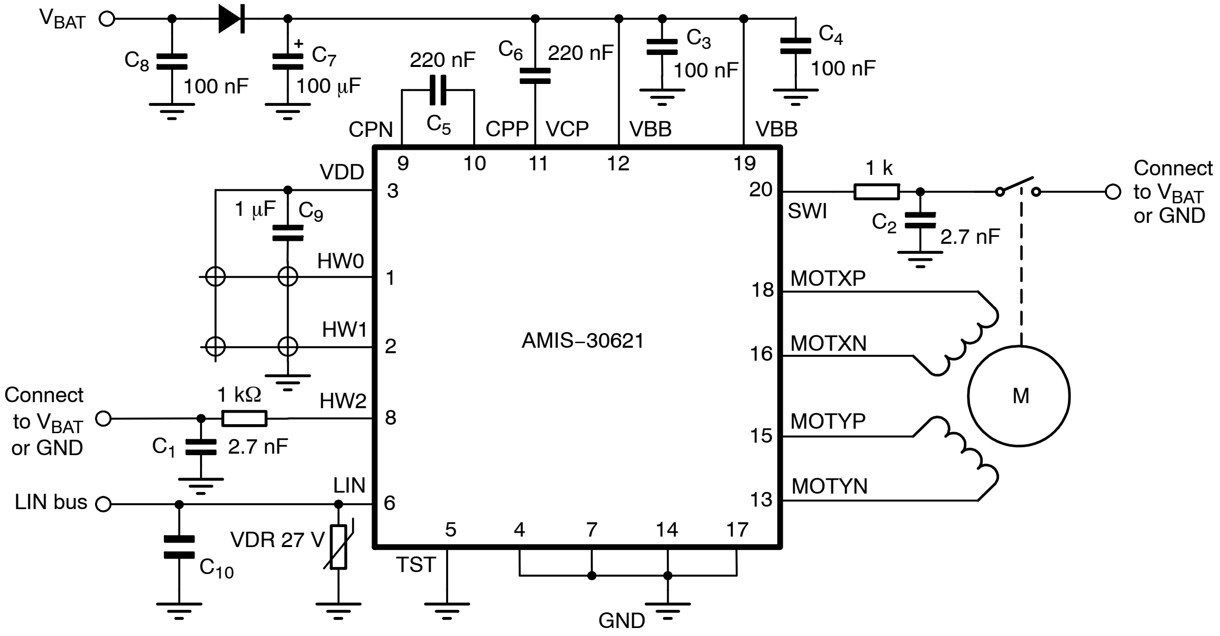


Figure 6. Typical Application Diagram for SO device.

15. All resistors are ±5%, 1/4 W
16. C_1, C_2 minimum value is 2.7 nF, maximum value is 10 nF
17. Depending on the application, the ESR value and working voltage of C_7 must be carefully chosen
18. C_3 and C_4 must be close to pins V_{BB} and GND
19. C_5 and C_6 must be as close as possible to pins CPN, CPP, VCP, and V_{BB} to reduce EMC radiation
20. C_9 must be a ceramic capacitor to assure low ESR
21. C_{10} is placed for EMC reasons; value depends on EMC requirements of the application

POSITIONING PARAMETERS

Stepping Modes

One of four possible stepping modes can be programmed:

- Half−stepping
- 1/4 micro−stepping
- 1/8 micro−stepping
- 1/16 micro−stepping

Maximum Velocity

For each stepping mode, the maximum velocity Vmax can be programmed to 16 possible values given in the table below.

The accuracy of Vmax is derived from the internal oscillator. Under special circumstances it is possible to change the V_{max} parameter while a motion is ongoing. All 16 entries for the Vmax parameter are divided into four groups. When changing Vmax during a motion the application must take care that the new Vmax parameter stays within the same group.

Table 7. MAXIMUM VELOCITY SELECTION TABLE

Vmax index		Vmax (full step/s)	Group	Stepping mode			
Hex	Dec			Half−stepping (half−step/s)	1/4th Micro−stepping (micro−step/s)	1/8th Micro−stepping (micro−step/s)	1/16th Micro−stepping (micro−step/s)
0	0	99	A	197	395	790	1579
1	1	136	B	273	546	1091	2182
2	2	167		334	668	1335	2670
3	3	197		395	790	1579	3159
4	4	213		425	851	1701	3403
5	5	228		456	912	1823	3647
6	6	243		486	973	1945	3891
7	7	273	C	546	1091	2182	4364
8	8	303		607	1213	2426	4852
9	9	334		668	1335	2670	5341
A	10	364		729	1457	2914	5829
B	11	395		790	1579	3159	6317
C	12	456		912	1823	3647	7294
D	13	546	D	1091	2182	4364	8728
E	14	729		1457	2914	5829	11658
F	15	973		1945	3891	7782	15564

Minimum Velocity

Once the maximum velocity is chosen, 16 possible values can be programmed for the minimum velocity Vmin. The table below provides the obtainable values in full−step/s. The accuracy of Vmin is derived from the internal oscillator.

Table 8. OBTAINABLE VALUES IN FULL−STEP/S FOR THE MINIMUM VELOCITY

V_{min} Index			Vmax (Full−step/s)															
			A	B						C						D		
Hex	**Dec**	**Vmax Factor**	**99**	**136**	**167**	**197**	**213**	**228**	**243**	**273**	**303**	**334**	**364**	**395**	**456**	**546**	**729**	**973**
0	0	1	99	136	167	197	213	228	243	273	303	334	364	395	456	546	729	973
1	1	1/32	3	4	5	6	6	7	7	8	8	10	10	11	13	15	19	27
2	2	2/32	6	8	10	11	12	13	14	15	17	19	21	23	27	31	42	57
3	3	3/32	9	12	15	18	19	21	22	25	27	31	32	36	42	50	65	88
4	4	4/32	12	16	20	24	26	28	30	32	36	40	44	48	55	65	88	118
5	5	5/32	15	21	26	31	32	35	37	42	46	51	55	61	71	84	111	149
6	6	6/32	18	25	31	36	39	42	45	50	55	61	67	72	84	99	134	179
7	7	7/32	21	30	36	43	46	50	52	59	65	72	78	86	99	118	156	210
8	8	8/32	24	33	41	49	52	56	60	67	74	82	90	97	113	134	179	240
9	9	9/32	28	38	47	55	59	64	68	76	84	93	101	111	128	153	202	271
A	10	10/32	31	42	51	61	66	71	75	84	93	103	113	122	141	168	225	301
B	11	11/32	34	47	57	68	72	78	83	93	103	114	124	135	156	187	248	332
C	12	12/32	37	51	62	73	79	85	91	101	113	124	135	147	170	202	271	362
D	13	13/32	40	55	68	80	86	93	98	111	122	135	147	160	185	221	294	393
E	14	14/32	43	59	72	86	93	99	106	118	132	145	158	172	198	237	317	423
F	15	15/32	46	64	78	93	99	107	113	128	141	156	170	185	214	256	340	454

NOTES: The Vmax factor is an approximation.
In case of motion without acceleration (**AccShape = 1**) the length of the steps = 1/**Vmin.** In case of accelerated motion (**AccShape** = 0) the length of the first step is shorter than 1/**Vmin** depending of **Vmin, Vmax** and **Acc**.

Acceleration and Deceleration

Sixteen possible values can be programmed for Acc (acceleration and deceleration between Vmin and Vmax). The table below provides the obtainable values in full−step/s^2. One observes restrictions for some combinations of acceleration index and maximum speed (gray cells).

The accuracy of Acc is derived from the internal oscillator.

Table 9. ACCELERATION AND DECELERATION SELECTION TABLE

<table>
<tr><th colspan="2">Vmax (FS/s) →</th><th>99</th><th>136</th><th>167</th><th>197</th><th>213</th><th>228</th><th>243</th><th>273</th><th>303</th><th>334</th><th>364</th><th>395</th><th>456</th><th>546</th><th>729</th><th>973</th></tr>
<tr><th colspan="2">↓ Acc Index</th><th colspan="16" rowspan="2">Acceleration (Full−step/s²)</th></tr>
<tr><th>Hex</th><th>Dec</th></tr>
<tr><td>0</td><td>0</td><td colspan="7">49</td><td colspan="6">106</td><td colspan="3">473</td></tr>
<tr><td>1</td><td>1</td><td colspan="13">218</td><td colspan="3">735</td></tr>
<tr><td>2</td><td>2</td><td colspan="16">1004</td></tr>
<tr><td>3</td><td>3</td><td colspan="16">3609</td></tr>
<tr><td>4</td><td>4</td><td colspan="16">6228</td></tr>
<tr><td>5</td><td>5</td><td colspan="16">8848</td></tr>
<tr><td>6</td><td>6</td><td colspan="16">11409</td></tr>
<tr><td>7</td><td>7</td><td colspan="16">13970</td></tr>
<tr><td>8</td><td>8</td><td colspan="16">16531</td></tr>
<tr><td>9</td><td>9</td><td rowspan="7">14785</td><td colspan="15">19092</td></tr>
<tr><td>A</td><td>10</td><td colspan="15">21886</td></tr>
<tr><td>B</td><td>11</td><td colspan="15">24447</td></tr>
<tr><td>C</td><td>12</td><td colspan="15">27008</td></tr>
<tr><td>D</td><td>13</td><td colspan="15">29570</td></tr>
<tr><td>E</td><td>14</td><td colspan="6" rowspan="2">29570</td><td colspan="9">34925</td></tr>
<tr><td>F</td><td>15</td><td colspan="9">40047</td></tr>
</table>

The formula to compute the number of equivalent full−steps during acceleration phase is:

$$\text{Nstep} = \frac{V\max^2 - V\min^2}{2 \times \text{Acc}}$$

Positioning

The position programmed in commands `SetPosition` and `SetPositionShort` is given as a number of (micro−)steps. According to the chosen stepping mode, the position words must be aligned as described in the table below. When using command `SetPositionShort` or `GotoSecurePosition`, data is automatically aligned.

Table 10. POSITION WORD ALIGNMENT

Stepping Mode	Position Word: `Pos[15:0]`																Shift
1/16th	**S**	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	No shift
1/8th	**S**	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	0	1−bit left ⇔ ×2
1/4th	**S**	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	0	0	2−bit left ⇔ ×4
Half−stepping	**S**	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	0	0	0	3−bit left ⇔ ×8
PositionShort	**S**	**S**	**S**	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	0	0	0	No Shift
SecurePosition	**S**	B9	B8	B7	B6	B5	B4	B3	B2	B1	**LSB**	0	0	0	0	0	No shift

NOTES: LSB: Least Significant Bit
S: Sign bit, two’s complement

Position Ranges

A position is coded by using the binary two's complement format. According to the positioning commands used and to the chosen stepping mode, the position range will be as shown in the following table.

Table 11. POSITION RANGE

Command	Stepping Mode	Position Range	Full Range Excursion	Number of Bits
SetPosition	Half−stepping	−4096 to +4095	8192 half−steps	13
	1/4th micro−stepping	−8192 to +8191	16384 micro−steps	14
	1/8th micro−stepping	−16384 to +16383	32768 micro−steps	15
	1/16th micro−stepping	−32768 to +32767	65536 micro−steps	16
SetPositionShort	Half−stepping	−1024 to +1023	2048 half−steps	11

When using the command `SetPosition`, although coded on 16 bits, the position word will have to be shifted to the left by a certain number of bits, according to the stepping mode.

Secure Position

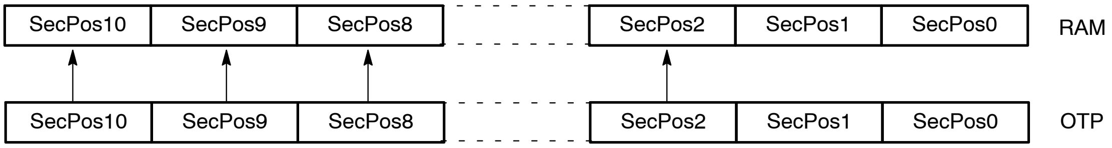
A secure position can be programmed. It is coded in 11−bits, thus having a lower resolution than normal positions, as shown in the following table. See also command `GotoSecurePosition` and LIN lost behavior.

Table 12. SECURE POSITION

Stepping Mode	Secure Position Resolution
Half−stepping	4 half−steps
1/4th micro−stepping	8 micro−steps (1/4th)
1/8th micro−stepping	16 micro−steps (1/8th)
1/16th micro−stepping	32 micro−steps (1/16th)

Important

NOTES: The secure position is disabled in case the programmed value is the reserved code "10000000000" (0x400 or most negative position).
At start up the OTP register is copied in RAM as illustrated below.



Shaft

A shaft bit, which can be programmed in OTP or with command `SetMotorParam`, defines whether a positive motion is a clockwise (CW) or counter−clockwise rotation (CCW) (an outer or an inner motion for linear actuators):

- Shaft = 0 ⇒ MOTXP is used as positive pin of the X coil, while MOTXN is the negative one.
- Shaft = 1 ⇒ opposite situation.

STRUCTURAL DESCRIPTION

See also the Block Diagram in Figure 1.

Stepper Motordriver

The Motor driver receives the control signals from the control logic. The main features are:

- Two H−bridges, designed to drive a stepper motor with two separated coils. Each coil (X and Y) is driven by one H−bridge, and the driver controls the currents flowing through the coils. The rotational position of the rotor, in unloaded condition, is defined by the ratio of current flowing in X and Y. The torque of the stepper motor when unloaded is controlled by the magnitude of the currents in X and Y.
- The control block for the H−bridges, including the PWM control, the synchronous rectification and the internal current sensing circuitry.

- The charge pump to allow driving of the H−bridges' high side transistors.
- Two pre−scale 4−bit DAC's to set the maximum magnitude of the current through X and Y.
- Two DAC's to set the correct current ratio through X and Y.

Battery voltage monitoring is also performed by this block, which provides the required information to the control logic part. The same applies for detection and reporting of an electrical problem that could occur on the coils or the charge pump.

Control Logic (Position Controller and Main Control)

The control logic block stores the information provided by the LIN interface (in a RAM or an OTP memory) and digitally controls the positioning of the stepper motor in terms of speed and acceleration, by feeding the right signals to the motor driver state machine.

It will take into account the successive positioning commands to properly initiate or stop the stepper motor in order to reach the set point in a minimum time.

It also receives feedback from the motor driver part in order to manage possible problems and decide on internal actions and reporting to the LIN interface.

LIN Interface

The LIN interface implements the physical layer and the MAC and LLC layers according to the OSI reference model. It provides and gets information to and from the control logic block, in order to drive the stepper motor, to configure the way this motor must be driven, or to get information such as actual position or diagnosis (temperature, battery voltage, electrical status...) and pass it to the LIN master node.

Miscellaneous

The AMIS−30621 also contains the following:

- An internal oscillator, needed for the LIN protocol handler as well as the control logic and the PWM control of the motor driver.
- An internal trimmed voltage source for precise referencing.
- A protection block featuring a thermal shutdown and a power−on−reset (POR) circuit.
- A 5 V regulator (from the battery supply) to supply the internal logic circuitry.

FUNCTIONS DESCRIPTION

This chapter describes the following functional blocks in more detail:

- Position controller
- Main control and register, OTP memory + ROM
- Motor driver

The LIN controller is discussed in a separate chapter.

Position Controller

Positioning and Motion Control

A positioning command will produce a motion as illustrated in Figure 7. A motion starts with an acceleration phase from minimum velocity (Vmin) to maximum velocity (Vmax) and ends with a symmetrical deceleration. This is defined by the control logic according to the position required by the application and the parameters programmed by the application during the configuration phase. The current in the coils is also programmable.

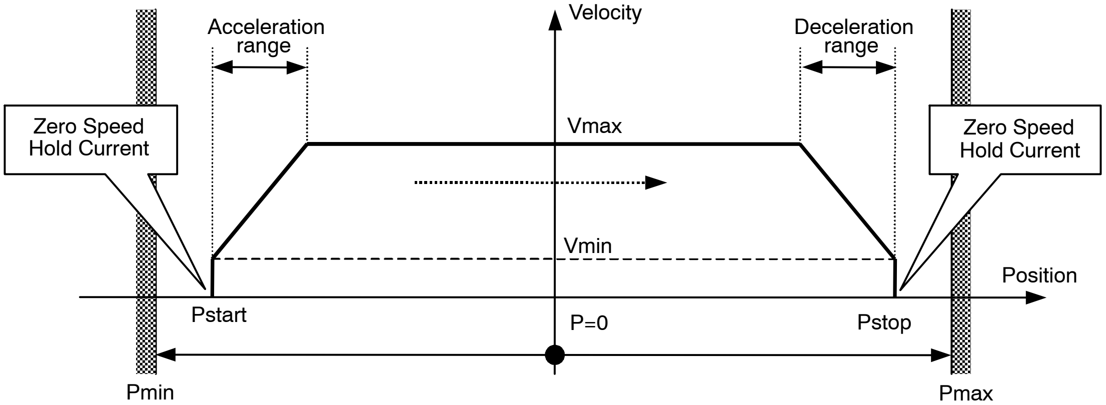


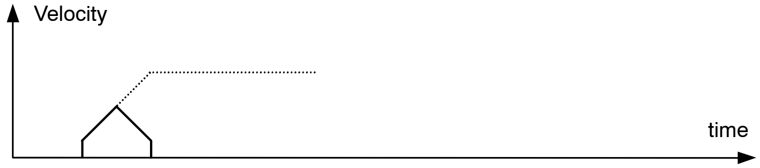
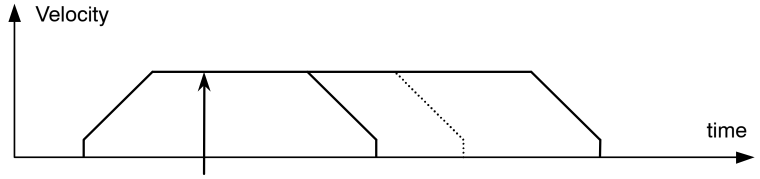
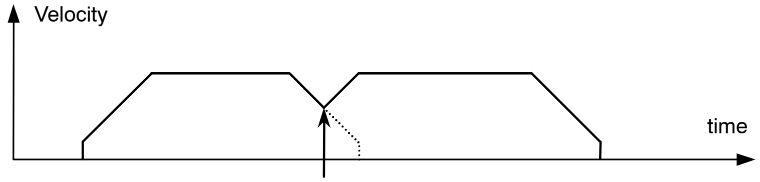
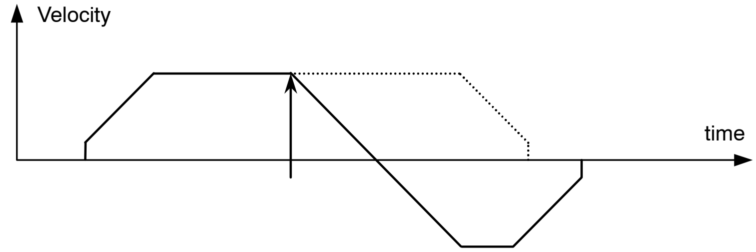
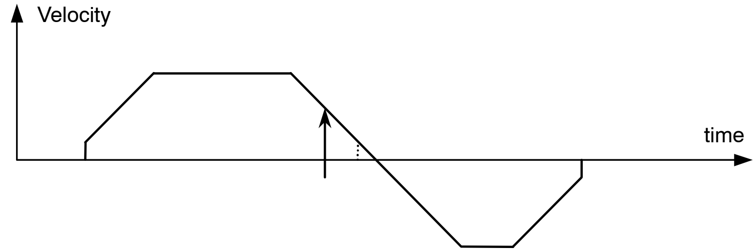
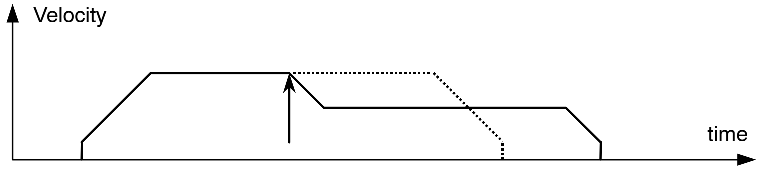
Figure 7. Positioning and Motion Control

Table 13. POSITION RELATED PARAMETERS

Parameter	Reference
Pmax – Pmin	See Positioning
Zero Speed Hold Current	See Ihold
Maximum Current	See Irun
Acceleration and Deceleration	See Acceleration and Deceleration
Vmin	See Minimum Velocity
Vmax	See Maximum Velocity

Different positioning examples are shown in the table below.

Table 14. POSITIONING EXAMPLES

Short motion.	
New positioning command in same direction, shorter or longer, while a motion is running at maximum velocity.	
New positioning command in same direction while in deceleration phase (Note 22) Note: there is no wait time between the deceleration phase and the new acceleration phase.	
New positioning command in reverse direction while motion is running at maximum velocity.	
New positioning command in reverse direction while in deceleration phase.	
New velocity programming while motion is running.	

22. Reaching the end position is always guaranteed, however velocity rounding errors might occur after consecutive accelerations during a deceleration phase. The velocity rounding error will be removed at Vmin (e.g. at end of acceleration or when AccShape=1).

Dual Positioning

A SetDualPosition command allows the user to perform a positioning using two different velocities. The first motion is done with the specified `Vmin` and `Vmax` velocities in the SetDualPosition command, with the acceleration (deceleration) parameter already in RAM, to a position `Pos1[15:0]` also specified in SetDualPosition.

Then a second motion to a position `Pos2[15:0]` is done at the specified `Vmin` velocity in the SetDualPosition command (no acceleration). Once the second motion is achieved, the `ActPos` register is reset to zero, whereas `TagPos` register is not changed.

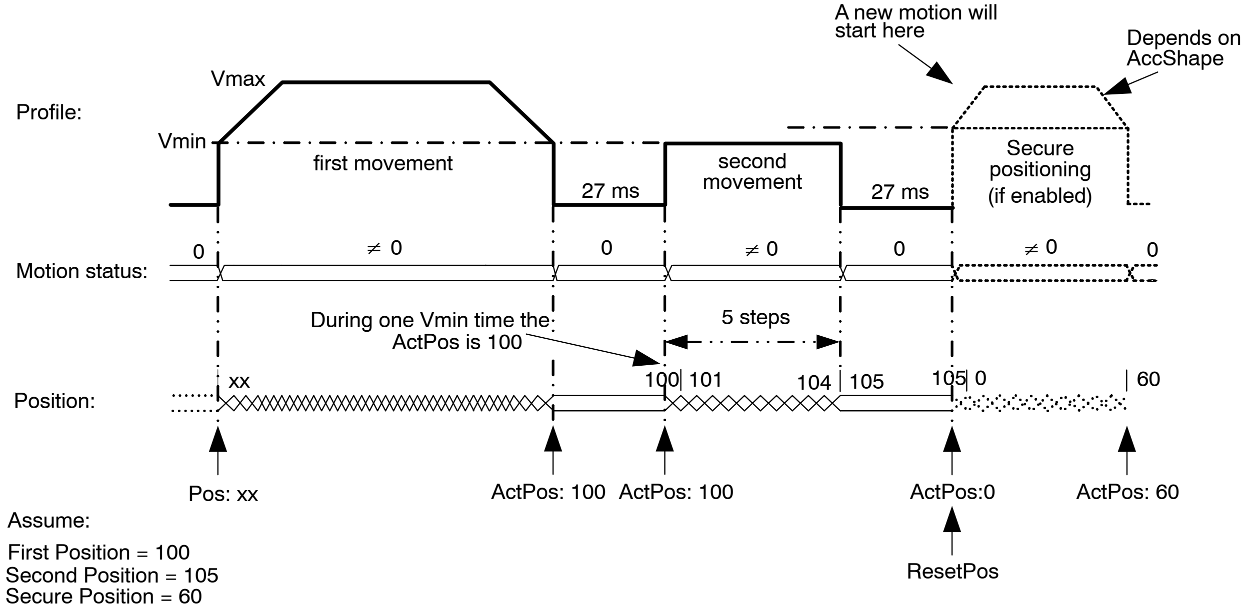


Figure 8. Dual Positioning

Remark: This operation cannot be interrupted or influenced by any further command unless the occurrence of the conditions driving to a motor shutdown or by a HardStop command. Sending a SetDualPosition command while a motion is already ongoing is not recommended. After dual positioning is executed the internal flag “Reference done” is set.

1. The **priority encoder** is describing the management of states and commands.
2. If a SetPosition(Short) command issued during a DualPosition sequence, it will be kept in position buffer memory and executed afterwards. This applies also for the commands sleep, SetMotorParam and GotoSecurePosition.
3. Commands such as GetActualPos or GetStatus will be executed while a dual positioning is running. This applies also for a dynamic **ID assignment** LIN frame.
4. A DualPosition sequence starts by setting TagPos buffer register to SecPos value, provided secure position is enabled otherwise TagPos is reset to zero.
5. The acceleration/deceleration value applied during a DualPosition sequence is the one stored in RAM before the SetDualPosition command is sent. The same applies for shaft bit, but not for Irun, Ihold and StepMode, which can be changed during the dual positioning sequence.
6. The Pos1, Pos2, Vmax and Vmin values programmed in a SetDualPosition command apply only for this sequence. All further positioning will use the parameters stored in RAM (programmed for instance by a former SetMotorParam command).
7. Commands ResetPosition, SetDualPosition and SoftStop will be ignored while a DualPosition sequence is ongoing, and will not be executed afterwards.
8. A SetMotorParam command should not be sent during a SetDualPosition sequence.
9. If for some reason ActPos equals Pos1[15:0] at the moment the SetDualPosition command is issued, the circuit will enter in deadlock state. Therefore, the application should check the actual position by a GetPosition or a GetFullStatus command prior to send the SetDualPosition command.

Position Periodicity

Depending on the stepping mode the position can range from –4096 to +4095 in half−step to –32768 to +32767 in 1/16th micro−stepping mode. One can project all these positions lying on a circle. When executing the command `SetPosition`, the position controller will set the movement direction in such a way that the traveled distance is minimal.

The figure below illustrates that the moving direction going from `ActPos` = +30000 to `TagPos` = –30000 is clockwise.

If a counter clockwise motion is required in this example, several consecutive `SetPosition` commands can be used.

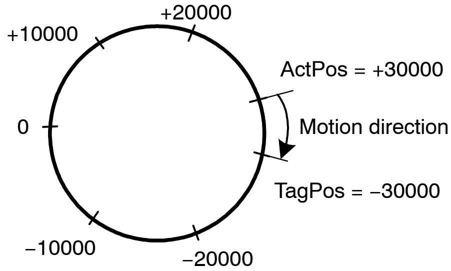


Figure 9. Motion Direction is Function of Difference between ActPos and TagPos

Hardwired Address HW2

In the drawing below, a simplified schematic diagram is shown of the HW2 comparator circuit.

The HW2 pin is sensed via 2 switches. The DriveHS and DriveLS control lines are alternatively closing the top and bottom switch connecting HW2 pin with a current to resistor converter. Closing S_{TOP} (DriveHS = 1) will sense a current to GND. In that case the top I→ R converter output is low, via the closed passing switch S_{PASS_T} this signal is fed to the “R” comparator which output HW2_Cmp is high. Closing bottom switch S_{BOT} (DriveLS = 1) will sense a current to VBAT. The corresponding I→ R converter output is low and via S_{PASS_B} fed to the comparator. The output HW2_Cmp will be high.

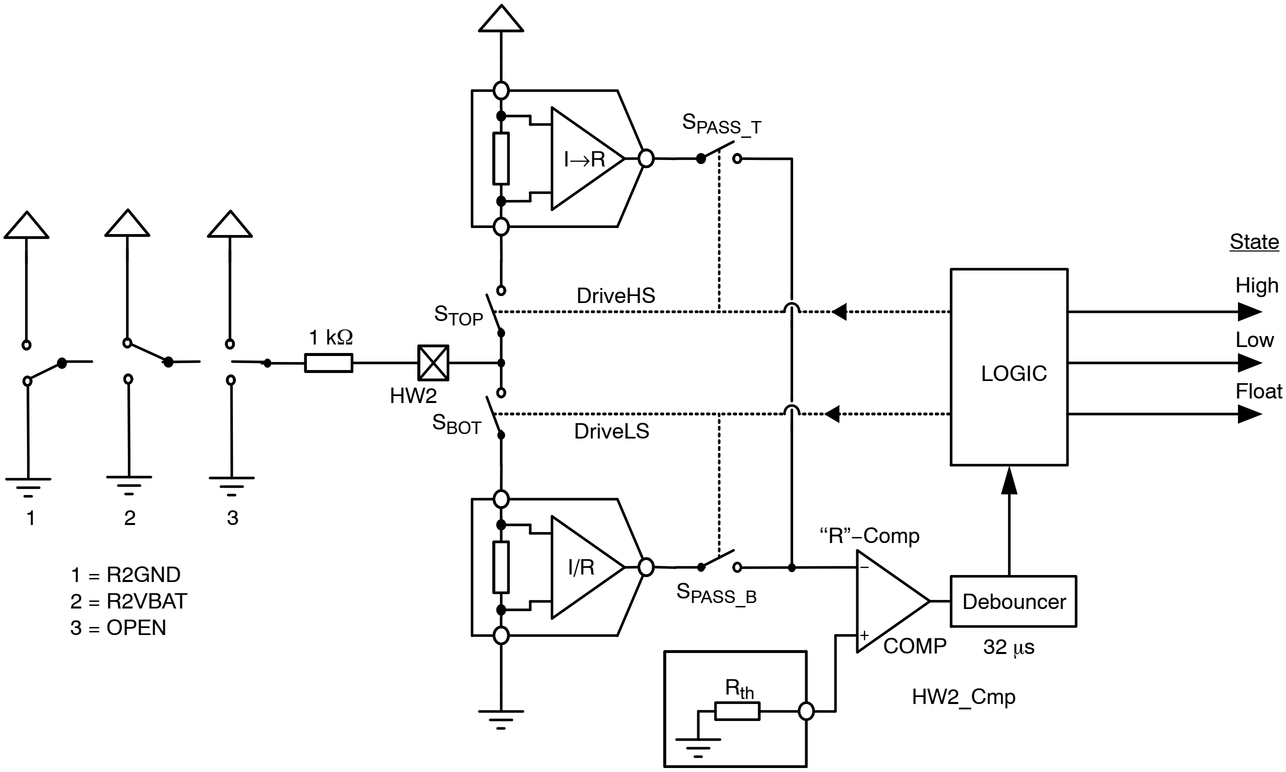


Figure 10. Simplified Schematic Diagram of the HW2 Comparator

3 cases can be distinguished (see also Figure 10 above):

- HW2 is connected to ground: R2GND or drawing 1
- HW2 is connected to VBAT: R2VBAT or drawing 2
- HW2 is floating: OPEN or drawing 3

Table 15. STATE DIAGRAM OF THE HW2 COMPARATOR

Previous State	DriveLS	DriveHS	HW2_Cmp	New State	Condition	Drawing
Float	1	0	0	Float	R2GND or OPEN	1 or 3
Float	1	0	1	High	R2VBAT	2
Float	0	1	0	Float	R2VBAT or OPEN	2 or 3
Float	0	1	1	Low	R2GND	1
Low	1	0	0	Low	R2GND or OPEN	1 or 3
Low	1	0	1	High	R2VBAT	2
Low	0	1	0	Float	R2VBAT or OPEN	2 or 3
Low	0	1	1	Low	R2GND	1
High	1	0	0	Float	R2GND or OPEN	1 or 3
High	1	0	1	High	R2VBAT	2
High	0	1	0	High	R2VBAT or OPEN	2 or 3
High	0	1	1	Low	R2GND	1

The logic is controlling the correct sequence in closing the switches and in interpreting the 32 μs debounced HW2_Cmp output accordingly. The output of this small state−machine is corresponding to:

- High or address = 1
- Low or address = 0
- Floating

As illustrated in the table above (Table 15), the state is depending on the previous state, the condition of the 2 switch controls (DriveLS and DriveHS) and the output of HW2_Cmp. The figure below is showing an example of a practical case where a connection to VBAT is interrupted.

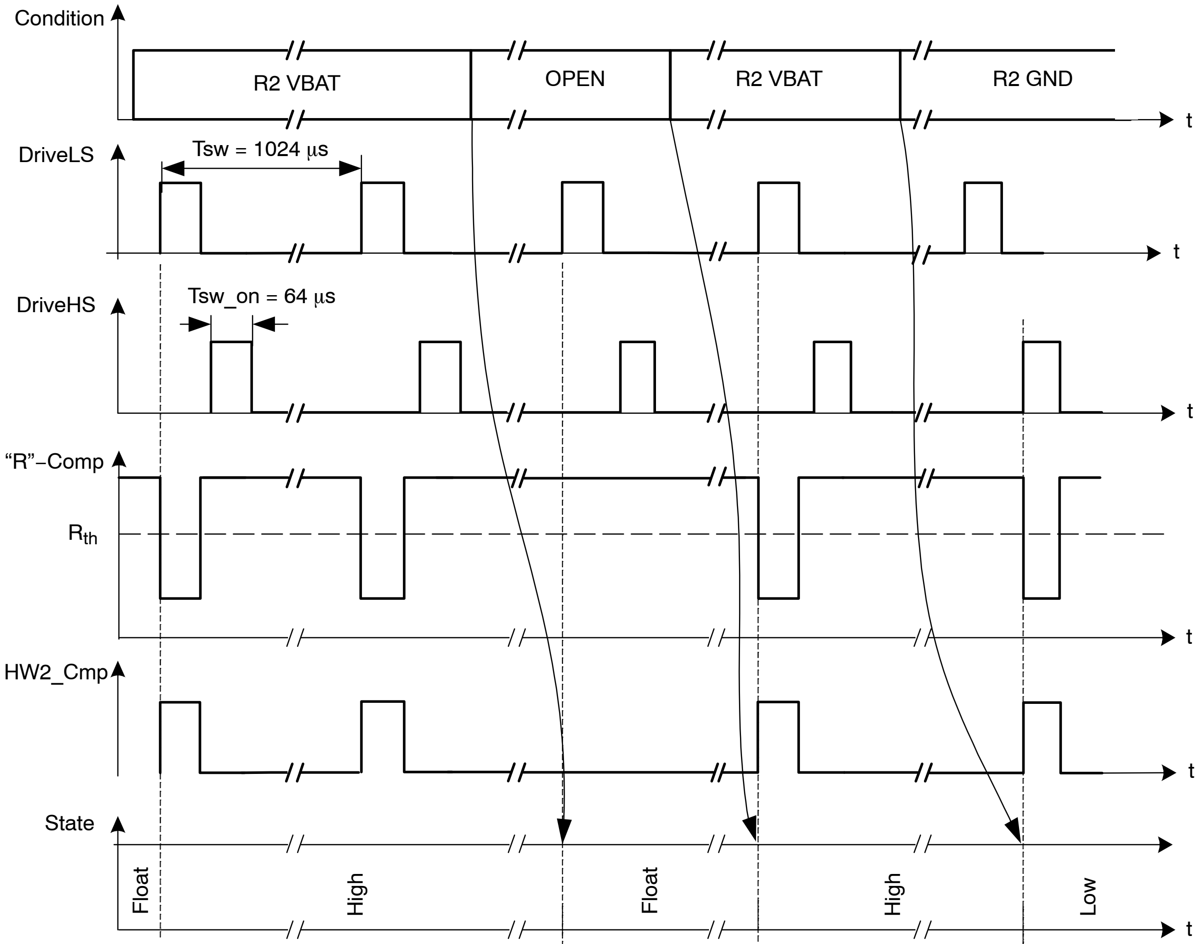


Figure 11. Timing Diagram Showing the Change in States for HW2 Comparator

R2VBAT

A resistor is connected between VBAT and HW2. Every 1024 μs S_{BOT} is closed and a current is sensed. The output of the I → R converter is low and the HW2_Cmp output is high. Assuming the previous state was floating, the internal logic will interpret this as a change of state and the new state will be high (see also Table 15). The next time S_{BOT} is closed the same conditions are observed. The previous state was high, so based on Table 15 the new state remains unchanged. This high state will be interpreted as HW2 address = 1.

OPEN

In case the HW2 connection is lost (broken wire, bad contact in connector) the next time S_{BOT} is closed, this will be sensed. There will be no current, the output of the corresponding I → R converter is high and the HW2_Cmp will be low. The previous state was high. Based on Table 15 one can see that the state changes to float. This will trigger a motion to secure position.

R2GND

If a resistor is connected between HW2 and the GND, a current is sensed every 1024 μs when S_{TOP} is closed. The output of the top I → R converter is low and as a result the HW2_Cmp output switches to high. Again based on the stated diagram in Table 15 one can see that the state will change to Low. This low state will be interpreted as HW2 address = 0.

External Switch SWI

As illustrated in Figure 12 the SWI comparator is almost identical to HW2. The major difference is in the limited number of states. Only open or closed is recognised leading to respectively ESW = 0 and ESW = 1.

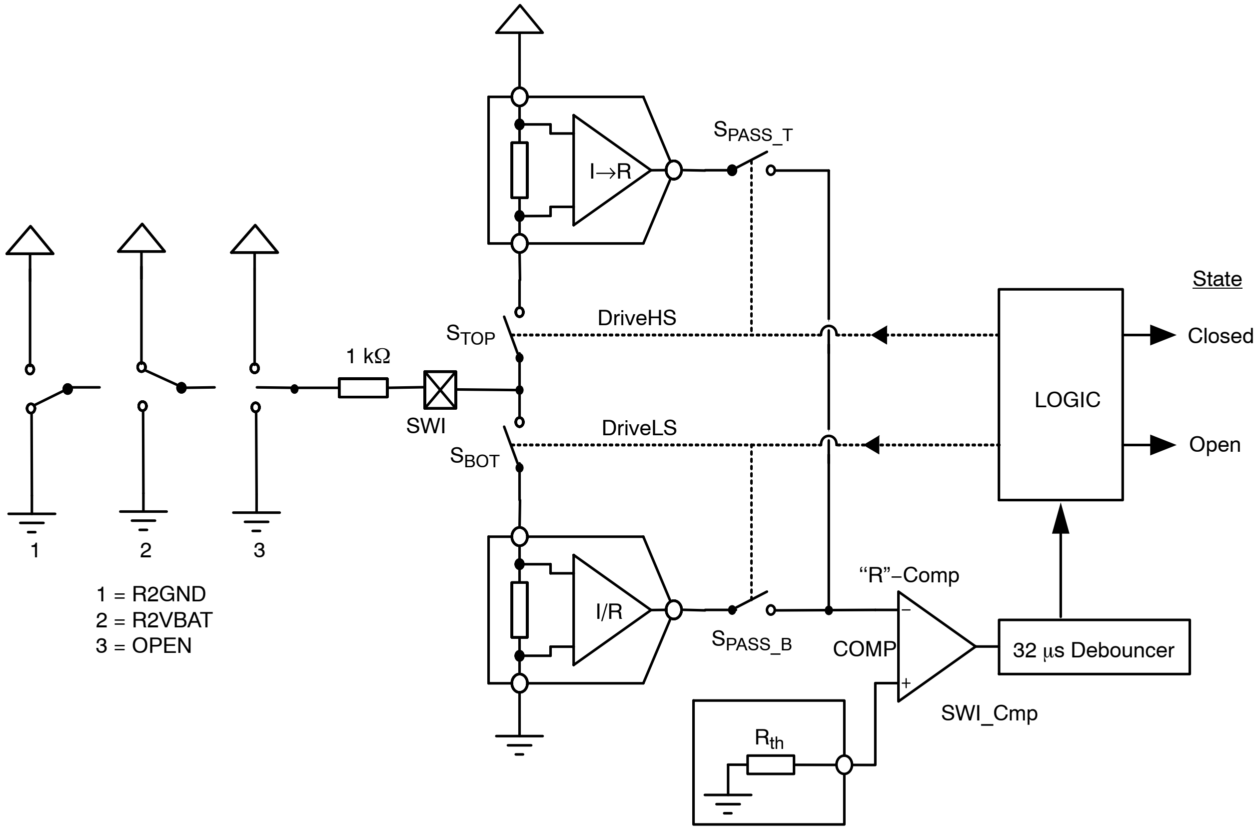


Figure 12. Simplified Schematic Diagram of the SWI Comparator

As illustrated in the drawing above, a change in state is always synchronized with DriveHS or DriveLS. The same synchronization is valid for updating the internal position register. This means that after every current pulse (or closing of S_{TOP} or S_{BOT}) the state of the position switch together with the corresponding position is memorized.

The GetActualPos command reads back the `<ActPos>` register and the status of ESW. In this way the master node may get synchronous information about the state of the switch together with the position of the motor. See Table 16 below.

Table 16. GetActualPos LIN COMMAND

Reading Frame									
		Structure							
Byte	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Identifier	*	*	1	0	ID3	ID2	ID1	ID0
1	Data 1	ESW	AD[6:0]						
2	Data 2	ActPos[15:8]							
3	Data 3	ActPos[7:0]							
4	Data 4	VddReset	StepLoss	ElDef	UV2	TSD	TW	Tinfo[1:0]	
5	Checksum	Checksum over data							

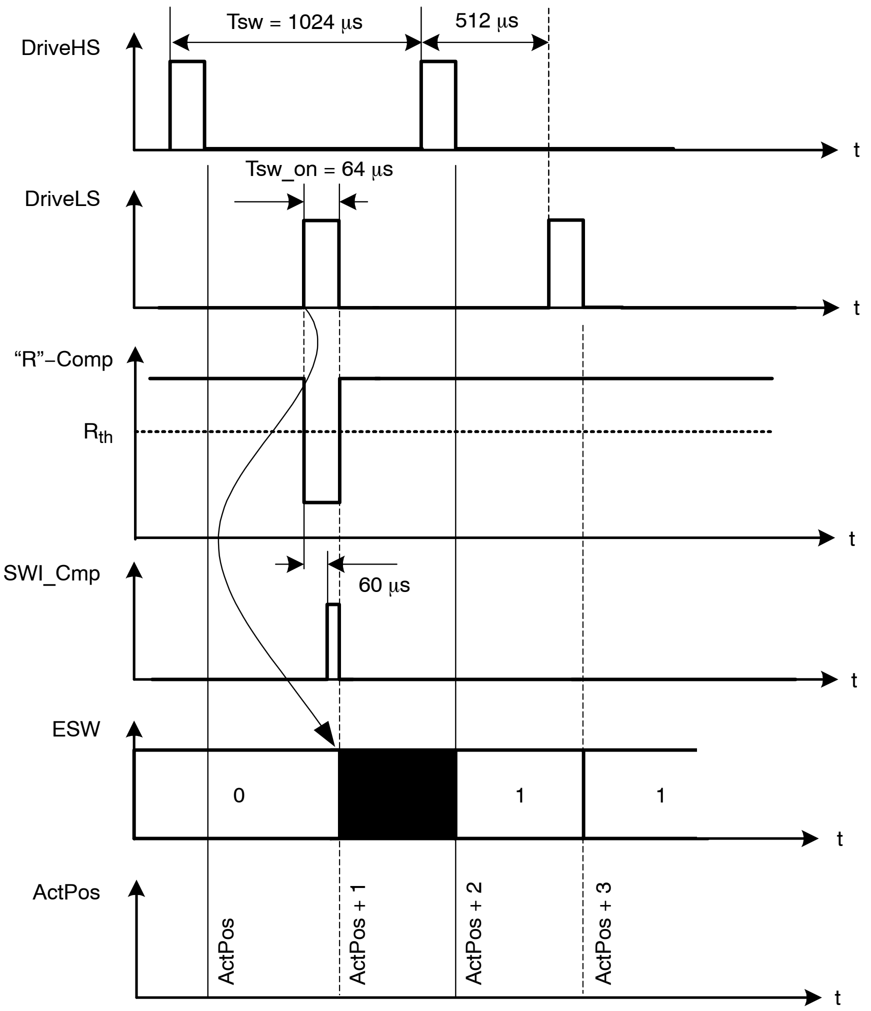


Figure 13. Simplified Timing Diagram Showing the Change in States for SWI Comparator

Main Control and Register, OTP memory + ROM

Power−up Phase

Power up phase of the AMIS−30621 will not exceed 10ms. After this phase, the AMIS−30621 is in standby mode, ready to receive LIN messages and execute the associated commands. After power−up, the registers and flags are in the reset state, while some of them are being loaded with the OTP memory content (see Table 19).

Reset

After power−up, or after a reset occurrence (e.g. a micro−cut on pin V_{BB} has made V_{DD} to go below $V_{DDReset}$ level), the H−bridges will be in high−impedance mode, and the registers and flags will have a predetermined value. This is documented in Tables 19 and 20.

Soft Stop

A soft stop is an immediate interruption of a motion, but with a deceleration phase. At the end of this action, the register `<TagPos>` is loaded with the value contained in register `<ActPos>`, see Table 19). The circuit is then ready to execute a new positioning command, provided thermal and electrical conditions allow for it.

Sleep Mode

When entering sleep mode, the stepper−motor can be driven to its secure position. After which, the circuit is completely powered down, apart from the LIN receiver, which remains active to detect a dominant state on the bus. In case sleep mode is entered while a motion is ongoing, a transition will occur towards secure position as described in Positioning and Motion Control provided `<SecPos>` is enabled. Otherwise, `<SoftStop>` is performed.

Sleep mode can be entered in the following cases:

- The circuit receives a LIN frame with identifier **0x3C** and first data byte containing **0x00**, as required by LIN specification rev 1.3. See also Sleep in the LIN Application Command section.
- In case the LIN bus is and remains inactive (or is lost) during more than 25000 time slots (1.30 s at 19.2 kbit/s), a time−out signal switches the circuit to sleep mode.

The circuit will return to normal mode if a valid LIN frame is received (this valid frame can be addressed to another slave).

Thermal Shutdown Mode

When thermal shutdown occurs, the circuit performs a `<SoftStop>` command and goes to motor shutdown mode (see Figure 14).

Temperature Management

The AMIS−30621 monitors temperature by means of two thresholds and one shutdown level, as illustrated in the state diagram and illustration of Figure 14 below. The only condition to reset flags `<TW>` and `<TSD>` (respectively thermal warning and thermal shutdown) is to be at a temperature lower than T_{tw} and to get the occurrence of a `GetStatus` or a `GetFullStatus` LIN frame.

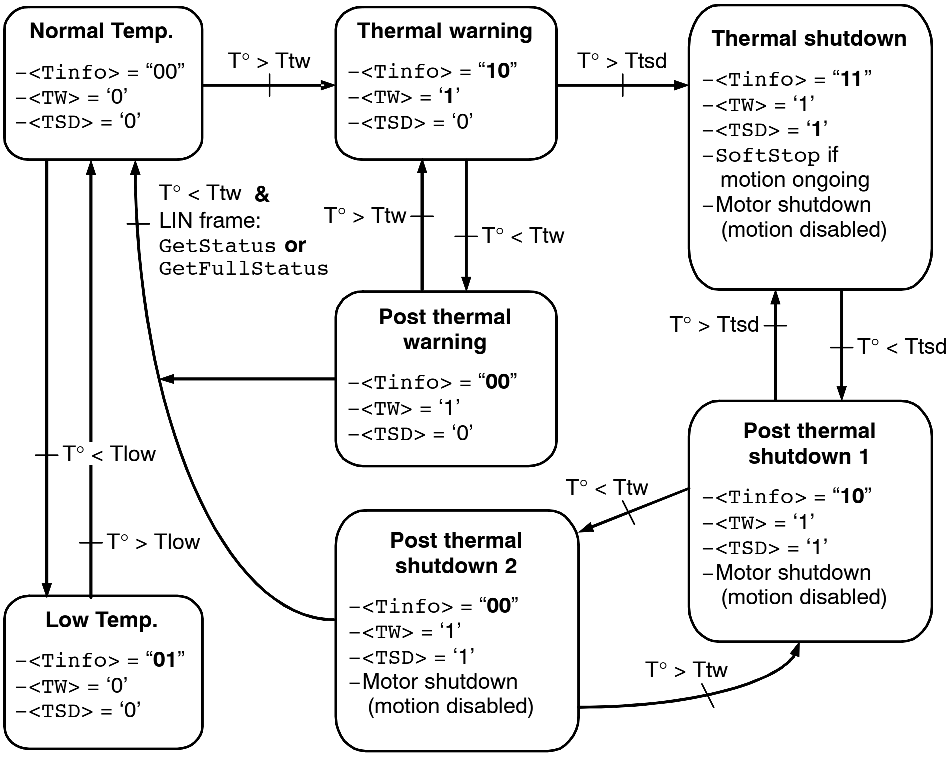


Figure 14. State Diagram Temperature Management

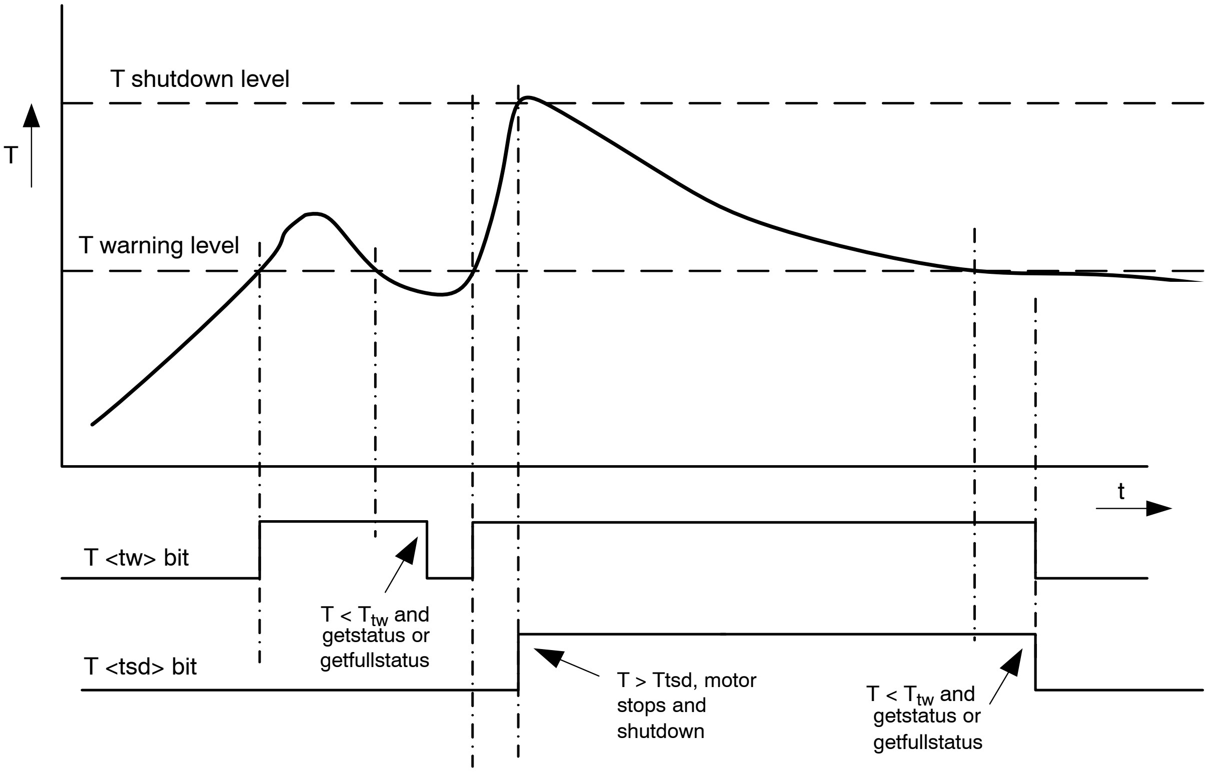


Figure 15. Illustration of Thermal Management Situation

Battery Voltage Management

The AMIS−30621 monitors the battery voltage by means of one threshold and one shutdown level. The only condition to reset flags `<UV2>` and `<StepLoss>` is to recover by a battery voltage higher than UV1 and to receive a `GetStatus` or a `GetFullStatus` command.

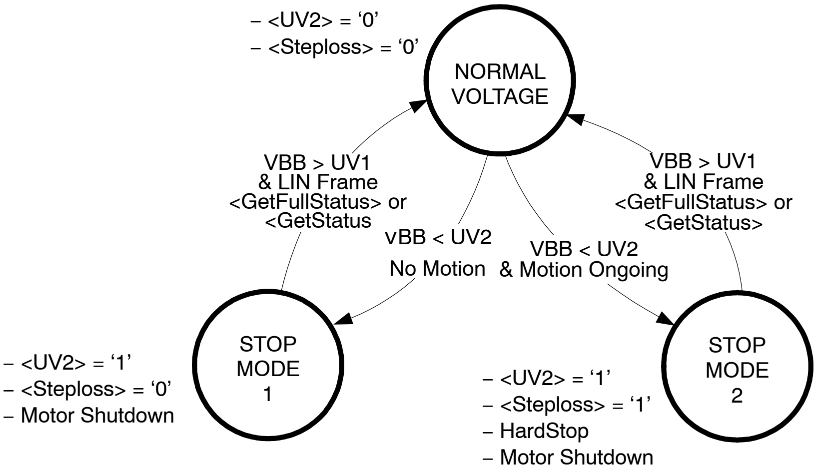


Figure 16. State Diagram Battery Voltage Management

In **Stop mode 1** the motor is put in shutdown state. The `<UV2>` **flag** is set. In case V_{BB} > UV1, AMIS−30621 accepts updates of the target position by means of the reception of `SetPosition`, `SetPositionShort` and `GotoSecurePosition` commands, only AFTER the `<UV2>` flag is cleared by receiving a `GetStatus` or `GetFullStatus` command.

In **Stop mode 2** the motor is stopped immediately and put in shutdown state. The `<UV2>` and `<Steploss>` **flags** are set. In case V_{BB} > UV1, AMIS−30621 accepts updates of the target position by means of the reception of `SetPosition`, `SetPositionShort` and `GotoSecurePosition` commands, only AFTER the `<UV2>` and `<Steploss>` flags are cleared by receiving a `GetStatus` or `GetFullStatus` command.

Important Notes:

- In the case of Stop mode 2, care needs to be taken because the accumulated steploss can cause a significant deviation between physical and stored actual position.
- The `SetDualPosition` command will only be executed after clearing the `<UV2>` and `<Steploss>` flags.
- RAM reset occurs when V_{DD} < V_{DD}Reset (digital POR level).

OTP Register

OTP Memory Structure

The table below shows how the parameters to be stored in the OTP memory are located.

Table 17. OTP MEMORY STRUCTURE

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	OSC3	OSC2	OSC1	OSC0	IREF3	IREF2	IREF1	IREF0
0x01	1	TSD2	TSD1	TSD0	BG3	BG2	BG1	BG0
0x02	ADM	(HW2) (Note 23)	(HW1) (Note 23)	(HW0) (Note 23)	PA3	PA2	PA1	PA0
0x03	Irun3	Irun2	Irun1	Irun0	Ihold3	Ihold2	Ihold1	Ihold0 (Note 24)
0x04	Vmax3	Vmax2	Vmax1	Vmax0	Vmin3	Vmin2	Vmin1	Vmin0
0x05	SecPos10	SecPos9	SecPos8	Shaft	Acc3	Acc2	Acc1	Acc0
0x06	SecPos7	SecPos6	SecPos5	SecPos4	SecPos3	SecPos2	SecPos1	SecPos0
0x07					StepMode1	StepMode0	LOCKBT	LOCKBG

23. Although not stored in the OTP memory the physical status of the hardware address input pins are returned by a read of the OTP contents (`GetOTPparam`).
24. Note for product version AMIS30621C6217G and AMIS30621C6217RG the Ihold0 bit is programmed to ’1’.

Parameters stored at address 0x00 and 0x01 and bit `<LOCKBT>` are already programmed in the OTP memory at circuit delivery. They correspond to the calibration of the circuit and are just documented here as an indication.

Each OTP bit is at ‘0’ when not zapped. Zapping a bit will set it to ‘1’. Thus only bits having to be at ‘1’ must be zapped. Zapping of a bit already at ‘1’ is disabled. Each OTP byte will be programmed separately (see command `SetOTPparam`). Once OTP programming is completed, bit `<LOCKBG>` can be zapped to disable future zapping, otherwise any OTP bit at ‘0’ could still be zapped by using a `SetOTPparam` command.

Table 18. OTP OVERWRITE PROTECTION

Lock Bit	Protected Bytes
LOCKBT (factory zapped before delivery)	0x00 to 0x01
LOCKBG	0x00 to 0x07

The command used to load the application parameters via the LIN bus in the RAM prior to an OTP Memory programming is `SetMotorParam`. This allows for a functional verification before using a `SetOTPparam` command to program and zap separately one OTP memory byte. A `GetOTPparam` command issued after each `SetOTPparam` command allows verifying the correct byte zapping.

Note: zapped bits will really be “active” after a `GetOTPparam` or a `ResetToDefault` command or after a power−up.

Application Parameters Stored in OTP Memory

Except for the physical address `<PA[3:0]>` these parameters, although programmed in a non−volatile memory can still be overridden in RAM by a LIN writing operation.

PA[3:0] In combination with HW[2:0] and ADM bit, it forms the physical address AD[6:0] of the stepper−motor. Up to 128 stepper−motors can theoretically be connected to the same LIN bus.

ADM Addressing mode bit enabling to swap the combination of OTP memory bits PA[3:0] with hardwired address bits HW[2:0] to form the physical address AD[6:0] of the stepper motor.

Irun[3:0] Current amplitude value to be fed to each coil of the stepper−motor. The table below provides the 16 possible values for `<IRUN>`.

Index	Irun				Run Current (mA)
0	0	0	0	0	59
1	0	0	0	1	71
2	0	0	1	0	84
3	0	0	1	1	100
4	0	1	0	0	119
5	0	1	0	1	141
6	0	1	1	0	168
7	0	1	1	1	200
8	1	0	0	0	238
9	1	0	0	1	283
A	1	0	1	0	336
B	1	0	1	1	400
C	1	1	0	0	476
D	1	1	0	1	566
E	1	1	1	0	673
F	1	1	1	1	800

Ihold[3:0] Hold current for each coil of the stepper−motor. The table below provides the 16 possible values for `<IHOLD>`.

Index	Ihold				Hold Current (mA)
0	0	0	0	0	59
1	0	0	0	1	71
2	0	0	1	0	84
3	0	0	1	1	100
4	0	1	0	0	119
5	0	1	0	1	141
6	0	1	1	0	168
7	0	1	1	1	200
8	1	0	0	0	238
9	1	0	0	1	283
A	1	0	1	0	336
B	1	0	1	1	400
C	1	1	0	0	476
D	1	1	0	1	566
E	1	1	1	0	673
F	1	1	1	1	800

Note: When the motor is stopped, the current is reduced from `<IRUN>` to `<IHOLD>`.

StepMode Setting of step modes.

Step Mode		Step Mode
0	0	1/2 stepping
0	1	1/4 stepping
1	0	1/8 stepping
1	1	1/16 stepping

Shaft This bit distinguishes between a clock−wise or counter−clock−wise rotation.