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AMIS-49587

Power Line Carrier Modem

ON Semiconductor's AMIS−49587 is an IEC 61334−5−1 compliant power line carrier modem using spread−FSK (S−FSK) modulation for robust low data rate communication over power lines. AMIS−49587 is built around an ARM 7TDMI processor core, and includes the MAC layer. With this robust modulation technique, signals on the power lines can pass long distances. The half−duplex operation is automatically synchronized to the mains, and can be up to 2400 bits/sec.

The product configuration is done via its serial interface, which allows the user to concentrate on the development of the application.

The AMIS−49587 is implemented in ON Semiconductor mixed signal technology, combining both analog circuitry and digital functionality on the same IC.

Features

- Power Line Carrier Modem for 50 and 60 Hz Mains
- Fully compliant to IEC 61334−5−1 and CENELEC EN 50065−1
- Complete Handling of Protocol Layers Physical to MAC
- Programmable Carrier Frequencies from 9 to 95 kHz in 10 Hz Steps
- Half Duplex
- Data Rate Selectable: 300 – 600 – 1200 – 2400 baud (@ 50 Hz)
  360 – 720 – 1440 – 2880 baud (@ 60 Hz)
- Synchronization on Mains
- Repetition Algorithm Boost the Robustness of Communication
- SCI Port to Application Microcontroller
- SCI Baudrate Selectable: 4.8 – 9.6 – 19.2 – 34.4 kb
- Power Supply 3.3 V
- Ambient Temperature Range: −40°C to +85°C
- These Devices are Pb−Free and are RoHS Compliant*

Typical Applications

- ARM: Automated Remote Meter Reading (Télérelevé)
- Remote Security Control
- Streetlight Control
- Transmission of Alerts (Fire, Gas Leak, Water Leak)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

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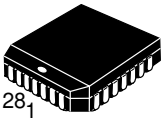
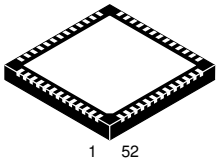
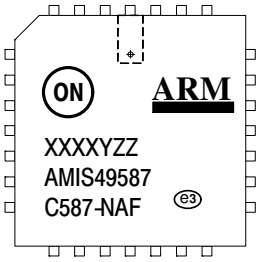


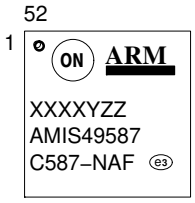
PLCC 28 Lead
CASE 776AA



QFN52 8x8, 0.5P
CASE 485M

MARKING DIAGRAMS





XXXX = Date Code
Y = Plant Identifier
ZZ = Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

1 APPLICATION

1.1 APPLICATION EXAMPLE

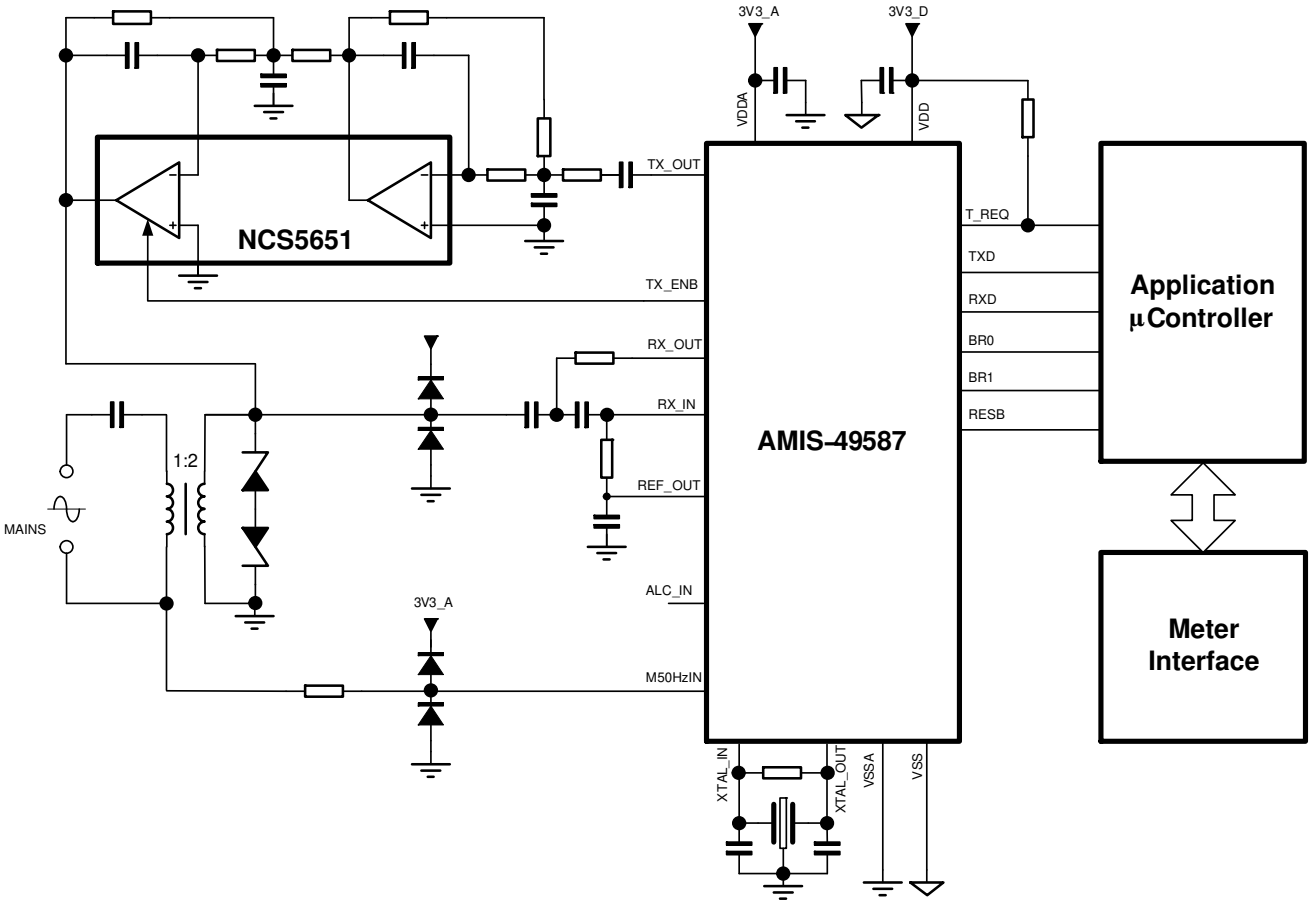


Figure 1. Typical Application for the AMIS−49587 S−FSK Modem

Table 1. ORDERING INFORMATION

Part No.	Temperature Range	Package	Shipping†
AMIS49587C5871G	−40°C – +85°C	PLCC−28 (Pb−Free)	Tube
AMIS49587C5871RG	−40°C – +85°C	PLCC−28 (Pb−Free)	Tape & Reel
AMIS49587C5872G	−40°C – +85°C	QFN−52 (Pb−Free)	Tube
AMIS49587C5872RG	−40°C – +85°C	QFN−52 (Pb−Free)	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table of Contents

2 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed in this clause may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

2.1.1 Power Supply Pins VDD, VDDA, VSS, VSSA

Table 2. ABSOLUTE MAXIMUM RATINGS SUPPLY

Rating	Symbol	Min	Max	Unit
Absolute maximum digital power supply	V_{DD_ABSM}	V_{SS}−0.3	3.9	V
Absolute maximum analog power supply	V_{DDA_ABSM}	V_{SSA}−0.3	3.9	V
Absolute maximum difference between digital and analog power supply	$V_{DD}-V_{DDA\_ABSM}$	−0.3	0.3	V
Absolute maximum difference between digital and analog ground	$V_{SS}-V_{SSA\_ABSM}$	−0.3	0.3	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2.1.2 Non 5V Safe Pins: TX_OUT, ALC_IN, RX_IN, RX_OUT, REF_OUT, M50HZ_IN, XIN, XOUT, TDO, TDI, TCK, TMS, TRSTB, TEST

Table 3. ABSOLUTE MAXIMUM RATINGS NON 5V SAFE PINS

Rating	Symbol	Min	Max	Unit
Absolute maximum input for normal digital inputs and analog inputs	V_{IN_ABSM}	V_{SS*}−0.3	V_{DD*}+0.3	V
Absolute maximum voltage at any output pin	V_{OUT_ABSM}	V_{SS*}−0.3	V_{DD*}+0.3	V

2.1.3 5V Safe Pins: TX_ENB, TXD, RXD, BR0, BR1, RESB, RX_DATA, TREQ, CRC, TX_DATA/PRE_SLOT

Table 4. ABSOLUTE MAXIMUM RATINGS 5V SAFE PINS

Rating	Symbol	Min	Max	Unit
Absolute maximum input for digital 5 V safe inputs	V_{5VS_ABSM}	V_{SS}−0.3	6.0	V
Absolute maximum voltage at 5 V safe output pin	V_{OUT5V_ABSM}	V_{SS}−0.3	3.9	V

2.2 Normal Operating Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device as described in the Receiver Block Diagram Section and for the reliability specifications as listed in the Local Transfer and Configuration Commands (LTC) Section. Functionality outside these limits is not implied.

Total cumulative dwell time outside the normal power supply voltage range or the ambient temperature under bias, must be less than 0.1% of the useful life as defined in the Local Transfer and Configuration Commands (LTC) Section.

Table 5. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Power Supply Voltage Range	V_{DD}	3.0	3.6	V
Ambient Temperature	T_A	–25	85	°C

3 PIN DESCRIPTION

3.1 PLCC Packaging

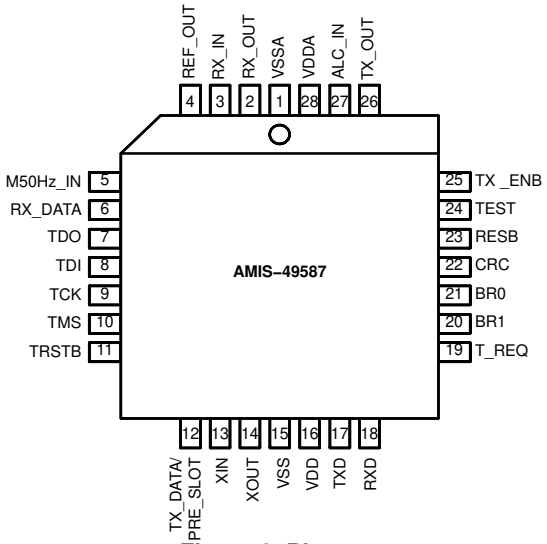


Figure 2. Pinout

Table 6. AMIS−49587 PLCC PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	I/O	Type	Description
1	VSSA		P	Analog ground
2	RX_OUT	Out	A	Output of receiver low noise operational amplifier
3	RX_IN	In	A	Positive input of receiver low noise operational amplifier
4	REF_OUT	Out	A	Reference output for stabilization
5	M50HZ_IN	In	A	50/60 Hz input for mains zero cross detection
6	RX_DATA	Out	D, 5V Safe	Data reception indication (open drain output)
7	TDO	Out	D	Test data output
8	TDI	In	D	Test data input (internal pulldown)
9	TCK	In	D	Test clock (internal pulldown)
10	TMS	In	D	Test mode select (internal pulldown)
11	TRSTB	In	D	Test reset bar (internal pulldown, active low)
12	TX_DATA/ PRE_SLOT	Out	D, 5V Safe	Data output corresponding to transmitted data or PRE_SLOT signal (open drain output)
13	XIN	In	A	Xtal input (can be driven by an internal clock)
14	XOUT	Out	A	Xtal output (output floating when XIN driven by external clock)
15	VSS		P	Digital ground
16	VDD		P	3.3 V digital supply
17	TXD	Out	D, 5V Safe	SCI transmit output (open drain)
18	RXD	In	D, 5V Safe	SCI receive input (Schmitt trigger input)
19	T_REQ	In	D, 5V Safe	Transmit request input
20	BR1	In	D, 5V Safe	SCI baud rate selection
21	BR0	In	D, 5V Safe	SCI baud rate selection
22	CRC	Out	D, 5V Safe	Correct frame CRC indication (open drain output)
23	RESB	In	D, 5V Safe	Master reset bar (Schmitt trigger input, active low)
24	TEST	In	D	Test enable (internal pulldown)
25	TX_ENB	Out	D, 5V Safe	TX enable bar (open drain)
26	TX_OUT	Out	A	Transmitter output
27	ALC_IN	In	A	Automatic level control input
28	VDDA		P	3.3 V analog supply

P: Power pin
A: Analog pin
D: Digital pin

5V Safe: IO that support the presence of 5V on bus line
Out: Output signal
In: Input signal
In/Out: Bi−directional pin

3.2 QFN Packaging

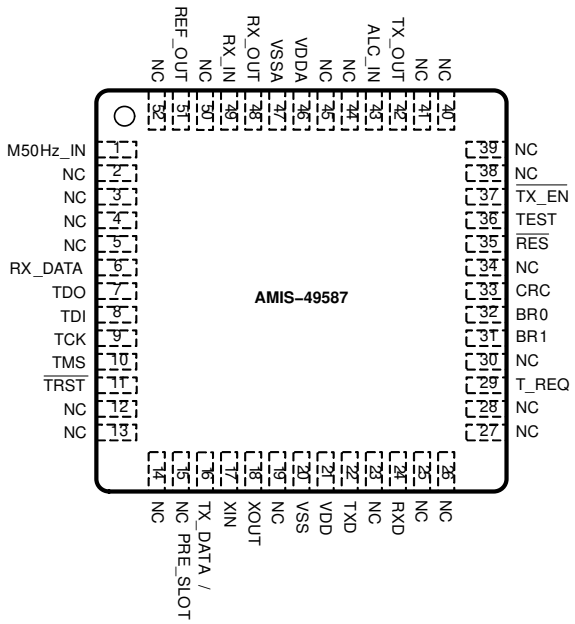


Figure 3. QFN Pin−out of AMIS−49587 (Top view)

Table 7. AMIS−49587 QFN PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	I/O	Type	Description
1	M50HZ_IN	In	A	50/60Hz input for mains zero cross detection
6	RX_DATA	Out	D, 5V Safe	Data reception indication (open drain output)
7	TDO	Out	D	Test data output
8	TDI	In	D	Test data input (internal pull down)
9	TCK	In	D	Test clock (internal pull down)
10	TMS	In	D	Test mode select (internal pull down)
11	TRSTB	In	D	Test reset bar (internal pull down, active low)
16	TX_DATA/PRE_SLOT	Out	D, 5V Safe	Data output corresponding to transmitted data or PRE_SLOT signal (open drain)
17	XIN	In	A	Xtal input (can be driven by an internal clock)
18	XOUT	Out	A	Xtal output (output floating when XIN driven by external clock)
20	VSS		P	Digital ground
21	VDD		P	3.3 V digital supply
22	TXD	Out	D, 5V Safe	SCI transmit output (open drain)
24	RXD	In	D, 5V Safe	SCI receive input (Schmitt trigger input)
29	T_REQ	In	D, 5V Safe	Transmit Request input
31	BR1	In	D, 5V Safe	SCI baud rate selection
32	BR0	In	D, 5V Safe	SCI baud rate selection
33	CRC	Out	D, 5V Safe	Correct frame CRC indication (open drain output)
35	RESB	In	D, 5V Safe	Master reset bar (Schmitt trigger input, active low)
36	TEST	In	D	Test enable (internal pull down)

P: Power pin
A: Analog pin
D: Digital pin

5V Safe: IO that support the presence of 5 V on bus line
Out: Output signal
In: Input signal

Table 7. AMIS−49587 QFN PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	I/O	Type	Description
37	TX_ENB	Out	D, 5V Safe	TX enable bar (open drain)
42	TX_OUT	Out	A	Transmitter output
43	ALC_IN	In	A	Automatic level control input
46	VDDA		P	3.3 V analog supply
47	VSSA		P	Analog ground
48	RX_OUT	Out	A	Output of receiver low noise operational amplifier
49	RX_IN	In	A	Positive input of receiver low noise operational amplifier
51	REF_OUT	Out	A	Reference output for stabilization
2, 3, .. 50, 52	NC			Pins 2, 3, 4, 5, 12, 13, 14, 15, 19,23, 25, 26, 27, 28, 30, 34, 38, 39, 40, 42, 44, 45, 50, 52 are not connected. These pins need to be left open or connected to the GND plane

P: Power pin
A: Analog pin
D: Digital pin
5V Safe: IO that support the presence of 5 V on bus line
Out: Output signal
In: Input signal

3.3 Detailed Pin Description

VDDA
VDDA is the positive analog supply pin. Nominal voltage is 3.3 V. A ceramic decoupling capacitor C_{DA} = 100 nF ± 10% must be placed between this pin and the VSSA. Connection path of this capacitance to the VSSA on the PCB should be kept as short as possible in order to minimize the serial resistance.

REF_OUT
REF_OUT is the analog output pin which provides the voltage reference used by the A/D converter. This pin must be decoupled to the analog ground by a 1 μF ± 10 percent ceramic capacitance C_{DREF}. The connection path of this capacitor to the VSSA on the PCB should be kept as short as possible in order to minimize the serial resistance.

VSSA
VSSA is the analog ground supply pin.

VDD
VDD is the 3.3 V digital supply pin. A ceramic decoupling capacitor C_{DD} = 100 nF ± 10% must be placed between this pin and the VSS. Connection path of this capacitance to the VSS on the PCB should be kept as short as possible in order to minimize the serial resistance.

VSS
VSS is the digital ground supply pin.

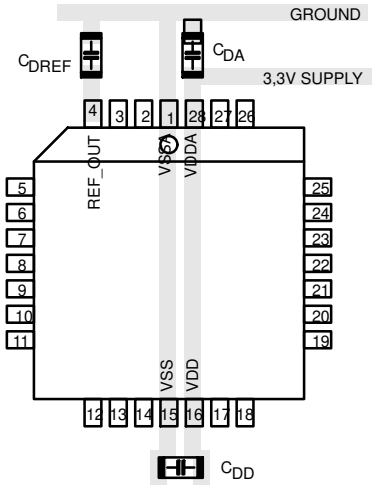


Figure 4. Recommended Layout of the Placement of Decoupling Capacitors for PLCC−28

RX_OUT
RX_OUT is the output analog pin of the receiver low noise input op−amp. This op−amp is in a negative feedback configuration.

RX_IN
RX_IN is the positive analog input pin of the receiver low noise input op−amp. Together with RX_OUT and REF_OUT, an active high pass filter is realized. This filter removes the main frequency (50 or 60 Hz) from the received signal. The filter characteristics are determined by external capacitors and resistors. A typical application schematic can be found in paragraph 50/60 Hz suppression filter.

M50Hz_IN
M50HZ_IN is the mains frequency analog input pin. The signal is used to detect the zero crossing of the 50 or 60 Hz sine wave. This information is used, after filtering with the internal PLL, to synchronize frames with the mains frequency. In case of direct connection to the mains it is advised to use a series resistor of 1 MΩ in combination with two external clamp diodes in order to limit the current flowing through the internal protection diodes.

RX_DATA
RX_DATA is a 5 V compliant open drain output. An external pull−up resistor defines the logic high level as illustrated in Figure 5. A typical value for the pull−up resistance “R” is 10 kΩ. The signal on this output depends on the status of the data reception. If AMIS−49587 waits for configuration RX_DATA outputs a pulse train with a 10 Hz frequency. After Synchronization Confirm Time out RX_DATA = 0. If AMIS−49587 is searching for synchronization RX_DATA = 1.

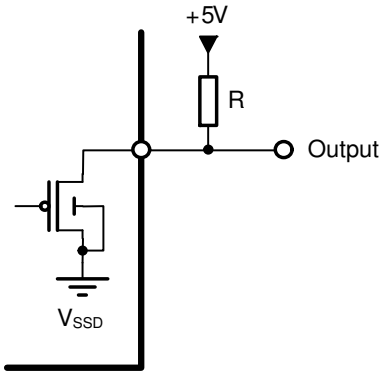


Figure 5. Representation of 5V Safe Output

TDO, TDI, TCK, TMS, and TRSTB

All these pins are part of the JTAG bus interface. The JTAG interface is used during production test of the IC and will not be described here. Input pins (TDI, TCK, TMS, and TRSTB) contain internal pull−down resistance. TDO is an output. When not used, the JTAG interface pins may be left floating.

TX_DATA/PRE_SLOT

TX_DATA/PRE_SLOT is the output for either the transmitting data (TX_DATA) or a synchronization signal with the time−slots (PRE_SLOT). More information can be found in paragraph Local Port.

XIN

XIN is the analog input pin of the oscillator. It is connected to the interval oscillator inverter gain stage. The clock signal can be created either internally with the external crystal and two capacitors or by connecting an external clock signal to XIN. For the internal generation case, the two external capacitors and crystal are placed as shown in Figure 6. For the external clock connection, the signal is connected to XIN and XOUT is left unused.

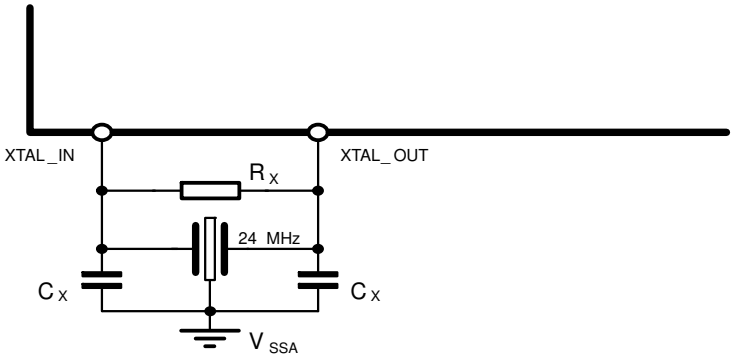


Figure 6. Placement of the Capacitors and Crystal with Clock Signal Generated Internally

The crystal is a classical parallel resonance crystal of 24 MHz. The values of the capacitors C_X are given by the manufacturer of the crystal. A typical value is 30 pF. The crystal has to fulfill impedance characteristics specified in the AMIS−49587 data sheet. As an oscillator is sensitive and precise, it is advised to put the crystal as close as possible on the board and to ground the case.

XOUT

XOUT is the analog output pin of the oscillator. When the clock signal is provided from an external generator, this output must be floating. When working with a crystal, this pin cannot be used directly as clock output because no additional loading is allowed on the pin (limited voltage swing).

TXD

TXD is the digital output of the asynchronous serial communication (SCI) unit. Only half−duplex transmission is supported. It is used to realize the communication between the AMIS−49587 and the application microcontroller. The TXD is an open drain IO (5 V safe). External pull−up resistances (typically 10 kΩ) are necessary to generate the 5 V level. See Figure 5 for the circuit schematic.

RXD

This is the digital input of the asynchronous SCI unit.
Only half−duplex transmission is supported. This pin supports a 5 V level. It is used to realize the communication between the AMIS−49587 and the application microcontroller. RXD is a 5 V safe input.

T_REQ

T_REQ is the transmission request input of the Serial Communication Interface. When pulled low its initiate a local communication from the application micro controller to AMIS−49587. T_REQ is a 5 V safe input.

BR1, BR0

BR0 and BR1 are digital input pins. They are used to select the baud rate (bits/second) of the Serial Communication Interface unit. The rate is defined according to Table 28: BR1, BR0 Baud Rates. The values are taken into account after a reset, hardware or software. Modification of the baud rate during function is not possible. BR0 and BR1 are 5 V safe.

CRC
CRC is a 5V compliant open drain output. An external pull−up resistor defines the logic high level as illustrated in Figure 5. A typical value for this pull−up resistance “R” is 10 kΩ. The signal on this output depends on the cyclic redundancy code result of the received frame. If the cyclic redundancy code is correct CRC = 1 during the pause between 2 time slots.

RESB
RESB is a digital input pin. It is used to perform a hardware reset of the AMIS−49587. This pin supports a 5 V voltage level. The reset is active when the signal is low (0 V).

TEST
TEST is a digital input pin. It is used to enable the test mode of the chip. Normal mode is activated when TEST signal is low (0 V). For normal operation, the TEST pin may be left unconnected. Due to the internal pulldown, the signal is maintained to low (0 V). TEST pin is not 5 V safe.

TX_ENB
TX_ENB is a digital output pin. It is low when the transmitter is activated. The signal is available to turn on the line driver. TX_ENB is a 5 V safe with open drain output, hence a pull−up resistance is necessary achieve the requested voltage level associated with a logical one. See also Figure 5 for reference.

TX_OUT
TX_OUT is the analog output pin of the transmitter. The provided signal is the S−FSK modulated frames. A filtering operation must be performed to reduce the second order harmonic distortion. For this purpose an active filter is realized. Figure 7 gives the representation of this filter.

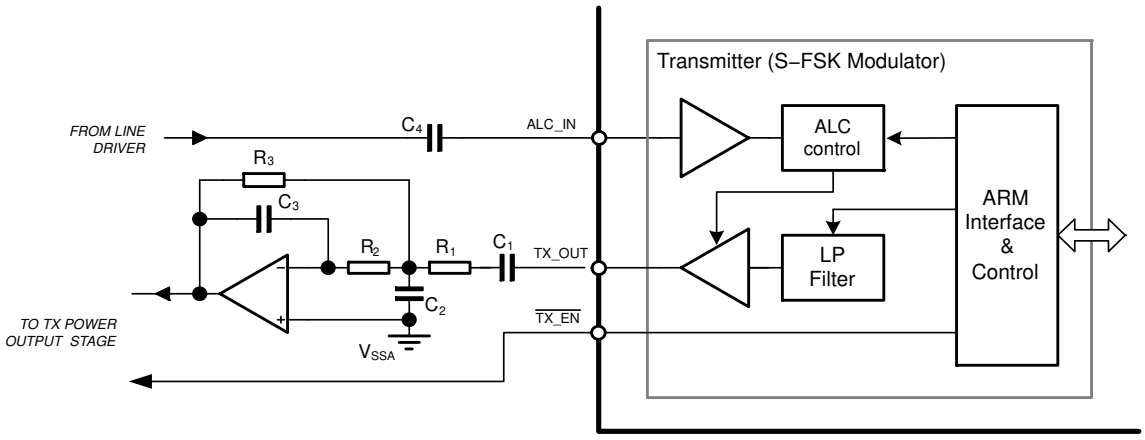


Figure 7. TX_OUT Filter

ALC_IN
ALC_IN is the automatic level control analog input pin. The signal is used to adjust the level of the transmitted signal. The signal level adaptation is based on the AC component. The DC level on the ALC_IN pin is fixed internally to 1.65 V. Comparing the peak voltage of the AC signal with two internal thresholds does the adaptation of the gain. Low threshold is fixed to 0.4 V. A value under this threshold will result in an increase of the gain. The high threshold is fixed to 0.6 V. A value over this threshold will result in a decrease of the gain. A serial capacitance is used to block the DC components. The level adaptation is performed during the transmission of the first two bits of a new frame. Eight successive adaptations are performed.

4 ELECTRICAL CHARACTERISTICS

4.1 DC AND AC CHARACTERISTICS

4.1.1 Oscillator: Pin XIN, XOUT

In production the actual oscillation of the oscillator and duty cycle will not be tested. The production test will be based on the static parameters and the inversion from XIN to XOUT in order to guarantee the functionality of the oscillator.

Table 8. OSCILLATOR

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Crystal frequency	(Note 1)	f_{CLK}	−100 ppm	24	+100 ppm	MHz
Duty cycle with quartz connected	(Note 1)		40		61	%
Start−up time	(Note 1)	$T_{startup}$			50	ms
Maximum Capacitive load on XOUT	XIN used as clock input	CL_{XOUT}			50	pF
Low input threshold voltage	XIN used as clock input	VIL_{XOUT}	0.3 V_{DD}			V
High input threshold voltage	XIN used as clock input	VIH_{XOUT}			0.7 V_{DD}	V
Low output voltage	XIN used as clock input, XOUT = 2 mA	VOL_{XOUT}			0.3	V
High input voltage	XIN used as clock input	VOH_{XOUT}			V_{DD}−0.3	V

1. Guaranteed by design. Maximum allowed series loss resistance up to 80 Ω.

4.1.2 Zero Crossing Detector and 50/60 Hz PLL: Pin M50HZ_IN

Table 9. ZERO CROSSING DETECTOR AND 50/60 Hz PLL

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Maximum peak input current		$Imp_{M50HZIN}$	−20		20	mA
Maximum average input current	During 1 ms	$Imavg_{M50HZIN}$	−2		2	mA
Mains voltage (ms) range	With protection resistor at M50HZIN	V_{MAINS}	90		550	V
Rising threshold level	(Note 2)	$VIRM_{50HZIN}$			1.9	V
Falling threshold level	(Note 2)	$VIFM_{50HZIN}$	0.82			V
Hysteresis	(Note 2)	VHY_{50HZIN}	0.4			V
Lock range for 50 Hz (Note 3)	MAINS_FREQ = 0 (50 Hz)	$Flock_{50Hz}$	45		55	Hz
Lock range for 60 Hz (Note 3)	MAINS_FREQ = 0 (60 Hz)	$Flock_{60Hz}$	54		66	Hz
Lock time (Note 3)	MAINS_FREQ = 0 (50 Hz)	$Tlock_{50Hz}$			15	s
Lock time (Note 3)	MAINS_FREQ = 0 (60 Hz)	$Tlock_{60Hz}$			20	s
Frequency variation without going out of lock (Note 3)	MAINS_FREQ = 0 (50 Hz)	DF_{60Hz}			0.1	Hz/s
Frequency variation without going out of lock (Note 3)	MAINS_FREQ = 0 (60 Hz)	DF_{50Hz}			0.1	Hz/s
Jitter of CHIP_CLK (Note 3)		$Jitter_{CHIP\_CLK}$	−25		25	μs

2. Measured relative to V_{SS}.
3. These parameters will not be measured in production since the performance is totally dependent of a digital circuit which will be guaranteed by the digital test patterns.

4.1.3 Transmitter External Parameters: Pin TX_OUT, ALC_IN, TX_ENB

To guarantee the transmitter external specifications the TX_CLK frequency must be 12 MHz ± 100 ppm.

Table 10. TRANSMITTER EXTERNAL PARAMETERS

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Maximum peak output level	fTX_OUT = 23.75 kHz fTX_OUT = 95 kHz Level control at max. output	V_{TX_OUT}	0.85 0.76		1.15 1.22	Vp
Second order harmonic distortion	fTX_OUT = 95 kHz Level control at max. output	HD2			−54	dB
Third order harmonic distortion	fTX_OUT = 95 kHz Level control at max. output	HD3			−56	dB
Frequency accuracy of the generated sine wave	(Notes 4 and 6)	Df_{TX_OUT}			30	Hz
Capacitive output load at pin TX_OUT	(Note 4)	CL_{TX_OUT}			20	pF
Resistive output load at pin TX_OUT		RL_{TX_OUT}	5			kΩ
Turn off delay of TX_ENB output	(Note 5)	Td_{TX_ENB}	0.25		0.5	ms
Automatic level control attenuation step		ALC_{step}	2.9		3.1	dB
Maximum attenuation		ALC_{range}	20.3		21.7	dB
Low threshold level on ALC_IN		VTL_{ALC_IN}	−0.49		−0.36	V
High threshold level on ALC_IN		VTH_{ALC_IN}	−0.71		−0.54	V
Input impedance of ALC_IN pin		R_{ALC_IN}	111		189	kΩ
Power supply rejection ration of the transmitter section		$PSRR_{TX\_OUT}$	10 (Note 7)		35 (Note 8)	dB

4. This parameter will not be tested in production.
5. This delay corresponds to the internal transmit path delay and will be defined during design.
6. Taking into account the resolution of the DDS and an accuracy of 100 ppm of the crystal.
7. A sinusoidal signal of 10 kHz and 100 mVpp is injected between VDDA and VSSA. The digital AD converter generates an idle pattern. The signal level at TX_OUT is measured to determine the parameter.
8. A sinusoidal signal of 50 Hz and 100 mVpp is injected between VDDA and VSSA. The digital AD converter generates an idle pattern. The signal level at TX_OUT is measured to determine the parameter.

The LPF filter + amplifier must have a frequency characteristic between the limits listed below. The absolute output level depends on the operating condition. In production the measurement will be done for relative output levels where the 0 dB reference value is measured at 50 kHz with a signal amplitude of 100 mV.

Table 11. TRANSMITTER FREQUENCY CHARACTERISTICS

	Attenuation		
Frequency (kHz)	Min	Max	Unit
10	−0.5	0.5	dB
95	−1.3	0.5	dB
130	−4.5	−2.0	dB
165		−3.0	dB
330		−18.0	dB
660		−36.0	dB
1000		−50	dB
2000		−50	dB

4.1.4 Receiver External Parameters: Pin RX_IN, RX_OUT, REF_OUT

Table 12. RECEIVER EXTERNAL PARAMETERS: Pin RX_IN, RX_OUT, REF_OUT

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Input offset voltage 42 dB	AGC gain = 42 dB	$V_{OFFS\_RX\_IN}$			5	mV
Input offset voltage 0 dB	AGC gain = 0 dB	$V_{OFFS\_RX\_IN}$			50	mV
Max. peak input voltage (corresponding to 62.5% of the SD full scale)	AGC gain = 0 dB (Note 9)	$V_{MAX\_RX\_IN}$	0.85		1.15	V_p
Input referred noise of the analog receiver path	AGC gain = 42 dB (Notes 9 and 10)	NF_{RX_IN}			150	nV/$\sqrt{Hz}$
Input leakage current of receiver input		$I_{LE\_RX\_IN}$	−1		1	μA
Max. current delivered by REF_OUT		$I_{Max\_REF\_OUT}$	−300		300	mA
Power supply rejection ratio of the receiver input section	AGC gain = 42 dB (Note 11) AGC gain = 42 dB (Note 12)	$PSRR_{LPF\_OUT}$	10 35			dB
AGC gain step		AGC_{step}	5.7		6.3	dB
AGC range		AGC_{range}	39.9		44.1	dB
Analog ground reference output voltage		V_{REF_OUT}	1.52		1.78	V
Signal to noise ratio at 62.5% of the SD full scale	(Notes 9 and 13)	SN_{AD_OUT}	54			dB
Clipping level at the output of the gain stage (RX_OUT)		$V_{CLIP\_AGC\_IN}$	1.15		1.65	Vp

9. Input at RX_IN, no other external components.
10. Characterization data only. Not tested in production.
11. A sinusoidal signal of 10 kHz and 100 mVpp is injected between VDDA and VSSA. The signal level at the differential LPF_OUT and REF_OUT output is measured to determine the parameter.
12. A sinusoidal signal of 50 Hz and 100 mVpp is injected between VDDA and VSSA. The signal level at the differential LPF_OUT output is measured to determine the parameter.
13. These parameters will be tested in production with an input signal of 95 kHz and 1 Vp by reading out the digital samples at the point AD_OUT with the default settings of T_RX_MOD[7], SDMOD_TYP, DEC_TYP, and COR_F_ENA. The AGC gain is switched to 0 dB.

The receive LPF filter + AGC + low noise amplifier must have a frequency characteristic between the limits listed below. The absolute output level depends on the operating condition. In production the measurement will be done for relative output levels where the 0 dB reference value is measured at 50 kHz with a signal amplitude of 100 mV.

Table 13. RECEIVER FREQUENCY CHARACTERISTICS

Frequency (kHz)	Attenuation		Unit
	Min	Max	
10	−0.5	0.5	dB
95	−1.3	0.5	dB
130	−4.5	−2.0	dB
165		−3.0	dB
330		−18.0	dB
660		−36.0	dB
1000		−50	dB
2000		−55	dB

4.1.5 Power−on−Reset (POR)

Table 14. POWER−ON−RESET (POR)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
POR threshold		V_{POR}	1.7		2.7	V
Power supply rise time	0 V to 3 V	T_{RPOR}	1			ms

4.1.6 Digital Outputs: TDO, CLK_OUT

Table 15. DIGITAL OUTPUTS: TDO, CLK_OUT

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low output voltage	I_{XOUT} = 4 mA	V_{OL}			0.4	V
High output voltage	I_{XOUT} = −4 mA	V_{OH}	0.85 V_{DD}			V

4.1.7 Digital Outputs with Open Drains: TX_ENB, TXD

Table 16. DIGITAL OUTPUTS WITH OPEN DRAIN: TX_END, TXD

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low output voltage	I_{XOUT} = 4 mA	V_{OL}			0.4	V

4.1.8 Digital Inputs: BR0, BR1

Table 17. DIGITAL INPUTS: BR0, BR1

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low input level		V_{IL}			0.2 V_{DD}	V
High input level	0 V to 3 V	V_{IH}	0.8 V_{DD}			V
Input leakage current		I_{LEAK}	−10		10	μA

4.1.9 Digital Inputs with Pulldown: TDI, TMS, TCK, TRSTB, TEST

Table 18. DIGITAL INPUTS WITH PULLDOWN: TDI, TMS, TCK, TRSTB, TEST

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Low input level		V_{IL}			0.2 V_{DD}	V
High input level		V_{IH}	0.8 V_{DD}			V
Pulldown resistor	(Note 14)	R_{PU}	7		50	kΩ

14. Measured around a bias point of $V_{DD}/2$.

4.1.10 Digital Schmitt Trigger Inputs: RXD, RESB

Table 19. DIGITAL SCHMITT TRIGGER INPUTS: RXD, RESB

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Rising threshold level		V_{T+}			0.8 V_{DD}	V
Falling threshold level		$V_{T−}$	0.2 V_{DD}			V
Input leakage current		I_{LEAK}	−10		1−	μA

4.1.11 Current Consumption

Table 20. CURRENT CONSUMPTION

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Current consumption in receive mode	Current through V_{DD} and V_{DDA} (Note 15)	I_{RX}	60		80	mA
Current consumption in transmit mode	Current through V_{DD} and V_{DDA} (Note 15)	I_{TX}	60		80	mA
Current consumption when RESB = 0	Current through V_{DD} and V_{DDA} (Note 15)	I_{RESET}			4	mA

15. CLKARM is < 12 MHz, fCLK = 24 MHz.

4.1.12 Main Modem Characteristics

Table 21. OPERATING CHARACTERISTICS

Parameter	Value	Unit
Positive supply voltage Negative supply voltage	3.0 to 3.6 −0.7 to + 0.3	V V
Max peak output level	1.2	Vp
HD2	−60	dB
HD3	−60	dB
ALC Steps	3	dB
ALC Range	(0 ... −21)	dB
Maximum input signal	1.15	Vp
Input impedance	100	kΩ
Input sensitivity	0.4	mV
AGC steps	6	dB
AGC range	(0 ... +42)	dB
Maximum 50 Hz variation	0, 1	Hz/s
Data rate	300/360 (Note 22) 600/720 (Note 22) 1200/1440 (Note 22) 2400/2880(Note 22)	baud baud baud baud
Programmable carrier (Note 21)		
Frequency band		
Frequency minimum	9	kHz
Frequency maximum	95	kHz
Frequency deviation between pairs	>10	kHz
Dynamic range	40 (Note 16) 60 (Note 17) 80 (Note 18)	dB dB dB
Narrow band interfere BER (Note 19)	10E−5	
Maximum 50 Hz variation	0.1	Hz/s

16. FER = 0%.
17. FER = 0.3%.
18. FER = 8.0%.
19. Signal between −60 dB and 0 dB interference signal level is 30 dB above signal level between 20 kHz and 95 kHz.
20. Input at −40 dB, duty cycle between 10 − 50% pulse noise frequency between 100 to 1000 Hz. BER: Bit error rate FER: Frame error rate (1frame is 288 bits).
21. Carriers frequency is programmable by steps of 10 Hz.
22. 60 Hz mains frequency.

5 INTRODUCTION

5.1 GENERAL DESCRIPTION

The AMIS−49587 is a single chip half duplex S−FSK modem dedicated to power line carrier (PLC) data transmission on low− or medium−voltage power lines. The device offers complete handling of the protocol layers from the physical up to the MAC. AMIS−49587 complies with the CENELEC EN 50065−1 and the IEC 61334−5−1 standards. It operates from a single 3.3 V power supply and is interfaced to the power line by an external power driver and transformer. An internal PLL is locked to the mains frequency and is used to synchronize the data transmission at data rates of 300, 600, 1200 and 2400 baud for a 50Hz mains frequency, or 360, 720, 1440 and 2880 baud for a 60 Hz mains frequency. In both cases this corresponds to 3,6,12 or 24 data bits per half cycle of the mains period.

S−FSK is a modulation and demodulation technique that combines some of the advantages of a classical spread spectrum system (e.g. immunity against narrow band interferers) with the advantages of the classical FSK system (low complexity). The transmitter assigns the space frequency f_S to “data 0” and the mark frequency f_M to “data 1”. The difference between S−FSK and the classical FSK lies in the fact that f_S and f_M are now placed far from each other, making their transmission quality independent from each other (the strengths of the small interferences and the signal attenuation are both independent at the two frequencies). The frequency pairs supported by the AMIS−49587 are in the range of 9−95 kHz with a typical separation of 10 kHz.

The conditioning and conversion of the signal is performed at the analog front−end of the circuit. The further processing of the signal and the handling of the protocol is digital. At the back−end side, the interface to the application is done through a serial interface. The digital processing of the signal is partitioned between hardwired blocks and a microprocessor block. The microprocessor is controlled by firmware. Where timing is most critical, the functions are implemented with dedicated hardware. For the functions where the timing is less critical, typically the higher level functions, the circuit makes use of the ARM 7TDMI microprocessor core.

The processor runs DSP algorithms and, at the same time, handles the communication protocol. The communication protocol, in this application, contains the MAC = Medium Access Control Layer. The program running on the microprocessor is stored into ROM. The working data necessary for the processing is stored in an internal RAM. At the back−end side the link to the application hardware is provided by a Serial Communication Interface (SCI). The SCI is an easy to use serial interface, which allows communication between an external processor used for the application software and the AMIS−49587 modem. The SCI works on two wires: TXD and RXD. Baud rate is programmed by setting 2 bits (BR0, BR1).

Because the low protocol layers are handled in the circuit, the AMIS−49587 provides an innovative architectural split. Thanks to this, the user has the benefit of a higher level interface of the link to the PLC medium. Compared to an interface at the physical level, the AMIS−49587 allows faster development of applications. The user just needs to send the raw data to the AMIS−49587 and no longer has to take care of the protocol detail of the transmission over the specific medium. This last part represents usually 50 percent of the software development costs.

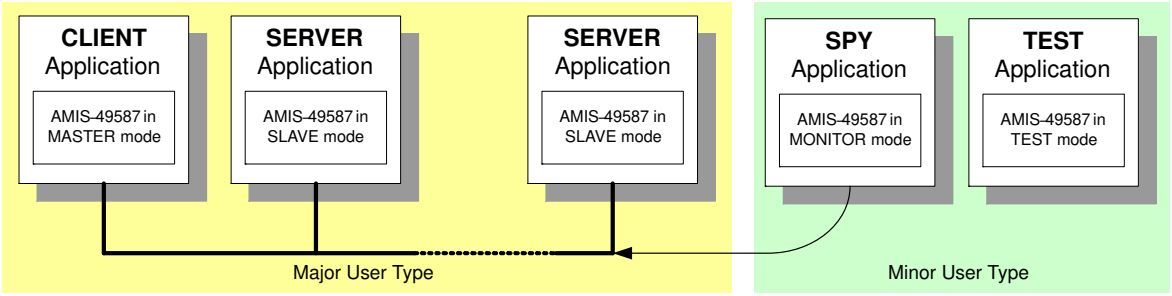


Figure 8. Application Examples

AMIS−49587 intended to connect equipment using Distribution Line Carrier (DLC) communication. It serves two major and two minor types of applications:

- Major types:
  - Master or Client:
    A Master is a client to the data served by one or many slaves on the power line. It collects data from and controls the slave devices. A typical application is a concentrator system.
  - Slave or Server:
    A Slave is a server of the data to the Master. A typical application is an electricity meter equipped with a PLC modem.
- Minor type:
  - Spy or Monitor:
    Spy or Monitor mode is used to only listen to the data that comes across the power line. Only the physical layer frame correctness is checked. When

the frame is correct, it is passed to the external processor.

- Test Mode:
  The Test Mode is used to test the compliance of a PLC modem conforms to CENELEC. EN 50065−1 by a Continuous broadcast of f_S or f_M.

5.1.1. CONVERTING AMIS−49587−BASED DESIGNS TO NCN49597

The NCN49597 is designed to allow easy adaptation of printed circuit board designs using the AMIS−49587. All connected pins of the latter (QFN package) are present in the same location in the NCN49597.

Four important hardware changes must be noted.

Most of the not−connected (NC) pins of the AMIS−49587 are functional in the NCN49597. If these pins were previously connected to ground (a commendable practice) this must be taken into account. IO4–IO10 are usually configured as inputs and can therefore be grounded safely.

However, it must be considered that some NC pins of AMIS−49587 are outputs in the NCN49597. These include SDO, SCK and, CSB. IO0 and IO1 are used typically used by the firmware as status indicators. IO3 is used by the ON PL110 firmware for controlling the amplifier enable signal.

Secondly, the NCN49597 incorporates an internal 1.8 V regulator to power the digital core. For stability, a 1 μF capacitor to ground must be connected on pin 19 (VDD1V8).

In addition, the lowest baud rate setting of the AMIS−49587 serial interface (BR0 & BR1 pulled low; 4800 baud) has been replaced by 115200 baud. All other BR0 and BR1 settings will result in the same baud rate.

Finally, a 48 MHz crystal is required for the NCN49597; the AMIS−49587 used a 24 MHz crystal.

The firmware running on the modem has been updated substantially compared to the AMIS−49587. As a result, the interface protocol between the user microcontroller and the modem is completely different. Refer to the firmware datasheet for details.

5.2 FUNCTIONAL DESCRIPTION

The block diagram below represents the main functional units of the AMIS−49587:

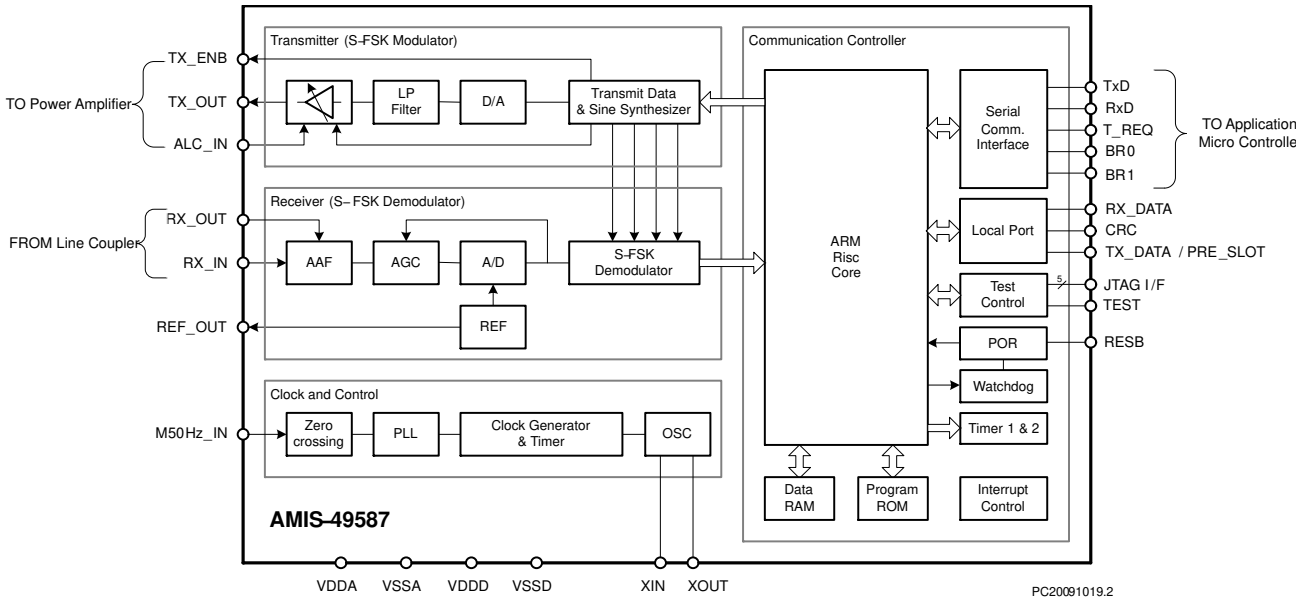


Figure 9. S−FSK Modem AMIS−49587 Block Diagram

5.2.1 Transmitter

The AMIS−49587 Transmitter function block prepares the communication signal which will be sent on the transmitting channel during the transmitting phase. This block is connected to a power amplifier which injects the output signal on the mains through a line−coupler.

5.2.2 Receiver

The analog signal coming from the line−coupler is low pass filtered in order to avoid aliasing during the conversion. Then the level of the signal is automatically adapted by an automatic gain control (AGC) block. This operation maximizes the dynamic range of the incoming signal. The signal is then converted to its digital representation using sigma delta modulation. From then on, the processing of the data is done in a digital way. By using dedicated hardware, a direct quadrature demodulation is performed. The signal demodulated in the base band is then low pass filtered to reduce the noise and reject the image spectrum.

Clock and Control

According to the IEC−61334−5−1 standard, the frame data is transmitted at the zero crossing of the mains voltage. In order to recover the information at the zero crossing, a zero crossing detection of the mains is performed. A phase−locked loop (PLL) structure is used in order to allow

a more reliable reconstruction of the synchronization. This PLL permits as well a safer implementation of the ”repetition with credit” function (also known as chorus transmission). The clock generator makes use of a precise quartz oscillator master. The clock signals are then obtained by the use of a programmed division scheme. The support circuits are also contained in this block. The support circuits include the necessary blocks to supply the references voltages for the AD and DA converters, the biasing currents and power supply sense cells to generate the right power off and startup conditions.

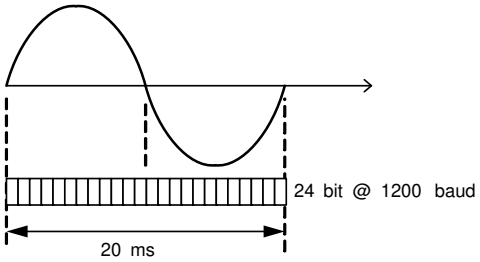


Figure 10. Data Stream is in Sync with Zero Crossings of the Mains (Example for 50 Hz)

5.2.3 Communication Controller

The Communication Controller block includes the micro−processor, its peripherals: RAM, ROM, UART, TIMER, and the Power on reset. The processor uses the ARM Reduced Instruction Set Computer (RISC) architecture optimized for IO handling. For most of the instructions, the machine is able to perform one instruction per clock cycle. The microcontroller contains the necessary hardware to implement interrupt mechanisms, timers and is able to perform byte multiplication over one instruction cycle. The microcontroller is programmed to handle the physical layer (chip synchronization), and the MAC layer conform to IEC 61334−5−1. The program is stored in a masked ROM. The RAM contains the necessary space to store the working data. The back−end interface is done through the Serial Communication Interface block. This back−end is used for data transmission with the application micro controller (containing the application layer for concentrator, power meter, or other functions) and for the definition of the modem configuration.

5.2.4 Local Port

The controller uses 3 output ports to inform about the actual status of the PLC communication. RX_DATA indicates if Receiving is in progress, or if AMIS−49587 is waiting for synchronization, or of it configures. CRC indicates if the received frames are valid (CRC = OK). TX_DATA / PRE_SLOT is the output for either the transmitting data (TX_DATA) or a synchronization signal with the time−slots (PRE_SLOT).

5.2.5 Serial Communication Interface

The local communication is a half duplex asynchronous serial link using a receiving input (RxD) and a transmitting output (TxD). The input port T_REQ is used to manage the local communication with the application micro controller and the baud rate can be selected depending on the status of two inputs BR0, BR1. These two inputs are taken in account after an AMIS−49587 reset. Thus when the application micro controller wants to change the baud rate, it has to set the two inputs and then provoke a reset.

6 DETAILED HARDWARE DESCRIPTION

6.1 CLOCK AND CONTROL

According to the IEC 61334−5−1 standard, the frame data is transmitted at the zero crossing of the mains voltage. In order to recover the information at the zero crossing, a zero crossing detection of the mains is performed. A phase−locked loop (PLL) structure is used in order to allow a more reliable reconstruction of the synchronization. The output of this block is the clock signal CHIP_CLK, 8 times over sampled with the bit rate. The oscillator makes use of a precise 24 MHz quartz. This clock signal together with CHIP_CLK is fed into the Clock Generator and time block. Here several internal clock signals and timings are obtained by the use of a programmed division scheme.

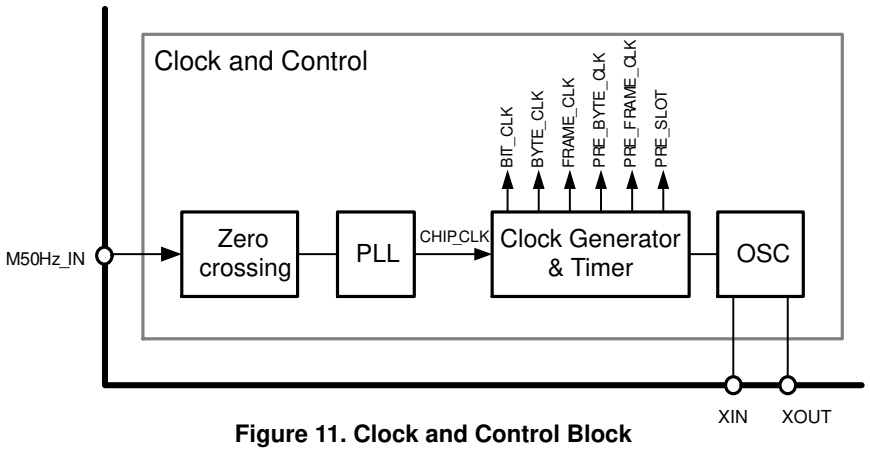


Figure 11. Clock and Control Block

6.1.1 Zero Crossing Detector

M50HZ_IN is the mains frequency analog input pin. The signal is used to detect the zero crossing of the 50 or 60 Hz sine wave. This information is used, after filtering with the internal PLL, to synchronize frames with the mains frequency. In case of direct connection to the mains it is advised to use a series resistor of 1 MΩ in combination with two external clamp diodes in order to limit the current flowing through the internal protection diodes.

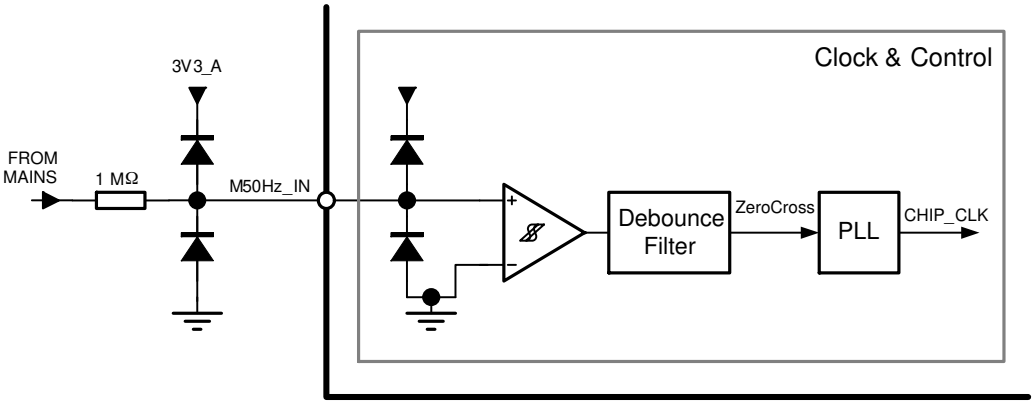


Figure 12. Zero Cross Detector with Falling Edge Debouncer

The zero crossing detector output is logic zero when the input is lower than the falling threshold level and a logic one when the input is higher than the rising threshold level. The falling edges of the output of the zero crossing detector are de−bounced by a period between 0.5 ms and 1 ms. The Rising edges are not de−bounced.

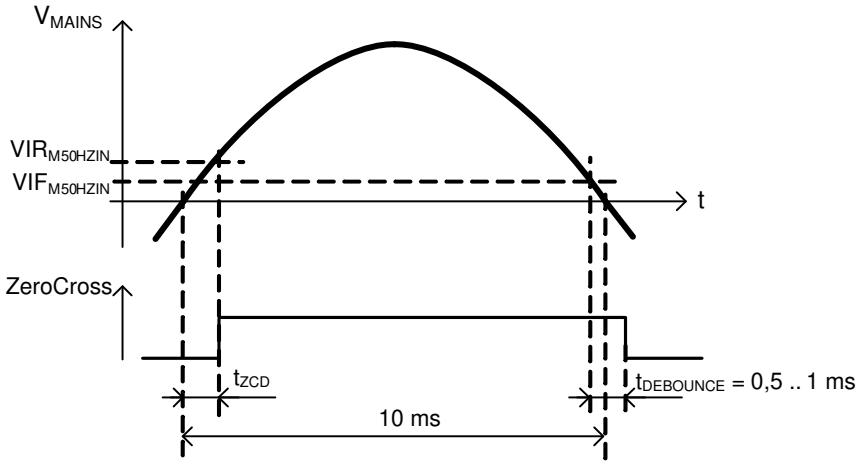


Figure 13. Zero Cross Detector Signals and Timing (Example for 50 Hz)

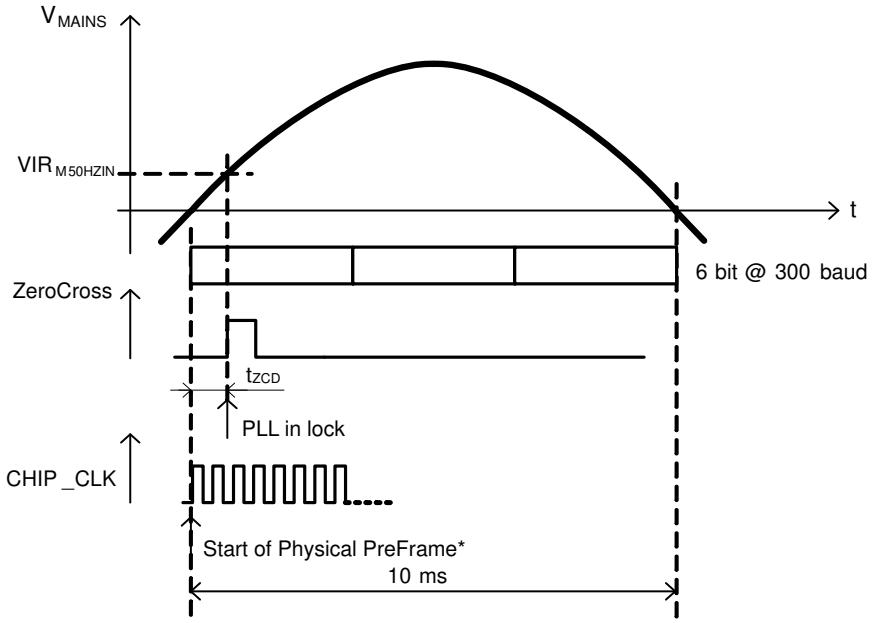
6.1.2 50/60 Hz PLL

The output of the zero crossing detector is used as an input for a PLL. The PLL generates the clock CHIP_CLK which is 8 times the bit rate and which is in phase with the rising edge crossings. The PLL locks on the zero crossing from negative to positive phase. The bit rate is always an even multiple of the mains frequency, so following combinations are possible:

Table 22. CHIP_CLK IN FUNCTION OF SELECTED BAUD RATE AND MAINS FREQUENCY

BAUD[1:0]	MAINS_FREQ	Baudrate	CHIP_CLK
00	50 Hz	300	2400 Hz
01		600	4800 Hz
10		1200	9600Hz
11		2400	19200 Hz
00	60 Hz	360	2880 Hz
01		720	5760 Hz
10		1440	11520Hz
11		2880	23040 Hz

In case no zero crossings are detected the PLL freezes its internal timers in order to maintain the CHIP_CLK timing.



*The start of the Physical Subframe is shifted back with R_ZC_ADJUST[7:0] x 26 μS = t_{ZCD} to compensate for the zero cross delay

Figure 14. Zero Cross Adjustment to Compensate for Zero Cross Delay (Example for 50 Hz)

The phase difference between the zero crossing of the mains and CHIP_CLK can be tuned. This opens the possibility to compensate for external delay t_{ZCD}(e.g. opto coupler) and for the 1.9 V positive threshold $VIR_{M50HZIN}$ of the zero crossing detector. This is done by pre−loading the PLL counter with a number value stored in register R_ZC_ADJUST[7:0]. The adjustment period or granularity is 26 μs. The maximum adjustment is 255 x 26 μs = 6.6 ms which corresponds with 1/3rd of the mains sine period.

Table 23. ZERO CROSS DELAY COMPENSATION

R_ZC_ADJUST[7:0]	Compensation
0000 0000	0 μs
0000 0001	26 μs
0000 0010	52 μs
0000 0011	78 μs
…	…
1111 1101	6589 μs
1111 1110	6615 μs
1111 1111	6641 μs

6.1.3 Oscillator

The oscillator works with a standard parallel resonance crystal of 24 MHz. XIN is the input to the oscillator inverter gain stage and XOUT is the output.

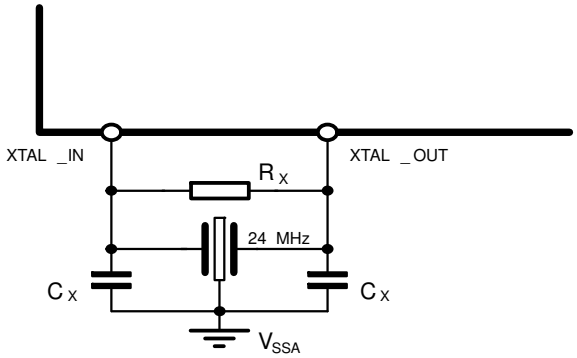


Figure 15. Placement of the Capacitors and Crystal with Clock Signal Generated Internally

For correct functionality the external circuit illustrated in Figure 15 must be connected to the oscillator pins. For a crystal requiring a parallel capacitance of 20 pF C_X must be around 30 pF. (Values of capacitors are indicative only and are given by the crystal manufacturer). To guarantee startup the series loss resistance of the crystal must be smaller than 80 Ω. A parallel resistor R_X = 1 MΩ is recommended to improve the clock symmetry.

The oscillator output f_{CLK} = 24 MHz is the base frequency for the complete IC. The clock frequency for the ARM f_{ARM} = f_{CLK}. The clock for the transmitter, f_{TX_CLK} is equal to f_{CLK} / 2 or 12 MHz. All the transmitter internal clock signals will be derived from f_{TX_CLK}. The clock for the receiver, f_{RX_CLK} is equal to f_{CLK} / 4 or 6 MHz. All the receiver internal clock signals will be derived from f_{RX_CLK}.

6.1.4 Clock Generator and Timer

The CHIP_CLK and f_{CLK} are used to generate a number of timing signals used for the synchronization and interrupt generation. The timing generation has a fixed repetition rate which corresponds to the length of a physical subframe. (see paragraph Send and Receive network data).

The timing generator is the same for transmit and receive mode. When AMIS−49587 switches from receive to transmit and back from transmit to receive, the R_CHIP_CNT counter value is maintained. As a result all timing signals for receive and transmit have the same relative timing. The following timing signals are defined as:

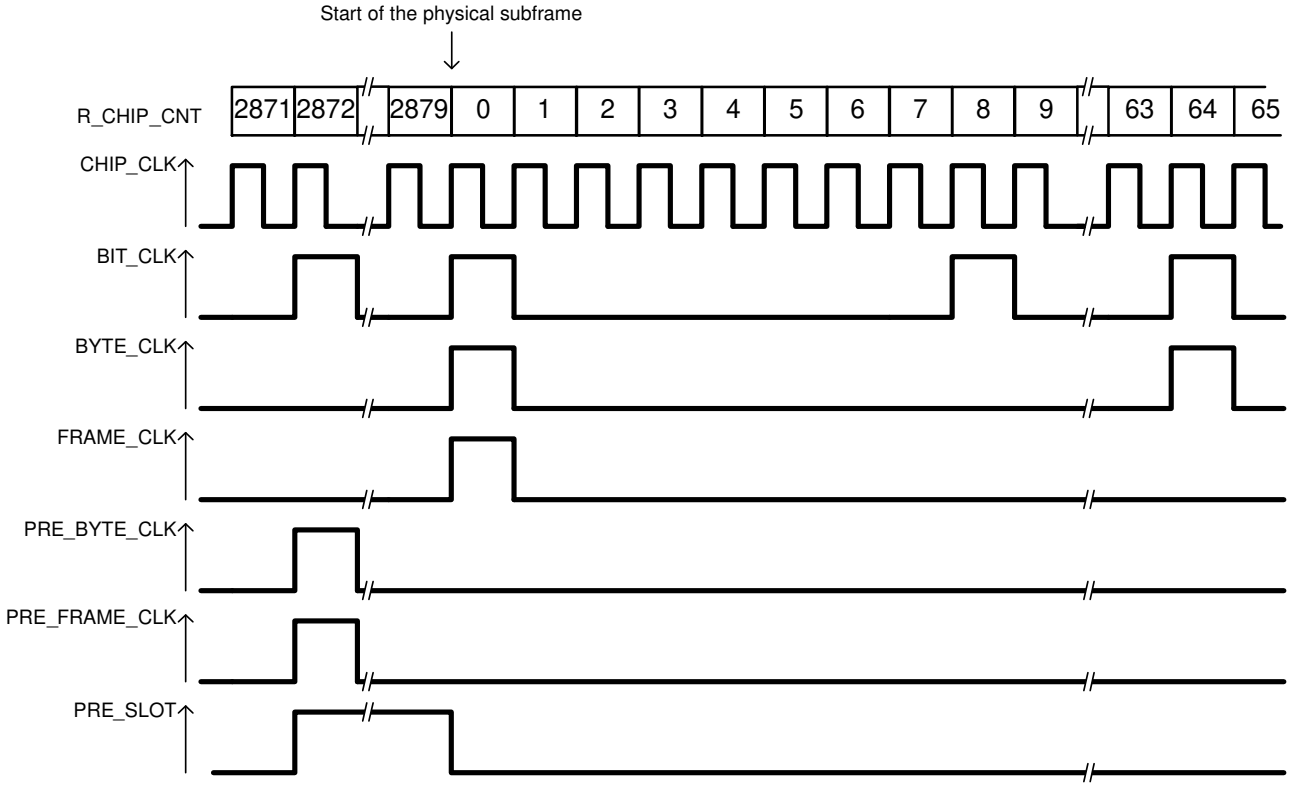


Figure 16. Timing Signals

CHIP_CLK is the output of the PLL and 8 times the bit rate on the physical interface. See also paragraph 50/60 Hz PLL
BIT_CLK is active at counter values 0,8,16, .. 2872 and inactive at all other counter values. This signal is used to indicate the transmission of a new bit.
BYTE_CLK is active at counter values 0,64,128, .. 2816 and inactive at all other counter values. This signal is used to indicate the transmission of a new byte.
FRAME_CLK is active at counter values 0 and inactive at all other counter values. This signal is used to indicate the transmission or reception of a new frame.
PRE_BYTE_CLK is a signal which is 8 CHIP_CLK sooner than BYTE_CLK. This signal is used as an interrupt for the internal microcontroller and indicates that a new byte for transmission must be generated.
PRE_FRAME_CLK is a signal which is 8 CHIP_CLK sooner than FRAME_CLK. This signal is used as an interrupt for the internal microcontroller and indicates that a new frame will start at the next FRAME_CLK.
PRE_SLOT is logic 1 between the rising edge of PRE_FRAME_CLK and the rising edge of FRAME_CLK. This signal can be provided at the digital output pin TX_DATA_PRE_SLOT when R_CONF[7] = 0 (See paragraph WriteConfigRequest, field TX_DATA_PRE−SLOT_SEL) and can be used by the external host controller to synchronize its software with the FRAME_CLK of AMIS−49587.

6.2 TRANSMITTER PATH DESCRIPTION (S−FSK MODULATOR)

For the generation of the space and mark frequencies, the direct digital synthesis (DDS) of the sine wave signals is performed under the control of the microprocessor. After a signal conditioning step, a digital to analog conversion is performed. As for the receive path, a sigma delta modulation technique is used. In the analog domain, the signal is low pass filtered, in order to remove the high frequency quantization noise, and passed to the automatic level controller (ACL) block, where the level of the transmitted signal can be adjusted. The determination of the signal level is done through the sense circuitry.

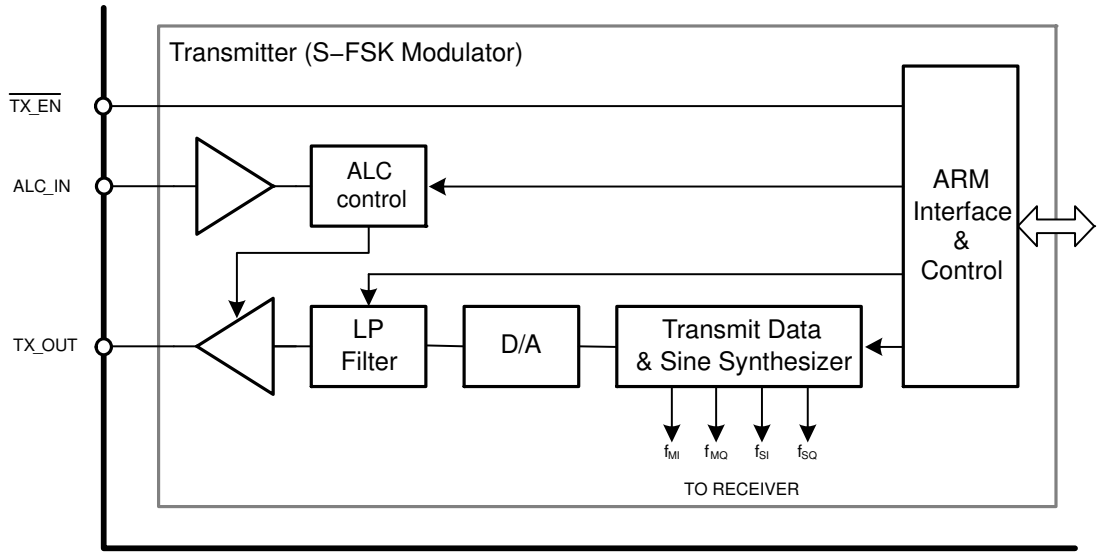


Figure 17. Transmitter Block Diagram

6.2.1 ARM Interface and Control

The interface with the ARM consists in a 8−bit data registers R_TX_DATA, 2 control registers R_TX_CTRL and R_ALC_CTRL, a flag TX_RXB defining transmit and receive and 2 16−bit wide frequency step registers R_FM and R_FS defining f_M (mark frequency = data 1) and f_S (space frequency = data 0). All these registers are memory mapped. Some of them are for internal use only and cannot be accessed by the user.

The processing of the physical frame (preamble, MAC address, CRC) is done by the ARM.

6.2.2 Sine Wave Generator

A sine wave is generated with a direct digital synthesizer DDS. The synthesizer generates in transmission mode a sine wave either for the space frequency (f_S, data 0) or for the mark frequency (f_M, data1). In reception the synthesizer generates the sine and cosine waves for the mixing process, f_{SI}, f_{SQ}, f_{MI}, f_{MQ} (space and mark signals in phase and quadrature). The space and mark frequencies are defined in an individual step 16 bit wide register.

Table 24. FS AND FM STEP REGISTERS

ARM Register	Hard Reset	Soft Reset	Description
R_FS[15:0]	0000h	0000h	Step register for the space frequency f_S
R_FM[15:0]	0000h	0000h	Step register for the mark frequency f_M

The space and mark frequency can be calculated as:

- $f_S = R\_FS[15:0]\_dec \times f_{DDS}/2^{18}$
- $f_M = R\_FM[15:0]\_dec \times f_{DDS}/2^{18}$

Or the content of both R_FS[15:0] and R_FM[15:0] are defined as:

- $R\_FS[15:0]\_dec = Round(2^{18} \times f_S/f_{DDS})$
- $R\_FM[15:0]\_dec = Round(2^{18} \times f_M/f_{DDS})$

  Where f_{DDS} = 3 MHz is the direct digital synthesizer clock frequency.

After a hard or soft reset or at the start of the transmission (when TX_RXB goes from 0 to 1) the phase accumulator

must start at it's 0 phase position, corresponding with a 0 V output level. When switching between f_M and f_S the phase accumulator must give a continuous phase and not restart from phase 0.

When AMIS−49587 goes into receive mode (when TX_RXB goes from 1 to 0) the sine wave generator must make sure to complete the active sine period.

The control logic for the transmitter generates a signal TX_ENB to enable the external power amplifier. TX_ENB is 1 when the AMIS−49587 is in receive mode. TX_ENB is 0 when AMIS−49587 is in transmit mode. When going from transmit to receive mode (TX_RXB goes from 1 to 0) the TX_ENB signal is kept active for a short period of t_{dTX_ENB}.

The control logic for the transmitter generates a signal TX_DATA which corresponds to the transmitted S−FSK signal. When transmitting f_M TX_DATA is logic 1. When transmitting f_S TX_DATA is logic 0. When the transmitter is not enabled (TX_RXB = 0) TX_DATA goes to logic 1 at the next BIT_CLK.

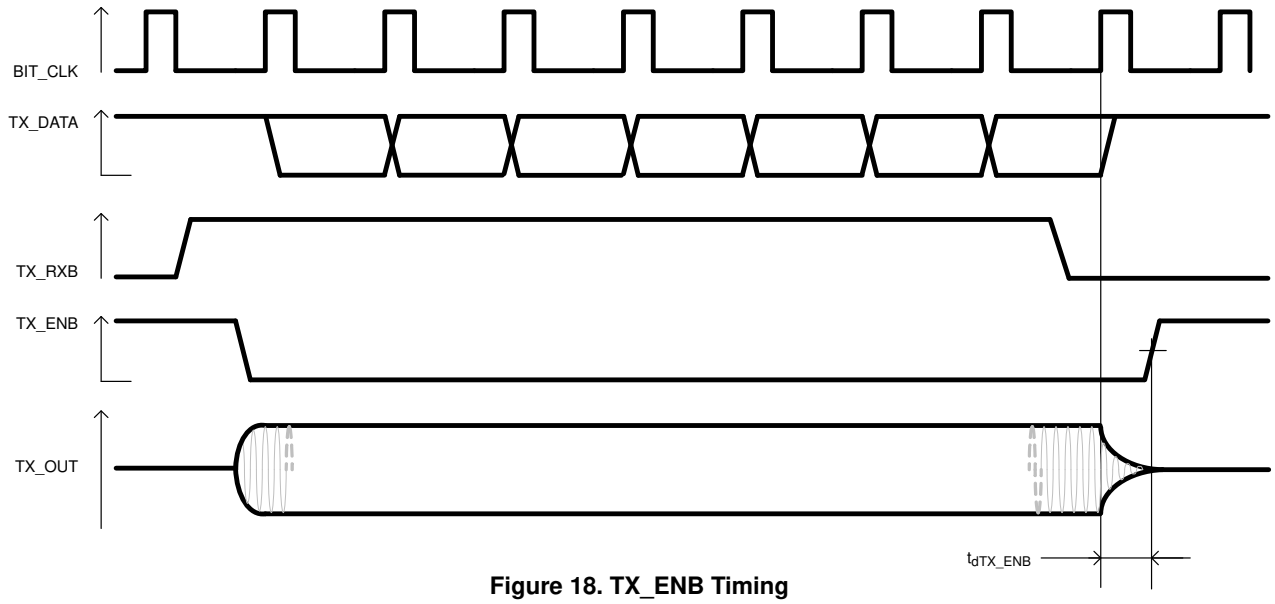


Figure 18. TX_ENB Timing

6.2.3 DA Converter

A digital to analog ΣΔ converter converts the sine wave digital word to a pulse density modulated (PDM) signal. The PDM signal is converted to an analog signal with a first order switched capacitor filter.

6.2.4 Low Pass Filter

A 3rd order continuous time low pass filter in the transmit path filters the quantization noise and noise generated by the ΣΔ DA converter. The low pass filter has a circuit which tunes the RC time constants of the filter towards the process characteristics. The C values for the LPF filter are controlled by the ARM micro controller.

6.2.5 Amplifier with Automatic Level Control (ALC)

The pin ALC_IN is used for level control of the transmitter output level. First a peak detection is done. The peak value is compared to 2 thresholds levels: VTL_{ALC_IN} and VTH_{ALC_IN}. The result of the peak detection is used to control the setting of the level of TX_OUT. The level of TX_OUT can be attenuated in 8 steps of 3 dB typical.

After hard or soft reset the level is set at minimum level (maximum attenuation) When going to reception mode (when TX_RXB goes from 1 to 0) the level is kept in memory so that the next transmit frame starts with the old level. The evaluation of the level is done during 1 CHIP_CLK period.

Depending on the value of peak level on ALC_IN the attenuation is updated:

- $Vp_{ALC\_IN} < VTL_{ALC}$: Increase the level with 1 step
- $VTL_{ALC} \leq Vp_{ALC\_IN} \leq VTH_{ALC}$: Don't change the level
- $Vp_{ALC\_IN} > VTH_{ALC}$: Decrease the level with 1 step

The gain changes in the next CHIP_CLK period.

An evaluation phase and a level adjustment takes 2 CHIP_CLK periods. ALC operation is enabled only during the first 16 CHIP_CLK cycles after a hard or soft reset or after going into transmit mode.

The automatic level control can be disabled by setting register R_ALC_CTRL[3] = 1. In this case the transmitter

output level is fixed to the programmed level in the register R_ALC_CTRL[2:0]. See also paragraph. WriteConfigRequest.

Table 25. FIXED TRANSMITTER OUTPUT ATTENUATION

ALC_CTRL[2:0]	Attenuation
000	0 dB
001	−3 dB
010	−6 dB
011	−9 dB
100	−12 dB
101	−15 dB
110	−18 dB
111	−21 dB

Remark: The analog part of AMIS−49587 works with an analogue ground REF_OUT. When connecting AMIS−49587 to external circuitry working with another ground one must make sure to place a decoupling capacitor.

6.3 RECEIVER PATH DESCRIPTION

6.3.1 Receiver Block Diagram

The receiver takes in the analog signal from the line coupler, conditions it and demodulates it in a data−stream to the communication controller. The operation mode and the baud rate are made according to the setting in R_CONF, R_FS and R_FM. The receive signal is applied first to a high pass filter. Therefore AMIS−49587 has a low noise operational amplifier at the input stage which can be used to make a high pass active filter to attenuate the mains frequency. This high pass filter output is followed by a gain stage which is used in an automatic gain control loop. This block also performs a single ended input to differential output conversion. This gain stage is followed by a continuous time low pass filter to limit the bandwidth. A 4^{th} order sigma delta converter converts the analog signal to digital samples. A quadrature demodulation for f_S and f_M is than performed by the ARM micro, as well the handling of the bits and the frames.

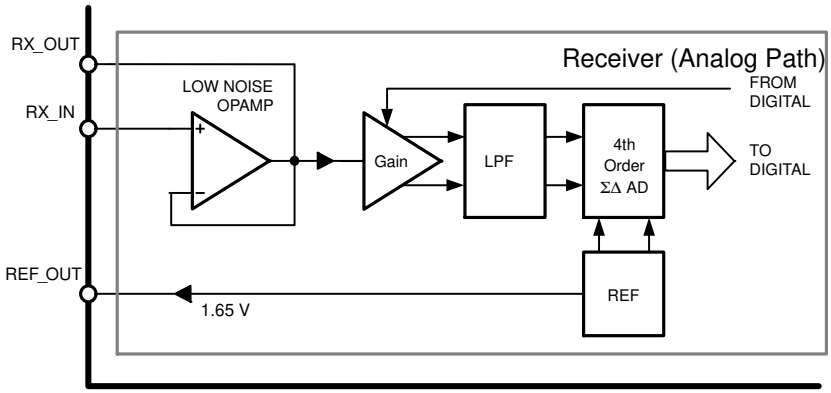


Figure 19. Analog Path of the Receiver

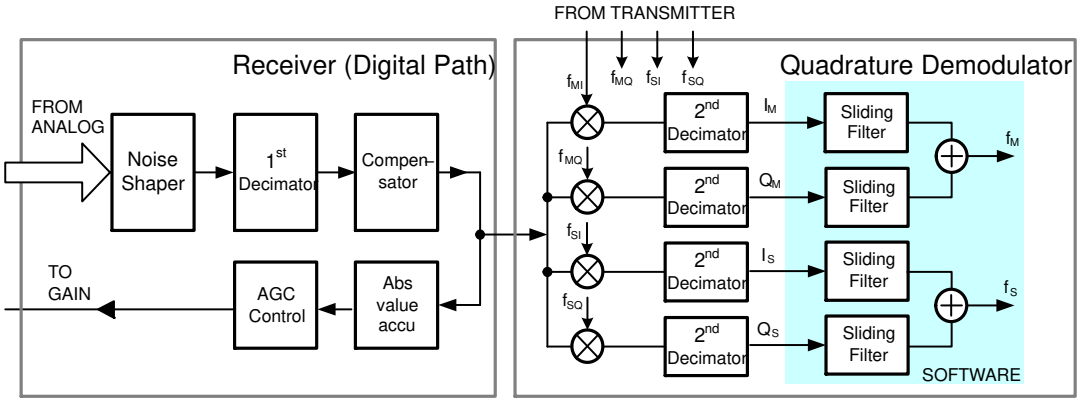


Figure 20. Digital Path of the Receiver ADC and Quadrature Demodulation