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AMMC-5040

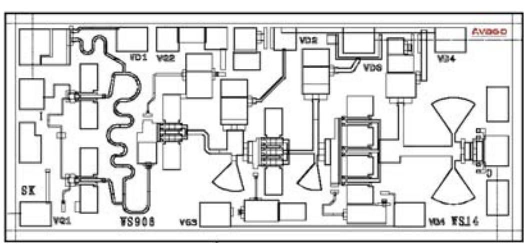
20 – 45 GHz GaAs Amplifier

Data Sheet

Description

The AMMC-5040 is a high gain broadband amplifier designed for both military applications and commercial communication systems. This four-stage amplifier has input and output matching circuitry for use in 50 ohm environments. It is fabricated using PHEMT integrated circuit structures that provide exceptional broadband performance. The backside of this chip is both RF and DC ground. This simplifies the assembly process and reduces assembly related performance variations and costs. For improved reliability and moisture protection, the die is passivated at the active areas. This MMIC is a cost effective alternative to hybrid (discrete-FET) amplifiers that require complex tuning and assembly process.

Package



Chip Size: 1720 x 760 µm (67.7 x 29.9 mils)
Chip Size Tolerance: ±10 µm (±0.4 mils)
Chip Thickness: 100 ± 10 µm (4 ± 0.4 mils)
Pad Dimensions: 75 x 75 µm (3 ± 0.4 mils)

Features

- Frequency range: 20 – 45 GHz
- High gain: 25 dB
- Gain flatness: ±1.5 dB
- Return loss:
  Input: 17 dB, Output: 11 dB
- Output power:
  P_{-1dB} = 21 dBm at 38 GHz
  P_{-3dB} = 22.5 dBm at 38 GHz

Applications

- Broadband gain block
- Broadband driver amplifier
- Point-to-point radio
- LMDS
- EW
- Instrumentation
- Frequency Multiplier (X2 and X3)

Absolute Maximum Ratings [1,2,3,4, 5]

Symbol	Parameters	Units	Minimum Values	Maximum Values	Notes
V_d-V_g	Drain to Gate Voltage	V		8	
V_d	Positive Supply Voltage [2]	V		5	
I_{DD}	Total Drain Current [2]	mA		550	2
V_g	Gate Supply Voltage	V	-3	0.5	
P_D	Power Dissipation [2,3]	W		2.09	2 and 3
P_{in}	CW Input Power [2]	dBm		21	2
T_{ch}	Operating Channel Temp [4,5]	°C		+150	4,5
T_{stg}	Storage Case Temp.	°C		-65 to +150	
T_{max}	Maximum Assembly Temp (30 sec max)	°C		+300	

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device. Functional operation at or near these limitations may significantly reduce the lifetime of the device.
2. Combinations of supply voltage, drain current, input power, and output power shall not exceed PD.
3. When operated at this condition with a base plate temperature of 85°C, the median time to failure (MTTF) is significantly reduced.
4. These ratings apply to each individual FET
5. The operating channel temperature will directly affect the device MTTF. For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

DC Specifications/Physical Properties [6]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
$V_{D1,2\text{-}3\text{-}4}$	Drain Supply Operating Voltage	V	2	4.5	5
I_{D1}	First Stage Drain Supply Current (V_{DD} = 4.5 V, V_{G1} = -0.5 V)	mA		50	
$I_{D2\text{-}3\text{-}4}$	Total Drain Supply Current for Stages 2, 3 and 4 (V_{DD} = 4.5 V, V_{GG}= -0.5 V)	mA		225	
$V_{G1,2\text{-}3\text{-}4}$	Gate Supply Operating Voltages (I_{DD} = 300 mA)	V		-0.45	
V_P	Pinch-off Voltage (V_{DD} = 4.5 V, I_{DD} < 10 mA)	V		-1.5	
$\theta_{ch\text{-}b}$	Thermal Resistance[2] (Channel-to-Backside)	°C/W		31	

Notes:

6. Measured in wafer form with T_{chuck} = 25°C (except $\theta_{ch\text{-}bs}$.)
7. Assume conductive epoxy to an evaluation RF board at 85°C base plate temperature.

Thermal Properties

Parameters	Test Conditions	Value
Maximum Power Dissipation	Tbaseplate = 85°C	P_D = 2.09W Tchannel = 150°C
Thermal Resistance (θjc)	Vd = 4.5V Idd = 300mA P_D = 1.35W Tbaseplate = 85°C	θjc = 31°C/W Tchannel = 126.85°C
Thermal Resistance (θjc) Under RF Drive	Vd = 4.5V Idd = 306mA Pout = 22dBm P_D = 1.25W Tbaseplate = 85°C	θjc = 31°C/W Tchannel = 123°C

RF Specifications [1,2] (V_{DD} = 4.5V, I_{DD} (Q) = 300 mA, Z_0 = 50Ω)

			Broadband		Narrow Band Typical Performance			
		Units	23–40		21–24	27–29	37–40	40–45
Symbol	**Parameters and Test Conditions**	**GHz**	**Min.**	**Typ.**	**Typical**			
$\|S_{21}\|^2$	Small-signal Gain	dB	20	25	25.5	25	22.4	21.3
$\Delta\|S_{21}\|^2$	Small-signal Gain Flatness	dB		±1.5	±0.2	±0.4	±0.2	±1.2
RL_{in}	Input Return Loss	dB	15	17	17	18	21	17
RL_{out}	Output Return Loss	dB	8	11	10	14	13	13
P_{-1dB}	Output Power @ 1 dB Gain Compression f = 22 GHz	dBm		20	20	22.5	21	20
P_{-3dB}	Output Power @ 3 dB Gain Compression, f = 22 GHz	dBm		21	21.6	23.5	22.5	21.5
OIP3	Output 3rd Order Intercept Point, Δf = 2 MHz, P_{in} = -8 dBm, f = 22 GHz	dBm		30	29	29	31	27
$\|S_{12}\|^2$	Isolation	dB	40	55	55	55	55	55

Notes:
1. Data measured in wafer form, T_{chuck} = 25°C.
2. 100% on-wafer RF test is done at frequency = 24, 27, 29, 37 and 40 GHz, except as noted.

AMMC-5040 Typical Performance (T_{chuck} = 25°C)

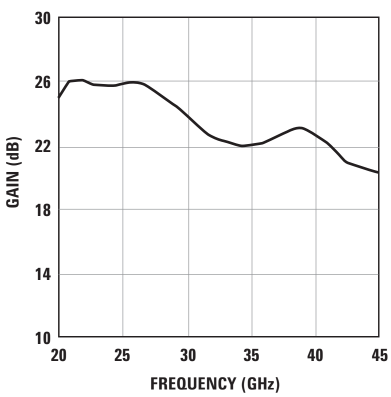


Figure 1. Gain, V_{DD}=4.5 V, I_{DD}=300 mA.

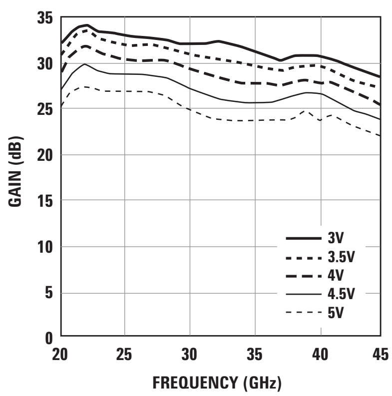


Figure 2. Gain and Drain Voltage, I_{DD}=300 mA.

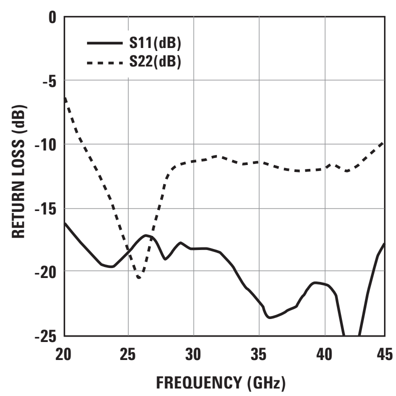


Figure 3. Input and Output Return Loss, V_{DD}=4.5V, I_{DD}=300 mA.

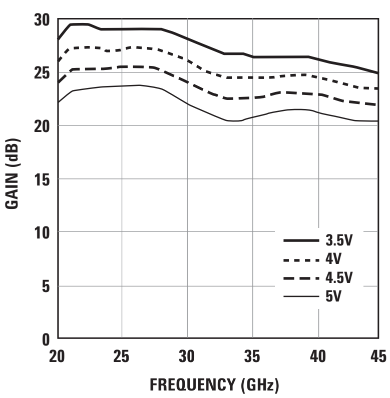


Figure 4. Gain and Drain Voltage, I_{DD}=350 mA.

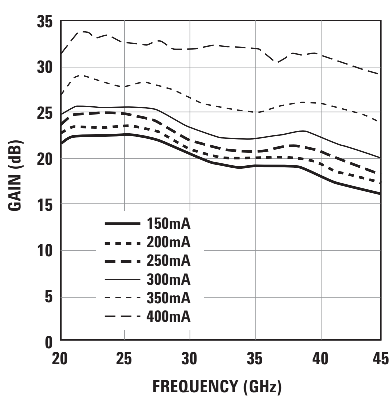


Figure 5. Gain and Drain Voltage, I_{DD}=4.5V.

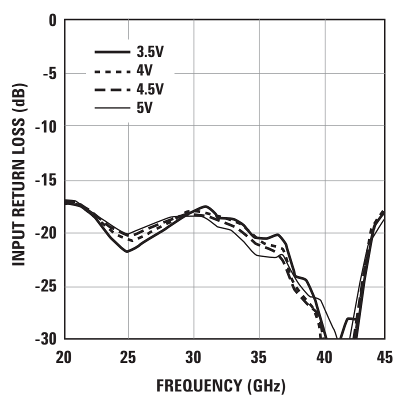


Figure 6. Input Return Loss and Drain Voltage, I_{DD}=350 mA.

AMMC-5040 Typical Performance (T_{chuck} = 25°C)

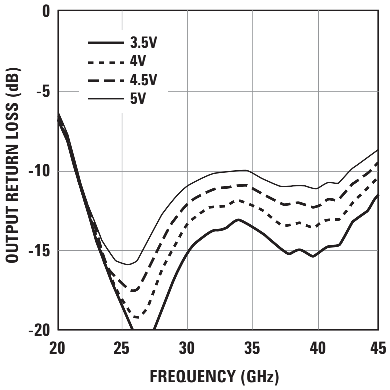


Figure 7. Output Return Loss and Drain Voltage, I_{DD}=350 mA.

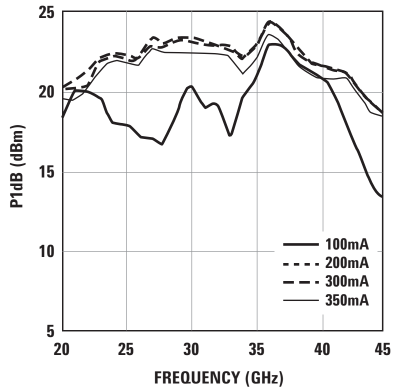


Figure 8. Output Power (P_{-1dB}) and Drain Current, V_{DD}=4.5V.

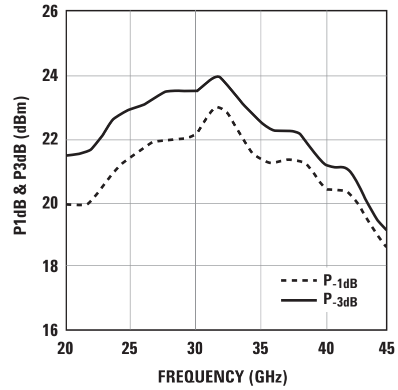


Figure 9. Output Power at P_{-1dB} and P_{-3dB}, V_{DD}=4.5V, I_{DD}=300 mA.

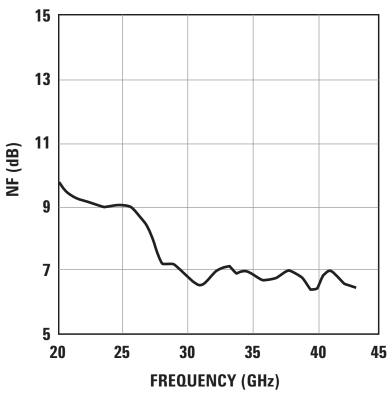


Figure 10. Noise Figure, V_{DD}=4.5V, I_{DD}=300 mA.

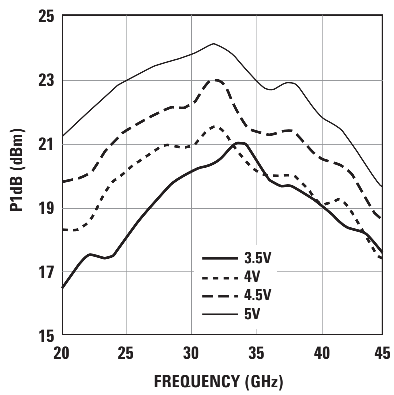


Figure 11. Output Power (P_{-1dB}) and Drain Voltage, I_{DD}=300 mA.

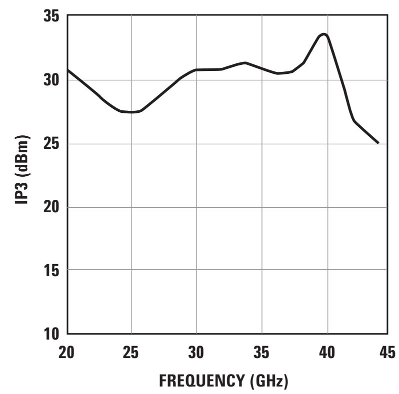


Figure 12. Output 3rd Order Intercept Point, V_{DD}=4.5V, I_{DD}=300 mA.

AMMC-5040 RF Performance for Frequency Multiplier Applications

Typical Performance as a X2 Frequency Multiplier, Input Power Optimized for Conversion Gain[1]

Input Frequency (GHz)	Input Power (dBm)	Output Frequency (GHz)	Output Power (dBm)	Conversion Gain (dB)
10	6	20	18.2	12.2
11	6	22	18.9	12.9
12	6.5	24	20.5	14.0
13	6.5	26	20.8	14.3
14	7.5	28	20.0	12.4
15	7.5	30	19.6	12.1
16	7.5	32	18.0	10.5
17	7.5	34	16.0	8.5
18	7	36	11.7	4.7
19	7	38	7.1	0.1
20	3	40	7.0	4.0
21	5	42	10.7	5.7
22	5	44	11.3	6.3
23	5	46	11.7	6.7

Typical Performance as a X2 Frequency Multiplier, Input Power Optimized for Output Power [1]

Input Frequency (GHz)	Input Power (dBm)	Output Frequency (GHz)	Output Power (dBm)	Conversion Gain (dB)
10	10	20	20.2	10.2
11	10	22	20.9	10.9
12	10	24	22.0	12.0
13	9.5	26	22.2	12.7
14	9.5	28	20.8	11.3
15	9.5	30	20.6	11.1
16	9.5	32	19.0	9.5

Typical Performance as a X3 Frequency Multiplier [1]

Input Frequency (GHz)	Input Power (dBm)	Output Frequency (GHz)	Output Power (dBm)	Conversion Gain (dB)
7	14.3	21	19.6	5.3
8	14.2	24	20.6	6.4
9	15.1	27	20.0	4.9
10	15.9	30	18.6	2.6
11	15.8	33	16.0	0.2
12	15.8	36	14.7	-1.0
13	15.7	39	12.9	-2.7
14	15.6	42	10.0	-5.5

Note:
1. T = 25°C. Refer to “Multiplier Biasing and Operation” section for bias conditions for operation as a multiplier.

AMMC-5040 Typical Scattering Parameters[1] (T_{chuck} = 25°C, V_{DD} = 4.5 V, I_{DD} = 300 mA, Z_{in} = Z_{out} = 50Ω)

Freq.		S_{11}			S_{21}			S_{12}			S_{22}	
GHz	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
2.045	-15.17	0.174	-11	-24.59	0.059	130	0.00	0.000	-94	-0.77	0.915	-28
3.045	-15.12	0.175	-21	-12.70	0.232	5	-119.33	0.000	-1	-1.30	0.861	-40
4.045	-16.33	0.153	-23	-7.42	0.425	-146	-79.88	0.000	-156	-2.55	0.746	-51
5.045	-15.91	0.160	-23	-23.80	0.065	89	-79.88	0.000	0	-2.26	0.771	-54
6.045	-15.32	0.171	-28	-20.96	0.090	104	-80.00	0.000	-62	-2.66	0.736	-65
7.045	-15.04	0.177	-36	-22.62	0.074	23	-80.00	0.000	-75	-2.93	0.714	-72
8.045	-15.02	0.177	-44	-32.63	0.023	0	-80.00	0.000	-5	-2.91	0.715	-81
9.045	-15.06	0.177	-51	-37.54	0.013	19	-79.72	0.000	-73	-3.10	0.700	-92
10.045	-15.13	0.175	-57	-40.69	0.009	6	-70.46	0.000	-109	-3.31	0.683	-102
11.045	-15.19	0.174	-64	-34.93	0.018	-113	-70.46	0.000	-127	-3.56	0.664	-112
12.045	-15.24	0.173	-71	-21.52	0.084	-154	-68.05	0.000	-148	-3.79	0.647	-123
13.045	-15.31	0.172	-79	-12.30	0.243	176	-67.96	0.000	-139	-3.97	0.633	-135
14.045	-15.36	0.171	-86	-4.87	0.571	146	-63.04	0.001	-147	-4.27	0.612	-148
15.045	-15.47	0.168	-94	1.65	1.209	115	-60.92	0.001	178	-4.55	0.592	-162
16.045	-15.59	0.166	-103	7.60	2.399	82	-60.05	0.001	170	-4.80	0.575	-178
17.045	-15.74	0.163	-111	13.18	4.562	45	-60.80	0.001	168	-5.01	0.562	162
18.045	-15.93	0.160	-120	18.42	8.337	3	-59.94	0.001	148	-5.25	0.546	135
19.045	-16.31	0.153	-129	22.92	14.001	-46	-59.17	0.001	142	-5.87	0.509	98
20.045	-16.82	0.141	-138	25.67	19.201	-101	-58.42	0.001	142	-7.80	0.407	51
21.045	-17.28	0.137	-149	26.62	21.432	-153	-56.52	0.001	131	-10.92	0.284	4
22.045	-18.39	0.120	-156	26.58	21.318	163	-56.43	0.002	129	-13.81	0.204	-35
23.045	-19.92	0.101	-159	26.44	20.994	125	-54.46	0.002	110	-16.17	0.155	-63
24.045	-20.37	0.096	-160	26.48	21.078	90	-54.90	0.002	101	-18.24	0.122	-80
25.045	-20.61	0.093	-160	26.46	21.031	56	-54.81	0.002	93	-20.03	0.100	-81
26.045	-20.03	0.100	-160	26.43	20.964	22	-55.44	0.002	73	-20.25	0.097	-74
27.045	-18.87	0.114	-156	25.97	19.873	-11	-54.43	0.002	67	-17.79	0.129	-67
28.045	-17.38	0.135	-168	25.38	18.579	-43	-56.89	0.001	54	-15.30	0.172	-73
29.045	-17.55	0.133	174	24.53	16.837	-72	-59.51	0.001	27	-13.65	0.208	-84
30.045	-18.15	0.124	164	23.74	15.384	-99	-66.02	0.001	39	-12.32	0.242	-98
31.045	-18.91	0.113	155	23.17	14.407	-124	-63.24	0.001	85	-11.70	0.260	-113
32.045	-20.15	0.098	148	22.75	13.721	-148	-62.96	0.001	92	-11.40	0.269	-127
33.045	-21.06	0.088	140	22.45	13.260	-174	-58.42	0.001	91	-11.95	0.253	-144
34.045	-22.94	0.071	144	22.15	12.814	164	-62.23	0.001	120	-12.75	0.231	-155
35.045	-24.74	0.058	143	22.16	12.819	141	-56.92	0.001	109	-13.59	0.209	-163
36.045	-27.27	0.043	160	22.51	13.343	117	-54.15	0.002	85	-13.86	0.203	-170
37.045	-24.62	0.059	176	22.99	14.110	90	-56.75	0.001	78	-13.87	0.203	177
38.045	-22.97	0.071	178	23.23	14.505	61	-54.49	0.002	73	-14.15	0.196	162
39.045	-22.55	0.075	168	22.94	14.022	31	-53.44	0.002	86	-15.02	0.177	146
40.045	-22.63	0.074	167	22.33	13.075	3	-51.15	0.003	68	-15.50	0.168	131
41.045	-24.00	0.063	164	21.78	12.275	-23	-52.29	0.002	63	-15.82	0.162	117
42.045	-25.45	0.053	168	21.48	11.861	-50	-51.10	0.003	54	-14.49	0.189	104
43.045	-27.06	0.044	-171	21.17	11.442	-78	-51.37	0.003	45	-12.76	0.230	84
44.045	-25.94	0.050	-139	20.75	10.907	-107	-51.37	0.003	43	-11.21	0.275	63
45.045	-22.48	0.075	-123	20.32	10.371	-136	-51.99	0.003	41	-9.70	0.327	44
46.045	-20.26	0.097	-112	19.51	9.453	-166	-49.59	0.003	22	-8.14	0.392	24
47.045	-15.70	0.164	-103	19.00	8.917	165	-50.75	0.003	18	-7.25	0.434	7
48.045	-11.42	0.269	-106	18.44	8.355	134	-53.08	0.002	17	-6.43	0.477	-8
49.045	-7.83	0.406	-113	17.70	7.677	101	-54.51	0.002	6	-5.73	0.517	-22
50.000	-4.72	0.581	-124	16.85	6.955	69	-54.43	0.002	13	-5.20	0.550	-34

Note:

1. Data obtained from on-wafer measurements.

AMMC-5040 Typical Scattering Parameters[1] (T_{chuck} = 25°C, V_{DD} = 4.5 V, I_{DD} = 350 mA, Z_{in} = Z_{out} = 50Ω)

Freq.	S_{11}			S_{21}			S_{12}			S_{22}		
GHz	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang
17.045	-15.90	0.160	-111	13.73	4.857	45	-61.03	0.001	168	-4.89	0.569	162
18.045	-16.10	0.157	-120	19.07	8.981	3	-59.90	0.001	148	-4.99	0.565	135
19.045	-16.50	0.150	-129	23.92	15.696	-46	-59.17	0.001	142	-5.06	0.558	98
20.045	-17.08	0.140	-138	27.37	23.362	-101	-59.17	0.001	142	-6.08	0.496	51
21.045	-17.41	0.135	-149	28.96	28.054	-153	-57.08	0.001	131	-8.51	0.375	4
22.045	-18.78	0.115	-156	29.01	28.221	163	-56.48	0.002	129	-11.29	0.273	-35
23.045	-20.82	0.091	-159	28.73	27.316	125	-54.47	0.002	110	-13.84	0.203	-63
24.045	-21.45	0.085	-160	28.65	27.069	90	-54.94	0.002	101	-16.02	0.158	-80
25.045	-21.92	0.080	-160	28.56	26.789	56	-54.94	0.002	93	-18.15	0.124	-81
26.045	-21.45	0.085	-160	28.55	26.759	22	-55.35	0.002	73	-19.22	0.109	-74
27.045	-20.21	0.098	-156	28.13	25.497	-11	-54.46	0.002	67	-17.68	0.131	-67
28.045	-18.06	0.125	-168	27.69	24.224	-43	-57.03	0.001	54	-15.15	0.175	-73
29.045	-17.86	0.128	174	26.95	22.266	-72	-58.31	0.001	27	-13.32	0.216	-84
30.045	-18.39	0.120	164	26.21	20.450	-99	-67.65	0.000	39	-11.78	0.258	-98
31.045	-19.04	0.112	155	25.65	19.164	-124	-63.27	0.001	85	-11.03	0.281	-113
32.045	-20.32	0.096	148	25.17	18.142	-148	-63.18	0.001	92	-10.68	0.293	-127
33.045	-21.10	0.088	140	24.88	17.541	-174	-59.22	0.001	91	-11.06	0.280	-144
34.045	-23.60	0.066	144	24.53	16.846	164	-62.19	0.001	120	-11.85	0.256	-155
35.045	-25.31	0.054	143	24.49	16.767	141	-57.76	0.001	109	-12.74	0.231	-163
36.045	-30.41	0.030	160	24.81	17.394	117	-54.43	0.002	85	-13.14	0.220	-170
37.045	-27.92	0.040	176	25.38	18.567	90	-57.60	0.001	78	-13.17	0.220	177
38.045	-25.80	0.051	178	25.75	19.376	61	-55.00	0.002	73	-13.64	0.208	162
39.045	-24.94	0.057	168	25.56	18.956	31	-54.00	0.002	86	-14.93	0.179	146
40.045	-25.03	0.056	167	25.03	17.850	3	-51.42	0.003	68	-15.86	0.161	131
41.045	-26.05	0.050	164	24.59	16.970	-23	-52.75	0.002	63	-16.32	0.153	117
42.045	-27.13	0.044	168	24.45	16.696	-50	-51.37	0.003	54	-14.81	0.182	104
43.045	-29.59	0.033	-171	24.29	16.386	-78	-51.37	0.003	45	-13.01	0.224	84
44.045	-29.99	0.032	-139	24.07	15.984	-107	-51.39	0.003	43	-11.47	0.267	63
45.045	-26.40	0.048	-123	23.89	15.652	-136	-52.38	0.002	41	-9.86	0.322	44
46.045	-24.89	0.057	-112	23.32	14.648	-166	-49.39	0.003	22	-7.99	0.398	24
47.045	-18.50	0.119	-103	23.14	14.361	165	-50.47	0.003	18	-7.07	0.443	7
48.045	-13.21	0.219	-106	22.81	13.814	134	-52.77	0.002	17	-6.17	0.492	-8
49.045	-9.10	0.351	-113	22.15	12.804	101	-53.15	0.002	6	-5.41	0.537	-22
50.000	-5.48	0.532	-124	21.30	11.608	69	-55.92	0.002	13	-4.88	0.570	-34

Note:
1. Data obtained from on-wafer measurements.

Biasing and Operation

The recommended DC bias condition for the AMMC-5040 is with all four drains connected to a single 4.5V supply and all four gates connected to an adjustable negative voltage supply as shown in Figure 15. The gate voltage is adjusted for a total drain supply current of typically 300 mA. Figures 1–12 can be used to help estimate the minimum drain voltage and current necessary for a given RF gain and output power.

As shown in Figure 13, the second, third, and fourth stage DC drain bias lines are connected internally and therefore require only a single bond wire. An additional bond wire is needed for the first stage DC drain bias, Vd1.

Only the third and fourth stage DC gate bias lines are connected internally. A total of three DC gate bond wires are required: one for Vg1, one for Vg2, and one for the Vg3/Vg4 connection. The internal matching circuitry at the RF input creates a 50-ohm DC and RF path to ground. A blocking capacitor should be used at the RF input. Any DC voltage applied to the RF input must be maintained below 1V. The RF output is AC coupled. No ground bond wires are needed since the ground connection is made by means of plated through via holes to the backside of the chip.

Frequency Multiplier Biasing and Operation

The AMMC-5040 can also be used as a frequency doubler, tripler or quadrupler.

As a frequency doubler, the AMMC-5040 provides conversion gain for input signals in the 10–23 GHz frequency range for output frequencies of 20–46 GHz. Similarly, 5–10 GHz signals can be quadrupled up to 20–40 GHz with some conversion loss.

Optimum conversion efficiency as a doubler is obtained with an input power level of 3–8 dBm. For use as a frequency tripler, an input power level of 14–16 dBm is recommended.

Frequency multiplication is achieved by reducing the bias on the first stage FET to efficiently generate harmonics. The remaining three stages are then used to provide amplification.

While many bias schemes may be used to generate and amplify the desired harmonics within the AMMC-5040, the following information is suggested as a starting point for multiplier applications.

Frequency doubling or quadrupling (generation of even harmonics) is accomplished by biasing the first stage FET at pinch-off by setting Vg1 = Vp ≈ -1.1 volts. The remaining three stages are biased for normal amplification, e.g., Vgg is adjusted such that Id2 + Id3 + Id4 ≈ 250 mA. The drain voltage, Vdd, for all four stages should be 3.5 – 4.5 volts. The assembly diagram shown in Figure 16 can be used as a guideline.

To operate the AMMC-5040 as a frequency tripler (odd harmonic), the device is biased as shown in Figure 17. The drain voltage for the first stage FET is biased separately with Vd1 reduced to 1.1 - 1.2 volts. The drain voltage for the remaining three stages, Vd2, Vd3, and Vd4, should be 3.5 - 4.5 volts. All four gate voltages, Vgg, are set to approximately –0.6 volts. If desired, Vgg can be adjusted to minimize second harmonics. Improved multiplier performance can be obtained by biasing both the gate and drain voltages for the first stage separately from stages 2–4.

In all cases, Cb > 100 nF to assure stability.

Assembly Techniques

The chip should be attached directly to the ground plane using electrically conductive epoxy [1]. For conductive epoxy, the amount should be just enough to provide a thin fillet around the bottom perimeter of the die. The ground plane should be free of any residue that may jeopardize electrical or mechanical attachment. Caution should be taken to not exceed the Absolute Maximum Rating for assembly temperature and time.

Thermo-sonic wedge bonding is the preferred method for wire attachment to the bond pads. The RF connections should be kept as short as possible to minimize inductance. 0.7mil gold wire is recommended. The recommended wire bonding stage temperature is 150±2˚C.

The chip is 100µm thick and should be handled with care.

This MMIC has exposed air bridges on the top surface. Handle at the edges or with a custom collet (do not pick up die with vacuum on die center).

This MMIC is also static sensitive and ESD handling precautions should be taken.

For more detailed information, see Avago Application Note 54 "GaAs MMIC ESD, Die Attach and Bonding Guide lines."

Notes:
1. Sumitomo 1295SA silver epoxy is recommended.
2. Eutectic attach is not recommended and may jeopardize reliability of the device.

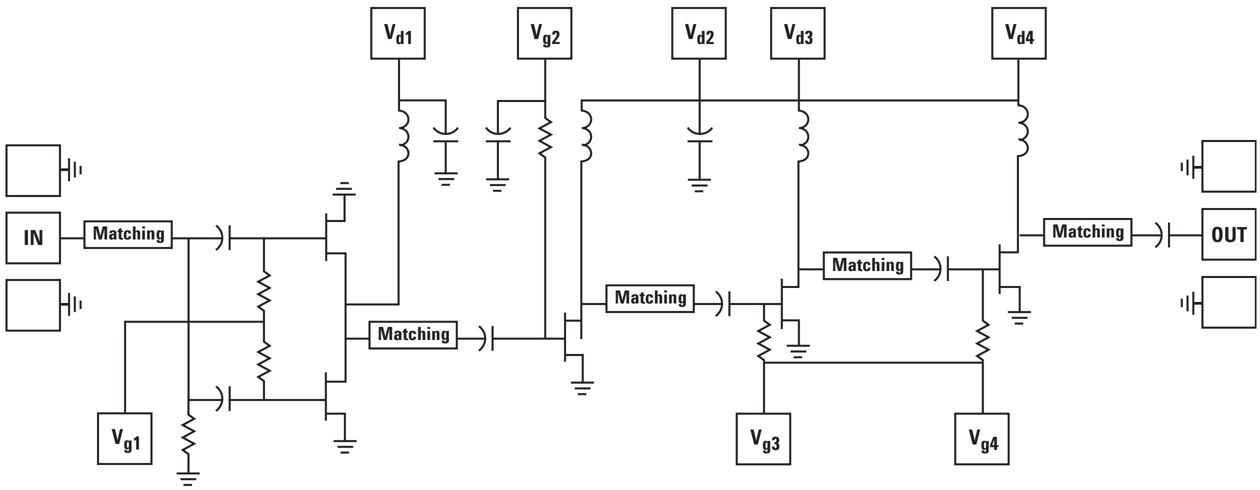


Figure 13. AMMC-5040 Simplified Schematic Diagram.

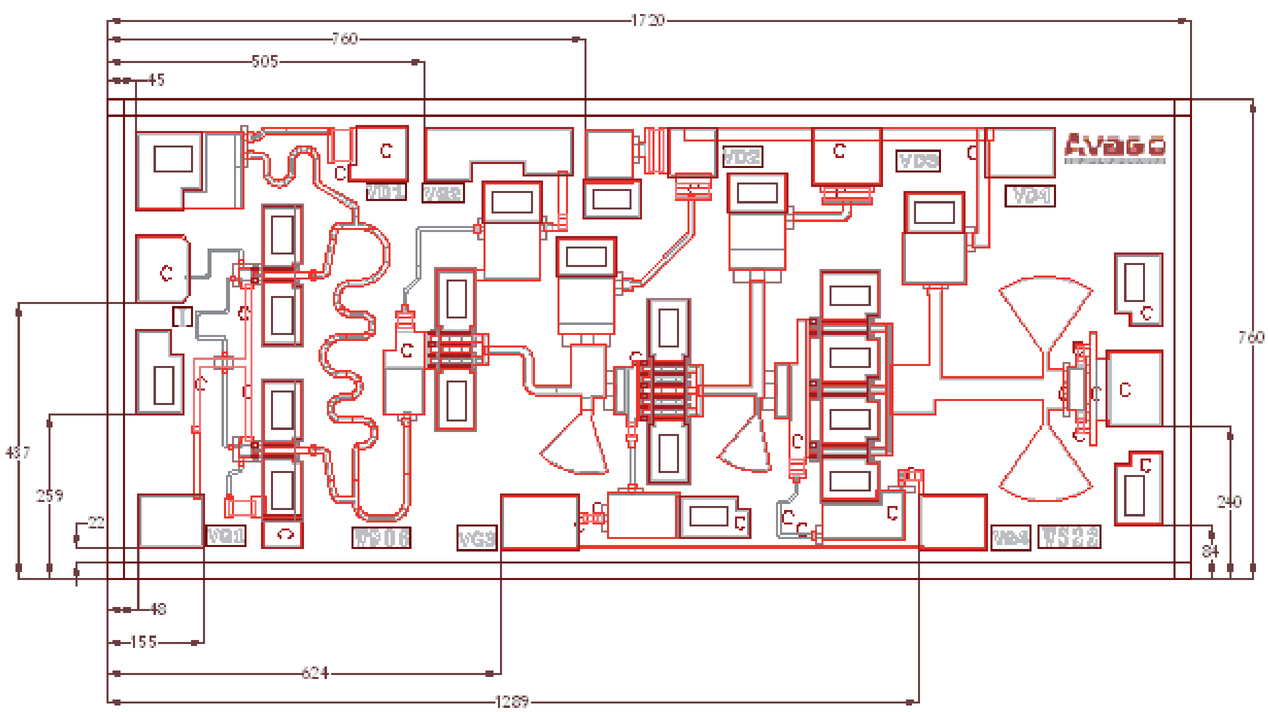


Figure 14. AMMC-5040 Bonding Pad Locations (dimensions in microns).

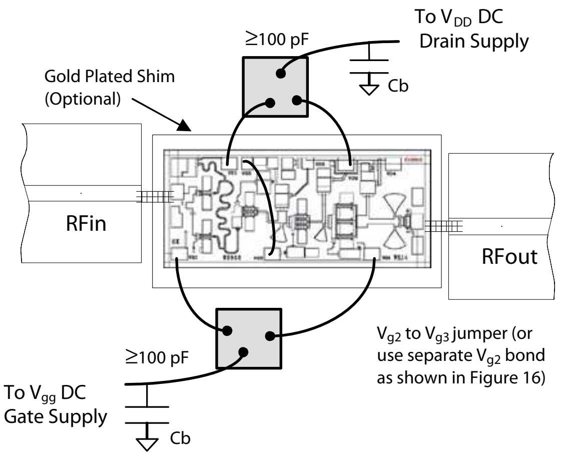


Figure 15. AMMC-5040 assembly for normal amplifier applications with single drain and single gate supply connections.

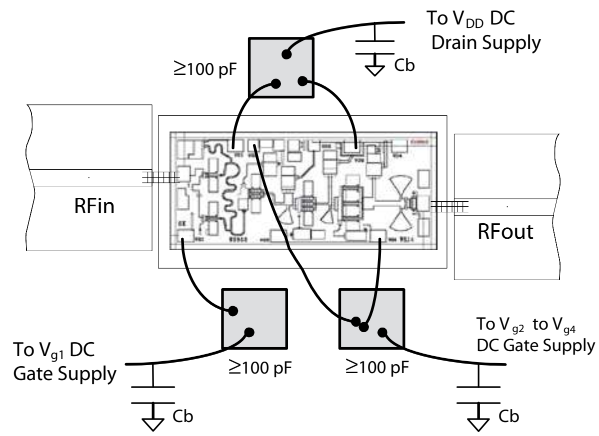


Figure 16. Separate first-stage gate bias for using the AMMC-5040 as a frequency doubler or quadrupler. This diagram also shows an option to the Vg_2 jumper bonding scheme used in Figure 15.

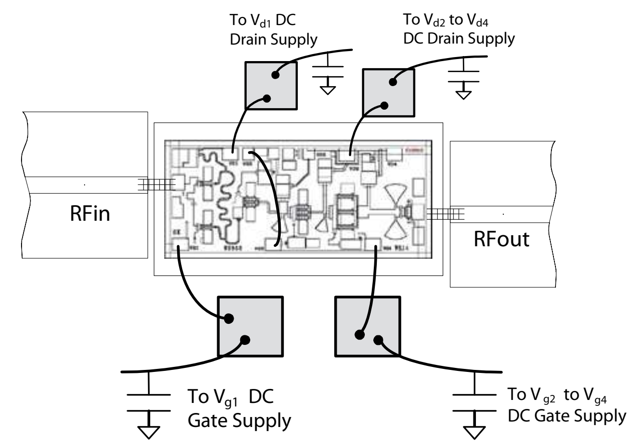


Figure 17. Separate first-stage gate and drain bias for using the AMMC-5040 as a frequency tripler.

Ordering Information

AMMC-5040-W10 = 10 devices per tray

AMMC-5040-W50 = 50 devices per tray

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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