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## $7 \times 7$ Dots Matrix LED Driver LSI

## FEATURES

- $7 \times 7$ LED Matrix Driver
(Total LED that can be driven $=49$ )
- Built-in memory (ROM, RAM)
- LDO : 2-ch
- SPI interface : 1-ch
- LED driver for RGB: 1-ch
- 35 pin Wafer Level Chip Size Package (WLCSP)


## DESCRIPTION

AN32051A is a 49 Dots Matrix LED Driver. It can drive up to 16 RGB LEDs.

## APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.


## TYPICAL APPLICATION



Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

## Panasonic

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ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit | Note |
| :---: | :---: | :---: | :---: | :---: |
| Supply voltage | $\mathrm{VB}_{\text {MAX }}$ | 6.0 | V | *1 |
|  | VLED ${ }_{\text {MAX }}$ | 6.5 | V | *1 |
| Operating ambience temperature | $\mathrm{T}_{\text {opr }}$ | -30 to +85 | ${ }^{\circ} \mathrm{C}$ | *2 |
| Operating junction temperature | $\mathrm{T}_{\mathrm{j}}$ | -30 to +125 | ${ }^{\circ} \mathrm{C}$ | *2 |
| Storage temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ | *2 |
| Input Voltage Range | LEDCTL, RSTB, CE, CLK, DI | -0.3 to 3.4 | V | - |
|  | LDOCNT | -0.3 to 6.0 | V | - |
| Output Voltage Range | INT, DO | -0.3 to 3.4 | V | - |
|  | $\begin{gathered} \mathrm{R}, \mathrm{G}, \mathrm{~B} \\ \mathrm{LDO} 1, \mathrm{LDO}, \\ \mathrm{X} 0, \mathrm{X} 1, \mathrm{X} 2, \mathrm{X} 3, \mathrm{X} 4, \mathrm{X} 5, \mathrm{X} 6, \\ \mathrm{Y} 0, \mathrm{Y} 1, \mathrm{Y} 2, \mathrm{Y} 3, \mathrm{Y} 4, \mathrm{Y} 5, \mathrm{Y} 6 \end{gathered}$ | -0.3 to 6.5 | V | - |
| ESD | HBM | 2.0 | kV | - |

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1: $V^{\text {MAX }}=V B, V_{L E D}$ MAX $=V L E D$.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
${ }^{*} 2$ : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C}$.

## POWER DISSIPATION RATING

| PACKAGE | $\theta_{\mathrm{JA}}$ | $\mathbf{P}_{\mathrm{D}}\left(\mathbf{T a}=\mathbf{2 5}{ }^{\circ} \mathrm{C}\right)$ | $\mathbf{P}_{\mathrm{D}}\left(\mathbf{T a}=\mathbf{8 5}{ }^{\circ} \mathbf{C}\right)$ |
| :---: | :---: | :---: | :---: |
| 35 pin Wafer Level Chip Size Package (WLCSP) | $141.5^{\circ} \mathrm{C} / \mathrm{W}$ | 0.706 W | 0.304 W |

Note) For the actual usage, please refer to the $P_{D}-$ Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

## CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

AN32051A

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply voltage range | VB | 3.1 | 3.7 | 4.6 | V | *1 |
|  | VLED | 3.1 | 5.0 | 5.6 | V | *1 |
| Input Voltage Range | LEDCTL, RSTB, CE, CLK, DI | -0.3 | - | 3.0 | V | - |
|  | LDOCNT | -0.3 | - | $V B+0.3$ | V | *2 |
| Output Voltage Range | INT, DO | -0.3 | - | 3.0 | V | - |
|  | $\begin{gathered} \mathrm{R}, \mathrm{G}, \mathrm{~B} \\ \mathrm{LDO} 1, \mathrm{LDO} 2 \\ \mathrm{X} 0, \mathrm{X} 1, \mathrm{X} 2, \mathrm{X} 3, \mathrm{X} 4, \mathrm{X} 5, \mathrm{X} 6, \\ \mathrm{Y} 0, \mathrm{Y} 1, \mathrm{Y} 2, \mathrm{Y} 3, \mathrm{Y} 4, \mathrm{Y} 5, \mathrm{Y} 6 \end{gathered}$ | -0.3 | - | VLED + 0.3 | V | *2 |

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, RGBGND and PGND.
VB is voltage for VB. VLED is voltage for VLED1 and VLED2.
*2: ( $V B+0.3$ ) $V$ must not exceed 6 V . ( $V L E D+0.3$ ) $V$ must not exceed 6.5 V .

## ELECTRICAL CHARACTERISTICS

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Current consumption |  |  |  |  |  |  |  |
| Current consumption (1) | ICC1 | At OFF mode LDOCNT = Low | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| Current consumption (2) | ICC2 | At Standby mode LDOCNT = Low LDO2 is active. | - | 8 | 12 | $\mu \mathrm{A}$ | - |
| Current consumption (3) | ICC3 | LDOCNT = High <br> LDO1 and LDO2 are active. | - | 18 | 24 | $\mu \mathrm{A}$ | - |
| Reference voltage |  |  |  |  |  |  |  |
| Output voltage | VREF | $\mathrm{I}_{\text {VREF }}=0 \mu \mathrm{~A}$ | 1.22 | 1.25 | 1.28 | V | - |
| Reference current |  |  |  |  |  |  |  |
| Output voltage | VIREF | $\mathrm{I}_{\text {REF }}=0 \mu \mathrm{~A}$ | 0.44 | 0.54 | 0.64 | V | - |
| Voltage regulator (LDO1) |  |  |  |  |  |  |  |
| Output voltage | VL1 | $\mathrm{I}_{\text {LDO } 1}=-30 \mathrm{~mA}$ | 1.79 | 1.85 | 1.91 | V | - |
| Short circuit protection current | IPT1 | $\begin{aligned} & \text { LDOCNT }=\text { High } \\ & \text { REG18 }=\text { High } \\ & \mathrm{V}_{\mathrm{LDO1}}=0 \mathrm{~V}, \mathrm{IPT} 1=\mathrm{I}_{\mathrm{LDO} 1} \end{aligned}$ | 50 | 100 | 200 | mA | - |
| Ripple rejection (1) | PSL11 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=1 \mathrm{kHz} \\ & \mathrm{l}_{\mathrm{LDO} 1}=-15 \mathrm{~mA} \\ & \mathrm{PSL} 11=20 \log \left(\mathrm{acV}_{\mathrm{LDO} 1} / 0.2\right) \end{aligned}$ | - | -45 | -40 | dB | - |
| Ripple rejection (2) | PSL12 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=10 \mathrm{kHz} \\ & \mathrm{l}_{\mathrm{LDO} 1}=-15 \mathrm{~mA} \\ & \text { PSL12 }=20 \log \left(\mathrm{ac}_{\mathrm{LDO} 1} / 0.2\right) \end{aligned}$ | - | -35 | -25 | dB | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Voltage regulator (LDO2) |  |  |  |  |  |  |  |
| Output voltage | VL2 | $\mathrm{I}_{\text {LDO2 }}=-30 \mathrm{~mA}$ | 2.76 | 2.85 | 2.94 | V | - |
| Short circuit protection current | IPT2 | $\begin{aligned} & \text { LDOCNT }=\text { High } \\ & V_{\text {LDO2 }}=0 \mathrm{~V} \\ & \text { IPT2 }=I_{\text {LDO2 }} \end{aligned}$ | 50 | 100 | 300 | mA | - |
| Ripple rejection (1) | PSL21 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=1 \mathrm{kHz} \\ & \mathrm{I}_{\mathrm{LDO2}}=-15 \mathrm{~mA} \\ & \mathrm{PSL} 21=20 \log \left(\mathrm{acV}_{\mathrm{LDO2}} / 0.2\right) \end{aligned}$ | - | -40 | -30 | dB | - |
| Ripple rejection (2) | PSL22 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=10 \mathrm{kHz} \\ & \mathrm{l}_{\mathrm{LDO2}}=-15 \mathrm{~mA} \\ & \mathrm{PSL} 22=20 \log \left(\mathrm{acV}_{\mathrm{LDO} 2} / 0.2\right) \end{aligned}$ | - | -25 | -15 | dB | - |
| Oscillator |  |  |  |  |  |  |  |
| Oscillation frequency | FDC | - | 0.96 | 1.20 | 1.44 | MHz | - |
| SCAN Switch |  |  |  |  |  |  |  |
| Resistance at the Switch ON | RSCAN | $\mathrm{I}_{\mathrm{YO}, \mathrm{Y} 1, \mathrm{Y} 2, Y 3, Y 4, Y 5, Y 6}=5 \mathrm{~mA}$ RSCAN $=\mathrm{V}_{\mathrm{YO}, \mathrm{Y} 1, \mathrm{Y} 2, \mathrm{Y} 3, Y 4, \mathrm{Y}_{5}, \mathrm{Y} 6} / 5 \mathrm{~mA}$ | - | 2 | 4.8 | $\Omega$ | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Current generator (For $7 \times 7$ dots matrix LED) |  |  |  |  |  |  |  |
| Output current (1) | IMX1 | At 1 mA setup $\begin{aligned} & V_{\mathrm{x0}, \mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3, \mathrm{x} 4, \mathrm{x} 5, \mathrm{x} 6}=1 \mathrm{~V} \\ & \mathrm{IMX1}=I_{\mathrm{x} 0}, \mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3, \mathrm{x} 4, \mathrm{x} 5, \mathrm{x} 6 \end{aligned}$ | 0.952 | 1.035 | 1.118 | mA | *1 |
| Output current (2) | IMX2 | At 2 mA setup $\begin{aligned} & V_{\mathrm{x0}, \mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3, \mathrm{x} 4, \mathrm{x} 5, \mathrm{x} 6}=1 \mathrm{~V} \\ & \mathrm{IMX2}=I_{\mathrm{x} 0, \mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3, \mathrm{x} 4, \mathrm{x} 5, \mathrm{x} 6} \end{aligned}$ | 1.923 | 2.090 | 2.258 | mA | *1 |
| Output current (3) | IMX4 | At 4 mA setup $\begin{aligned} & V_{x 0, x 1, x 2, x 3, x 4, x 5, x 6}=1 \mathrm{~V} \\ & \mathrm{IMX4}=I_{\mathrm{x} 0, \mathrm{x} 1, x 2, x 3, x 4, x 5, x 6} \end{aligned}$ | 3.843 | 4.177 | 4.512 | mA | *1 |
| Output current (4) | IMX8 | At 8 mA setup | 7.692 | 8.361 | 9.030 | mA | *1 |
| Output current (5) | IMX15 | At 15 mA setup | 14.399 | 15.651 | 16.903 | mA | *1 |
| Leakage Current when matrix LED turns off | IMXOFF | Current OFF setup $\begin{aligned} & V_{\mathrm{x} 0, \mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3, \mathrm{x} 4, \mathrm{x}, \mathrm{x} 6}=4.75 \mathrm{~V} \\ & \mathrm{IMXOFF}=I_{\mathrm{x} 0, \mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3, \mathrm{x} 4, \mathrm{x} 5, \mathrm{x} 6} \end{aligned}$ | - | - | 1 | $\mu \mathrm{A}$ | - |
| The error between channels | IMXCH | The average value of all channels, and the current error of each channel | -5 | - | 5 | \% | - |

*1: Values when recommended parts (ERJ2RHD273X) are used for IREF terminal. The other current settings are combination of above items.

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Current generator (For RGB color unit) |  |  |  |  |  |  |  |
| Output current (1) | IRGB1 | At 1 mA setup $V_{R, G, B}=1 \mathrm{~V}$ | 0.949 | 1.031 | 1.114 | mA | *1 |
| Output current (2) | IRGB2 | At 2 mA setup $V_{R, G, B}=1 \mathrm{~V}$ | 1.901 | 2.066 | 2.231 | mA | *1 |
| Output current (3) | IRGB4 | At 4 mA setup $V_{R, G, B}=1 \mathrm{~V}$ | 3.781 | 4.110 | 4.438 | mA | *1 |
| Output current (4) | IRGB8 | At 8 mA setup $V_{R, G, B}=1 \mathrm{~V}$ | 7.554 | 8.210 | 8.867 | mA | *1 |
| Leakage Current when RGB turn off | IRGBOFF | Current OFF setup $\begin{aligned} & \mathrm{V}_{\mathrm{R}, \mathrm{G}, \mathrm{~B}}=4.75 \mathrm{~V} \\ & \mathrm{IRGBOFF}=\mathrm{I}_{\mathrm{R}, \mathrm{G}, \mathrm{~B}} \end{aligned}$ | - | - | 1 | $\mu \mathrm{A}$ | - |
| The error between channels | IRGBCH | The average value of all channels, and the current error of each channel | -5 | - | 5 | \% | - |

*1: Values when recommended parts (ERJ2RHD273X) are used for IREF terminal.
The other current settings are combination of above items.

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| SPI I/F, LEDCTL, RSTB |  |  |  |  |  |  |  |
| Input voltage range of Highlevel | VIH | High-level recognition voltage | 1.38 | - | $\begin{aligned} & \text { LDO2 } \\ & +0.3 \end{aligned}$ | V | - |
| Input voltage range of Lowlevel | VIL | Low-level recognition voltage | -0.3 | - | 0.4 | V | - |
| Input current of High-level | IIH | $\mathrm{V}_{\text {LEDCTL, }}$ RSTB, CE, CLK, DI $=1.85 \mathrm{~V}$ <br> IIH $=I_{\text {LEDCTL }}$, RSTB, CE, CLK, DI | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| Input current of Low-level | IIL | $\begin{aligned} & V_{\text {LEDCTL, RSTB, CSB, CLK, DI }}=0 \mathrm{~V} \\ & \text { IIL }=I_{\text {LEDCTL, }} \text { RSTB, CE, CLK, DI } \\ & \hline \end{aligned}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| INT |  |  |  |  |  |  |  |
| Output voltage of High-level (1) | VOH1 | $\begin{aligned} & \mathrm{l}_{\mathrm{INT}}=-2 \mathrm{~mA} \\ & \text { VDDSEL }=\mathrm{LDO} 2 \end{aligned}$ | $\begin{gathered} \mathrm{LDO} 2 \\ \times 0.8 \end{gathered}$ | - | - | V | - |
| Output voltage of Low-level (1) | VOL1 | $\begin{aligned} & \mathrm{I}_{\mathrm{INT}}=2 \mathrm{~mA} \\ & \mathrm{VDDSEL}=\mathrm{LDO} 2 \\ & \left(\mathrm{I}_{\mathrm{INT}}=0.5 \mathrm{~mA}\right) \end{aligned}$ | - | - | $\begin{gathered} \mathrm{LDO} 2 \\ \times 0.2 \end{gathered}$ | V | - |
| Output voltage of High-level (2) | VOH2 | $\begin{aligned} & \mathrm{l}_{\mathrm{INT}}=-2 \mathrm{~mA} \\ & \mathrm{VDDSEL}=\mathrm{LDO} \end{aligned}$ | $\begin{gathered} \text { LDO1 } \\ \times 0.8 \end{gathered}$ | - | - | V | - |
| Output voltage of Low-level (2) | VOL2 | $\begin{aligned} & \mathrm{I}_{\mathrm{INT}}=2 \mathrm{~mA} \\ & \mathrm{VDDSEL}=\mathrm{LDO} 1 \\ & \left(\mathrm{I}_{\mathrm{INT}}=0.5 \mathrm{~mA}\right) \end{aligned}$ | - | - | $\begin{gathered} \text { LDO1 } \\ \times 0.3 \end{gathered}$ | V | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| LDOCNT |  |  |  |  |  |  |  |
| Input voltage range of High-level | VIH | High-level recognition voltage | $\begin{gathered} \text { VB } \\ \times 0.7 \end{gathered}$ | - | $\begin{gathered} \text { VB } \\ +0.3 \end{gathered}$ | V | - |
| Input voltage range of Low-level | VIL | Low-level recognition voltage | -0.3 | - | 0.4 | V | - |
| Input current of High-level | IIH | $\begin{aligned} & \mathrm{V}_{\text {LDOCNT }}=3.6 \mathrm{~V} \\ & \mathrm{IIH}=\mathrm{I}_{\text {LDOCNT }} \end{aligned}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| Input current of Low-level | IIL | $\begin{aligned} & \mathrm{V}_{\text {LDOCNT }}=0 \mathrm{~V} \\ & \text { IIL }=\mathrm{I}_{\text {LDOCNT }} \end{aligned}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| DO |  |  |  |  |  |  |  |
| Output voltage of High-level | VOH | $\mathrm{I}_{\mathrm{DO}}=-2 \mathrm{~mA}$ | $\begin{gathered} \text { LDO1 } \\ \times 0.8 \end{gathered}$ | - | - | V | - |
| Output voltage of Low-level | VOL | $\mathrm{I}_{\mathrm{DO}}=2 \mathrm{~mA}$ | - | - | $\begin{aligned} & \text { LDO1 } \\ & \times 0.2 \end{aligned}$ | V | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Voltage regulator (LDO1) Output capacitor $1 \mu \mathrm{~F}$, Output capacitor's ESR less than $0.1 \Omega$ |  |  |  |  |  |  |  |
| Rise time | Tsu1 | Time until output voltage reaches to 0 V to $90 \%$ | - | 0.25 | - | ms | *2 |
| Fall time | Tsd1 | Time until output voltage reaches to $10 \%$ | - | 5 | - | ms | *2 |
| Maximum load current | IOMAX1 | - | - | 15 | - | mA | *3 |
| Load transient response (1) | Vtr11 | $\mathrm{I}_{\text {LDO1 }}=-50 \mu \mathrm{~A} \rightarrow-15 \mathrm{~mA}(1 \mu \mathrm{~s})$ | - | 70 | - | mV | *3 |
| Load transient response (2) | Vtr12 | $\mathrm{I}_{\text {LDO1 }}=-15 \mathrm{~mA} \rightarrow-50 \mu \mathrm{~A}(1 \mu \mathrm{~s})$ | - | 70 | - | mV | *3 |


| Voltage regulator (LDO2) Output capacitor $1 \mu \mathrm{~F}$, Output capacitor's ESR less than $0.1 \Omega$ |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Rise time | Tsu2 | Time until output voltage reaches to 0 V to $90 \%$ | - | 0.25 | - | ms | *2 |
| Fall time | Tsd2 | Time until output voltage reaches to $10 \%$ | - | 5 | - | ms | *2 |
| Maximum load current | IOMAX2 | - | - | 15 | - | mA | *3 |
| Load transient response (1) | Vtr21 | $\mathrm{I}_{\text {LDO2 }}=-50 \mu \mathrm{~A} \rightarrow-15 \mathrm{~mA}(1 \mu \mathrm{~s})$ | - | 70 | - | mV | *3 |
| Load transient response (2) | Vtr22 | $\mathrm{I}_{\text {LDO2 } 2}=-15 \mathrm{~mA} \rightarrow-50 \mu \mathrm{~A}(1 \mu \mathrm{~s})$ | - | 70 | - | mV | *3 |

TSD (Thermal shutdown circuit)

| Detection temperature | Tdet | Temperature which LDO1, LDO2, <br> Constant current circuit, Matrix SW <br> and RGB turns off. | - | 160 | - | ${ }^{\circ} \mathrm{C}$ | $* 3$ <br> $* 4$ |
| :--- | :---: | :--- | :--- | :--- | :--- | :--- | :--- |
| Return temperature | Tsd11 | Returning temperature | - | 110 | - | ${ }^{\circ} \mathrm{C}$ | $* 3$ <br> $* 5$ |

Note) *2: Rise time and Fall time are defined as below.
Actual evaluation result of rise time: LDO1: 290 to $400 \mu \mathrm{~s}, \quad$ LDO2 : 220 to $310 \mu \mathrm{~s}$
Actual evaluation result of fall time : LDO1: 6.2 to $8.5 \mathrm{~ms}, \quad$ LDO2: 5.8 to 7.9 ms
*3 : Typical Design Value
*4 : LDO1, LDO2, Constant current circuit, and Matrix SW and RGB are turned off when TSD is High.
When TSD is High, the register is set as $14 \mathrm{hD1}=1$. However, data can be read only when the register is read immediately after INT occurs since internal regulator is turned off.
*5 : Only LDO1 and LDO2 return after ON state of TSD. A logic part will be in Reset state.


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## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Microcomputer interface characteristic (Vdd $=1.85 \mathrm{~V} \pm 3$ \%) Write access Timing |  |  |  |  |  |  |  |
| CLK cycle time | tscyc1 | - | - | 125 | - | ns | *3 |
| CLK cycle time High period | twhc1 | - | - | 60 | - | ns | *3 |
| CLK cycle time Low period | twlc1 | - | - | 60 | - | ns | *3 |
| Serial-data setup time | tss1 | - | - | 62 | - | ns | *3 |
| Serial-data hold time | tsh1 | - | - | 62 | - | ns | *3 |
| Transceiver interval | tcsw1 | - | - | 62 | - | ns | *3 |
| Chip enable setup time | tcss1 | - | - | 5 | - | ns | *3 |
| Chip enable hold time | tcgh1 | - | - | 5 | - | ns | *3 |

Microcomputer interface characteristic (Vdd =1.85 V $\pm 3$ \%) Read access Timing

| CLK cycle time | tscyc1 | - | - | 125 | - | ns | $* 3$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CLK cycle time High period | twhc1 | - | - | 60 | - | ns | $* 3$ |
| CLK cycle time Low period | twlc1 | - | - | 60 | - | ns | $* 3$ |
| Serial-data setup time | tss1 | - | - | 62 | - | ns | $* 3$ |
| Serial-data hold time | tsh1 | - | - | 62 | - | ns | $* 3$ |
| Transceiver interval | tcsw1 | - | - | 62 | - | ns | $* 3$ |
| Chip enable setup time | tcss1 | - | - | 5 | - | ns | $* 3$ |
| Chip enable hold time | tcgh1 | - | - | 5 | - | ns | $* 3$ |
| DC delay time | tdodly1 | Only read mode | - | 25 | - | ns | $* 3$ |

Note) *3: Typical Design Value


## PIN CONFIGURATION

Top View


PIN FUNCTIONS

| Pin No. | Pin name | Type |  |
| :---: | :--- | :---: | :--- |
| B2 | VB | Power supply | Power supply for Bandgap circuit and LDO circuit |
| A2 | LDO1 | Output | LDO1 ( 1.85 V ) output pin |
| C4 | RSTB | Input | Reset input ( Active : High ) |
| A3 | IREF | Output | Resistor connection pin for constant current setup |
| B3 | LDOCNT | Input | ON/OFF control pin for LDO1 and LDO2 |
| A4 | VREFD | Output | Bandgap circuit output |
| B4 | AGND | Ground | GND for analog block |
| A5 | Y6 | Output | Constant current circuit, output pin of PWM control <br> It connects with the G column of matrix LED. |
| B5 | Y5 | Output | Constant current circuit, output pin of PWM control <br> It connects with the F column of matrix LED. |
| B6 | Y4 | Output | Constant current circuit, output pin of PWM control <br> It connects with the E column of matrix LED. |
| C5 | Y3 | Output | Constant current circuit, output pin of PWM control <br> It connects with the D column of matrix LED. |
| C6 | Y2 | Output | Constant current circuit, output pin of PWM control <br> It connects with the C column of matrix LED. |

## PIN FUNCTIONS (Continued)

| Pin No. | Pin name | Type | Description |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { D6 } \\ & \text { A6 } \end{aligned}$ | VLED1 <br> VLED2 | Power supply | Power supply connection pin for matrix LED |
| D5 | Y1 | Output | Constant current circuit, output pin of PWM control It connects with the $B$ column of matrix LED. |
| E6 | YO | Output | Constant current circuit, output pin of PWM control It connects with the A column of matrix LED. |
| D4 | LEDCTL | Input | ON/OFF operation control of LED lighting ( by serial address 0Ah ) |
| F6 | X0 | Output | Constant current circuit, output pin of PWM control It connects with the 1st row of matrix LED. |
| E5 | X1 | Output | Constant current circuit, output pin of PWM control It connects with the 2 nd row of matrix LED. |
| F5 | X2 | Output | Constant current circuit, output pin of PWM control It connects with the 3rd row of matrix LED. |
| E4 | X3 | Output | Constant current circuit, output pin of PWM control It connects with the 4th row of matrix LED. |
| F4 | PGND | Ground | GND for matrix LED |
| E3 | X4 | Output | Constant current circuit, output pin of PWM control It connects with the 5th row of matrix LED. |
| F3 | X5 | Output | Constant current circuit, output pin of PWM control It connects with the 6th row of matrix LED. |
| F2 | X6 | Output | Constant current circuit, output pin of PWM control It connects with the 7th row of matrix LED. |
| F1 | R | Output | LED connection pin |
| E2 | RGBGND | Ground | GND for RGB pin |
| E1 | G | Output | LED connection pin |
| D1 | B | Output | LED connection pin |
| D2 | DO | Output | SPI interface data output |
| D3 | DI | Input | SPI interface data input |
| C1 | CLK | Input | SPI interface clock input |
| C2 | CE | Input | SPI interface chip enable (Active : High ) |
| C3 | INT | Output | Interrupt output |
| A1 | LDO2 | Output | LDO2 ( 2.85 V ) output |

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FUNCTIONAL BLOCK DIAGRAM


Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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## OPERATION

1. Explanation of each mode ( Power supply startup sequence )

\begin{tabular}{|c|c|c|c|c|}
\hline Mode \& LDOCNT \& REG18 \& REG28 \& Note \\
\hline OFF mode \& Low \& 0 \& 0 \& - LDOCNT should be set to High in order to recover from OFF mode. \\
\hline \begin{tabular}{l}
OFF mode
\[
\rightarrow
\] \\
Normal mode
\end{tabular} \& Low \(\rightarrow\) High

High \& $0 / 1$

$0 / 1$ \& $0 / 1$

$0 / 1$ \& | - Serial signal is not received at LDOCNT = Low and REG28 $=[0]$ or REG18 $=$ [0]. |
| :--- |
| - This LSI shifts to Standby mode at LDOCNT = Low, REG28 = [1] and REG18 = [0]. |
| - Serial signal is not received at Standby mode. (Power supplies for logic are LDO1 and LDO2.) Therefore, Standby mode cannot be released by serial signal. |
| - When LDOCNT is changed from Low to High, it is impossible to shift Standby mode to Normal mode. |
| - It is impossible to shift Standby mode to OFF mode. Once returning to Normal mode, shift to OFF mode. | <br>


\hline Normal mode $\rightarrow$ OFF mode \& \multirow[t]{2}{*}{High $\rightarrow$ Low} \& 0 \& 0 \& | - At LDOCNT = High, LDO1 turns on regardless of REG18. |
| :--- |
| - At LDOCNT = High, LDO2 turns on regardless of REG28. |
| - At RSTB = Low, serial signal is not received. |
| - It is possible to receive the serial signal at 5 ms or more after LDOCNT is set to High. |
| - The Low interval of RSTB should be one internal clock or more. |
| - Don't input a signal except rectangle wave to RSTB pin. | <br>


\hline | Normal mode $\rightarrow$ |
| :--- |
| Standby mode | \& \& 0 \& 1 \& | - All register's settings become default values if RSTB is set to Low. (The default value of REG18 and REG28 bit is [1]. Note that LDO1 and LDO2 don't turn off when RSTB is set to Low before LDOCNT is set to Low.) |
| :--- |
| - All register's settings are reset when LDO2 turns off. (Register setting initialization) |
| - The setup step to OFF mode is as follows. REG18, $28=[0] \rightarrow$ LDOCNT $=$ Low $\rightarrow$ RSTB $=$ Low | <br>

\hline
\end{tabular}

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OPERATION (continued)

1. Explanation of each mode ( Power supply startup sequence ) (continued)


- Shift to Normal mode from Standby mode


Note) The above waveform is under the condition that the register setup is reset in standby mode.
Maintain the state of RSTB = High to hold the register setup.

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## OPERATION (continued)



- Shift to Standby mode from Normal mode


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## OPERATION (continued)

## 1. Explanation of each mode ( Power supply startup sequence ) (continued)

Mode which is specified by VBAT / LDOCNT

| VBAT | LDOCNT | MODE |
| :---: | :---: | :---: |
| Low | Low | OFF |
| Low | High | Prohibition |
| High | Low | OFF |
| High | High | ON |

Note) "Low" in column of VBAT and LDOCNT means 0 V .
"High" in column of VBAT and LDOCNT means 3.1 V to 4.6 V (operation supply voltage range).

Logic pin conditions

The following setting is common for OFF, Standby and Normal mode.
The pin setting when RSTB = Low, under Normal mode is as follows.

| Pin name | Pin state | Logic state $^{*}$ |
| :---: | :---: | :---: |
| INT | Output | Low |
| CE | Input | Low |
| CLK | Input | Low |
| DI | Input | Low |
| DO | Output | Low |
| LEDCTL | Input | Low |
| LDOCNT | Input | Depends on each mode setup |

Note)*: Logic state for pins indicated as "Output" under Pin state shows the output level.
Logic state for pins indicated as "Input" under Pin state shows the input level to be set to the pins.

## OPERATION (continued)

## 2. Explanation of operation

Matrix part operation waveform
The following waveform is a timing chart example at operation.
It is controlled by internal 1.2 MHz clock under the default condition.
Y side switches from Y0 to Y 6 in that order. The ON period of each pin is constant $945 \mathrm{clk}(787.5 \mu \mathrm{~s})$.
The ON period includes an 8clk( $6.67 \mu \mathrm{~s}$ ) interval.
In the case of the following figure, "*" mark shows ON period. Therefore, D3 and D4 are OFF period.
$7 \times 7$ matrix display is controlled by the lines of X 1 to X 6 .
The following waveforms are internal signals. The actual waveform of $Y x$ pin becomes $\mathrm{Hi}-\mathrm{Z}$ at $\mathrm{Yx}=\mathrm{Xx}=$ Low.


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## OPERATION (continued)

## 3. Block configuration

RESET part block configuration


Note) All the logic portions and blocks to which the power supply is not connected are supplied from VB.

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## OPERATION (continued)

## 3. Block configuration (continued)

Explanation of matrix LED part, matrix LED's number
LED matrix driver can display characters and patterns by controlling $7 \times 7$ matrix LED individually. In this product standards, LED's number controlled by each pin is as the following figure.
An internal logic circuit is controlled by internal clock.
In scroll mode, the display of character specified in the following arrangement is moved from right to left.


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## OPERATION (continued)

## 3. Block configuration (continued)

Equivalent circuit example of constant current driver

In case of $X 0$ pin


The constant current equivalent circuit example ( XO pin) for LED driver is shown in the above figure.
The reference current for constant current driver is calculated by the following formula.
$\mathrm{V}($ IREF $) / \mathrm{R}($ IREF $)=0.54 \mathrm{~V} / 27 \mathrm{k} \Omega=20 \mu \mathrm{~A}$
The LED driver current can be set to the range of 0 mA to 30 mA by setting the mirror ratio between Q1 and Q2 by DAC via serial interface.
The constant current can be changed by the resistor connected to IREF pin, but the accuracy in case
of this setting is not guaranteed.
It is recommended that ERJ2RHD273X is used as R(IREF) to keep the accuracy of constant current of LED driver.

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## OPERATION (continued)

## 4. Register and Address

Register map

| Sub address | R/W | Data name | Data |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01h | W | POWERCNT | - | - | - | - | - | OSCEN | - | - |
| 02h | W | LDOCNT | - | - | - | - | - | - | REG18 | REG28 |
| 03h | For test |  |  |  |  |  |  |  |  |  |
| 04h | For test |  |  |  |  |  |  |  |  |  |
| 05h | For test |  |  |  |  |  |  |  |  |  |
| 06h | For test |  |  |  |  |  |  |  |  |  |
| 07h | For test |  |  |  |  |  |  |  |  |  |
| 08h | For test |  |  |  |  |  |  |  |  |  |
| 09h | For test |  |  |  |  |  |  |  |  |  |
| OAh | W | LEDCTL | LEDACT | - | - | - | - | DISMTX | DISRGB | - |
| ! |  |  |  |  |  |  |  |  |  |  |
| 10h | For test |  |  |  |  |  |  |  |  |  |
| 11h | For test |  |  |  |  |  |  |  |  |  |
| 12h | For test |  |  |  |  |  |  |  |  |  |
| 13h | For test |  |  |  |  |  |  |  |  |  |
| 14h | R | IOFACTOR | FACGD1 | - | - | - | $\begin{aligned} & \text { RAM } \\ & \text { ACT } \end{aligned}$ | FRMINT | CPUWRER | TSD |
| 15h | For test |  |  |  |  |  |  |  |  |  |
| 16h | For test |  |  |  |  |  |  |  |  |  |
| 17h | For test |  |  |  |  |  |  |  |  |  |
| 18h | For test |  |  |  |  |  |  |  |  |  |
| 19h | For test |  |  |  |  |  |  |  |  |  |
| 1Ah | W/R | VDDSEL | INTVSEL | - | - | - | - | - | - | - |

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## OPERATION (continued)

## 4. Register and Address (continued)

Register map (continued)

| Sub address | R/W | Data name | Data |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 20h | R/W | MTXON | - | - | - | - | - | - | - | MTXON |
| 21h | R/W | MTXDATA | MTXDATA[7 : 0] |  |  |  |  |  |  |  |
| 22h | R/W | FFROM | - | - | - | - | - | - | ROM77[1 : 0] |  |
| 23h | R/W | ROMSEL | SELROM[7 : 0] |  |  |  |  |  |  |  |
| 24h | R/W | RAMCOPY | - | - | - | - | - | - | SELRAM | COPY START |
| 25h | R/W | SETFROM | SETFROM[7:0] |  |  |  |  |  |  |  |
| 26h | R/W | SETTO | SETTO[7 : 0] |  |  |  |  |  |  |  |
| 27h | R/W | REPON | - | - | - | - | - | - | - | REPON |
| 28h | R/W | SETTIME | - | - | - | - | - | - | SETTIME[1 : 0] |  |
| 29h | R/W | RAMRST | - | - | - | - | - | - | RAM1 | RAM2 |
| 2Ah | R/W | SCROLL | - | - | - | - | - | - | - | SCLON |
| 2Bh | For test |  |  |  |  |  |  |  |  |  |
| 2Ch | R/W | RGBON | - | - | - | - | - | - | - | RGBON |
| 2Dh | R/W | RGBDATA | - | - | RGBDATA[5:0] |  |  |  |  |  |
| 2Eh | For test |  |  |  |  |  |  |  |  |  |
| 30h | R/W | RAMNUM | - | - | - | - | - | - | - | RAMNUM |
| ! |  |  |  |  |  |  |  |  |  |  |
| 6Bh | For test |  |  |  |  |  |  |  |  |  |
| 6Dh | For test |  |  |  |  |  |  |  |  |  |
| 6Fh | For test |  |  |  |  |  |  |  |  |  |
| 70h | For test |  |  |  |  |  |  |  |  |  |
| 71h | For test |  |  |  |  |  |  |  |  |  |
| 72h | For test |  |  |  |  |  |  |  |  |  |
| 73h | For test |  |  |  |  |  |  |  |  |  |
| 74h | For test |  |  |  |  |  |  |  |  |  |
| 75h | For test |  |  |  |  |  |  |  |  |  |
| 76h | For test |  |  |  |  |  |  |  |  |  |
| 77h | For test |  |  |  |  |  |  |  |  |  |

Note) Don't access to the address 6Bh to 77h.

