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Panasonic

AN32054B

http://www.semicon.panasonic.co.jp/en/

7 x 17 Dots Matrix LED Driver LSI

FEATURES

- 7 x 17 LED Matrix Driver
  (Total LED that can be driven = 119)
- Internal memory RAM (2-side)
- LDO (1-ch.)
- I^2C interface + SPI interface
- 50 pin Wafer Level Chip Size Package (WLCSP)

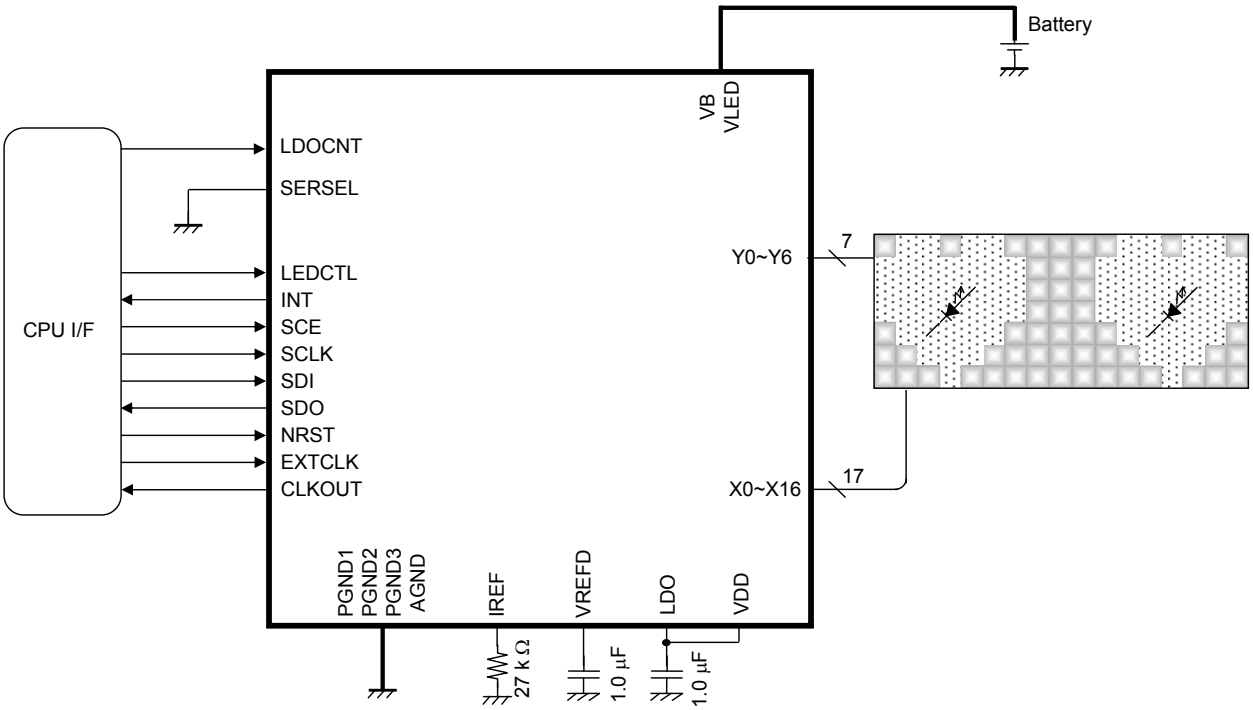
DESCRIPTION

AN32054B is a 7 x 17 LED Matrix Driver equipped with RAM.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VDD_{MAX}	4.3	V	*1
	VB_{MAX}	6.0	V	*1
	$VLED_{MAX}$	6.5	V	*1
Operating ambience temperature	T_{opr}	–30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	NRST, SCLK, SDI	– 0.3 to 4.3	V	—
	SERSEL, EXTCLK, LDOCNT, SCE, LEDCTL	– 0.3 to 6.0	V	—
Output Voltage Range	SDO, CLKOUT, INT	– 0.3 to 4.3	V	—
	LDO	– 0.3 to 6.0	V	—
	X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16 Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3 to 6.5	V	—
ESD	HBM	1.5 to 2.0	kV	—

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1: VB_{MAX} = VB, VDD_{MAX} = VDD, $VLED_{MAX}$ = VLED, the values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
50 pin Wafer Level Chip Size Package (WLCSP)	107.3 °C /W	0.932 W	0.373 W

Note) For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VDD	1.7	1.85	3.5	V	*1
	VB	3.1	3.7	4.6	V	*1
	VLED	3.1	5.0	5.6	V	*1
Input Voltage Range	NRST, SCLK, SDI	– 0.3	—	VDD + 0.3	V	*2
	SERSEL, EXTCLK, LDOCNT, SCE, LEDCTL	– 0.3	—	VB + 0.3	V	*2
Output Voltage Range	SDO, CLKOUT, INT	– 0.3	—	VDD + 0.3	V	*2
	LDO	– 0.3	—	VB + 0.3	V	*2
	X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16 Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3	—	VLED + 0.3	V	*2

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, PGND1, PGND2 and PGND3.
VDD is voltage for VDD. VB is voltage for VB. VLED is voltage for VLED.
*2: (VDD + 0.3) V must not exceed 4.3 V. (VB + 0.3) V must not exceed 6 V.
(VLED + 0.3) V must not exceed 6.5 V.

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ELECTRICAL CHARACTERISTICS

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current consumption							
Current consumption (1) Off mode	ICC1	LDOCNT = Low	—	0	1	μA	—
Current consumption (2) Normal mode	ICC2	LDOCNT = High ILOAD = 0 μA	—	14	20	μA	—
Reference voltage source							
Output voltage	VREF	I_{VREF} = 0 μA	1.21	1.24	1.27	V	—
Reference current source							
Output voltage	VIREF	Connect the register of 39 kΩ between IREF and GND. I_{IREF} = 0 μA	0.2	0.3	0.4	V	—
EXTCLK, NRST, LDOCNT, SERSEL, LEDCTL							
High-level input voltage range	VIH1	High-level recognition voltage of EXTCLK, NRST, LDOCNT, SERSEL, LEDCTL	1.4	—	VB + 0.3	V	—
Low-level input voltage range	VIL1	Low-level recognition voltage of EXTCLK, NRST, LDOCNT, SERSEL, LEDCTL	– 0.3	—	0.4	V	—
High-level input current	IIH1	$V_{EXTCLK, NRST, LDOCNT, SERSEL, LEDCTL}$ = 1.85 V	—	0	1	μA	—
Low-level input current	IIL1	$V_{EXTCLK, NRST, LDOCNT, SERSEL, LEDCTL}$ = 0 V	—	0	1	μA	—

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ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SCE, SCLK, SDI							
High-level input voltage range	VIH2	High-level recognition voltage of SCE, SCLK, SDI	0.7 × VDD	—	VDD_{max} + 0.5	V	—
Low-level input voltage range	VIL2	Low-level recognition voltage of SCE, SCLK, SDI	– 0.5	—	0.3 × VDD	V	—
High-level input current	IIH2	$V_{SCE, SCLK, SDI}$ = 1.85 V	—	0	1	μA	—
Low-level input current	IIL2	$V_{SCE, SCLK, SDI}$ = 0 V	—	0	1	μA	—
Low-level output voltage (1)	VOL1	I_{SDI} = 3 mA, VDD > 2 V, VOL1 = V_{SDI}	0	—	0.4	V	—
Low-level output voltage (2)	VOL2	I_{SDI} = 3 mA, VDD < 2 V VOL2 = V_{SDI}	0	—	0.2 × VDD	V	—
SDO, INT, CLKOUT							
High-level output voltage	VOH1	$I_{SDO, INT, CLKOUT}$ = – 2 mA	VDD × 0.8	—	—	V	—
Low-level output voltage	VOL3	$I_{SDO, INT, CLKOUT}$ = 2 mA	—	—	VDD × 0.2	V	—

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ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current generator (for matrix LED)							
Output current (1)	IMX1	At 1.333 mA setup $V_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$ = 1 V IMX1 = $I_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$	1.226	1.333	1.440	mA	*1, 2
Output current (2)	IMX2	At 2.666 mA setup $V_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$ = 1 V IMX2 = $I_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$	2.452	2.666	2.879	mA	*1, 2
Output current (3)	IMX4	At 5.332 mA setup $V_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$ = 1 V IMX4 = $I_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$	4.905	5.332	5.759	mA	*1, 2
Output current (4)	IMX8	At 10.66 mA setup $V_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$ = 1 V IMX8 = $I_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$	9.81	10.66	11.52	mA	*1, 2
Output current (5)	IMX15	At 20.00 mA setup $V_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$ = 1 V IMX15 = $I_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$	18.40	20.00	21.60	mA	*1, 2
Leak current at the time of OFF	IMXOFF	Current OFF setup $V_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$ = 4.75 V IMXOFF = $I_{X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16}$	—	—	1	μA	—
The error between channels	IMXCH	Difference current between the average of all channels and each channel.	– 5	—	5	%	*2

Note) *1: Values when recommended parts (ERJ2RHD393X) are used for IREF pin. The other current settings are combination of above items.

*2: All of the setting values of matrix block are with absolute accuracy of ± 8 %, the error between channels of ± 5 %.

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ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SCAN Switch							
Resistance at the switch ON	RSCAN	$I_{Y0, Y1, Y2, Y3, Y4, Y5, Y6}$ = – 5 mA RSCAN = $V_{Y0, Y1, Y2, Y3, Y4, Y5, Y6}$ / 5 mA	—	1	2	Ω	—
Voltage regulator (LDO)							
Output voltage	VL1	I_{LDO} = – 30 mA	1.79	1.85	1.91	V	—
Short current protection current	IPT1	LDOCNT = High REG18 = [1] V_{LDO} = 0 V	50	100	200	mA	—
Ripple rejection ratio (1)	PSL11	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO} = – 15 mA PSL11 = 20log(acVP31 / 0.2)	—	–45	–40	dB	—
Ripple rejection ratio (2)	PSL12	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO} = – 15 mA PSL12 = 20log(acVP31 / 0.2)	—	–35	–25	dB	—
Oscillation circuit							
Oscillation frequency	FOSC	OSCEN = [1]	0.96	1.2	1.44	MHz	—

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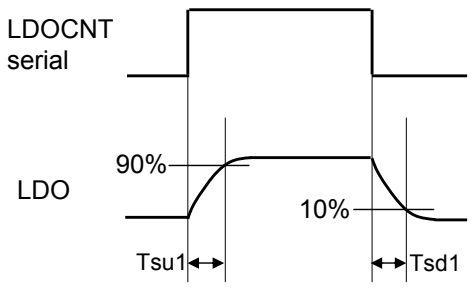
ELECTRICAL CHARACTERISTICS (continued)

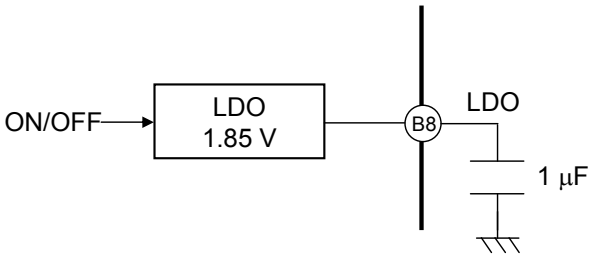
VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
TSD (Thermal shutdown circuit)							
Detection temperature	Tdet	Temperature which LDO, Constant current circuit, and Matrix SW turn off.	—	160	—	°C	*3 *5
Return temperature	Tsd11	Returning temperature	—	110	—	°C	*4 *5
Voltage regulator (LDO) Output capacitor 1 μF, Output capacitor's ESR less than 0.1 Ω							
Rise time	Tsu1	Time until output voltage reaches 0 V to 90%	—	0.25	—	ms	*5
Fall time	Tsd1	Time until output voltage reaches 10%.	—	5	—	ms	*5
Maximum load current	IOMAX1	—	—	15	—	mA	*5
Load transient response (1)	Vtr11	I_{LDO} = – 50 mA → – 15 μA (1 μs)	—	70	—	mV	*5
Load transient response (2)	Vtr12	I_{LDO} = – 15 mA → – 50 μA (1 μs)	—	70	—	mV	*5

Note) *3: LDO, Constant current circuit, and Matrix SW are turned off when TSD operates.
*4: Only LDO returns after ON state of TSD. A logic part will be in Reset state.
*5: Typical design value.





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ELECTRICAL CHARACTERISTICS (continued)

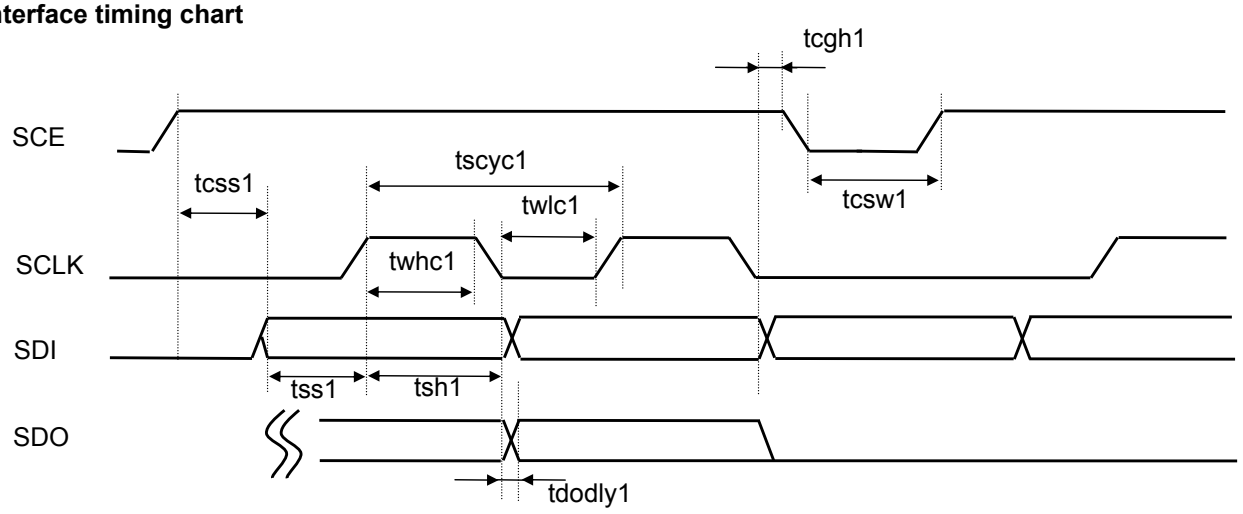
VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Microcomputer interface characteristics (VDD = 1.85 V ± 3 %) Write access timing							
SCLK cycle time	tscyc1	—	—	125	—	ns	*5
SCLK cycle time High period	twhc1	—	—	60	—	ns	*5
SCLK cycle time Low period	twlc1	—	—	60	—	ns	*5
Serial-data setup time	tss1	—	—	62	—	ns	*5
Serial-data hold time	tsh1	—	—	62	—	ns	*5
Transceiver interval	tcsw1	—	—	62	—	ns	*5
Chip enable setup time	tcss1	—	—	5	—	ns	*5
Chip enable hold time	tcgh1	—	—	5	—	ns	*5
Microcomputer interface characteristics (VDD = 1.85 V ± 3 %) Read access timing							
SCLK cycle time	tscyc1	—	—	333	—	ns	*5
SCLK cycle time High period	twhc1	—	—	160	—	ns	*5
SCLK cycle time Low period	twlc1	—	—	160	—	ns	*5
Serial-data setup time	tss1	—	—	125	—	ns	*5
Serial-data hold time	tsh1	—	—	125	—	ns	*5
Transceiver interval	tcsw1	—	—	125	—	ns	*5
Chip enable setup time	tcss1	—	—	5	—	ns	*5
Chip enable hold time	tcgh1	—	—	5	—	ns	*5
DC delay time	tdody1	Only read mode	—	100	—	ns	*5

Note) *5: Typical design value

Interface timing chart



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ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C I/F							
Input voltage hysteresis(1)	Vhys1	Hysteresis voltages of Pad No.37, 38 VDD > 2 V	0.05 × VDD	—	—	mV	*6 *7
Input voltage hysteresis(2)	Vhys2	Hysteresis voltages of Pad No.37, 38 VDD < 2 V	0.1 × VDD	—	—	mV	*6 *7
Output fall time	Tof	Bus's capacitance 10 pF to 400 pF Ip < 6 mA	20 + 0.1C_b	—	250	ns	*6 *7
Pulse width of the spike oppressed by an input filter	Tsp	—	0	—	50	ns	*6 *7
I/O pin's capacitance	Ci	Bus's capacitance 10 pF to 400 pF	—	—	10	pF	*6 *7

Note) *6: The timing of Fast-mode and Normal mode devices in I²C-bus is specified in Page.13. All values referred to V_{IHMIN} and V_{ILMAX} level.

*7: These are values checked by design but not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C I/F (continued)							
Hold period (repeat)	$t_{HD:STA}$	The first clock pulse is generated after $t_{HD:STA}$.	0.6	—	—	µs	*6 *7
SCLK clock Low period	t_{LOW}	—	1.3	—	—	µs	*6 *7
SCLK clock High period	t_{HIGH}	—	0.6	—	—	µs	*6 *7
Repeated start condition setup time	$t_{SU:STA}$	—	0.6	—	—	µs	*6 *7
Data hold time	$t_{HD:DAT}$	—	0	—	0.9	µs	*6 *7
Data setup time	$t_{SU:DAT}$	—	100	—	—	ns	*6 *7
Rise time of both SDA and SCL signals	tr	—	20 + 0.1C_b	—	300	ns	*6 *7
Fall time of both SDA and SCL signals	t_f	—	20 + 0.1C_b	—	300	ns	*6 *7
STOP condition setup time	$t_{SU:STO}$	—	0.6	—	—	µs	*6 *7
Bus free time between STOP condition and START condition	t_{BUF}	—	1.3	—	—	µs	*6 *7
Bus line capacitive load	C_b	—	—	—	400	pF	*6 *7
Low-level noise margin of the connected device	V_{aL}	—	0.1 × VDD	—	—	V	*6 *7
High-level noise margin of the connected device	V_{aH}	—	0.2 × VDD	—	—	V	*6 *7

Note) *6: The timing of Fast-mode and Normal mode devices in I²C-bus is specified in Page.13. All values referred to V_{IHMIN} and V_{ILMAX} level.

*7: These are values checked by design but not production tested.

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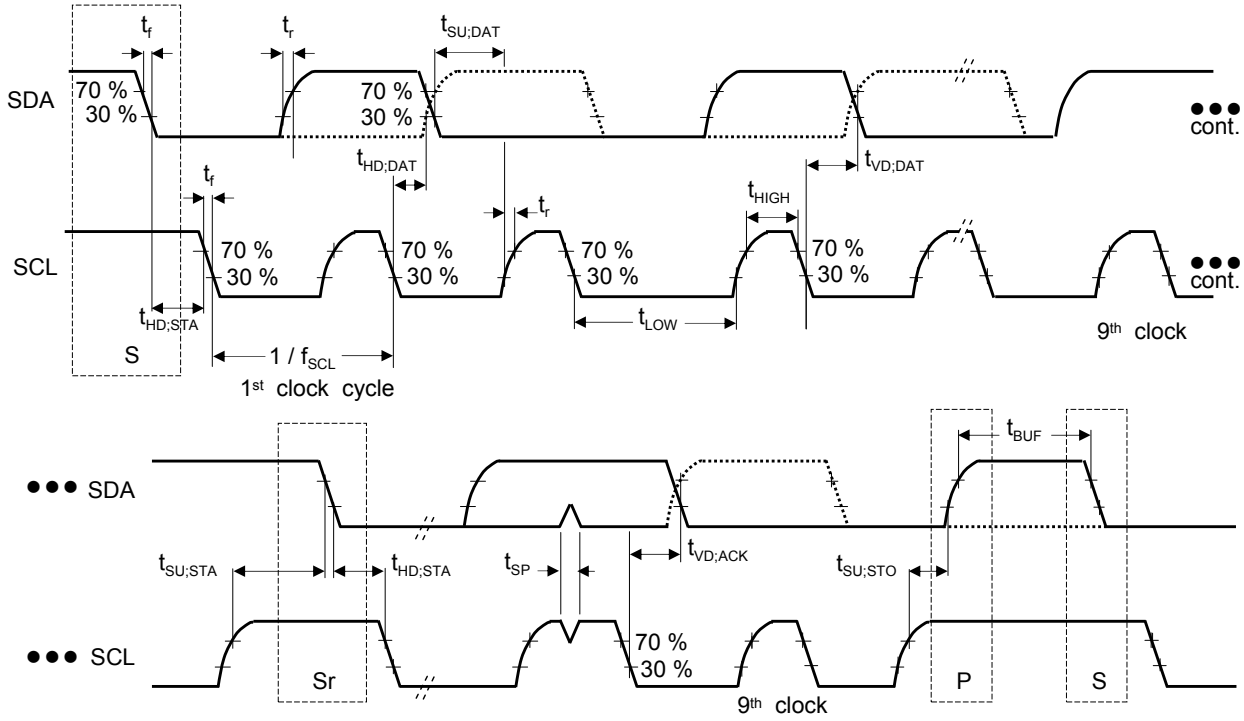
ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.



V_{ILMAX} = 0.3 V_{DD}

V_{IHMIN} = 0.7 V_{DD}

S : START condition

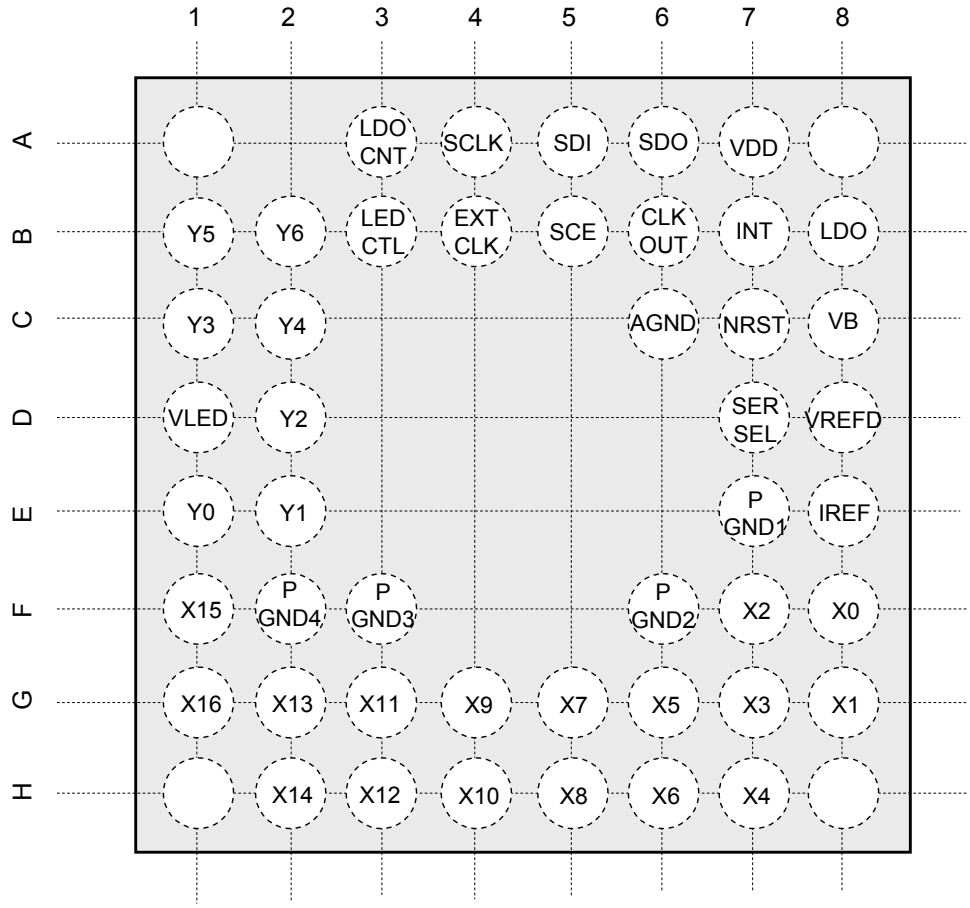
Sr : Repeat START condition

P : STOP condition

Establ ished : 2 0 0-0 1-3 (
Revised : 2 0 1-0 40 2

PIN CONFIGURATION

TOP VIEW



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PIN FUNCTIONS

Pin No.	Pin name	Type	Description
F8(1)	X0	Output	The output pin of PWM control with constant current circuit. It connects with A column of matrix LED.
G8(2)	X1	Output	The output pin of PWM control with constant current circuit. It connects with B column of matrix LED.
E7(3) F6(8) F3(13) F2(18)	PGND1 PGND2 PGND3 PGND4	Ground	GND for matrix LED
F7(4)	X2	Output	The output pin of PWM control with constant current circuit. It connects with C column of matrix LED.
G7(5)	X3	Output	The output pin of PWM control with constant current circuit. It connects with D column of matrix LED.
H7(6)	X4	Output	The output pin of PWM control with constant current circuit. It connects with E column of matrix LED.
G6(7)	X5	Output	The output pin of PWM control with constant current circuit. It connects with F column of matrix LED.
H6(9)	X6	Output	The output pin of PWM control with constant current circuit. It connects with G column of matrix LED.
G5(10)	X7	Output	The output pin of PWM control with constant current circuit. It connects with H column of matrix LED.
H5(11)	X8	Output	The output pin of PWM control with constant current circuit. It connects with I column of matrix LED.
G4(12)	X9	Output	The output pin of PWM control with constant current circuit. It connects with J column of matrix LED.
H4(14)	X10	Output	The output pin of PWM control with constant current circuit. It connects with K column of matrix LED.
G3(15)	X11	Output	The output pin of PWM control with constant current circuit. It connects with L column of matrix LED.
H3(16)	X12	Output	The output pin of PWM control with constant current circuit. It connects with M column of matrix LED.
G2(17)	X13	Output	The output pin of PWM control with constant current circuit. It connects with N column of matrix LED.
H2(19)	X14	Output	The output pin of PWM control with constant current circuit. It connects with O column of matrix LED.
F1(20)	X15	Output	The output pin of PWM control with constant current circuit. It connects with P column of matrix LED.
G1(21)	X16	Output	The output pin of PWM control with constant current circuit. It connects with Q column of matrix LED.

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PIN FUNCTIONS (Continued)

Pin No.	Pin name	Type	Description
E1(22)	Y0	Output	The output pin of PWM control with constant current circuit. It connects with the 1st row of matrix LED.
E2(23)	Y1	Output	The output pin of PWM control with constant current circuit. It connects with the 2nd row of matrix LED.
D2(24)	Y2	Output	The output pin of PWM control with constant current circuit. It connects with the 3rd row of matrix LED.
D1(25)	VLED	Power supply	Power supply's connect pin for matrix LED Connect with the output of battery or step-up converter to supply sufficient LED voltage.
C1(26)	Y3	Output	The output pin of PWM control with constant current circuit. It connects with the 4th row of matrix LED.
C2(27)	Y4	Output	The output pin of PWM control with constant current circuit. It connects with the 5th row of matrix LED.
B1(28)	Y5	Output	The output pin of PWM control with constant current circuit. It connects with the 6th row of matrix LED.
B2(29)	Y6	Output	The output pin of PWM control with constant current circuit. It connects with the 7th row of matrix LED.
C8(30)	VB	Power supply	Power supply's connect pin for BGR circuit and LDO circuit
B8(31)	LDO	Output	Power supply output pin for the internal serial interface input block and internal logic
D8(32)	VREFD	Output	Band Gap Reference circuit output pin
A7(33)	VDD	Power supply	Power supply's connect pin for interface output
E8(34)	IREF	Output	Resistor connection pin to set up the internal reference constant current
C6(35)	AGND	Ground	GND pin for Analog circuit
B5(36)	SCE	Input	SPI interface chip-enable pin (High active) (Slave address selection control pin in I^2C mode)
A4(37)	SCLK	Input	Common clock input pin in both SPI interface and I^2C interface
A5(38)	SDI	Input / Output	Data input pin for SPI interface Data input/output pin for I^2C interface
A6(39)	SDO	Output	Data output pin for SPI interface
B7(40)	INT	Output	Interrupt signal output pin to notify IC condition to CPU
C7(41)	NRST	Input	Reset input pin (Low active)
A3(42)	LDOCNT	Input	LDO ON/OFF control pin
B4(43)	EXTCLK	Input	External clock input pin This clock can be used as the reference clock for this IC instead of the internal clock.
D7(44)	SERSEL	Input	SPI, I^2C interface selection pin
B3(45)	LEDCTL	Input	External synchronous signal input pin This signal can control LED on/off with the internal register setting.
B6(46)	CLKOUT	Output	Internal clock output pin This clock can be used as the reference clock for another AN32054B when more than 2 ICs are used in the application.

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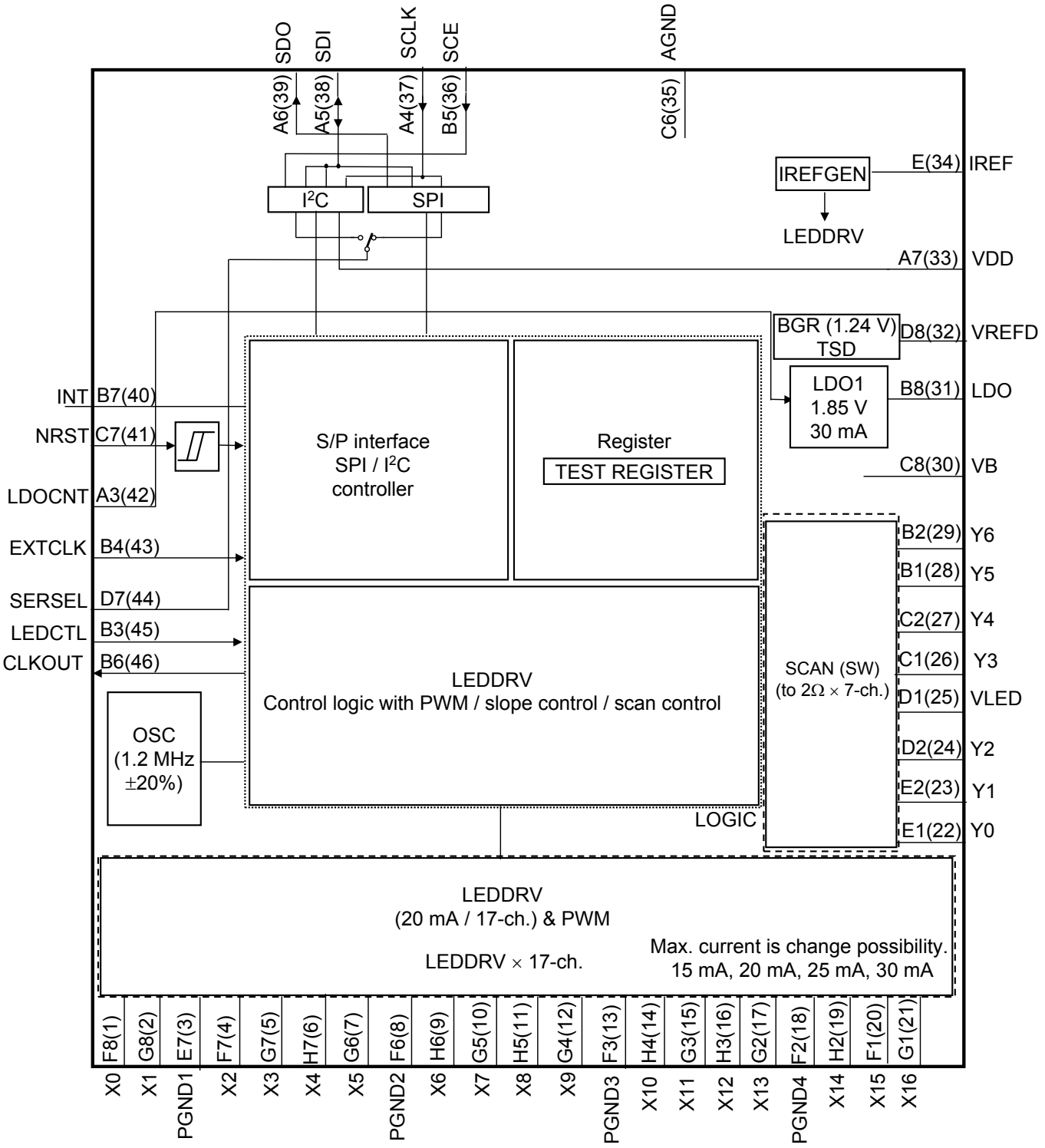
FUNCTIONAL BLOCK DIAGRAM



Note) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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OPERATION

1. Power supply sequence control

Power supply on/off sequence

Mode	LDOCNT	REG18	Note
OFF	Low	0	• It is necessary to make it LDOCNT = High for the return from OFF-mode.
OFF → Normal Mode	Low → High	0/1	• The signal from serial interface is not received in LDOCNT = Low and the state of REG18 = [0]
	High	0/1	
OFF → Normal mode	High → Low	0	• Regardless of the value of REG18, LDO turns on at LDOCNT = High. • Serial interface signal is not received at RSTB = Low • After more than 5 ms from LDOCNT = High, the IC can recognize the serial interface signal. • To activate RSTB, RSTB should be kept low for more than one internal clock period. • RSTB terminal prohibits the input signal of those other than a rectangle wave. • All register setting become default setting once RSTB = Low. (The default setting of REG18 is [1]. If RSTB = Low before LDOCNT = Low, LDO can't turn off.) All register setting become default setting when LDO turns off. • The correct setting order to set off mode is as following. REG18 = [0] → LDOCNT = Low → RSTB = Low

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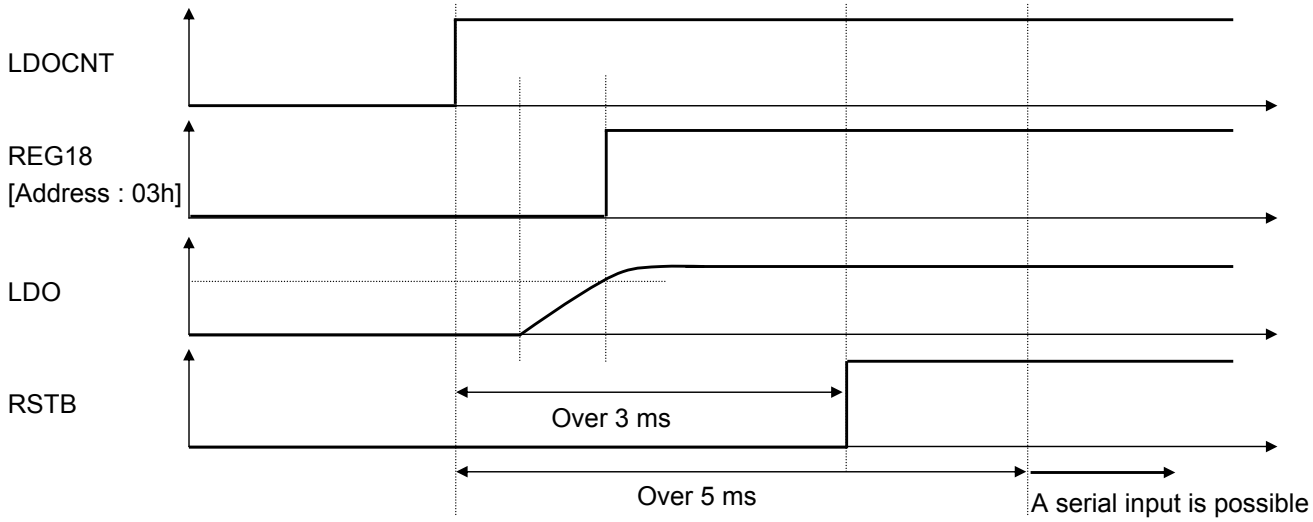
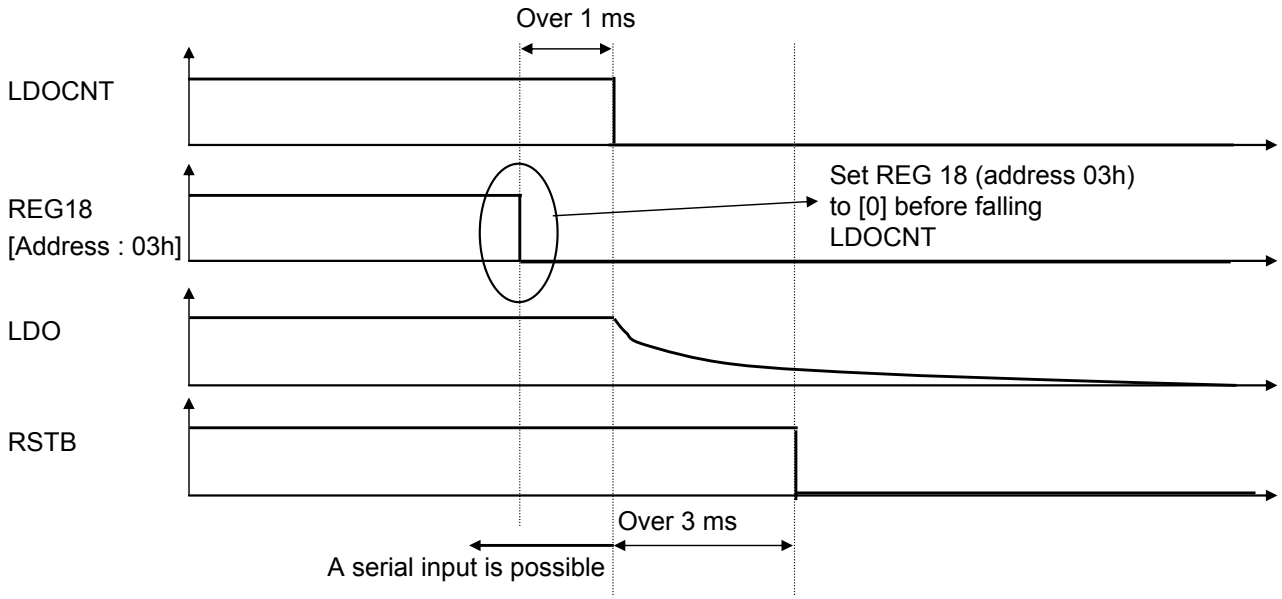
OPERATION (continued)

1. Power supply sequence control (continued)

Shift to Normal mode from OFF-mode



Shift to OFF-mode from Normal mode



Established : 2009-01-30
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OPERATION (continued)

2. Register Map (1)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	R/W	MAPCHG	—	—	—	—	—	—	—	MAPCHG *1
02h	R/W	POWERCNT	—	—	—	—	—	—	—	OSCEN
03h	R/W	LDOCNT	—	—	—	—	—	—	—	REG18
04h	R	TEST0	TEST0							
05h	R	INT	—	—	—	—	—	—	RAMACT	FRMINT
06h	R/W	OPTION	LEDACT	DISMTX	—	—	—	—	CLKOUT	EXTCLK
07h	R/W	MTXON	—	—	—	—	—	—	—	MTXON
08h	R/W	MTXDATA	—	—	—	—	—	—	MTXDATA	
09h	R/W	RAMRST	—	—	—	—	—	—	RAM1	RAM2
0Ah	R/W	SCROLL	—	—	—	—	—	—	—	SCLON
0Bh	R/W	SCLMODE	—	UP	DOWN	RIGHT	LEFT	SCLTIME[2:0]		
0Dh	R/W	RESET	—	—	—	—	—	—	—	SRST
10h	R/W	XCONST1	X16	X15	X14	X13	X12	X11	X10	X9
11h	R/W	XCONST2	X8	X7	X6	X5	X4	X3	X2	X1
12h	R/W	XCONST3	—	—	—	—	—	—	—	X0
13h	R/W	IMAX	—	—	—	—	—	—	IMAX[1:0]	
20h	R/W	TEST1	TEST1							
:	:	:	:							
:	:	:	:							
36h	R/W	TEST22	TEST22							
40h	R/W	TEST23	TEST23							
41h	R/W	TEST24	TEST24							

Note) Access the address from 20h to 41h is prohibited.
*1: When 01h D0 is set to "0", Register Map (1) is selected, when 01h D0 is set to "1", Register Map (2) is selected.

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OPERATION (continued)

2. Register Map (2)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
02h	R/W	RAMNUM	—	—	—	—	—	—	—	RAMNUM
03h	R/W	A1	BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
04h	R/W	A2	BLA2[3:0]				FRA2[1:0]		DLA2[1:0]	
05h	R/W	A3	BLA3[3:0]				FRA3[1:0]		DLA3[1:0]	
06h	R/W	A4	BLA4[3:0]				FRA4[1:0]		DLA4[1:0]	
07h	R/W	A5	BLA5[3:0]				FRA5[1:0]		DLA5[1:0]	
08h	R/W	A6	BLA6[3:0]				FRA6[1:0]		DLA6[1:0]	
09h	R/W	A7	BLA7[3:0]				FRA7[1:0]		DLA7[1:0]	
0Ah	R/W	B1	BLB1[3:0]				FRB1[1:0]		DLB1[1:0]	
0Bh	R/W	B2	BLB2[3:0]				FRB2[1:0]		DLB2[1:0]	
0Ch	R/W	B3	BLB3[3:0]				FRB3[1:0]		DLB3[1:0]	
0Dh	R/W	B4	BLB4[3:0]				FRB4[1:0]		DLB4[1:0]	
0Eh	R/W	B5	BLB5[3:0]				FRB5[1:0]		DLB5[1:0]	
0Fh	R/W	B6	BLB6[3:0]				FRB6[1:0]		DLB6[1:0]	
10h	R/W	B7	BLB7[3:0]				FRB7[1:0]		DLB7[1:0]	
11h	R/W	C1	BLC1[3:0]				FRC1[1:0]		DLC1[1:0]	
12h	R/W	C2	BLC2[3:0]				FRC2[1:0]		DLC2[1:0]	
13h	R/W	C3	BLC3[3:0]				FRC3[1:0]		DLC3[1:0]	
14h	R/W	C4	BLC4[3:0]				FRC4[1:0]		DLC4[1:0]	
15h	R/W	C5	BLC5[3:0]				FRC5[1:0]		DLC5[1:0]	
16h	R/W	C6	BLC6[3:0]				FRC6[1:0]		DLC6[1:0]	
17h	R/W	C7	BLC7[3:0]				FRC7[1:0]		DLC7[1:0]	
18h	R/W	D1	BLD1[3:0]				FRD1[1:0]		DLD1[1:0]	
19h	R/W	D2	BLD2[3:0]				FRD2[1:0]		DLD2[1:0]	
1Ah	R/W	D3	BLD3[3:0]				FRD3[1:0]		DLD3[1:0]	
1Bh	R/W	D4	BLD4[3:0]				FRD4[1:0]		DLD4[1:0]	
1Ch	R/W	D5	BLD5[3:0]				FRD5[1:0]		DLD5[1:0]	
1Dh	R/W	D6	BLD6[3:0]				FRD6[1:0]		DLD6[1:0]	
1Eh	R/W	D7	BLD7[3:0]				FRD7[1:0]		DLD7[1:0]	
1Fh	R/W	E1	BLE1[3:0]				FRE1[1:0]		DLE1[1:0]	
20h	R/W	E2	BLE2[3:0]				FRE2[1:0]		DLE2[1:0]	
21h	R/W	E3	BLE3[3:0]				FRE3[1:0]		DLE3[1:0]	
22h	R/W	E4	BLE4[3:0]				FRE4[1:0]		DLE4[1:0]	
23h	R/W	E5	BLE5[3:0]				FRE5[1:0]		DLE5[1:0]	
24h	R/W	E6	BLE6[3:0]				FRE6[1:0]		DLE6[1:0]	
25h	R/W	E7	BLE7[3:0]				FRE7[1:0]		DLE7[1:0]	

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OPERATION (continued)

2. Register Map (2) (continued)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
26h	R/W	F1	BLF1[3:0]				FRF1[1:0]		DLF1[1:0]	
27h	R/W	F2	BLF2[3:0]				FRF2[1:0]		DLF2[1:0]	
28h	R/W	F3	BLF3[3:0]				FRF3[1:0]		DLF3[1:0]	
29h	R/W	F4	BLF4[3:0]				FRF4[1:0]		DLF4[1:0]	
2Ah	R/W	F5	BLF5[3:0]				FRF5[1:0]		DLF5[1:0]	
2Bh	R/W	F6	BLF6[3:0]				FRF6[1:0]		DLF6[1:0]	
2Ch	R/W	F7	BLF7[3:0]				FRF7[1:0]		DLF7[1:0]	
2Dh	R/W	G1	BLG1[3:0]				FRG1[1:0]		DLG1[1:0]	
2Eh	R/W	G2	BLG2[3:0]				FRG2[1:0]		DLG2[1:0]	
2Fh	R/W	G3	BLG3[3:0]				FRG3[1:0]		DLG3[1:0]	
30h	R/W	G4	BLG4[3:0]				FRG4[1:0]		DLG4[1:0]	
31h	R/W	G5	BLG5[3:0]				FRG5[1:0]		DLG5[1:0]	
32h	R/W	G6	BLG6[3:0]				FRG6[1:0]		DLG6[1:0]	
33h	R/W	G7	BLG7[3:0]				FRG7[1:0]		DLG7[1:0]	
34h	R/W	H1	BLH1[3:0]				FRH1[1:0]		DLH1[1:0]	
35h	R/W	H2	BLH2[3:0]				FRH2[1:0]		DLH2[1:0]	
36h	R/W	H3	BLH3[3:0]				FRH3[1:0]		DLH3[1:0]	
37h	R/W	H4	BLH4[3:0]				FRH4[1:0]		DLH4[1:0]	
38h	R/W	H5	BLH5[3:0]				FRH5[1:0]		DLH5[1:0]	
39h	R/W	H6	BLH6[3:0]				FRH6[1:0]		DLH6[1:0]	
3Ah	R/W	H7	BLH7[3:0]				FRH7[1:0]		DLH7[1:0]	
3Bh	R/W	I1	BLI1[3:0]				FRI1[1:0]		DLI1[1:0]	
3Ch	R/W	I2	BLI2[3:0]				FRI2[1:0]		DLI2[1:0]	
3Dh	R/W	I3	BLI3[3:0]				FRI3[1:0]		DLI3[1:0]	
3Eh	R/W	I4	BLI4[3:0]				FRI4[1:0]		DLI4[1:0]	
3Fh	R/W	I5	BLI5[3:0]				FRI5[1:0]		DLI5[1:0]	
40h	R/W	I6	BLI6[3:0]				FRI6[1:0]		DLI6[1:0]	
41h	R/W	I7	BLI7[3:0]				FRI7[1:0]		DLI7[1:0]	
42h	R/W	J1	BLJ1[3:0]				FRJ1[1:0]		DLJ1[1:0]	
43h	R/W	J2	BLJ2[3:0]				FRJ2[1:0]		DLJ2[1:0]	
44h	R/W	J3	BLJ3[3:0]				FRJ3[1:0]		DLJ3[1:0]	
45h	R/W	J4	BLJ4[3:0]				FRJ4[1:0]		DLJ4[1:0]	
46h	R/W	J5	BLJ5[3:0]				FRJ5[1:0]		DLJ5[1:0]	
47h	R/W	J6	BLJ6[3:0]				FRJ6[1:0]		DLJ6[1:0]	
48h	R/W	J7	BLJ7[3:0]				FRJ7[1:0]		DLJ7[1:0]	

OPERATION (continued)

2. Register Map (2) (continued)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
49h	R/W	K1	BLK1[3:0]				FRK1[1:0]		DLK1[1:0]	
4Ah	R/W	K2	BLK2[3:0]				FRK2[1:0]		DLK2[1:0]	
4Bh	R/W	K3	BLK3[3:0]				FRK3[1:0]		DLK3[1:0]	
4Ch	R/W	K4	BLK4[3:0]				FRK4[1:0]		DLK4[1:0]	
4Dh	R/W	K5	BLK5[3:0]				FRK5[1:0]		DLK5[1:0]	
4Eh	R/W	K6	BLK6[3:0]				FRK6[1:0]		DLK6[1:0]	
4Fh	R/W	K7	BLK7[3:0]				FRK7[1:0]		DLK7[1:0]	
50h	R/W	L1	BLL1[3:0]				FRL1[1:0]		DLL1[1:0]	
51h	R/W	L2	BLL2[3:0]				FRL2[1:0]		DLL2[1:0]	
52h	R/W	L3	BLL3[3:0]				FRL3[1:0]		DLL3[1:0]	
53h	R/W	L4	BLL4[3:0]				FRL4[1:0]		DLL4[1:0]	
54h	R/W	L5	BLL5[3:0]				FRL5[1:0]		DLL5[1:0]	
55h	R/W	L6	BLL6[3:0]				FRL6[1:0]		DLL6[1:0]	
56h	R/W	L7	BLL7[3:0]				FRL7[1:0]		DLL7[1:0]	
57h	R/W	M1	BLM1[3:0]				FRM1[1:0]		DLM1[1:0]	
58h	R/W	M2	BLM2[3:0]				FRM2[1:0]		DLM2[1:0]	
59h	R/W	M3	BLM3[3:0]				FRM3[1:0]		DLM3[1:0]	
5Ah	R/W	M4	BLM4[3:0]				FRM4[1:0]		DLM4[1:0]	
5Bh	R/W	M5	BLM5[3:0]				FRM5[1:0]		DLM5[1:0]	
5Ch	R/W	M6	BLM6[3:0]				FRM6[1:0]		DLM6[1:0]	
5Dh	R/W	M7	BLM7[3:0]				FRM7[1:0]		DLM7[1:0]	
5Eh	R/W	N1	BLN1[3:0]				FRN1[1:0]		DLN1[1:0]	
5Fh	R/W	N2	BLN2[3:0]				FRN2[1:0]		DLN2[1:0]	
60h	R/W	N3	BLN3[3:0]				FRN3[1:0]		DLN3[1:0]	
61h	R/W	N4	BLN4[3:0]				FRN4[1:0]		DLN4[1:0]	
62h	R/W	N5	BLN5[3:0]				FRN5[1:0]		DLN5[1:0]	
63h	R/W	N6	BLN6[3:0]				FRN6[1:0]		DLN6[1:0]	
64h	R/W	N7	BLN7[3:0]				FRN7[1:0]		DLN7[1:0]	
65h	R/W	O1	BLO1[3:0]				FRO1[1:0]		DLO1[1:0]	
66h	R/W	O2	BLO2[3:0]				FRO2[1:0]		DLO2[1:0]	
67h	R/W	O3	BLO3[3:0]				FRO3[1:0]		DLO3[1:0]	
68h	R/W	O4	BLO4[3:0]				FRO4[1:0]		DLO4[1:0]	
69h	R/W	O5	BLO5[3:0]				FRO5[1:0]		DLO5[1:0]	
6Ah	R/W	O6	BLO6[3:0]				FRO6[1:0]		DLO6[1:0]	
6Bh	R/W	O7	BLO7[3:0]				FRO7[1:0]		DLO7[1:0]	

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OPERATION (continued)

2. Register Map (2) (continued)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
6Ch	R/W	P1	BLP1[3:0]				FRP1[1:0]		DLP1[1:0]	
6Dh	R/W	P2	BLP2[3:0]				FRP2[1:0]		DLP2[1:0]	
6Eh	R/W	P3	BLP3[3:0]				FRP3[1:0]		DLP3[1:0]	
6Fh	R/W	P4	BLP4[3:0]				FRP4[1:0]		DLP4[1:0]	
70h	R/W	P5	BLP5[3:0]				FRP5[1:0]		DLP5[1:0]	
71h	R/W	P6	BLP6[3:0]				FRP6[1:0]		DLP6[1:0]	
72h	R/W	P7	BLP7[3:0]				FRP7[1:0]		DLP7[1:0]	
73h	R/W	Q1	BLQ1[3:0]				FRQ1[1:0]		DLQ1[1:0]	
74h	R/W	Q2	BLQ2[3:0]				FRQ2[1:0]		DLQ2[1:0]	
75h	R/W	Q3	BLQ3[3:0]				FRQ3[1:0]		DLQ3[1:0]	
76h	R/W	Q4	BLQ4[3:0]				FRQ4[1:0]		DLQ4[1:0]	
77h	R/W	Q5	BLQ5[3:0]				FRQ5[1:0]		DLQ5[1:0]	
78h	R/W	Q6	BLQ6[3:0]				FRQ6[1:0]		DLQ6[1:0]	
79h	R/W	Q7	BLQ7[3:0]				FRQ7[1:0]		DLQ7[1:0]	

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OPERATION (continued)

3. Register Map (1) Detail descriptions

Address 01h to 13h

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
01h MAPCHG	Data name	—	—	—	—	—	—	—	MAPCHG
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : MAPCHG Register Map selection bit

[0] : Register selection for matrix default setup control (default)

It is possible to access Address 01h to 13h described in Register Map (1) (Page 20).

[1] : RAM1, RAM2 selection bit, Address selection for RAM1, RAM2 data setup

It is possible to access Address 01h to 79h described in Register Map (2) (Page 21 to Page 24).

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
02h POWERCNT	Data name	—	—	—	—	—	—	—	OSCEN
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : OSCEN ON/OFF bit for internal oscillators

[0] : Internal oscillator is OFF (default)

[1] : Internal oscillator is ON

The variation width of an internal oscillator is set to 0.96 MHz to 1.44 MHz.

The variation width of an internal clock is set to 694.4 ns to 1,042 ns.

When 01hD0 : MAPCHG = "0“ is set, this address is effective.