## : ©hipsmall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation, and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!


## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email \& Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, \#122 Zhenhua RD., Futian, Shenzhen, China

## 7 x 7 Dots Matrix LED Driver LSI

## FEATURES

- $7 \times 7$ LED Matrix Driver
(Total LED that can be driven $=49$ )
- Built-in memory (ROM and RAM)
- LDO
: 2-ch
- SPI Interface : 1-ch
- Driver for RGB color unit : 1-ch
- 44 pin Plastic Quad Flat Non-leaded package (QFN Type)


## DESCRIPTION

AN32058A is 49 Dots Matrix LED Driver. It can drive up to 16 RGB LEDs.

## APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.


## TYPICAL APPLICATION



Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

## Panasonic

## CONTENTS

- FEATURES ..... 1
- DESCRIPTION ..... 1
- APPLICATIONS ..... 1
- TYPICAL APPLICATION ..... 1
- CONTENTS ..... 2
■ ABSOLUTE MAXIMUM RATINGS ..... 3
- POWER DISSIPATION RATING ..... 3
■ RECOMMENDED OPERATING CONDITIONS ..... 4
- ELECTRICAL CHARACTERISTICS ..... 5
- PIN CONFIGURATION ..... 13
- PIN FUNCTIONS ..... 14
■ FUNCTIONAL BLOCK DIAGRAM ..... 16
- OPERATION ..... 17
- PACKAGE INFORMATION ..... 63
■ IMPORTANT NOTICE ..... 64

Doc No. TA4-EA-04725
Revision. 3

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit | Note |
| :---: | :---: | :---: | :---: | :---: |
| Supply voltage | $V^{\text {M }}$ MAX | 6.0 | V | *1 |
|  | VLED ${ }_{\text {MAX }}$ | 6.5 | V | *1 |
| Operating ambience temperature | $\mathrm{T}_{\text {opr }}$ | -30 to +85 | ${ }^{\circ} \mathrm{C}$ | *2 |
| Operating junction temperature | $\mathrm{T}_{\mathrm{j}}$ | -30 to +125 | ${ }^{\circ} \mathrm{C}$ | *2 |
| Storage temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ | *2 |
| Input Voltage Range | LEDCTL, RSTB, CE, CLK, DI | -0.3 to 3.4 | V | - |
|  | LDOCNT | -0.3 to 6.0 | V | - |
| Output Voltage Range | INT, DO | -0.3 to 3.4 | V | - |
|  | $\begin{gathered} \mathrm{R}, \mathrm{G}, \mathrm{~B} \\ \text { LDO1, LDO2, } \\ \mathrm{X} 0, \mathrm{X} 1, \mathrm{X} 2, \mathrm{X} 3, \mathrm{X} 4, \mathrm{X} 5, \mathrm{X} 6, \\ \mathrm{Y} 0, \mathrm{Y} 1, \mathrm{Y} 2, \mathrm{Y} 3, \mathrm{Y} 4, \mathrm{Y} 5, \mathrm{Y} 6 \end{gathered}$ | -0.3 to 6.5 | V | - |
| ESD | HBM (Human Body Model) | 2.0 | kV | - |

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1 $\mathrm{VB}_{\mathrm{MAX}}=\mathrm{VB}, \mathrm{VLED}_{\text {max }}=\mathrm{VLED} 1$ = VLED2.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2 Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for $\mathrm{Ta}=25^{\circ} \mathrm{C}$.

## POWER DISSIPATION RATING

| PACKAGE | $\theta^{\mathrm{JA}}$ | $\mathbf{P}_{\mathrm{D}}\left(\mathbf{T a = 2 5}{ }^{\circ} \mathbf{C}\right)$ | $\mathbf{P}_{\mathrm{D}}\left(\mathbf{T a}=\mathbf{8 5}{ }^{\circ} \mathbf{C}\right)$ |
| :---: | :---: | :---: | :---: |
| 44 pin Plastic Quad Flat Non-leaded package (QFN Type) | $71.8^{\circ} \mathrm{C} / \mathrm{W}$ | 1.392 W | 0.557 W |

Note) For the actual usage, please refer to the $P_{D}-$ Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

## CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply voltage range | VB | 3.1 | 3.7 | 4.6 | V | *1 |
|  | VLED | 3.1 | 5.0 | 5.6 | V | *1 |
| Input Voltage Range | LEDCTL, RSTB, CE, CLK, DI | -0.3 | - | 3.0 | V | - |
|  | LDOCNT | -0.3 | - | $\mathrm{VB}+0.3$ | V | *2 |
| Output Voltage Range | INT, DO | -0.3 | - | 3.0 | V | - |
|  | $\begin{gathered} \text { R, G, B, } \\ \text { LDO1, LDO2, } \\ \mathrm{X0}, \mathrm{X} 1, \mathrm{X} 2, \mathrm{X} 3, \mathrm{X} 4, \mathrm{X} 5, \mathrm{X} 6, \\ \mathrm{Y} 0, \mathrm{Y} 1, \mathrm{Y} 2, \mathrm{Y} 3, \mathrm{Y} 4, \mathrm{Y} 5, \mathrm{Y} 6 \end{gathered}$ | -0.3 | - | VLED + 0.3 | V | *2 |

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation. Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, RGBGND and PGND. VB is voltage for VB. VLED is voltage for VLED1 and VLED2.
*2: ( $\mathrm{VB}+0.3$ ) V must not exceed 6 V . ( $\mathrm{VLED}+0.3$ ) V must not exceed 6.5 V .

## ELECTRICAL CHARACTERISTICS

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Current consumption |  |  |  |  |  |  |  |
| Current consumption (1) | ICC1 | At OFF mode LDOCNT = Low | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| Current consumption (2) | ICC2 | At Standby mode LDOCNT = Low LDO2 is active. | - | 8 | 12 | $\mu \mathrm{A}$ | - |
| Current consumption (3) | ICC3 | LDOCNT = High <br> LDO1 and LDO2 are active. | - | 18 | 24 | $\mu \mathrm{A}$ | - |
| Reference voltage |  |  |  |  |  |  |  |
| Output voltage | VREF | $\mathrm{I}_{\text {VREF }}=0 \mu \mathrm{~A}$ | 1.21 | 1.24 | 1.27 | V | - |
| Reference current |  |  |  |  |  |  |  |
| Output voltage | VIREF | $\mathrm{I}_{\text {REF }}=0 \mu \mathrm{~A}$ | 0.44 | 0.54 | 0.64 | V | - |
| Voltage regulator (LDO1) |  |  |  |  |  |  |  |
| Output voltage | VL1 | $\mathrm{I}_{\text {LDO } 1}=-30 \mathrm{~mA}$ | 1.79 | 1.85 | 1.91 | V | - |
| Short circuit protection current | IPT1 | $\begin{aligned} & \text { LDOCNT }=\text { High } \\ & \text { REG18 }=\text { High } \\ & \mathrm{V}_{\mathrm{LDO1}}=0 \mathrm{~V}, \mathrm{IPT} 1=\mathrm{I}_{\mathrm{LDO} 1} \end{aligned}$ | 50 | 100 | 200 | mA | - |
| Ripple rejection (1) | PSL11 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=1 \mathrm{kHz} \\ & \mathrm{l}_{\mathrm{LDO} 1}=-15 \mathrm{~mA} \\ & \mathrm{PSL} 11=20 \log \left(\mathrm{acV}_{\mathrm{LDO} 1} / 0.2\right) \end{aligned}$ | - | -45 | -40 | dB | - |
| Ripple rejection (2) | PSL12 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=10 \mathrm{kHz} \\ & \mathrm{l}_{\mathrm{LDO} 1}=-15 \mathrm{~mA} \\ & \text { PSL12 }=20 \log \left(\mathrm{ac}_{\mathrm{LDO} 1} / 0.2\right) \end{aligned}$ | - | -35 | -25 | dB | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Voltage regulator (LDO2) |  |  |  |  |  |  |  |
| Output voltage | VL2 | $\mathrm{I}_{\text {LDO2 }}=-30 \mathrm{~mA}$ | 2.76 | 2.85 | 2.94 | V | - |
| Short circuit protection current | IPT2 | $\begin{aligned} & \text { LDOCNT }=\text { High } \\ & V_{\text {LDO2 }}=0 \mathrm{~V} \\ & \text { IPT2 }=I_{\text {LDO2 }} \end{aligned}$ | 50 | 100 | 300 | mA | - |
| Ripple rejection (1) | PSL21 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=1 \mathrm{kHz} \\ & \mathrm{I}_{\mathrm{LDO2}}=-15 \mathrm{~mA} \\ & \mathrm{PSL} 21=20 \log \left(\mathrm{acV}_{\mathrm{LDO2}} / 0.2\right) \end{aligned}$ | - | -35 | -30 | dB | - |
| Ripple rejection (2) | PSL22 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=10 \mathrm{kHz} \\ & \mathrm{l}_{\mathrm{LDO2}}=-15 \mathrm{~mA} \\ & \mathrm{PSL} 22=20 \log \left(\mathrm{acV}_{\mathrm{LDO} 2} / 0.2\right) \end{aligned}$ | - | -25 | -15 | dB | - |
| Oscillator |  |  |  |  |  |  |  |
| Oscillation frequency | FDC | - | 0.96 | 1.20 | 1.44 | MHz | - |
| SCAN Switch |  |  |  |  |  |  |  |
| Resistance at the Switch ON | RSCAN | $\mathrm{I}_{\mathrm{YO}, \mathrm{Y} 1, \mathrm{Y} 2, Y 3, Y 4, Y 5, Y 6}=5 \mathrm{~mA}$ RSCAN $=\mathrm{V}_{\mathrm{YO}, \mathrm{Y} 1, \mathrm{Y} 2, \mathrm{Y} 3, Y 4, \mathrm{Y}_{5}, \mathrm{Y} 6} / 5 \mathrm{~mA}$ | - | 2 | 4.8 | $\Omega$ | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Current generator (For $7 \times 7$ dots matrix LED) |  |  |  |  |  |  |  |
| Output current (1) | IMX1 | At 1 mA setup $\begin{aligned} & V_{\mathrm{x0}, \mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3, \mathrm{x} 4, \mathrm{x} 5, \mathrm{x} 6}=1 \mathrm{~V} \\ & \mathrm{IMX1}=I_{\mathrm{x} 0, \mathrm{x} 1, \mathrm{x} 2, x_{3}, \mathrm{x} 4, \mathrm{x} 5, \mathrm{x} 6} \end{aligned}$ | 0.950 | 1.033 | 1.116 | mA | *1 |
| Output current (2) | IMX2 | At 2 mA setup $\begin{aligned} & V_{x 0, x 1, x 2, x 3, x_{4}, x_{5}, x 6}=1 \mathrm{~V} \\ & \mathrm{IMX2}=I_{\mathrm{x} 0, x_{1}, x_{2}, x_{3}, x 4, x 5, x 6} \end{aligned}$ | 1.907 | 2.073 | 2.239 | mA | *1 |
| Output current (3) | IMX4 | At 4 mA setup $\begin{aligned} & V_{x 0, x 1, x 2, x 3, x 4, x 5, x 6}=1 \mathrm{~V} \\ & \mathrm{IMX4}=I_{\mathrm{x0}, \mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3, \mathrm{x} 4, \mathrm{x} 5, \mathrm{x} 6} \end{aligned}$ | 3.824 | 4.157 | 4.490 | mA | *1 |
| Output current (4) | IMX8 | At 8 mA setup $\begin{aligned} & V_{\mathrm{x0}, \mathrm{x} 1, \mathrm{x} 2, x_{3}, x_{4}, x_{5}, x_{6}}=1 \mathrm{~V} \\ & \mathrm{IMX8}=I_{\mathrm{x} 0, x_{1}, x_{2}, x_{3}, x 4, x 5, x 6} \end{aligned}$ | 7.660 | 8.326 | 8.992 | mA | *1 |
| Output current (5) | IMX15 | At 15 mA setup $\begin{aligned} & V_{x 0, x 1, x 2, x 3, x 4, x 5, x 6}=1 \mathrm{~V} \\ & \text { IMX15 }=I_{x 0, x 1, x 2, x 3, x 4, x 5, x 6} \end{aligned}$ | 14.408 | 15.661 | 16.914 | mA | *1 |
| Leakage Current when matrix LED turns off | IMXOFF | Current OFF setup $\begin{aligned} & V_{\mathrm{x0}, \mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3, \mathrm{x} 4, \mathrm{x} 5, \mathrm{x} 6}=4.75 \mathrm{~V} \\ & \text { IMXOFF }=I_{\mathrm{x} 0, \mathrm{x} 1, \mathrm{x} 2, \mathrm{x} 3, \mathrm{x} 4, \mathrm{x}, \mathrm{x} 6} \end{aligned}$ | - | - | 1 | $\mu \mathrm{A}$ | - |
| The error between channels | IMXCH | The average value of all channels, and the current error of each channel | -5 | - | 5 | \% | - |

*1: Values when recommended parts (ERJ2RHD273X) are used for IREF terminal. The other current settings are combination of above items.

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Current generator (For RGB color unit) |  |  |  |  |  |  |  |
| Output current (1) | IRGB1 | At 1 mA setup $V_{R, G, B}=1 \mathrm{~V}$ | 0.949 | 1.031 | 1.113 | mA | *1 |
| Output current (2) | IRGB2 | At 2 mA setup $V_{R, G, B}=1 \mathrm{~V}$ | 1.892 | 2.056 | 2.220 | mA | *1 |
| Output current (3) | IRGB4 | At 4 mA setup $V_{R, G, B}=1 \mathrm{~V}$ | 3.764 | 4.091 | 4.418 | mA | *1 |
| Output current (4) | IRGB8 | At 8 mA setup $V_{R, G, B}=1 \mathrm{~V}$ | 7.510 | 8.163 | 8.816 | mA | *1 |
| Leakage Current when RGB turn off | IRGBOFF | Current OFF setup $\begin{aligned} & \mathrm{V}_{\mathrm{R}, \mathrm{G}, \mathrm{~B}}=4.75 \mathrm{~V} \\ & \mathrm{IRGBOFF}=\mathrm{I}_{\mathrm{R}, \mathrm{G}, \mathrm{~B}} \end{aligned}$ | - | - | 1 | $\mu \mathrm{A}$ | - |
| The error between channels | IRGBCH | The average value of all channels, and the current error of each channel | -5 | - | 5 | \% | - |

*1: Values when recommended parts (ERJ2RHD273X) are used for IREF terminal.
The other current settings are combination of above items.

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| SPI I/F, LEDCTL, RSTB |  |  |  |  |  |  |  |
| Input voltage range of Highlevel | VIH | High-level recognition voltage | $\begin{gathered} \text { LDO1 } \\ \times 0.8 \end{gathered}$ | - | $\begin{aligned} & \text { LDO2 } \\ & +0.3 \end{aligned}$ | V | - |
| Input voltage range of Lowlevel | VIL | Low-level recognition voltage | -0.3 | - | 0.4 | V | - |
| Input current of High-level | IIH | $\begin{aligned} & \mathrm{V}_{\text {LEDCTL, RSTB, CE }} \text { CLK, DI }=1.85 \mathrm{~V} \\ & \text { IIH }=\mathrm{I}_{\text {LEDCTL, }} \text { RSTB, CE, CLK, DI } \end{aligned}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| Input current of Low-level | IIL | $\begin{aligned} & \mathrm{V}_{\text {LEDCTL, RSTB, }} \text { CSB, CLK, DI }=0 \mathrm{~V} \\ & \text { IIL }=\mathrm{I}_{\text {LEDCTL, }} \text { RSTB, CE, CLK, DI } \end{aligned}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| INT |  |  |  |  |  |  |  |
| Output voltage of High-level (1) | VOH1 | $\begin{aligned} & \mathrm{I}_{\mathrm{INT}}=-2 \mathrm{~mA} \\ & \mathrm{VDDSEL}=\mathrm{LDO} 2 \end{aligned}$ | $\begin{gathered} \mathrm{LDO} 2 \\ \times 0.8 \end{gathered}$ | - | - | V | - |
| Output voltage of Low-level (1) | VOL1 | $\begin{aligned} & \mathrm{I}_{\mathrm{INT}=2 \mathrm{~mA}} \\ & \mathrm{VDDSEL}=\mathrm{LDO} 2 \\ & \left(\mathrm{I}_{\mathrm{INT}}=0.5 \mathrm{~mA}\right) \end{aligned}$ | - | - | $\begin{gathered} \text { LDO2 } \\ \times 0.2 \\ (0.15) \end{gathered}$ | V | - |
| Output voltage of High-level (2) | VOH2 | $\begin{aligned} & \mathrm{l}_{\mathrm{INT}}=-2 \mathrm{~mA} \\ & \mathrm{VDDSEL}=\mathrm{LDO1} \end{aligned}$ | $\begin{array}{r} \text { LDO1 } \\ \times 0.8 \end{array}$ | - | - | V | - |
| Output voltage of Low-level (2) | VOL2 | $\begin{aligned} & \mathrm{I}_{\mathrm{INT}}=2 \mathrm{~mA} \\ & \mathrm{VDDSEL}=\mathrm{LDO} 1 \\ & \left(\mathrm{I}_{\mathrm{INT}}=0.5 \mathrm{~mA}\right) \end{aligned}$ | - | - | $\begin{gathered} \text { LDO1 } \\ \times 0.3 \\ (0.15) \end{gathered}$ | V | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| LDOCNT |  |  |  |  |  |  |  |
| Input voltage range of High-level | VIH | High-level recognition voltage | $\begin{gathered} \text { VB } \\ \times 0.7 \end{gathered}$ | - | $\begin{gathered} \text { VB } \\ +0.3 \end{gathered}$ | V | - |
| Input voltage range of Low-level | VIL | Low-level recognition voltage | -0.3 | - | 0.4 | V | - |
| Input current of High-level | IIH | $\begin{aligned} & \mathrm{V}_{\text {LDOCNT }}=3.6 \mathrm{~V} \\ & \mathrm{IIH}=\mathrm{I}_{\text {LDOCNT }} \end{aligned}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| Input current of Low-level | IIL | $\begin{aligned} & \mathrm{V}_{\text {LDOCNT }}=0 \mathrm{~V} \\ & \text { IIL }=\mathrm{I}_{\text {LDOCNT }} \end{aligned}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| DO |  |  |  |  |  |  |  |
| Output voltage of High-level | VOH | $\mathrm{I}_{\mathrm{DO}}=-2 \mathrm{~mA}$ | $\begin{gathered} \text { LDO1 } \\ \times 0.8 \end{gathered}$ | - | - | V | - |
| Output voltage of Low-level | VOL | $\mathrm{I}_{\mathrm{DO}}=2 \mathrm{~mA}$ | - | - | $\begin{aligned} & \text { LDO1 } \\ & \times 0.2 \end{aligned}$ | V | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Voltage regulator (LDO1) Output capacitor $1 \mu \mathrm{~F}$, Output capacitor's ESR less than $0.1 \Omega$ |  |  |  |  |  |  |  |
| Rise time | Tsu1 | Time until output voltage reaches to 0 V to $90 \%$ | - | 0.25 | - | ms | $\begin{aligned} & * 2 \\ & * 3 \end{aligned}$ |
| Fall time | Tsd1 | Time until output voltage reaches to $10 \%$ | - | 5 | - | ms | $\begin{aligned} & \text { *2 } \\ & \text { *3 } \end{aligned}$ |
| Maximum load current | IOMAX1 | - | - | 15 | - | mA | *3 |
| Load transient response (1) | Vtr11 | $\mathrm{I}_{\text {LDO1 }}=-50 \mu \mathrm{~A} \rightarrow-15 \mathrm{~mA}(1 \mu \mathrm{~s})$ | - | 70 | - | mV | *3 |
| Load transient response (2) | Vtr12 | $\mathrm{I}_{\text {LDO1 }}=-15 \mathrm{~mA} \rightarrow-50 \mu \mathrm{~A}(1 \mu \mathrm{~s})$ | - | 70 | - | mV | *3 |
| Voltage regulator (LDO2) Output capacitor $1 \mu \mathrm{~F}$, Output capacitor's ESR less than $0.1 \Omega$ |  |  |  |  |  |  |  |
| Rise time | Tsu2 | Time until output voltage reaches to 0 V to $90 \%$ | - | 0.25 | - | ms | $\begin{aligned} & \text { *2 } \\ & \text { *3 } \end{aligned}$ |
| Fall time | Tsd2 | Time until output voltage reaches to $10 \%$ | - | 5 | - | ms | $\begin{aligned} & \text { *2 } \\ & \text { *3 } \end{aligned}$ |
| Maximum load current | IOMAX2 | - | - | 15 | - | mA | *3 |
| Load transient response (1) | Vtr21 | $\mathrm{I}_{\text {LDO2 }}=-50 \mu \mathrm{~A} \rightarrow-15 \mathrm{~mA}(1 \mu \mathrm{~s})$ | - | 70 | - | mV | *3 |
| Load transient response (2) | Vtr22 | $\mathrm{I}_{\text {LDO2 }}=-15 \mathrm{~mA} \rightarrow-50 \mu \mathrm{~A}(1 \mu \mathrm{~s})$ | - | 70 | - | mV | *3 |
| TSD (Thermal shutdown circuit) |  |  |  |  |  |  |  |
| Detection temperature | Tdet | Temperature which LDO1, LDO2, Constant current circuit, Matrix SW and RGB turns off. | - | 160 | - | ${ }^{\circ} \mathrm{C}$ | $\begin{aligned} & * 3 \\ & * 4 \end{aligned}$ |
| Return temperature | Tsd11 | Returning temperature | - | 110 | - | ${ }^{\circ} \mathrm{C}$ | *3 |

Note) *2: Rise time and Fall time are defined as below.
Actual evaluation result of rise time : LDO1: 290 to $400 \mu \mathrm{~s}, \quad$ LDO2: 220 to $310 \mu \mathrm{~s}$
Actual evaluation result of fall time : LDO1: 6.2 to $8.5 \mathrm{~ms}, \quad$ LDO2 : 5.8 to 7.9 ms
*3 : Typical Design Value
*4 : LDO1, LDO2, Constant current circuit, and Matrix SW and RGB are turned off when TSD is High.
When TSD is High, the register is set as $14 \mathrm{hD1}=1$. However, data can be read only when the register is read immediately after INT occurs since internal regulator is turned off.
*5 : Only LDO1 and LDO2 return after ON state of TSD. A logic part will be in Reset state.


## Panasonic

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=3.6 \mathrm{~V}, \mathrm{VLED} 1=\mathrm{VLED} 2=4.9 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified.

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Microcomputer interface characteristic (Vdd = 1.85 V $\pm$ \% \%) Write access Timing |  |  |  |  |  |  |  |
| CLK cycle time | tscyc1 | - | - | 125 | - | ns | *3 |
| CLK cycle time High period | twhc1 | - | - | 60 | - | ns | *3 |
| CLK cycle time Low period | twlc1 | - | - | 60 | - | ns | *3 |
| Serial-data setup time | tss1 | - | - | 62 | - | ns | *3 |
| Serial-data hold time | tsh1 | - | - | 62 | - | ns | *3 |
| Transceiver interval | tcsw1 | - | - | 62 | - | ns | *3 |
| Chip enable setup time | tcss1 | - | - | 5 | - | ns | *3 |
| Chip enable hold time | tcgh1 | - | - | 5 | - | ns | *3 |

Microcomputer interface characteristic (Vdd $=1.85 \mathrm{~V} \pm 3 \%$ ) Read access Timing

| CLK cycle time | tscyc1 | - | - | 125 | - | ns | $* 3$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CLK cycle time High period | twhc1 | - | - | 60 | - | ns | $* 3$ |
| CLK cycle time Low period | twlc1 | - | - | 60 | - | ns | $* 3$ |
| Serial-data setup time | tss1 | - | - | 62 | - | ns | $* 3$ |
| Serial-data hold time | tsh1 | - | - | 62 | - | ns | $* 3$ |
| Transceiver interval | tcsw1 | - | - | 62 | - | ns | $* 3$ |
| Chip enable setup time | tcss1 | - | - | 5 | - | ns | $* 3$ |
| Chip enable hold time | tcgh1 | - | - | 5 | - | ns | $* 3$ |
| DC delay time | tdodly1 | Only read mode | - | 25 | - | ns | $* 3$ |

Note) *3: Typical Design Value


## PIN CONFIGURATION

Top View


Doc No. TA4-EA-04725
Revision. 3

PIN FUNCTIONS

| Pin No. | Pin name | Type | Description |
| :---: | :---: | :---: | :---: |
| $\begin{gathered} \hline 1 \\ 10 \\ 11 \\ 12 \\ 22 \\ 23 \\ 32 \\ 33 \\ 44 \end{gathered}$ | N.C. | - | No Connection |
| 2 | VB | Power supply | The power supply's connect terminal for BGR circuit and LDO circuit. |
| 3 | LDO1 | Output | LDO1 ( 1.85 V ) output terminal. |
| 4 | RSTB | Input | Reset input terminal ("L" active ) |
| 5 | IREF | Output | The resistance connect terminal for constant current value setup. |
| 6 | LDOCNT | Input | ON/OFF control terminal of LDO1 and LDO2. |
| 7 | VREFD | Output | BGR circuit output terminal. |
| 8 | AGND | Ground | The GND terminal for Analog circuitry. |
| 9 | Y6 | Output | The output terminal of matrix switching control. It connects with the G Column of matrix LED. |
| $\begin{aligned} & 13 \\ & 18 \end{aligned}$ | VLED2 VLED1 | Power supply | The power supply's connect terminal for matrix LED. Connect with the output of battery or step-up DC/DC converter |
| 14 | Y5 | Output | The output terminal of matrix switching control. It connects with the F Column of matrix LED. |
| 15 | Y4 | Output | The output terminal of matrix switching control. It connects with the E Column of matrix LED. |
| 16 | Y3 | Output | The output terminal of matrix switching control. It connects with the D Column of matrix LED. |
| 17 | Y2 | Output | The output terminal of matrix switching control. It connects with the C Column of matrix LED. |
| 19 | Y1 | Output | The output terminal of matrix switching control. It connects with the B Column of matrix LED. |
| 20 | Y0 | Output | The output terminal of matrix switching control. It connects with the A Column of matrix LED. |
| 21 | LEDCTL | Input | LED's lighting ON/OFF control terminal. ( It is based on register OAh.) |

AN32058A

PIN FUNCTIONS (continued)

| Pin No. | Pin name | Type | Description |
| :---: | :---: | :---: | :---: |
| 24 | X0 | Output | Constant current circuit. The output terminal of PWM control. It connects with the 1st Row of matrix LED. |
| 25 | X1 | Output | Constant current circuit. The output terminal of PWM control. It connects with the 2nd Row of matrix LED. |
| 26 | X2 | Output | Constant current circuit. The output terminal of PWM control. It connects with the 3rd Row of matrix LED. |
| 27 | X3 | Output | Constant current circuit. The output terminal of PWM control. It connects with the 4th Row of matrix LED. |
| 28 | PGND | Ground | The GND terminal for matrix LED |
| 29 | X4 | Output | Constant current circuit. The output terminal of PWM control. It connects with the 5th Row of matrix LED. |
| 30 | X5 | Output | Constant current circuit. The output terminal of PWM control. It connects with the 6th Row of matrix LED. |
| 31 | X6 | Output | Constant current circuit. The output terminal of PWM control. It connects with the 7th Row of matrix LED. |
| 34 | R | Output | LED contact terminal. |
| 35 | RGBGND | Ground | The GND terminal for RGB terminal. |
| 36 | G | Output | LED contact terminal. |
| 37 | B | Output | LED contact terminal. |
| 38 | DO | Output | Data output terminal for SPI interface. |
| 39 | DI | Input | Data input terminal for SPI interface. |
| 40 | CLK | Input | Clock input terminal for SPI interface. |
| 41 | CE | Input | Chip-enable terminal for SPI1 interface. ("H" active ) |
| 42 | INT | Output | Interrupt output terminal. |
| 43 | LDO2 | Output | LDO2 ( 2.85 V ) output terminal. |

## FUNCTIONAL BLOCK DIAGRAM



Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

## OPERATION

1. Explanation in each mode (Power supply starting sequence)

\begin{tabular}{|c|c|c|c|c|}
\hline Mode \& LDOCNT \& REG18 \& REG28 \& Note <br>
\hline OFF \& Low \& 0 \& 0 \& - It is necessary to make it LDOCNT $=$ High for the return from OFF-mode. <br>
\hline OFF $\rightarrow$ Normal mode \& "L" $\rightarrow$ "H" \& $0 / 1$

$0 / 1$ \& $0 / 1$

$0 / 1$ \& | - The signal from serial interface is not received in LDOCNT = Low and the state of REG28 = Low or REG18 = Low. |
| :--- |
| - It shifts to standby mode with LDOCNT = Low and REG28 = High. |
| - The signal from serial interface is not received at Standby-mode. (Power supply for Logic is LDO1 and LDO2.) Therefore, standby release by the signal from serial interface cannot be performed. |
| - In Standby-mode, if LDOCNT is switched to High from Low, it will return to the normal mode. |
| - It cannot shift to OFF-mode from Standby-mode. Once returning to the normal mode, please shift to OFF-mode. | <br>


\hline | Normal mode |
| :--- |
| $\rightarrow$ |
| OFF | \& \& 0 \& 0 \& \multirow[t]{2}{*}{| - Regardless of the value of REG18, LDO1 turns on at LDOCNT = High. |
| :--- |
| - Regardless of the value of REG28, LDO2 turns on at LDOCNT = High. |
| - Serial interface signal is not received at RSTB = Low |
| - 5 ms after being set to LDOCNT = High, the receptionist of serial interface signal is attained. |
| - RSTB terminal prohibits the input signal of those other than a rectangle wave. |
| - All register setting become default setting if RSTB = Low |
| - (The default setting of REG18 and REG28 are [1] |
| - If RSTB = Low before LDOCNT = Low, LDO1 and LDO2 can't turn off. ) |
| - All register setting become default setting when LDO2 turn off. |
| - The setting order to change off mode is as following. |
| - REG18, $28=[0] \rightarrow$ LDOCNT $=$ "L" $\rightarrow$ RSTB $=$ "L" |} <br>

\hline Normal mode $\rightarrow$ Standby mode \& "H" $\rightarrow$ "L" \& 0 \& 1 \& <br>
\hline
\end{tabular}

Doc No. TA4-EA-04725
Revision. 3

AN32058A

## OPERATION (continued)

## 1. Explanation in each mode (Power supply starting sequence) (continued)

- Shift to the Normal mode from OFF-mode

- Shift to the Normal mode from Standby mode

* It is a waveform in the case of applying reset to register setup at Standby mode.
* Maintain the state of RSTB = High to hold the register setup.

Established : 2007-05-24
Revised : 2013-04-15

AN32058A

## OPERATION (continued)

## 1. Explanation in each mode (Power supply starting sequence) (continued)

- Shift to the OFF-mode from Normal mode

- Shift to the Standby mode from Normal mode


Established : 2007-05-24
Revised

AN32058A

## OPERATION (continued)

## 1. Explanation in each mode (Power supply starting sequence) (continued)

- Shift to the OFF-mode from Normal mode

| VBAT | LDOCNT | MODE |
| :---: | :---: | :---: |
| "L" | "L" | OFF |
| "L" | "H" | Prohibition |
| "H" | "L" | OFF |
| "H" | "H" | ON |

Note) "L" in column of VBAT and LDOCNT means 0 V , "H" means 3.1 to 4.6 V ( operating supply voltage range ).

- Logic pin condition

The following setting is common for OFF, Standby and Normal mode.
The pin setting when RSTB = Low, under Normal mode is as follows.

| Pin name | Pin state | Logic* |
| :---: | :---: | :---: |
| INT | Output | "L" |
| CE | Input | "L" |
| CLK | Input | "L" |
| DI | Input | "L" |
| DO | Output | "L" |
| LEDCTL | Input | "L" |
| LDOCNT | Input | Depends on each mode |

[^0]AN32058A

## OPERATION (continued)

## 2. Explanation of operation

- Matrix part operation waveform
- The following waveform is an internal signal. In following $Y x=X x=$ Low, the waveform of actual $Y x$ terminal is set to $\mathrm{Hi}-\mathrm{Z}$.
- It is controlled by internal 1.2 MHz clock in default condition.
- $Y$ side switches from $Y 0$ to $Y 6$ in that order. The turning on term of each pin is constant 945 clock ( $787.5 \mu \mathrm{~s}$ ) and each turning on term includes 8clock ( $6.67 \mu \mathrm{~s}$ ) interval.
- "*" mark shows the turning on term and D3, D6 is the turning off term in the following figure.
- $7 \times 7$ matrix display is controlled by X 0 to X 6 with Yx switching timing.



## OPERATION (continued)

## 3. Block configuration

- RESET part block configuration


All the logic portions to which the power supply is not connected are connected to VB as power supplies.

Established : 2007-05-24
Revised : 2013-04-15

## OPERATION (continued)

## 3. Block configuration (continued)

- Explanation of matrix LED part, matrix LED's number
- LED matrix driver circuit can display character and pattern by controlling the $7 \times 7$ matrix LED individually.
- In this specification, LED's number controlled by each terminal can be matched off against the following figure.
- It is controlled by internal 1.2 MHz clock in default condition.
- In the scroll mode, LED matrix can move the display of character from right to left as the following arrangement.


AN32058A

## OPERATION (continued)

## 3. Block configuration (continued)

- Equivalent circuit of matrix LED driver

X0 terminal case


- The reference current for constant current driver is calculated by the following formula.

$$
\mathrm{V}(\mathrm{IREF}) / \mathrm{R}(\mathrm{IREF})=0.54 \mathrm{~V} / 27 \mathrm{k} \Omega=20 \mu \mathrm{~A}
$$

- The LED driver current can be set from 0 mA to 30 mA by register setting via serial interface.
- The constant current value can be changed by the external resistor value of IREF terminal, but the accuracy in case of that setting is not guaranteed.
- ERJ2RHD273X is recommended for the external resistor of IREF terminal to keep the constant current accuracy.

Doc No. TA4-EA-04725
Revision. 3

AN32058A

## OPERATION (continued)

4. Register and Address

- Register Map

| Sub address | R/W | Data name | Data |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01h | W | POWERCNT | - | - | - | - | - | OSCEN | - | - |
| 02h | W | LDOCNT | - | - | - | - | - | - | REG18 | REG28 |
| 03h | For test |  |  |  |  |  |  |  |  |  |
| 04h | For test |  |  |  |  |  |  |  |  |  |
| 05h | For test |  |  |  |  |  |  |  |  |  |
| 06h | For test |  |  |  |  |  |  |  |  |  |
| 07h | For test |  |  |  |  |  |  |  |  |  |
| 08h | For test |  |  |  |  |  |  |  |  |  |
| 09h | For test |  |  |  |  |  |  |  |  |  |
| 0A餪 | W | LEDCTL | LEDACT | - | - | - | - | DISMTX | DISRGB | - |
| 10h | For test |  |  |  |  |  |  |  |  |  |
| 11h | For test |  |  |  |  |  |  |  |  |  |
| 12h | For test |  |  |  |  |  |  |  |  |  |
| 13h | For test |  |  |  |  |  |  |  |  |  |
| 14h | R | IOFACTOR | FACGD1 | - | - | - | $\begin{aligned} & \text { RAM } \\ & \text { ACT } \end{aligned}$ | FRMINT | CPUWRER | TSD |
| 15h | For test |  |  |  |  |  |  |  |  |  |
| 16h | For test |  |  |  |  |  |  |  |  |  |
| 17h | For test |  |  |  |  |  |  |  |  |  |
| 18h | For test |  |  |  |  |  |  |  |  |  |
| 19h | For test |  |  |  |  |  |  |  |  |  |
| 1Ah | W/R | VDDSEL | INTVSEL | - | - | - | - | - | - | - |

Established : 2007-05-24
Revised


[^0]:    Note)*: Logic state for pins indicated as "Output" under Pin state shows the output level.
    Logic state for pins indicated as "Input" under Pin state shows the input level to be set to the pins.

