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# LED Driver LSI with Step-up Charge Pump Control Circuit 

## FEATURES

- $7 \times 7$ LED Matrix Driver
(Total LED that can be driven $=49$ )
- Step-up charge pump DC/DC converter : 300 mA
- LDO : 2-ch.
- GPIO : 3-ch.
- GPO : 6-ch. (They are in common with LED driver terminals.)
- SPI interface / $\mathrm{I}^{2} \mathrm{C}$ interface selectable
- LED drivers (for backlight : 7-ch., for RGB : 3-ch., matrix LED driver : $7 \times 7$-ch.)
- LED brightness control function with an external illumination sensor
- 55pin Wafer Level Chip Size Package (WLCSP)


## DESCRIPTION

AN32150B is a LED driver and a light intensity controller. It can drive up to 7 channels of LCD backlight, 3 channels of RGB LEDs and 7 channels of LED matrix.
Voltage is supplied by a step-up charge pump DC/DC converter.

## APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.


## TYPICAL APPLICATION



Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

## Panasonic

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## Panasonic

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit | Note |
| :---: | :---: | :---: | :---: | :---: |
| Supply voltage | $\mathrm{VB}_{\text {MAX }}$ | 6.0 | V | *1 |
|  | VLED ${ }_{\text {MAX }}$ | 6.5 | V | *1 |
|  | $\mathrm{VDD}_{\text {MAX }}$ | 4.3 | V | *1 |
| Operating ambience temperature | $\mathrm{T}_{\text {opr }}$ | -30 to +85 | ${ }^{\circ} \mathrm{C}$ | *2 |
| Operating junction temperature | $\mathrm{T}_{\mathrm{j}}$ | -30 to +125 | ${ }^{\circ} \mathrm{C}$ | *2 |
| Storage temperature | $\mathrm{T}_{\text {stg }}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ | *2 |
| Input Voltage Range | GPIO1, GPIO2, GPIO3, PD2, PD3, SERSEL, SLAVE, SCL, SDA | -0.3 to 4.3 | V | - |
|  | NRESET, LDOCNT | -0.3 to 6.0 | V | - |
| Output Voltage Range | PD1 | -0.3 to 4.3 | V | - |
|  | LDO1, LDO2, INT | -0.3 to 6.0 | V | - |
|  | SW1, SW2, SW3, SW4, SW5, SW6, SW7, LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11, LED12, LED13, LED14, LED15, LED16, LED17 | -0.3 to 6.5 | V | - |
| ESD | HBM | 1.0 to 1.5 | kV | - |

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1: $\mathrm{VB}_{\mathrm{MAX}}=\mathrm{VBCP}=\mathrm{VB}, \mathrm{VDD}_{\mathrm{MAX}}=\mathrm{VDD}, \mathrm{VLED}_{\mathrm{MAX}}=\mathrm{VLED}$
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C}$.

POWER DISSIPATION RATING

| PACKAGE | $\theta_{\text {JA }}$ | $\mathbf{P}_{\mathrm{D}}\left(\mathbf{T a}=\mathbf{2 5}{ }^{\circ} \mathbf{C}\right)$ | $\mathbf{P}_{\mathrm{D}}\left(\mathbf{T a}=\mathbf{8 5}{ }^{\circ} \mathbf{C}\right)$ |
| :---: | :---: | :---: | :---: |
| 55 pin Wafer Level Chip Size Package (WLCSP) | $120.02^{\circ} \mathrm{C} / \mathrm{W}$ | 0.833 W | 0.333 W |

Note) For the actual usage, please refer to the $P_{D}$-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

## CAUTION

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Supply voltage range | VB | 3.1 | 3.6 | 4.6 | V | *1 |
|  | VLED | 3.1 | 4.5 | 5.8 | V | *1 |
|  | VDD | 1.7 | 1.85 | 3.2 | V | *1 |
| Input Voltage Range | GPIO1, GPIO2, GPIO3, PD2, PD3, SERSEL, SLAVE, SCL, SDA | -0.3 | - | VDD + 0.3 | V | *2 |
|  | NRESET, LDOCNT | -0.3 | - | $V B+0.3$ | V | *2 |
| Output Voltage Range | PD1 | -0.3 | - | VDD + 0.3 | V | *2 |
|  | LDO1, LDO2, INT | -0.3 | - | $V B+0.3$ | V | *2 |
|  | SW1, SW2, SW3, SW4, SW5, SW6, SW7, <br> LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11, LED12, LED13, LED14, LED15, LED16, LED17 | -0.3 | - | VLED + 0.3 | V | *2 |

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, CPGND, LEDGND1, LEDGND2 and LEDGND3.

VDD is voltage for VDD. VB is voltage for VB and VBCP. VLED is voltage for VLED.
*2: (VDD + 0.3) V must not exceed 4.3 V . ( $\mathrm{VB}+0.3$ ) V must not exceed 6 V .
(VLED + 0.3) V must not exceed 6.5 V.

AN32150B

## ELECTRICAL CHARACTERISTICS

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Current consumption |  |  |  |  |  |  |  |
| Current consumption (1) at OFF mode | ICC1 | $\begin{aligned} & \mathrm{VB}=4.6 \mathrm{~V} \\ & \mathrm{LDOCNT}=\text { Low } \end{aligned}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| Current consumption (2) at LDO1 and LDO2 normal mode | ICC2 | LDO1 to 2PS = [0] <br> (LDO1, 2 normal mode) <br> LDO1ON = [1] (LDO1 ON) <br> $\mathrm{VB}=4.6 \mathrm{~V}$ <br> LDOCNT = High | - | 130 | 300 | $\mu \mathrm{A}$ | - |
| Current consumption (3) at LDO1 OFF mode, LDO2 power save mode | ICC3 | LDO2 PS = [1] <br> (LDO2 power save mode) LDO1ON $=$ [0] (LDO1 OFF) $\mathrm{VB}=4.6 \mathrm{~V}$ <br> LDOCNT = High | - | 10 | 25 | $\mu \mathrm{A}$ | - |
| Current consumption (4) at VB through mode, LDO1 OFF mode, LDO2 power save mode | ICC4 | LDO2 PS = [1] <br> (LDO2 power save mode) LDO1ON = [0] (LDO1 OFF) $\mathrm{VB}=4.6 \mathrm{~V}$ LDOCNT = High <br> VB through mode $\mathrm{I}_{\mathrm{CPOUT}}=0 \mathrm{~mA}$ <br> LED10ON = [1] (Current 0) | - | 1.0 | 3.0 | mA | - |
| Current consumption (5) at charge pump $1.5 \times$ ( 600 kHz operating) mode, LDO1 OFF mode, LDO2 power save mode | ICC5 | LDO2 PS = [1] <br> (LDO2 power save mode) LDO1ON = [0] (LDO1 OFF) $\mathrm{VB}=3.1 \mathrm{~V}$ LDOCNT = High LED10ON = [1] (current 0) Charge Pump ON, $1.5 \times$, 600 kHz operating mode $\mathrm{I}_{\text {CPOUT }}=0 \mathrm{~mA}$ | - | 2.0 | 5.0 | mA | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Current consumption |  |  |  |  |  |  |  |
| Current consumption (6) at charge pump $1.5 \times$ <br> (1.2 MHz operating) mode, <br> LDO1 OFF mode, <br> LDO2 power save mode | ICC6 | LDO2 PS = [1] <br> (LDO2 power save mode) <br> LDO1ON = [0] (LDO1 OFF) <br> $\mathrm{VB}=3.1 \mathrm{~V}$ <br> LDOCNT = High <br> LED10ON = [1] (current 0) <br> Charge Pump ON, $1.5 \times$, <br> 1.2 MHz operating mode $I_{\text {CPOUT }}=0 \mathrm{~mA}$ | - | 5.0 | 9.0 | mA | - |
| Reference voltage |  |  |  |  |  |  |  |
| Output voltage | VREF | $\mathrm{VB}=3.1 \mathrm{~V}$ to 4.6 V | 1.21 | 1.24 | 1.27 | V | - |
| Voltage regulator (LDO1) normal mode loutmax $=\mathbf{- 1 0 0} \mathrm{mA}$ |  |  |  |  |  |  |  |
| Output voltage (1) 1.85 V mode | VL11 | $\begin{aligned} & \mathrm{VB}=3.1 \mathrm{~V} \text { to } 4.6 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LDO} 1}=-10 \mu \mathrm{~A} \text { to }-100 \mathrm{~mA} \end{aligned}$ | 1.79 | 1.85 | 1.91 | V | - |
| Output voltage (2) 2.85 V mode | VL12 | $\begin{aligned} & \mathrm{VB}=3.1 \mathrm{~V} \text { to } 4.6 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LDO} 1}=-10 \mu \mathrm{~A} \text { to }-100 \mathrm{~mA} \end{aligned}$ | 2.76 | 2.85 | 2.94 | V | - |
| Short circuit protection current (1) 1.85 V mode | IPT11 | LDOCNT = High $\mathrm{V}_{\mathrm{LDO} 1}=0 \mathrm{~V}$ | 20 | 50 | 150 | mA | - |
| Short circuit protection current (2) 2.85 V mode | IPT12 | $\begin{aligned} & \text { LDOCNT }=\text { High } \\ & \mathrm{V}_{\mathrm{LDO} 1}=0 \mathrm{~V} \end{aligned}$ | 20 | 50 | 150 | mA | - |
| Ripple rejection (1) 1.85 V mode | PSL11 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=1 \mathrm{kHz} \\ & \mathrm{l}_{\mathrm{LDO} 1}=-50 \mathrm{~mA} \\ & \mathrm{PSL} 11=20 \log \left(\mathrm{acV}_{\mathrm{LDO} 1} / 0.2\right) \end{aligned}$ | - | -70 | -60 | dB | - |
| Ripple rejection (2) 1.85 V mode | PSL12 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=10 \mathrm{kHz} \\ & \mathrm{l}_{\mathrm{LDO} 1}=-50 \mathrm{~mA} \\ & \mathrm{PSL} 12=20 \log \left(\mathrm{acV}_{\mathrm{LDO} 1} / 0.2\right) \end{aligned}$ | - | -60 | -50 | dB | - |
| Ripple rejection (3) 2.85 V mode | PSL13 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=1 \mathrm{kHz} \\ & \mathrm{l}_{\mathrm{LDO} 1}=-50 \mathrm{~mA} \\ & \mathrm{PSL} 13=20 \log \left(\mathrm{ac}_{\mathrm{LDO} 1} / 0.2\right) \end{aligned}$ | - | -70 | -60 | dB | - |
| Ripple rejection (4) 2.85 V mode | PSL14 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=10 \mathrm{kHz} \\ & \mathrm{I}_{\mathrm{LDO} 1}=-50 \mathrm{~mA} \\ & \text { PSL14 }=20 \log \left(\mathrm{acV}_{\mathrm{LDO} 1} / 0.2\right) \end{aligned}$ | - | -60 | -50 | dB | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Voltage regulator (LDO1) power save mode : loutmax $=-15 \mathrm{~mA}$ (loutmax $=-5 \mathrm{~mA}$ at 2.85 V setting) |  |  |  |  |  |  |  |
| Output voltage (1) | VLPS11 | $\begin{aligned} & \mathrm{VB}=3.1 \mathrm{~V} \text { to } 4.6 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LDO} 1}=-10 \mu \mathrm{~A} \text { to }-15 \mathrm{~mA} \end{aligned}$ | 1.79 | 1.85 | 1.91 | V | - |
| Output voltage (2) | VLPS12 | $\begin{aligned} & \begin{array}{l} \mathrm{VB}=3.1 \mathrm{~V} \text { to } 4.6 \mathrm{~V} \\ \mathrm{I}_{\mathrm{LDO} 1}=-10 \mu \mathrm{to}-5 \mathrm{~mA} \\ \hline \end{array}{ }^{2}=1 \end{aligned}$ | 2.76 | 2.85 | 2.94 | V | - |
| Voltage regulator (LDO2) normal mode loutmax $=\mathbf{- 1 0 0} \mathrm{mA}$ |  |  |  |  |  |  |  |
| Output voltage | VL2 | $\begin{aligned} & \mathrm{VB}=3.1 \mathrm{~V} \text { to } 4.6 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LDO} 2}=-10 \mu \mathrm{~A} \text { to }-100 \mathrm{~mA} \end{aligned}$ | 2.76 | 2.85 | 2.94 | V | - |
| Short circuit protection current | IPT2 | $\begin{aligned} & \text { LDOCNT }=\text { High } \\ & \mathrm{V}_{\text {LDO2 } 2}=0 \mathrm{~V} \end{aligned}$ | 20 | 50 | 150 | mA | - |
| Ripple rejection (1) | PSL21 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=1 \mathrm{kHz} \\ & \mathrm{~L} \mathrm{LDO2}=-50 \mathrm{~mA} \\ & \mathrm{PSL} 21=20 \log \left(\mathrm{ac} \mathrm{~V}_{\mathrm{LDO2}} / 0.2\right) \end{aligned}$ | - | -70 | -60 | dB | - |
| Ripple rejection (2) | PSL22 | $\begin{aligned} & \mathrm{VB}=3.6 \mathrm{~V}+0.2 \mathrm{~V}[\mathrm{p}-\mathrm{p}] \\ & \mathrm{f}=10 \mathrm{kHz} \\ & \mathrm{~L} \text { LDo2 }=-50 \mathrm{~mA} \\ & \mathrm{PSL} 22=20 \log \left(\mathrm{ac} \mathrm{~V}_{\mathrm{LDO} 2} / 0.2\right) \end{aligned}$ | - | -60 | - 50 | dB | - |
| Voltage regulator (LDO2) power save mode loutmax $=-5 \mathrm{~mA}$ |  |  |  |  |  |  |  |
| Output voltage | VLPS2 | $\begin{aligned} & \mathrm{VB}=3.1 \mathrm{~V} \text { to } 4.6 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{LDO} 2}=-10 \mu \mathrm{to}-5 \mathrm{~mA} \end{aligned}$ | 2.76 | 2.85 | 2.94 | V | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Charge pump DC/DC converter |  |  |  |  |  |  |  |
| Oscillator frequency | FDC1 | $\mathrm{VB}=3.1 \mathrm{~V}$ to 4.6 V | 1.92 | 2.40 | 2.88 | MHz | - |
| VB through switch |  |  |  |  |  |  |  |
| Resistance at switch ON | RVBS | $\begin{aligned} & \mathrm{VB}=4.5 \mathrm{~V} \\ & \mathrm{I}_{\text {CPOUT }}=-30 \mathrm{~mA} \\ & \mathrm{RVBS}=\left(\mathrm{V}_{\text {VBCP }}-\mathrm{V}_{\text {CPOUT }}\right) / 30 \\ & \mathrm{~mA} \end{aligned}$ | - | 0.6 | 1 | $\Omega$ | - |
| SCAN switch |  |  |  |  |  |  |  |
| Resistance at switch ON | RSCAN | $\begin{aligned} & \mathrm{VLED}=4.5 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{SW} 1} \text { to } \mathrm{I}_{\mathrm{SW} 7}=20 \mathrm{~mA} \\ & \mathrm{RSCAN}=\mathrm{V}_{\mathrm{SW} 1} \text { to } \mathrm{V}_{\mathrm{SW} 7} / 20 \\ & \mathrm{~mA} \end{aligned}$ | - | 1 | 2 | $\Omega$ | - |
| Current regulator (LED1 to 7) |  |  |  |  |  |  |  |
| Output current (1) | IBL1 | At 31.750 mA setting <br> $\mathrm{V}_{\text {LED } 1}$ to $\mathrm{V}_{\text {LED } 7}=1 \mathrm{~V}$ <br> $\mathrm{IBL} 1=\mathrm{I}_{\text {LED } 1}$ to $\mathrm{I}_{\text {LED7 }}$ | 30.132 | 31.718 | 33.304 | mA | *1 |
| Output current (2) | IBL2 | At 1 mA setting $\mathrm{V}_{\text {LED1 }}$ to $\mathrm{V}_{\text {LED } 7}=1 \mathrm{~V}$ IBL2 $=\mathrm{I}_{\text {LED1 }}$ to $\mathrm{I}_{\text {LED } 7}$ | 0.948 | 0.998 | 1.048 | mA | *1 |
| Current step | IBSTEP | Minimum current step | 0 | 125 | 250 | $\mu \mathrm{A}$ | - |
| Off leak current | IBLOFF | OFF setting <br> $\mathrm{V}_{\text {LED } 1}$ to $\mathrm{V}_{\text {LED } 7}=4.5 \mathrm{~V}$ <br> IBLOFF $=\mathrm{I}_{\text {LED } 1}$ to $\mathrm{I}_{\text {LED } 7}$ | - | - | 1 | $\mu \mathrm{A}$ | - |
| Error between channels | IBLCH | At 16 mA setting Current error between each channel and the median of LED1 to LED7 | -5 | - | 5 | \% | - |

Note) *1: Allowable value at the time when the recommended parts (ERJ2RHD393X) is connected to IREF.

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Current regulator (LED8 to 10) |  |  |  |  |  |  |  |
| Output current (1) | IRGB1 | At 31.750 mA setting <br> $\mathrm{V}_{\mathrm{LEDB}}$ to $\mathrm{V}_{\mathrm{LED} 10}=1 \mathrm{~V}$ <br> IRGB1 $=I_{\text {LED } 8}$ to $I_{\text {LED10 }}$ | 30.087 | 31.671 | 33.254 | mA | *1 |
| Output current (2) | IRGB2 | At 1 mA setting $\mathrm{V}_{\text {LED } 8}$ to $\mathrm{V}_{\text {LED } 10}=1 \mathrm{~V}$ IRGB2 $=I_{\text {LED } 8}$ to $I_{\text {LED10 }}$ | 0.946 | 0.996 | 1.046 | mA | *1 |
| Current step | IRGBSTEP | Minimum current step | 0 | 125 | 250 | $\mu \mathrm{A}$ | - |
| Off leak current | IRGBOFF | OFF setting <br> $\mathrm{V}_{\text {LEDB }}$ to $\mathrm{V}_{\text {LED10 }}=4.5 \mathrm{~V}$ <br> IRGBOFF $=I_{\text {LED }}$ to $I_{\text {LED10 }}$ | - | - | 1 | $\mu \mathrm{A}$ | - |
| Error between channels | IRGBCH | At 16 mA setting Current error between each channel and the median of LED8 to LED10 | -5 | - | 5 | \% | - |
| Current regulator (LED11 to 17) |  |  |  |  |  |  |  |
| Output current (1) | IMX1 | $\begin{aligned} & \text { At } 1 \mathrm{~mA} \text { setting } \\ & \mathrm{V}_{\text {LED11 }} \text { to } \mathrm{V}_{\text {LED17 }}=1 \mathrm{~V} \\ & \text { IMX1 }=\mathrm{I}_{\text {LED11 }} \text { to } \mathrm{I}_{\text {LED17 }} \end{aligned}$ | 0.943 | 0.993 | 1.043 | mA | *1 |
| Output current (2) | IMX2 | At 2 mA setting <br> $\mathrm{V}_{\text {LED11 }}$ to $\mathrm{V}_{\text {LED17 }}=1 \mathrm{~V}$ <br> IMX2 $=\mathrm{I}_{\text {LED11 }}$ to $\mathrm{I}_{\text {LED17 }}$ | 1.891 | 1.990 | 2.090 | mA | *1 |
| Output current (3) | IMX3 | $\begin{aligned} & \text { At } 4 \mathrm{~mA} \text { setting } \\ & \mathrm{V}_{\text {LED11 }} \text { to } \mathrm{V}_{\text {LED17 }}=1 \mathrm{~V} \\ & \text { IMX3 }=\mathrm{I}_{\text {LED11 }} \text { to } \mathrm{I}_{\text {LED17 }} \end{aligned}$ | 3.768 | 3.966 | 4.164 | mA | *1 |
| Output current (4) | IMX4 | At 8 mA setting <br> $\mathrm{V}_{\text {LED11 }}$ to $\mathrm{V}_{\text {LED17 }}=1 \mathrm{~V}$ <br> IMX4 $==\mathrm{I}_{\text {LED11 }}$ to $\mathrm{I}_{\text {LED17 }}$ | 7.558 | 7.956 | 8.354 | mA | *1 |
| Output current (5) | IMX5 | At 15 mA setting <br> $\mathrm{V}_{\text {LED11 }}$ to $\mathrm{V}_{\text {LED17 }}=1 \mathrm{~V}$ <br> IMX5 $==\mathrm{I}_{\text {LED11 }}$ to $\mathrm{I}_{\text {LED17 }}$ | 14.172 | 14.918 | 15.663 | mA | *1 |
| Off leak current | IMXOFF | OFF setting $\mathrm{V}_{\text {LED11 }}$ to $\mathrm{V}_{\text {LED17 }}=4.5 \mathrm{~V}$ IMXOFF $=\mathrm{I}_{\text {LED11 }}$ to $\mathrm{I}_{\text {LED17 }}$ | - | - | 1 | $\mu \mathrm{A}$ | - |
| Error between channels | IMXCH | At 15 mA setting Current error between each channel and the median of LED11 to LED17 | -5 | - | 5 | \% | - |

Note) *1: Allowable value at the time when the recommended parts (ERJ2RHD393X) is connected to IREF.

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2{ }^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Overvoltage detection |  |  |  |  |  |  |  |
| Detection voltage | VOV | Charge pump DC/DC overvoltage detection | 5.3 | 5.5 | 5.7 | V | - |
| Step-up mode switch of charge pump |  |  |  |  |  |  |  |
| Detection voltage (1) | VLD1 | LED1 to LED7 pin voltage at the time when the step-up mode switch of charge pump changes | - | 0.35 | 0.40 | V | - |
| Detection voltage (2) | VLD2 | LED8, 9 and 10 pin voltage at the time when the step-up mode switch of charge pump changes | - | 0.35 | 0.40 | V | - |
| Minimum voltage at which LED driver can keep constant current value |  |  |  |  |  |  |  |
| Minimum voltage at which LED driver can keep constant current value | VLD3 | 95\% LED current value at the time when LED1 to LED17 pin voltage is set to 1 V . Minimum value of LED1 to LED17 pin voltage | - | 0.20 | 0.35 | V | - |



## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter |  | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min |  | Typ | Max |  |  |
| GPIO I/F |  |  |  |  |  |  |  |  |
|  | High-level input voltage range (1) at 1.85 V mode operation |  | VIH1 | High-level recognition voltage of GPIO1 to 3. <br> IOVSEL1 to 3 = [1] <br> (Output voltage LDO1 level setting) LDO1VSEL = [0] | 1.5 | - | $\begin{aligned} & \text { LDO1 } \\ & +0.3 \end{aligned}$ | V | - |
|  | Low-level input voltage range (1) at 1.85 V mode operation | VIL1 | Low-level recognition voltage of GPIO1 to 3. <br> IOVSEL1 to 3 = [1] <br> (Output voltage LDO1 level setting) LDO1VSEL $=$ [0] | -0.3 | - | 0.4 | V | - |
|  | High-level input voltage range (2) at 2.85 V mode operation | VIH2 | High-level recognition voltage of GPIO1 to 3. <br> LDO1VSEL = [1] | 2.3 | - | $\begin{aligned} & \text { LDO1 } \\ & +0.3 \end{aligned}$ | V | - |
|  | Low-level input voltage range (2) at 2.85 V mode operation | VIL2 | Low-level recognition voltage of GPIO1 to 3 . LDO1VSEL = [1] | -0.3 | - | 0.6 | V | - |
|  | High-level input current | IIH1 | $\mathrm{V}_{\mathrm{GPIO} 1}$ to $\mathrm{V}_{\mathrm{GPIO} 3}=2.85 \mathrm{~V}$ $\mathrm{IIH} 1=\mathrm{I}_{\text {GPIO } 1}$ to $\mathrm{I}_{\text {GPIO3 }}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
|  | Low-level input current | IIL1 | $\mathrm{V}_{\text {GPIO } 1}$ to $\mathrm{V}_{\text {GPIO3 }}=0 \mathrm{~V}$ <br> IIL1 $=I_{\text {GPIO1 }}$ to $I_{\text {GPIO3 }}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
|  | High-level output voltage (1) | VOH1 | $\mathrm{V}_{\mathrm{GPIO} 1}$ to $\mathrm{V}_{\text {GPIO3 }}=-2 \mathrm{~mA}$ IOVSEL1 to 3 = [0] <br> (Output voltage LDO2 level setting) | $\begin{gathered} \text { LDO2 } \\ \times 0.8 \end{gathered}$ | - | - | V | - |
|  | Low-level output voltage (1) | VOL1 | $\mathrm{I}_{\text {GPIO } 1}$ to $\mathrm{I}_{\text {GPIO3 }}=2 \mathrm{~mA}$ IOVSEL1 to 3 = [0] <br> (Output voltage LDO2 level setting) | - | - | $\begin{array}{\|c} \mathrm{LDO} 2 \\ \times 0.2 \end{array}$ | V | - |
|  | High-level output voltage (2) | VOH2 | $\mathrm{I}_{\mathrm{GPIO} 1}$ to $\mathrm{I}_{\mathrm{GPIO} 3}=-2 \mathrm{~mA}$ IOVSEL1 to 3 = [1] <br> (Output voltage LDO1 level setting) | $\begin{array}{r} \text { LDO1 } \\ \times 0.8 \end{array}$ | - | - | V | - |
|  | Low-level output voltage (2) | VOL2 | $\mathrm{I}_{\text {GPIO } 1}$ to $\mathrm{I}_{\text {GPIO3 }}=2 \mathrm{~mA}$ IOVSEL1 ~ 3 = [1] <br> (Output voltage LDO1 level setting) | - | - | $\begin{gathered} \text { LDO1 } \\ \times 0.2 \end{gathered}$ | V | - |
|  | Pull-down resistance | RPD | $\begin{aligned} & \mathrm{I}_{\mathrm{GPIO} 1} \text { to } \mathrm{I}_{\mathrm{GPIO} 3}=5 \mu \mathrm{~A} \\ & \mathrm{RPD}=\mathrm{V}_{\mathrm{GPIO} 1} \text { to } \mathrm{V}_{\mathrm{GPIO} 3} / 5 \mu \mathrm{~A} \end{aligned}$ | 60 | 110 | 210 | k $\Omega$ | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2{ }^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| LDOCNT |  |  |  |  |  |  |  |
| High-level input voltage range | VIH3 | High-level recognition voltage | 1.6 | - | $\begin{gathered} \text { VB } \\ +0.3 \end{gathered}$ | V | - |
| Low-level input voltage range | VIL3 | Low-level recognition voltage | $-0.3$ | - | 0.4 | V | - |
| High-level input current | IIH2 | $\mathrm{V}_{\text {LDOCNT }}=3.6 \mathrm{~V}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| Low-level input current | IIL2 | $\mathrm{V}_{\text {LDOCNT }}=0 \mathrm{~V}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| NRESET |  |  |  |  |  |  |  |
| High-level input voltage range | VIH4 | High-level recognition voltage | 1.5 | - | $\begin{gathered} \text { VB } \\ +0.3 \end{gathered}$ | V | - |
| Low-level input voltage range | VIL4 | Low-level recognition voltage | $-0.3$ | - | 0.6 | V | - |
| High-level input current | IIH3 | $\mathrm{V}_{\text {NRESET }}=3.6 \mathrm{~V}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| Low-level input current | IIL3 | $\mathrm{V}_{\text {NRESET }}=0 \mathrm{~V}$ | - | 0 | 1 | $\mu \mathrm{A}$ | - |
| INT |  |  |  |  |  |  |  |
| ON resistance | RINTON | $\begin{aligned} & \mathrm{I}_{\mathrm{INT}}=5 \mathrm{~mA} \\ & \mathrm{RINTON}^{2}=\mathrm{V}_{\mathrm{INT}} / 5 \mathrm{~mA} \end{aligned}$ | - | - | 50 | $\Omega$ | - |

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| $\mathrm{I}^{2} \mathrm{C}$ I/F |  |  |  |  |  |  |  |
| High-level input voltage | VIH5 | High-level recognition voltage of SDA, SCL | $\begin{aligned} & 0.7 \times \\ & \text { VDD } \end{aligned}$ | - | $\begin{gathered} \text { VDD } \\ +0.5 \\ 3.2 \end{gathered}$ | V | *2 |
| Low-level input voltage | VIL5 | Low-level recognition voltage of SDA, SCL | -0.5 | - | $\begin{aligned} & 0.3 \times \\ & \text { VDD } \end{aligned}$ | V | - |
| Low-level output voltage 1 | VOL3 | $\begin{aligned} & \mathrm{VDD}>2 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{SDA}}=3 \mathrm{~mA} \end{aligned}$ | 0 | - | 0.4 | V | - |
| Low-level output voltage 2 | VOL4 | $\begin{aligned} & \mathrm{VDD}<2 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{SDA}}=3 \mathrm{~mA} \end{aligned}$ | 0 | - | $\begin{aligned} & 0.2 \times \\ & \text { VDD } \end{aligned}$ | V | - |
| Input current each I/O pin | li | $\mathrm{V}_{\text {SDA }}, \mathrm{V}_{\mathrm{SCL}}=0.1 \mathrm{~V}$ to 2.88 V | - 10 | 0 | 10 | $\mu \mathrm{A}$ | - |
| SCL clock frequency | $\mathrm{f}_{\text {SCL }}$ | - | 0 | - | 400 | kHz | - |
| Light Intensity Control |  |  |  |  |  |  |  |
| PD1 pin ON resistance | RPD10N | - | - | - | 100 | $\Omega$ | - |
| PD3 pin ON resistance | RPD3ON | - | - | - | 50 | $\Omega$ | - |
| A/D converted value (1) | AD1 | $\mathrm{V}_{\mathrm{PD} 2}=\mathrm{VLPS} 2 / 256$ <br> Read value of the register, ADC_DATA[9:2] | - | 1 | 5 | LSB | - |
| A/D converted value (2) | AD2 | $V_{P D 2}=V L P S 2 \times 128 / 256$ <br> Read value of the register, ADC_DATA[9:2] | 124 | 128 | 132 | LSB | - |
| A/D converted value (3) | AD3 | $V_{P D 2}=V L P S 2 \times 255 / 256$ <br> Read value of the register, ADC_DATA[9:2] | 251 | 255 | - | LSB | - |

Note) *2 : Maximum value of High-level input voltage range is the lower one of (VDD +0.5 V ) and 3.2 V .

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| Current consumption |  |  |  |  |  |  |  |
| Current consumption (1) at OFF mode | ICC1 | $\begin{aligned} & \mathrm{VB}=3.1 \mathrm{~V} \text { to } 4.6 \mathrm{~V} \\ & \text { LDOCNT = Low } \end{aligned}$ | - | 0 | - | $\mu \mathrm{A}$ | *3 |
| Current consumption (2) at LDO1 and LDO2 normal mode | ICC2 | LDO1 to 2PS = [0] <br> (LDO1, 2 normal mode) <br> LDO1ON = [1] (LDO1 ON) <br> $\mathrm{VB}=3.1 \mathrm{~V}$ to 4.6 V <br> LDOCNT $=$ High | - | 130 | - | $\mu \mathrm{A}$ | *3 |
| Current consumption (3) at LDO1 OFF mode, LDO2 power save mode | ICC3 | LDO2 PS = [1] <br> (LDO2 power save mode) <br> LDO1ON $=[0]$ (LDO1 OFF) <br> $\mathrm{VB}=3.1 \mathrm{~V}$ to 4.6 V <br> LDOCNT $=$ High | - | 10 | - | $\mu \mathrm{A}$ | *3 |
| Current consumption (4) at VB through mode, LDO1 OFF mode, LDO2 power save mode | ICC4 | LDO2 PS = [1] <br> (LDO2 power save mode) LDO1ON = [0] (LDO1 OFF) <br> $\mathrm{VB}=3.1 \mathrm{~V}$ to 4.6 V <br> LDOCNT $=$ High <br> VB through mode <br> $I_{\text {CPOUT }}=0 \mathrm{~mA}$ <br> LED10ON = [1] (Current 0) | - | 1.0 | - | mA | *3 |

Note) *3 : Typical Design Value

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified


Note) *3 : Typical Design Value

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| $\mathrm{I}^{2} \mathrm{C}$ I/F |  |  |  |  |  |  |  |
| Hysteresis of Schmitt trigger input 1 | Vhys1 | $\mathrm{V}_{\mathrm{DD}}>2 \mathrm{~V},$ <br> Hysteresis voltage of SDA, SCL | $\begin{gathered} 0.05 \times \\ \text { VDD } \end{gathered}$ | - | - | V | *4 |
| Hysteresis of Schmitt trigger input 2 | Vhys2 | $\mathrm{V}_{\mathrm{DD}}<2 \mathrm{~V},$ <br> Hysteresis voltage of SDA, SCL | $\begin{aligned} & 0.1 \times \\ & \text { VDD } \end{aligned}$ | - | - | V | *4 |
| Output fall time from $\mathrm{V}_{\text {IHmin }}$ to $\mathrm{V}_{\text {ILmax }}$ | Tof | Bus capacitance : 10 pF to 400 pF $\mathrm{I}_{\mathrm{P}} \leq 6 \mathrm{~mA}\left(\mathrm{~V}_{\text {OLmax }}=0.6 \mathrm{~V}\right)$ <br> $\mathrm{I}_{\mathrm{P}}$ : Max. sink current | $\begin{gathered} 20+ \\ 0.1 \times C_{b} \end{gathered}$ | - | 250 | ns | *4 |
| Pulse width of spikes which must be suppressed by the input filter | Tsp | - | 0 | - | 50 | ns | *4 |
| Capacitance for each I/O pin | Ci | - | - | - | 10 | pF | *4 |

Note) *4: The timing of Fast-mode Plus devices in I² ${ }^{2}$-bus is specified in Page. 19. All values referred to $\mathrm{V}_{\text {IHmin }}$ and $\mathrm{V}_{\text {ILmax }}$ level.
*5 : These are values checked by design but not production tested.

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| $\mathrm{I}^{2} \mathrm{C}$ I/F (continued) |  |  |  |  |  |  |  |
| Hold time (repeated) | $\mathrm{t}_{\text {HD:STA }}$ | The first clock pulse is generated after thD:STA | 0.6 | - | - | $\mu \mathrm{S}$ | *4 |
| Low period of the SCL clock | tow | - | 1.3 | - | - | $\mu \mathrm{S}$ | *4 |
| High period of the SCL clock | $t_{\text {HIGH }}$ | - | 0.6 | - | - | $\mu \mathrm{S}$ | *4 |
| Set-up time for a repeat START condition | $\mathrm{t}_{\text {SU:STA }}$ | - | 0.6 | - | - | $\mu \mathrm{S}$ | *4 |
| Data hold time | $\mathrm{t}_{\text {HD: }}$ DAT | - | 0 | - | 0.9 | $\mu \mathrm{S}$ | *4 |
| Data set-up time | $\mathrm{t}_{\text {SU:DAT }}$ | - | 100 | - | - | ns | *4 |
| Rise time of both SDA and SCL signals | tr | - | $\begin{gathered} 20+ \\ 0.1 \times C_{b} \end{gathered}$ | - | 300 | ns | *4 |
| Fall time of both SDA and SCL signals | $\mathrm{t}_{\mathrm{f}}$ | - | $\begin{gathered} 20+ \\ 0.1 \times \mathrm{C}_{\mathrm{b}} \end{gathered}$ | - | 300 | ns | $* 4$ $* 5$ |
| Set-up time of STOP condition | $\mathrm{t}_{\text {SU:STO }}$ | - | 0.6 | - | - | $\mu \mathrm{S}$ | *4 |
| Bus free time between a STOP and START condition | $\mathrm{t}_{\text {BUF }}$ | - | 1.3 | - | - | $\mu \mathrm{S}$ | *4 |
| Capacitive load for each bus line | $\mathrm{C}_{\mathrm{b}}$ | - | - | - | 400 | pF | *4 |
| Noise margin at the Low-level for each connected device | $\mathrm{VaL}_{\mathrm{aL}}$ | - | $\begin{aligned} & 0.1 \times \\ & \text { VDD } \end{aligned}$ | - | - | V | *4 |
| Noise margin at the High-level for each connected device | $\mathrm{V}_{\mathrm{aH}}$ | - | $0.2 \times$ VDD | - | - | V | *4 |

Note) *4: The timing of Fast-mode Plus devices in $I^{2} \mathrm{C}$-bus is specified in Page. 19. All values referred to $\mathrm{V}_{\text {IHmin }}$ and $\mathrm{V}_{\text {ILMAX }}$ level. *5 : These are values checked by design but not production tested.

## ELECTRICAL CHARACTERISTICS (continued)

$\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}$
Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified

| Parameter | Symbol | Condition | Limits |  |  | Unit | Note |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| SPI interface characteristics (VDD $=1.85 \mathrm{~V} \pm 3 \%$ ) Reception timing |  |  |  |  |  |  |  |
| SCL cycle time | tscyc1 | - | - | 152 | - | ns | *3 |
| SCL cycle time High period | twhc1 | - | - | 70 | - | ns | *3 |
| SCL cycle time Low period | twlc1 | - | - | 70 | - | ns | *3 |
| Serial data setup time | tss1 | - | - | 62 | - | ns | *3 |
| Serial data hold time | tsh1 | - | - | 62 | - | ns | *3 |
| Transmitting and receiving interval | tcsw1 | - | - | 62 | - | ns | *3 |
| Chip enable setup time | tcss1 | - | - | 5 | - | ns | *3 |
| Chip enable hold time | tcgh1 | - | - | 5 | - | ns | *3 |

SPI interface characteristics (VDD $=1.85 \mathrm{~V} \pm 3 \%$ ) Transmission timing

| SCL cycle time | tscyc1 | - | - | 152 | - | ns | *3 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SCL cycle time High period | twhc1 | - | - | 70 | - | ns | *3 |
| SCL cycle time Low period | twlc1 | - | - | 70 | - | ns | *3 |
| Serial data setup time | tss1 | - | - | 62 | - | ns | *3 |
| Serial data hold time | tsh1 | - | - | 62 | - | ns | *3 |
| Transmitting and receiving interval | tcsw1 | - | - | 62 | - | ns | *3 |
| Chip enable setup time | tcss1 | - | - | 5 | - | ns | *3 |
| Chip enable hold time | tcgh1 | - | - | 5 | - | ns | *3 |
| DC delay time | tdodly1 | Only read mode | - | 30 | - | ns | *3 |

Note) *3 : Typical Design Value
SPI interface timing chart (SERSEL $=$ High)


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## ELECTRICAL CHARACTERISTICS (continued)

$$
\mathrm{VB}=\mathrm{VBCP}=3.6 \mathrm{~V}, \mathrm{VLED}=4.5 \mathrm{~V}, \mathrm{VDD}=1.85 \mathrm{~V}
$$

Note) $\mathrm{T}_{\mathrm{a}}=25^{\circ} \mathrm{C} \pm 2^{\circ} \mathrm{C}$ unless otherwise specified


$$
\begin{aligned}
& V_{\text {ILMAX }}=0.3_{\mathrm{VDD}} \\
& \mathrm{~V}_{\text {IHMIN }}=0.7_{\mathrm{VDD}}
\end{aligned}
$$

S : START condition
Sr : Repeat START condition
P: STOP condition

## PIN CONFIGURATION

TOP VIEW


Doc No. TA4-EA-05344
Revision. 2

## PIN FUNCTIONS

| Pin <br> No. | Pin name | Type | Description | Pin processing at unused |
| :---: | :---: | :---: | :---: | :---: |
| A1 | SW1 | Output | Control switch pin for matrix driver Connected to A column of matrix LED. | Open |
| A2 | LDO2 | Output | LDO2 (2.85 V) output pin | (Required pin) |
| A3 | VB | Power supply | Power supply connection pin for BGR and LDO circuits | (Required pin) |
| A4 | LDO1 | Output | LDO1 (1.85 V / 2.85 V) output pin (Default : 1.85 V output) | (Required pin) |
| A5 | CPOUT | Output | Charge pump output pin (Output pin for VB through SW) | Open |
| A6 | CN1 | Output | Capacitor connection pin for charge pump DC/DC converter | Open |
| A7 | VBCP | Power supply | Power supply connection pin for charge pump DC/DC converter and for through switch | (Required pin) |
| A8 | CPGND | Ground | GND for charge pump DC/DC converter | Connect to GND |
| B1 | SW3 | Output | Control switch pin for matrix driver Connected to C column of matrix LED. | Open |
| B2 | SW2 | Output | Control switch pin for matrix driver Connected to $B$ column of matrix LED. | Open |
| B3 | VREFD | Output | Capacitor connection pin for BGR circuit | (Required pin) |
| B4 | GPIO1 | Input / <br> Output | GPIO input / output port pin (Default input mode with pull-down) | Recommended to connect to GND |
| B5 | CP1 | Output | Capacitor connection pin for charge pump DC/DC converter | Open |
| B6 | CP2 | Output | Capacitor connection pin for charge pump DC/DC converter | Open |
| B7 | CN2 | Output | Capacitor connection pin for charge pump DC/DC converter | Open |
| B8 | IREF | Output | Resistor connection pin for constant current setup | (Required pin) |
| C1 | SW4 | Output | Control switch pin for matrix driver Connected to D column of matrix LED. | Open |
| C2 | VLED | Power supply | Power supply for matrix driver <br> Connected to the output of battery or step-up charge pump DC/DC converter. | Connect to VBAT or CPOUT (Open disabled) |
| C3 | LDOCNT | Input | BGR circuit, ON/OFF control pin of LDO1 and LDO2 | (Required pin) |
| C4 | GPIO2 | Input / Output | GPIO input / output port pin (Default input mode with pull-down) <br> At SERSEL pin = High (SPI mode) : SCE pin | Recommended to connect to GND |
| C5 | GPIO3 | Input / Output | GPIO input / output port pin (Default input mode with pull-down) | Recommended to connect to GND |
| C6 | INT | Output | Interrupt output pin | Open |
| C7 | PD2 | Input | Photo diode connection pin | Connect to GND |
| C8 | PD1 | Output | Photo diode connection pin | Open |
| D1 | SW5 | Output | Control switch pin for matrix driver Connected to E column of matrix LED. | Open |
| D2 | SW6 | Output | Control switch pin for matrix driver Connected to F column of matrix LED. | Open |
| D3 | AGND | Ground | GND for analog block | Connect to GND |
| D4 | NRESET | Input | Reset input pin | (Required pin) |
| D5 | SCL | Input | SPI / ${ }^{2} \mathrm{C}$ interface common clock input pin | (Required pin) |

PIN FUNCTIONS (continued)

| Pin <br> No. | Pin name | Type | Description | Pin processing at unused |
| :---: | :---: | :---: | :---: | :---: |
| D6 | SDA | Input / <br> Output | Data input / output pin for $\mathrm{I}^{2} \mathrm{C}$ interface <br> At SERSEL pin = High (SPI mode) : Data input pin | (Required pin) |
| D7 | VDD | Power supply | Power supply for $\mathrm{I}^{2} \mathrm{C}$ interface | (Required pin) |
| D8 | PD3 | Input | Detection resistor connection pin for photo diode adjustment | Open |
| E1 | SW7 | Output | Control switch pin for matrix driver Connected to G column of matrix LED. | Open |
| $\begin{aligned} & \text { E2 } \\ & \text { E3 } \end{aligned}$ | LEDGND3 LEDGND2 | Ground | GND for matrix LED | Connect to GND |
| E4 | SLAVE | Input / Output | Slave address selection pin for $I^{2} \mathrm{C}$ interface At SERSEL pin = High (SPI mode) : SDO pin | (Required pin) |
| E5 | SERSEL | Input | $1^{2} \mathrm{C} / \mathrm{SPI}$ interface selection pin | Connect to GND or VDD |
| E6 | LEDGND1 | Ground | GND for BL pin | Connect to GND |
| E7 | LED1 | Output | Constant current output pin for LED driver | Open |
| F1 | LED16 | Output | Constant current circuit, PWM control output pin Connected to the 6th row of matrix LED. <br> And GPO (open drain) output pin | Open |
| F2 | LED14 | Output | Constant current circuit, PWM control output pin Connected to the 4th row of matrix LED. | Open |
| F3 | LED12 | Output | Constant current circuit, PWM control output pin Connected to the 2nd row of matrix LED. | Open |
| F4 | LED10 | Output | Constant current output pin for LED driver, and GPO (open drain) output pin | Open |
| F5 | LED8 | Output | Constant current output pin for LED driver, and GPO (open drain) output pin | Open |
| F6 | LED6 | Output | Constant current output pin for LED driver | Open |
| F7 | LED4 | Output | Constant current output pin for LED driver | Open |
| F8 | LED2 | Output | Constant current output pin for LED driver | Open |
| G1 | LED17 | Output | Constant current circuit, PWM control output pin Connected to the 7th row of matrix LED. <br> And GPO (open drain) output pin | Open |
| G2 | LED15 | Output | Constant current circuit, PWM control output pin Connected to the 5th row of matrix LED. <br> And GPO (open drain) output pin | Open |
| G3 | LED13 | Output | Constant current circuit, PWM control output pin Connected to the 3rd row of matrix LED. | Open |
| G4 | LED11 | Output | Constant current circuit, PWM control output pin Connected to the 1st row of matrix LED. | Open |
| G5 | LED9 | Output | Constant current output pin for LED driver, and GPO (open drain) output pin | Open |
| G6 | LED7 | Output | Constant current output pin for LED driver | Open |
| G7 | LED5 | Output | Constant current output pin for LED driver | Open |
| G8 | LED3 | Output | Constant current output pin for LED driver | Open |

## Panasonic

FUNCTIONAL BLOCK DIAGRAM


Note) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

## OPERATION

## 1. Power-on / Power-off sequence

Description of each mode

| Mode | LDOCNT | LDO10N | LDO2STB | LD01PS | LDO2PS | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OFF | Low | 0 | 0 | 0 | 0 | - The serial signal is not received at LDOCNT = Low. <br> It is necessary to set LDOCNT to High for the return from OFF mode. |
| OFF $\downarrow$ <br> Power save | $\begin{gathered} \text { Low } \\ \downarrow \\ \text { High } \end{gathered}$ | 1 | 0 | 1 | 1 | - The serial signal can be received after 5 ms from LDOCNT $=$ High. <br> - The setting of registers is initialized after this LSI return from OFF mode. Then LDO1 and LDO2 operate in power save mode respectively. |
| Normal | High | 0/1 | 0 | 0 | 0 | - When NRESET is set to Low, the setting of registers is initialized. Then LDO1 and LDO2 operate in power save mode respectively. <br> - The serial signal is turned LDO1 on or off. <br> - LDO2 turns on at LDOCNT = High. <br> - The serial signal is not received at NRESET = Low. <br> - Low period of one or more internal clocks is required during NRESET = Low. <br> - NRESET prohibits the input signal of those other than a rectangle wave. <br> - When NRESET is set to Low, all the registers are set to the default value. |
| Normal / power save $\downarrow$ OFF | $\begin{gathered} \text { High } \\ \downarrow \\ \text { Low } \end{gathered}$ | 0 | 0 | $\begin{gathered} 0 / 1 \\ \downarrow \\ 0 \end{gathered}$ | $\begin{gathered} 0 / 1 \\ \downarrow \\ 0 \end{gathered}$ | - The setting order to change into OFF mode is as follows. <br> LDOCNT $=$ Low $\rightarrow$ NRESET $=$ Low, or <br> NRESET $=$ Low $\rightarrow$ LDOCNT $=$ Low |
| Normal $\downarrow$ Power save Power save $\downarrow$ Normal | High | 0/1 | 0 | 0/1 | 0/1 | - LDO1, 2 can be individually shifted to power save mode by the serial signal. <br> - It is possible to return from power save mode to normal mode with serial signal. |
|  | $\begin{gathered} \text { High } \\ \downarrow \\ \text { Low } \end{gathered}$ | 1 | 1 | 0/1 | 0/1 | - When LDO1 output is used as power supply for $I^{2} \mathrm{C}$ I/F and LDO1 is turned OFF by LDO1ON via serial interface, LDO1 cannot return to ON mode via serial interface. <br> - When LDO1 output is used as power supply fro $I^{2} \mathrm{C}$ I/F, write [1] in LDO2STB first. After that, LDOCNT changes from High to Low, and LDO1 only shifts to OFF mode. |
| OFF(LDO1 only) <br> $\downarrow$ <br> Normal / power save | $\begin{gathered} \text { Low } \\ \downarrow \\ \text { High } \end{gathered}$ |  |  |  |  | - If LDOCNT is set to High from Low, this LSI can shift from standby to normal mode. |

AN32150B

## OPERATION (continued)

1. Power-on / Power-off sequence (continued)
1.1 Shift to LDO1, 2 power save mode from OFF mode at the rising edge of VB


Note) Set LDOCNT to High-level after VB, VBCP reach 3.1 V or more.
LDO1, LDO2 operate at power save mode after they just rise.
1.2 Shift to OFF mode from LDO1, 2 normal / power save mode


Note) *: There is no problem if NRESET falling timing is before or after LDOCNT falls.

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