Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Panasonic

AN32151A

http://www.semicon.panasonic.co.jp/en/

7 x 17 Dots Matrix LED Driver LSI

FEATURES

- 7 x 17 LED Matrix Driver
  (Total LED that can be driven = 119)
- Internal memory RAM (1-side)
- LDO (1-ch)
- I^2C interface + SPI interface
- 49 pin Wafer Level Chip Size Package (WLCSP)

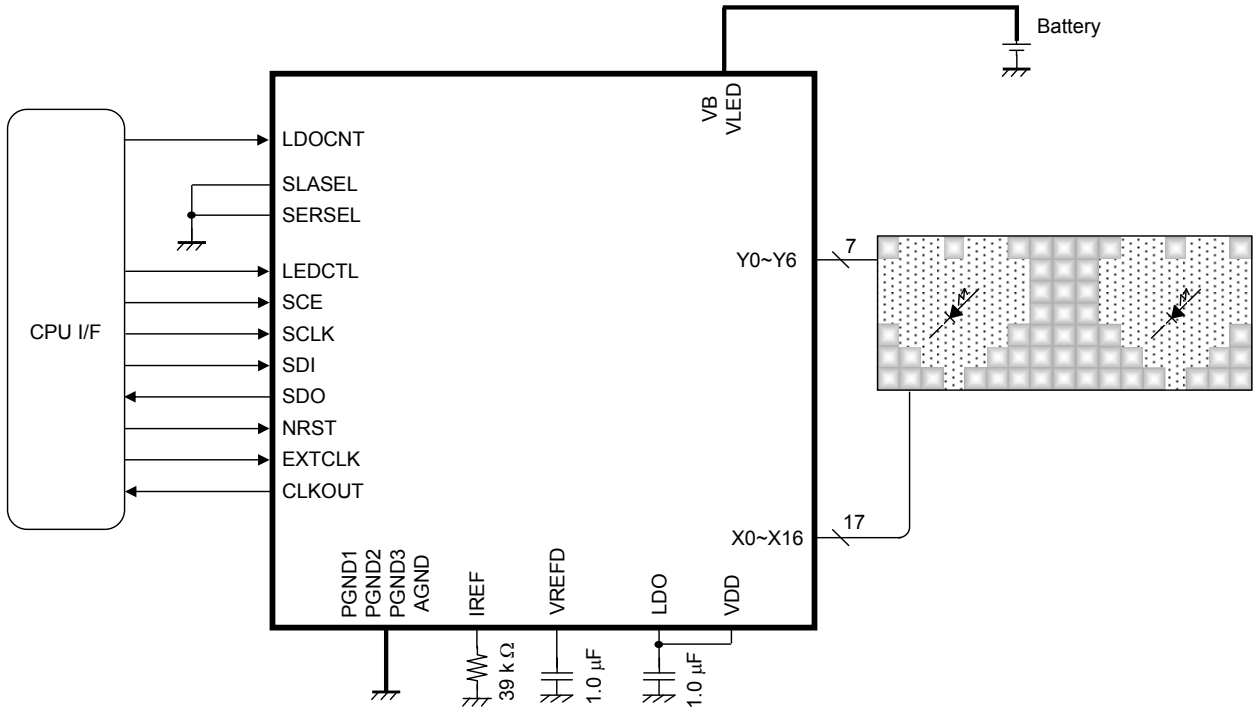
DESCRIPTION

AN32151A is a 7 x 17 LED Matrix Driver equipped with RAM.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

Established : 2009-07-23
Revised : 2013-04-01

CONTENTS

Established : 2009-07-23
Revised : 2013-04-01

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VDD_{MAX}	4.3	V	*1
	VB_{MAX}	6.0	V	*1
	$VLED_{MAX}$	6.5	V	*1
Operating ambience temperature	T_{opr}	–30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	SCE, SLASEL, SCLK, SDI	– 0.3 to 4.3	V	—
	SERSEL, EXTCLK, NRST, LDOCNT, LEDCTL	– 0.3 to 6.0	V	—
Output Voltage Range	SDO, CLKOUT	– 0.3 to 4.3	V	—
	LDO	– 0.3 to 6.0	V	—
	X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16 Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3 to 6.5	V	—
ESD	HBM	1.5 to 2.0	kV	—

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1: VDD_{MAX} = VDD, VB_{MAX} = VB, $VLED_{MAX}$ = VLED.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
49 pin Wafer Level Chip Size Package (WLCSP)	171.05 °C /W	0.585 W	0.234 W

Note) For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

Established : 2009-07-23
Revised : 2013-04-01

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VDD	1.7	2.6	3.5	V	*1
	VB	3.1	3.6	4.6	V	*1
	VLED	3.1	4.9	5.6	V	*1
Input Voltage Range	SCE, SLASEL, SCLK, SDI	– 0.3	—	VDD + 0.3	V	*2
	SERSEL, EXTCLK, NRST, LDOCNT, LEDCTL	– 0.3	—	VB + 0.3	V	*2
Output Voltage Range	SDO, CLKOUT	– 0.3	—	VDD + 0.3	V	*2
	LDO	– 0.3	—	VB + 0.3	V	*2
	X0, X1, X2, X3, X4, X5, X6, X7, X8, X9, X10, X11, X12, X13, X14, X15, X16 Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3	—	VLED + 0.3	V	*2

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, PGND1, PGND2 and PGND3.
VDD is voltage for VDD. VB is voltage for VB. VLED is voltage for VLED.
*2: (VDD + 0.3) V must not exceed 4.3 V. (VB + 0.3) V must not exceed 6 V.
(VLED + 0.3) V must not exceed 6.5 V.

Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current consumption							
Current consumption (1) Off mode	ICC1	VB = 3.6 V LDOCNT = Low	—	0	1	μA	—
Current consumption (2) Normal mode	ICC2	VB = 3.6 V LDOCNT = High ILOAD = 0 μA	—	14	20	μA	—
Reference voltage source							
Output voltage	VREF	VB = 3.6 V I_{VREF} = 0 μA	1.17	1.20	1.23	V	—
EXTCLK, NRST, LDOCNT, SERSEL, LEDCTL							
High-level input voltage range	VIH1	High-level recognition voltage	1.4	—	VB + 0.3	V	—
Low-level input voltage range	VIL1	Low-level recognition voltage	–0.3	—	0.4	V	—
High-level input current	IIH1	Vin = 1.85 V	—	0	1	μA	—
Low-level input current	IIL1	Vin = 0 V	—	0	1	μA	—
SCLK, SDI							
High-level input voltage range	VIH2	High-level recognition voltage	VDD × 0.7	—	VDD_{max} + 0.5	V	—
Low-level input voltage range	VIL2	Low-level recognition voltage	– 0.5	—	VDD × 0.3	V	—
High-level input current	IIH2	Vin = 1.85 V	—	0	1	μA	—
Low-level input current	IIL2	Vin = 0 V	—	0	1	μA	—
Low-level output voltage (1)	VOL1	I_{SDI} = 3 mA, VDD > 2 V VOL1 = V_{SDI}	0	—	0.4	V	—
Low-level output voltage (2)	VOL2	I_{SDI} = 3 mA, VDD < 2 V VOL2 = V_{SDI}	0	—	VDD × 0.2	V	—
Clock frequency	FSCL	Input frequency at SCLK	0	—	400	kHz	—

Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SCE, SLASEL							
High-level input voltage range	VIH3	High-level recognition voltage	VDD × 0.7	—	VDD_{max} + 0.5	V	—
Low-level input voltage range	VIL3	Low-level recognition voltage	– 0.5	—	VDD × 0.3	V	—
High-level input current	IIH3	Vin = 1.85 V	—	0	1	µA	—
Low-level input current	IIL3	Vin = 0 V	—	0	1	µA	—
SDO, CLKOUT							
High-level output voltage	VOH4	Iin = – 2 mA	VDD × 0.8	—	—	V	—
Low-level output voltage	VOL4	Iin = 2 mA	—	—	VDD × 0.2	V	—
Constant voltage source (LDO)							
Output voltage (1)	VL1	I_{LDO} = – 10 µA	1.79	1.85	1.91	V	—
Output voltage (2)	VL2	VB = 3.1 V I_{LDO} = – 30 mA	1.79	1.85	1.91	V	—
Short-circuit protection current	IPT1	LDOCNT = "H" REG18 = [1] V_{LDO} = 0 V	50	100	200	mA	—
Ripple rejection ratio (1)	PSL11	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO} = – 15 mA PSL11 = 20log(acV_{LDO} / 0.2)	—	– 45	– 40	dB	—
Ripple rejection ratio (2)	PSL12	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO} = – 15 mA PSL12 = 20log(acV_{LDO} / 0.2)	—	– 35	– 25	dB	—
Oscillator							
Oscillation frequency	FOSC	OSCEN = [1]	0.96	1.2	1.44	MHz	—
SDO, CLKOUT							
High-level output voltage	VOH4	Iin = – 2 mA	VDD × 0.8	—	—	V	—
Low-level output voltage	VOL4	Iin = 2 mA	—	—	VDD × 0.2	V	—

Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Constant current source (for matrix LED)							
Output current (1)	IMX1	At 1.400 mA setup V_{X0} to V_{X16} = 1 V IMX1 = I_{X0} to I_{X16}	1.288	1.400	1.512	mA	*1, 2
Output current (2)	IMX2	At 2.800 mA setup V_{X0} to V_{X16} = 1 V IMX2 = I_{X0} to I_{X16}	2.576	2.800	3.024	mA	*1, 2
Output current (3)	IMX4	At 5.600 mA setup V_{X0} to V_{X16} = 1 V IMX4 = I_{X0} to I_{X16}	5.152	5.600	6.048	mA	*1, 2
Output current (4)	IMX8	At 11.20 mA setup V_{X0} to V_{X16} = 1 V IMX8 = I_{X0} to I_{X16}	10.30	11.20	12.10	mA	*1, 2
Output current (5)	IMX16	At 21.00 mA setup V_{X0} to V_{X16} = 1 V IMX16 = I_{X0} to I_{X16}	19.32	21.00	22.68	mA	*1, 2
Leak current at Off mode	IMXOFF	At Off setup V_{X0} to V_{X16} = 4.75 V IMXOFF = I_{X0} to I_{X16}	—	—	1	μA	—
Error between channels	IMXCH	Difference current between the average of all channels and each channel	– 5	—	5	%	*2
SCAN switch							
Resistance at switch On	RSCAN	V_{VLED}= 4.62 V I_{Y0} to I_{Y6} = – 5 mA RSCAN = V_{Y0} to V_{Y6} / 5 mA	—	1	2	Ω	—

Note) *1 : Values when recommended parts (ERJ2RHD393X) are used for IREF pin. The other current settings are combination of above items.

*2 : All of the setting values of matrix block are with absolute accuracy of ± 8 %, the error between channels of ± 5 %.

Established : 2009-07-23
Revised : 2013-04-01

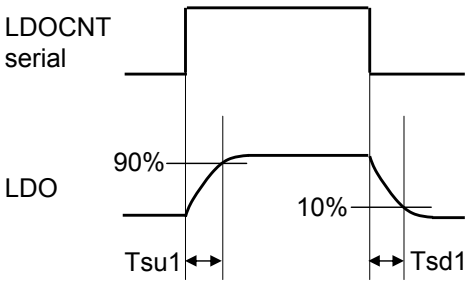
ELECTRICAL CHARACTERISTICS (continued)

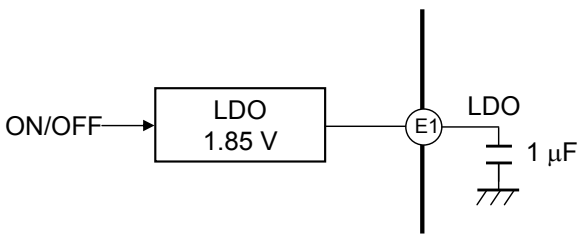
VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Constant current source (for matrix LED)							
Saturation voltage	Vsat	Voltage value when the setting current value changes to 5 % or more of by V_{X0} to V_{X16}	—	0.2	0.4	V	—
TSD (Thermal shutdown protection circuit)							
Detection temperature	Tdet	Temperature which LDO, Constant current circuit, and Matrix SW turn off.	—	160	—	°C	*3 *4
Recovery temperature	Tsd11	Recovering temperature	—	110	—	°C	*4 *5
Constant voltage regulator (LDO) Output capacitor : 1 µF, Output capacitor's ESR : less than 0.1 Ω							
Rise time	Tsu1	Time until output voltage reaches 0 V to 0%. (No load)	—	0.25	—	ms	*4
Fall time	Tsd1	Time until output voltage reaches 10 %.	—	5	—	ms	*4
Maximum load current	IOMAX1	—	—	15	—	mA	*4
Load transient response (1)	Vtr11	Iout = –50 µA → –15 mA (1 µs)	—	70	—	mV	*4
Load transient response (2)	Vtr12	Iout = –15 mA → –50 µA (1 µs)	—	70	—	mV	*4

Note) *3 : LDO, Constant current circuit, and Matrix SW turn off when TSD operates.
*4 : Typical Design Value
*5 : LDO only recovers after TSD becomes ON state. Logic block becomes reset state.





Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

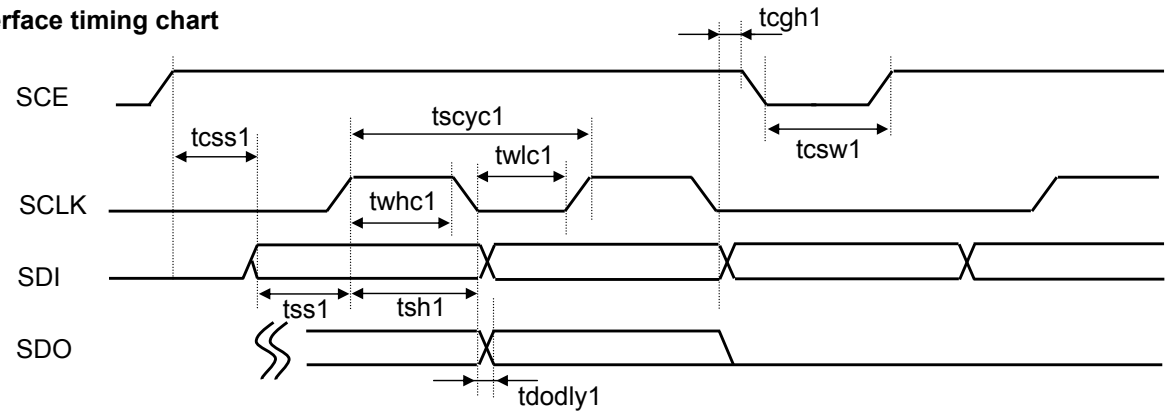
VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Microcomputer interface characteristics (VDD = 1.85 V ± 3%) Reception timing							
SCLK cycle period	tscyc1	—	—	152	—	ns	*4
SCLK cycle period High period	twhc1	—	—	70	—	Ns	*4
SCLK cycle period Low period	Twlc1	—	—	70	—	Ns	*4
Serial data setup time	Tss1	—	—	62	—	ns	*4
Serial data hold time	tsh1	—	—	62	—	ns	*4
Transceiving interval	tcsw1	—	—	62	—	ns	*4
Chip enable setup time	tcss1	—	—	5	—	ns	*4
Chip enable hold time	tcgh1	—	—	5	—	ns	*4
Microcomputer interface characteristics (VDD = 1.85 V ± 3%) Transmission timing							
SCLK cycle period	tscyc1	—	—	152	—	ns	*4
SCLK cycle period High period	twhc1	—	—	70	—	ns	*4
SCLK cycle period Low period	twlc1	—	—	70	—	ns	*4
Serial data setup time	tss1	—	—	62	—	ns	*4
Serial data hold time	tsh1	—	—	62	—	ns	*4
Transceiving interval	tcsw1	—	—	62	—	ns	*4
Chip enable setup time	tcss1	—	—	5	—	ns	*4
Chip enable hold time	tcgh1	—	—	5	—	ns	*4
DC delay time	tdodly1	Read mode only	—	30	—	ns	*4

Note) *4 : Typical Design Value

Interface timing chart



Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Internal I/O stage characteristics)							
Hysteresis of Schmitt trigger input 1	Vhys1	Hysteresis of SCLK, SDI VDD > 2 V	0.05 × VDD	—	—	V	*6 *7
Hysteresis of Schmitt trigger input 2	Vhys2	Hysteresis of SCLK, SDI VDD < 2 V	0.1 × VDD	—	—	V	*6 *7
Output fall time from V_{IHmin} to V_{ILmax}	Tof	Bus capacitance : 10 pF to 400pF $I_P \leq 6$ mA (V_{OLmax} = 0.6 V) I_P : Max. sink current	20 + 0.1C_b	—	250	ns	*6 *7
Pulse width of spikes which must be suppressed by the input filter	Tsp	—	0	—	50	ns	*6 *7
Capacitance for each I/O pin	Ci	—	—	—	10	pF	*6 *7

Note) *6 : The timing of Fast-mode and Normal mode devices in I²C-bus is specified in Page.12. All values referred to V_{IHMIN} and V_{ILMAX} level.

*7 : These are values checked by design but not production tested.

Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Bus line specifications)							
Hold time (repeated) START condition	$t_{HD:STA}$	The first clock pulse is generated after this period	0.6	—	—	µs	*6 *7
Low period of the SCL clock	t_{LOW}	—	1.3	—	—	µs	*6 *7
High period of the SCL clock	t_{HIGH}	—	0.6	—	—	µs	*6 *7
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.6	—	—	µs	*6 *7
Data hold time	$t_{HD:DAT}$	—	0	—	0.9	µs	*6 *7
Data set-up time	$t_{SU:DAT}$	—	100	—	—	ns	*6 *7
Rise time of both SDA and SCL signals	tr	—	20 + 0.1C_b	—	300	ns	*6 *7
Fall time of both SDA and SCL signals	t_f	—	20 + 0.1C_b	—	300	ns	*6 *7
Set-up time of STOP condition	$t_{SU:STO}$	—	0.6	—	—	µs	*6 *7
Bus free time between STOP and START condition	t_{BUF}	—	1.3	—	—	µs	*6 *7
Capacitive load for each bus line	C_b	—	—	—	400	pF	*6 *7
Noise margin at the Low-level for each connected device (with hysteresis)	V_{aL}	—	0.1 × VDD	—	—	V	*6 *7
Noise margin at the High-level for each connected device (with hysteresis)	V_{aH}	—	0.2 × VDD	—	—	V	*6 *7

Note) *6 : The timing of Fast-mode and Normal mode devices in I²C-bus is specified in Page.12. All values referred to V_{IHMIN} and V_{ILMAX} level.

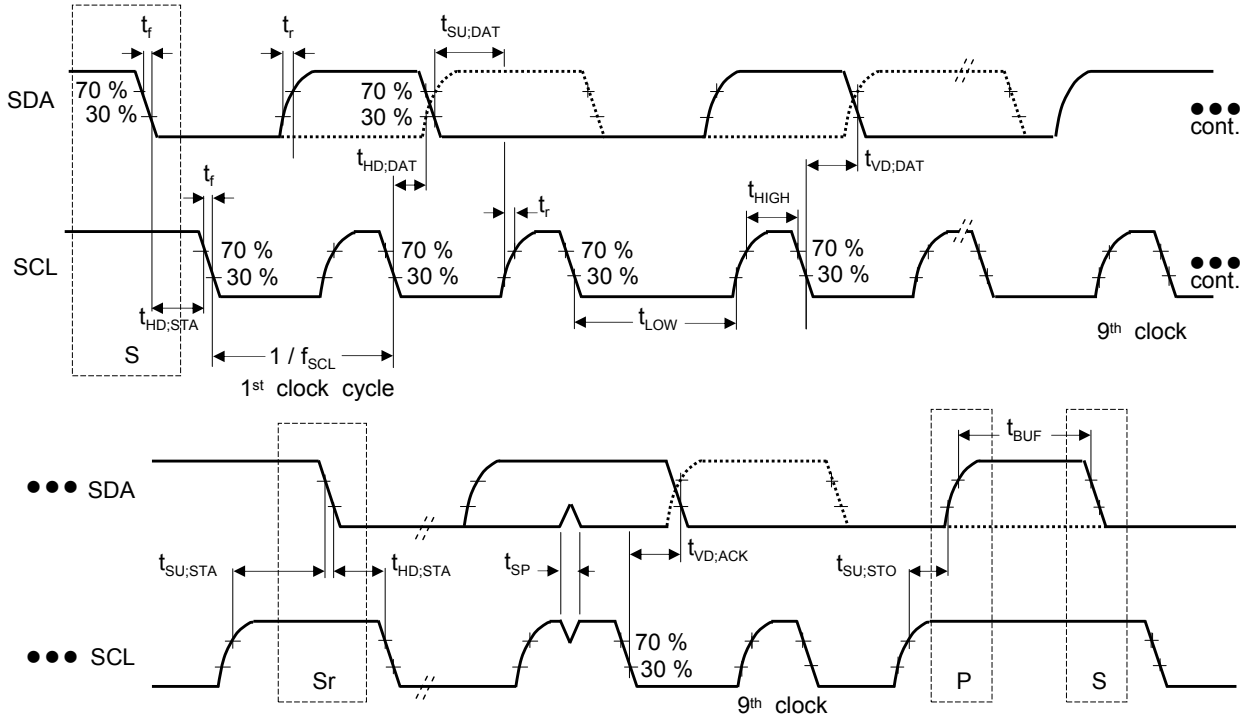
*7 : These are values checked by design but not production tested.

Established : 2009-07-23
Revised : 2013-04-01

ELECTRICAL CHARACTERISTICS (continued)

VDD = 2.6 V, VB = 3.6 V, VLED = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.



V_{ILMAX} = 0.3 V_{DD}

V_{IHMIN} = 0.7 V_{DD}

S : START condition

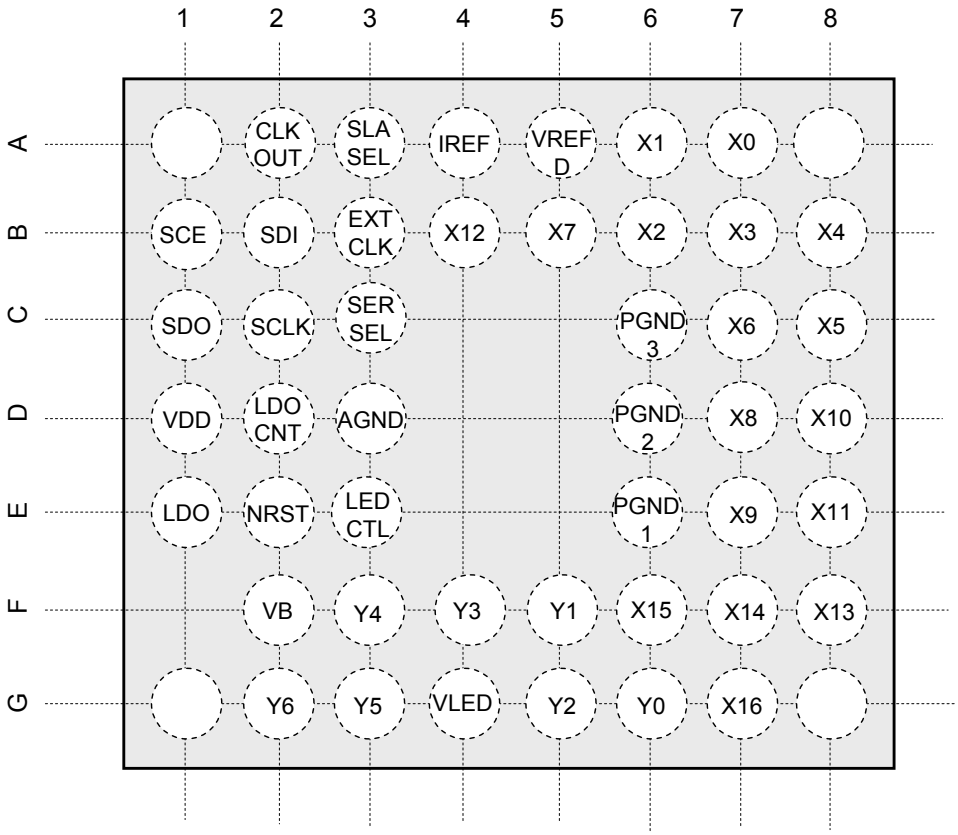
Sr : Repeat START condition

P : STOP condition

Establ i shed : 2 0 0 0-0 7-2 3
Revised : 2 0 1 1-0 4 0 1

PIN CONFIGURATION

Top View



Note) Four-cornered pins have been connected to GND.

Established : 2009-07-23
Revised : 2013-04-01

PIN FUNCTIONS

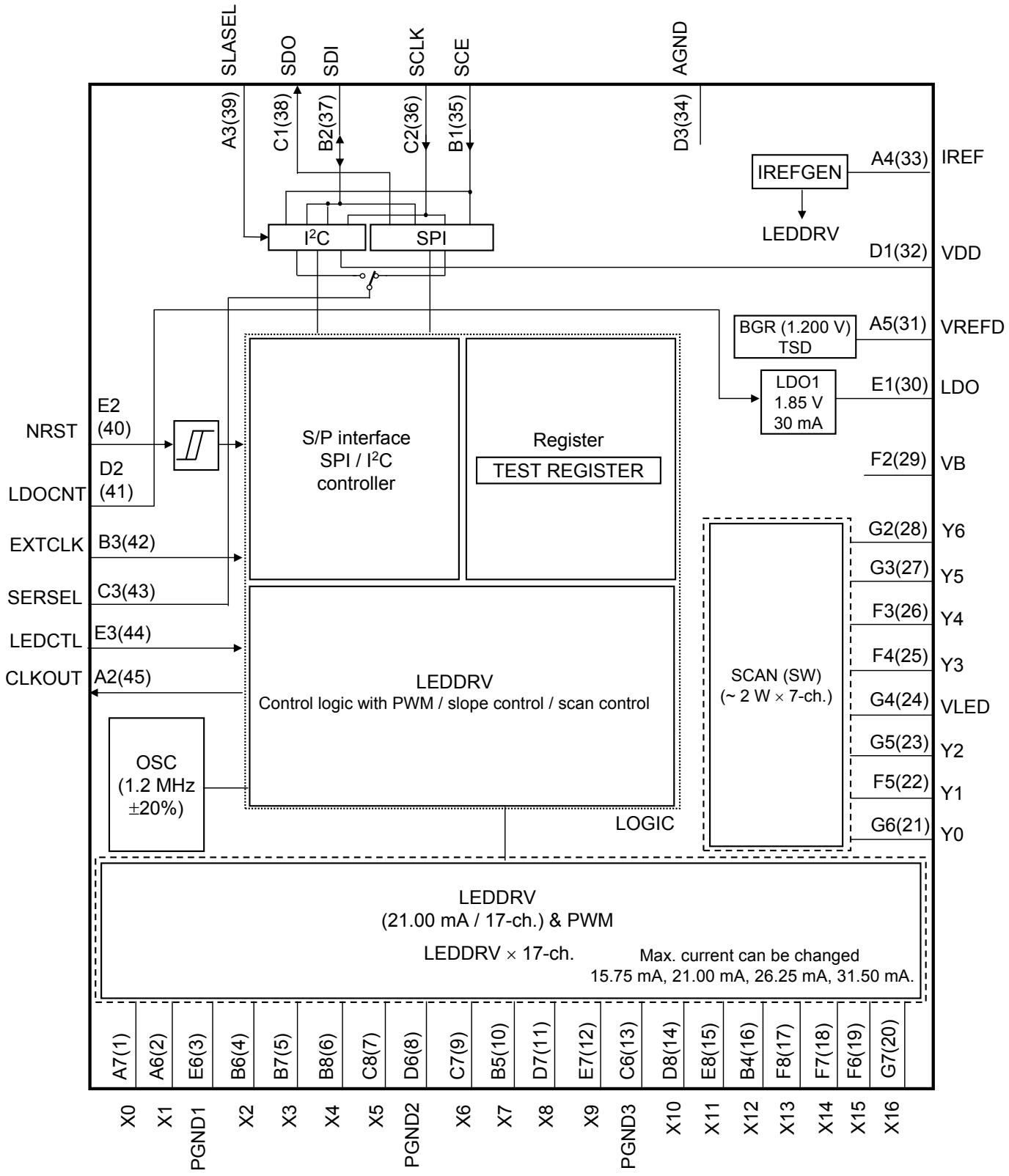
Pin No.	Pin name	Type	Description
A7(1)	X0	Output	PWM control output pin with constant current circuit This pin is connected with A column of matrix LED.
A6(2)	X1	Output	PWM control output pin with constant current circuit This pin is connected with B column of matrix LED.
E6(3) D6(8) C6(13)	PGND1 PGND2 PGND3	Ground	Ground pin for matrix LED
B6(4)	X2	Output	PWM control output pin with constant current circuit This pin is connected with C column of matrix LED.
B7(5)	X3	Output	PWM control output pin with constant current circuit This pin is connected with D column of matrix LED.
B8(6)	X4	Output	PWM control output pin with constant current circuit This pin is connected with E column of matrix LED.
C8(7)	X5	Output	PWM control output pin with constant current circuit This pin is connected with F column of matrix LED.
C7(9)	X6	Output	PWM control output pin with constant current circuit This pin is connected with G column of matrix LED.
B5(10)	X7	Output	PWM control output pin with constant current circuit This pin is connected with H column of matrix LED.
D7(11)	X8	Output	PWM control output pin with constant current circuit This pin is connected with I column of matrix LED.
E7(12)	X9	Output	PWM control output pin with constant current circuit This pin is connected with J column of matrix LED.
D8(14)	X10	Output	PWM control output pin with constant current circuit This pin is connected with K column of matrix LED.
E8(15)	X11	Output	PWM control output pin with constant current circuit This pin is connected with L column of matrix LED.
B4(16)	X12	Output	PWM control output pin with constant current circuit This pin is connected with M column of matrix LED.
F8(17)	X13	Output	PWM control output pin with constant current circuit This pin is connected with N column of matrix LED.
F7(18)	X14	Output	PWM control output pin with constant current circuit This pin is connected with O column of matrix LED.
F6(19)	X15	Output	PWM control output pin with constant current circuit This pin is connected with P column of matrix LED.
G7(20)	X16	Output	PWM control output pin with constant current circuit This pin is connected with Q column of matrix LED.
G6(21)	Y0	Output	PWM control output pin with constant current circuit This pin is connected with the 1st row of matrix LED.
F5(22)	Y1	Output	PWM control output pin with constant current circuit This pin is connected with the 2nd row of matrix LED.

PIN FUNCTIONS (continued)

Pin No.	Pin name	Type	Description
G5(23)	Y2	Output	PWM control output pin with constant current circuit This pin is connected with the 3rd row of matrix LED.
G4(24)	VLED	Power supply	Power supply's connection pin for matrix LED This pin should be connected with the output of battery or step-up converter.
F4(25)	Y3	Output	PWM control output pin with constant current circuit This pin is connected with the 4th row of matrix LED.
F3(26)	Y4	Output	PWM control output pin with constant current circuit This pin is connected with the 5th row of matrix LED.
G3(27)	Y5	Output	PWM control output pin with constant current circuit This pin is connected with the 6th row of matrix LED.
G2(28)	Y6	Output	PWM control output pin with constant current circuit This pin is connected with the 7th row of matrix LED.
F2(29)	VB	Power supply	Power supply's connection pin for BGR circuit and LDO circuit
E1(30)	LDO	Output	Power supply's connection pin for serial interface input block and internal logic.
A5(31)	VREFD	Output	BGR circuit output pin
D1(32)	VDD	Power supply	Power supply pin for output interface
A4(33)	IREF	Output	Resistor connection pin for constant current setup
D3(34)	AGND	Ground	Ground pin for analogue circuitry
B1(35)	SCE	Input	SPI interface chip-enable pin (High active) (Slave address selection control pin 1 at I^2C mode)
C2(36)	SCLK	Input	Common clock input pin in both SPI interface and I^2C interface
B2(37)	SDI	Input / Output	Data input pin for SPI interface Data input/output pin for I^2C interface
C1(38)	SDO	Output	Data output pin for SPI interface
A3(39)	SLASEL	Input	Slave address selection control pin 2 at I^2C mode
E2(40)	NRST	Input	Reset input pin (Low active)
D2(41)	LDOCNT	Input	LDO ON/OFF control pin
B3(42)	EXTCLK	Input	External clock input pin
C3(43)	SERSEL	Input	SPI, I^2C selection pin
E3(44)	LEDCTL	Input	LED lit external synchronous input pin
A2(45)	CLKOUT	Output	Internal clock output pin

Established : 2009-07-23
Revised : 2013-04-01

FUNCTIONAL BLOCK DIAGRAM



Note) This block diagram is for explaining functions.
Part of the block diagram may be omitted, or it may be simplified.

Established : 2009-07-23
Revised : 2013-04-01

OPERATION

1. Power supply sequence control

Power supply turn on/off sequence

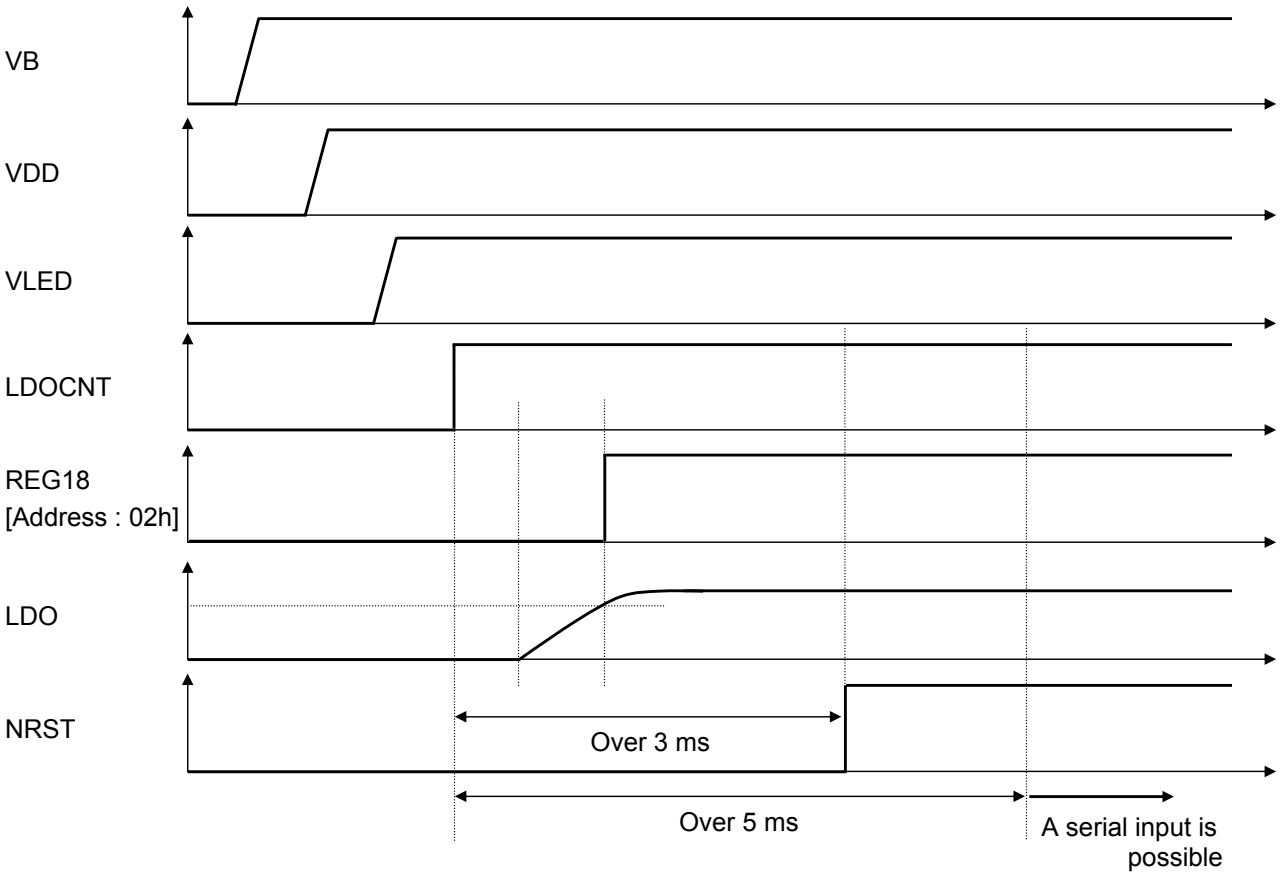
Mode	LDOCNT	REG18	Remarks
OFF	Low	0	LDOCNT should be set to High for the recovery from OFF mode.
OFF ↓ Normal mode	Low → High	0/1	Serial signal is not received at LDOCNT = Low and REG18 = [0].
	High	0/1	
Normal mode ↓ OFF	High → Low	0	LDO turns on at LDOCNT = High regardless of REG18. Serial signal is not received at NRST = Low. Serial signal can be received 5 ms or more after LDOCNT = High. NRST should have one or more Low period of internal clock. Inputting signal except rectangular wave into NRST pin is prohibited. When NRST = Low, the settings of all registers become default values. (Since the default value of REG18 bit becomes [1] at NRST= Low, LDO shifts to OFF mode at LDOCNT = Low.) All register setting become default setting when LDO turns off. The setting order to change to off mode is as follows. REG18 = [0] → LDOCNT = Low → NRST = Low

Established : 2009-07-23
Revised : 2013-04-01

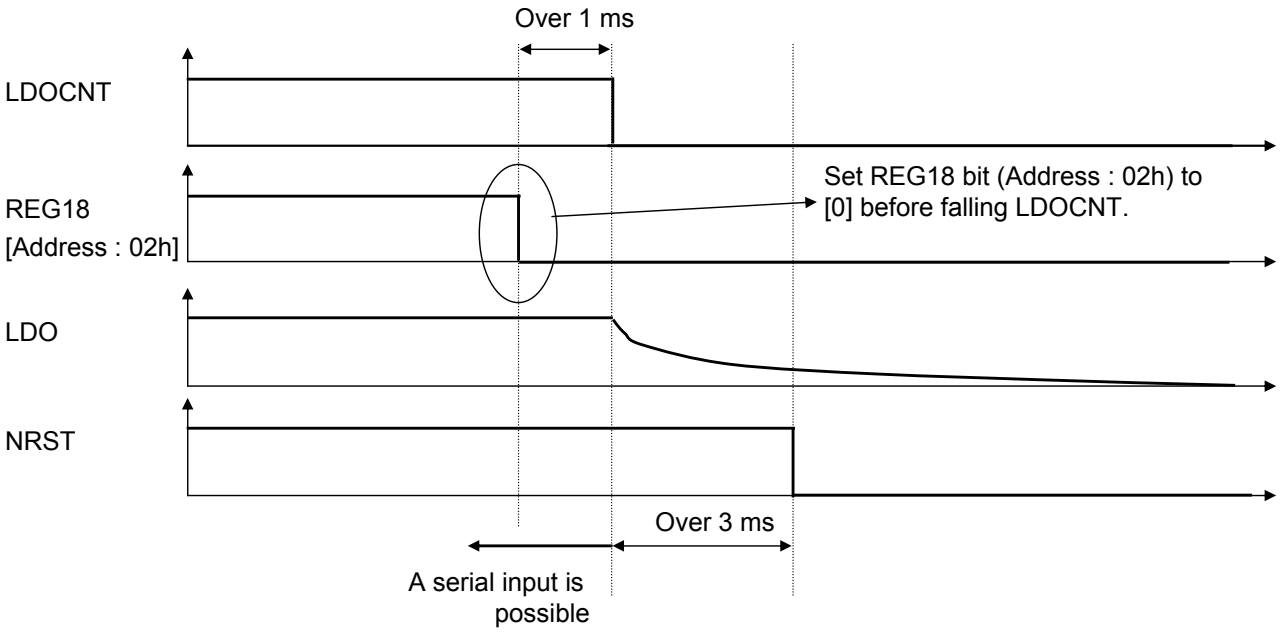
OPERATION (continued)

1. Power supply sequence control (continued)

Shift to Normal mode from OFF mode



Shift to OFF mode from Normal mode



Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

2. Register map (1)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
00h	R/W	RST	—	—	—	—	—	—	RAMRST	SRST
01h	R/W	POWERCNT	—	—	—	—	—	—	—	OSCEN
02h	R/W	LDOCNT	—	—	—	—	—	—	—	REG18
03h	R	LSITEST	For test (Access inhibit)							
04h	R/W	OPTION	LEDACT	DISMTX	—	—	—	—	CLKOUT	EXTCLK
05h	R/W	MTXON	—	—	—	—	IMAX[1:0]		—	MTXON
06h	R/W	XCONST1	X16	X15	X14	X13	X12	X11	X10	X9
07h	R/W	XCONST2	X8	X7	X6	X5	X4	X3	X2	X1
08h	R/W	XCONST3	—	—	—	—	—	—	—	X0

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

2. Register map (2)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
09h	R/W	A1	BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
0Ah	R/W	A2	BLA2[3:0]				FRA2[1:0]		DLA2[1:0]	
0Bh	R/W	A3	BLA3[3:0]				FRA3[1:0]		DLA3[1:0]	
0Ch	R/W	A4	BLA4[3:0]				FRA4[1:0]		DLA4[1:0]	
0Dh	R/W	A5	BLA5[3:0]				FRA5[1:0]		DLA5[1:0]	
0Eh	R/W	A6	BLA6[3:0]				FRA6[1:0]		DLA6[1:0]	
0Fh	R/W	A7	BLA7[3:0]				FRA7[1:0]		DLA7[1:0]	
10h	R/W	B1	BLB1[3:0]				FRB1[1:0]		DLB1[1:0]	
11h	R/W	B2	BLB2[3:0]				FRB2[1:0]		DLB2[1:0]	
12h	R/W	B3	BLB3[3:0]				FRB3[1:0]		DLB3[1:0]	
13h	R/W	B4	BLB4[3:0]				FRB4[1:0]		DLB4[1:0]	
14h	R/W	B5	BLB5[3:0]				FRB5[1:0]		DLB5[1:0]	
15h	R/W	B6	BLB6[3:0]				FRB6[1:0]		DLB6[1:0]	
16h	R/W	B7	BLB7[3:0]				FRB7[1:0]		DLB7[1:0]	
17h	R/W	C1	BLC1[3:0]				FRC1[1:0]		DLC1[1:0]	
18h	R/W	C2	BLC2[3:0]				FRC2[1:0]		DLC2[1:0]	
19h	R/W	C3	BLC3[3:0]				FRC3[1:0]		DLC3[1:0]	
1Ah	R/W	C4	BLC4[3:0]				FRC4[1:0]		DLC4[1:0]	
1Bh	R/W	C5	BLC5[3:0]				FRC5[1:0]		DLC5[1:0]	
1Ch	R/W	C6	BLC6[3:0]				FRC6[1:0]		DLC6[1:0]	
1Dh	R/W	C7	BLC7[3:0]				FRC7[1:0]		DLC7[1:0]	
1Eh	R/W	D1	BLD1[3:0]				FRD1[1:0]		DLD1[1:0]	
1Fh	R/W	D2	BLD2[3:0]				FRD2[1:0]		DLD2[1:0]	
20h	R/W	D3	BLD3[3:0]				FRD3[1:0]		DLD3[1:0]	
21h	R/W	D4	BLD4[3:0]				FRD4[1:0]		DLD4[1:0]	
22h	R/W	D5	BLD5[3:0]				FRD5[1:0]		DLD5[1:0]	
23h	R/W	D6	BLD6[3:0]				FRD6[1:0]		DLD6[1:0]	
24h	R/W	D7	BLD7[3:0]				FRD7[1:0]		DLD7[1:0]	
25h	R/W	E1	BLE1[3:0]				FRE1[1:0]		DLE1[1:0]	
26h	R/W	E2	BLE2[3:0]				FRE2[1:0]		DLE2[1:0]	
27h	R/W	E3	BLE3[3:0]				FRE3[1:0]		DLE3[1:0]	
28h	R/W	E4	BLE4[3:0]				FRE4[1:0]		DLE4[1:0]	
29h	R/W	E5	BLE5[3:0]				FRE5[1:0]		DLE5[1:0]	
2Ah	R/W	E6	BLE6[3:0]				FRE6[1:0]		DLE6[1:0]	
2Bh	R/W	E7	BLE7[3:0]				FRE7[1:0]		DLE7[1:0]	

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

2. Register map (2) (continued)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
2Ch	R/W	F1	BLF1[3:0]				FRF1[1:0]		DLF1[1:0]	
2Dh	R/W	F2	BLF2[3:0]				FRF2[1:0]		DLF2[1:0]	
2Eh	R/W	F3	BLF3[3:0]				FRF3[1:0]		DLF3[1:0]	
2Fh	R/W	F4	BLF4[3:0]				FRF4[1:0]		DLF4[1:0]	
30h	R/W	F5	BLF5[3:0]				FRF5[1:0]		DLF5[1:0]	
31h	R/W	F6	BLF6[3:0]				FRF6[1:0]		DLF6[1:0]	
32h	R/W	F7	BLF7[3:0]				FRF7[1:0]		DLF7[1:0]	
33h	R/W	G1	BLG1[3:0]				FRG1[1:0]		DLG1[1:0]	
34h	R/W	G2	BLG2[3:0]				FRG2[1:0]		DLG2[1:0]	
35h	R/W	G3	BLG3[3:0]				FRG3[1:0]		DLG3[1:0]	
36h	R/W	G4	BLG4[3:0]				FRG4[1:0]		DLG4[1:0]	
37h	R/W	G5	BLG5[3:0]				FRG5[1:0]		DLG5[1:0]	
38h	R/W	G6	BLG6[3:0]				FRG6[1:0]		DLG6[1:0]	
39h	R/W	G7	BLG7[3:0]				FRG7[1:0]		DLG7[1:0]	
3Ah	R/W	H1	BLH1[3:0]				FRH1[1:0]		DLH1[1:0]	
3Bh	R/W	H2	BLH2[3:0]				FRH2[1:0]		DLH2[1:0]	
3Ch	R/W	H3	BLH3[3:0]				FRH3[1:0]		DLH3[1:0]	
3Dh	R/W	H4	BLH4[3:0]				FRH4[1:0]		DLH4[1:0]	
3Eh	R/W	H5	BLH5[3:0]				FRH5[1:0]		DLH5[1:0]	
3Fh	R/W	H6	BLH6[3:0]				FRH6[1:0]		DLH6[1:0]	
40h	R/W	H7	BLH7[3:0]				FRH7[1:0]		DLH7[1:0]	
41h	R/W	I1	BLI1[3:0]				FRI1[1:0]		DLI1[1:0]	
42h	R/W	I2	BLI2[3:0]				FRI2[1:0]		DLI2[1:0]	
43h	R/W	I3	BLI3[3:0]				FRI3[1:0]		DLI3[1:0]	
44h	R/W	I4	BLI4[3:0]				FRI4[1:0]		DLI4[1:0]	
45h	R/W	I5	BLI5[3:0]				FRI5[1:0]		DLI5[1:0]	
46h	R/W	I6	BLI6[3:0]				FRI6[1:0]		DLI6[1:0]	
47h	R/W	I7	BLI7[3:0]				FRI7[1:0]		DLI7[1:0]	
48h	R/W	J1	BLJ1[3:0]				FRJ1[1:0]		DLJ1[1:0]	
49h	R/W	J2	BLJ2[3:0]				FRJ2[1:0]		DLJ2[1:0]	
4Ah	R/W	J3	BLJ3[3:0]				FRJ3[1:0]		DLJ3[1:0]	
4Bh	R/W	J4	BLJ4[3:0]				FRJ4[1:0]		DLJ4[1:0]	
4Ch	R/W	J5	BLJ5[3:0]				FRJ5[1:0]		DLJ5[1:0]	
4Dh	R/W	J6	BLJ6[3:0]				FRJ6[1:0]		DLJ6[1:0]	
4Eh	R/W	J7	BLJ7[3:0]				FRJ7[1:0]		DLJ7[1:0]	

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

2. Register map (2) (continued)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
4Fh	R/W	K1	BLK1[3:0]				FRK1[1:0]		DLK1[1:0]	
50h	R/W	K2	BLK2[3:0]				FRK2[1:0]		DLK2[1:0]	
51h	R/W	K3	BLK3[3:0]				FRK3[1:0]		DLK3[1:0]	
52h	R/W	K4	BLK4[3:0]				FRK4[1:0]		DLK4[1:0]	
53h	R/W	K5	BLK5[3:0]				FRK5[1:0]		DLK5[1:0]	
54h	R/W	K6	BLK6[3:0]				FRK6[1:0]		DLK6[1:0]	
55h	R/W	K7	BLK7[3:0]				FRK7[1:0]		DLK7[1:0]	
56h	R/W	L1	BLL1[3:0]				FRL1[1:0]		DLL1[1:0]	
57h	R/W	L2	BLL2[3:0]				FRL2[1:0]		DLL2[1:0]	
58h	R/W	L3	BLL3[3:0]				FRL3[1:0]		DLL3[1:0]	
59h	R/W	L4	BLL4[3:0]				FRL4[1:0]		DLL4[1:0]	
5Ah	R/W	L5	BLL5[3:0]				FRL5[1:0]		DLL5[1:0]	
5Bh	R/W	L6	BLL6[3:0]				FRL6[1:0]		DLL6[1:0]	
5Ch	R/W	L7	BLL7[3:0]				FRL7[1:0]		DLL7[1:0]	
5Dh	R/W	M1	BLM1[3:0]				FRM1[1:0]		DLM1[1:0]	
5Eh	R/W	M2	BLM2[3:0]				FRM2[1:0]		DLM2[1:0]	
5Fh	R/W	M3	BLM3[3:0]				FRM3[1:0]		DLM3[1:0]	
60h	R/W	M4	BLM4[3:0]				FRM4[1:0]		DLM4[1:0]	
61h	R/W	M5	BLM5[3:0]				FRM5[1:0]		DLM5[1:0]	
62h	R/W	M6	BLM6[3:0]				FRM6[1:0]		DLM6[1:0]	
63h	R/W	M7	BLM7[3:0]				FRM7[1:0]		DLM7[1:0]	
64h	R/W	N1	BLN1[3:0]				FRN1[1:0]		DLN1[1:0]	
65h	R/W	N2	BLN2[3:0]				FRN2[1:0]		DLN2[1:0]	
66h	R/W	N3	BLN3[3:0]				FRN3[1:0]		DLN3[1:0]	
67h	R/W	N4	BLN4[3:0]				FRN4[1:0]		DLN4[1:0]	
68h	R/W	N5	BLN5[3:0]				FRN5[1:0]		DLN5[1:0]	
69h	R/W	N6	BLN6[3:0]				FRN6[1:0]		DLN6[1:0]	
6Ah	R/W	N7	BLN7[3:0]				FRN7[1:0]		DLN7[1:0]	
6Bh	R/W	O1	BLO1[3:0]				FRO1[1:0]		DLO1[1:0]	
6Ch	R/W	O2	BLO2[3:0]				FRO2[1:0]		DLO2[1:0]	
6Dh	R/W	O3	BLO3[3:0]				FRO3[1:0]		DLO3[1:0]	
6Eh	R/W	O4	BLO4[3:0]				FRO4[1:0]		DLO4[1:0]	
6Fh	R/W	O5	BLO5[3:0]				FRO5[1:0]		DLO5[1:0]	
70h	R/W	O6	BLO6[3:0]				FRO6[1:0]		DLO6[1:0]	
71h	R/W	O7	BLO7[3:0]				FRO7[1:0]		DLO7[1:0]	

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

2. Register map (2) (continued)

Sub Address	R/W	Data name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
72h	R/W	P1	BLP1[3:0]				FRP1[1:0]		DLP1[1:0]	
73h	R/W	P2	BLP2[3:0]				FRP2[1:0]		DLP2[1:0]	
74h	R/W	P3	BLP3[3:0]				FRP3[1:0]		DLP3[1:0]	
75h	R/W	P4	BLP4[3:0]				FRP4[1:0]		DLP4[1:0]	
76h	R/W	P5	BLP5[3:0]				FRP5[1:0]		DLP5[1:0]	
77h	R/W	P6	BLP6[3:0]				FRP6[1:0]		DLP6[1:0]	
78h	R/W	P7	BLP7[3:0]				FRP7[1:0]		DLP7[1:0]	
79h	R/W	Q1	BLQ1[3:0]				FRQ1[1:0]		DLQ1[1:0]	
7Ah	R/W	Q2	BLQ2[3:0]				FRQ2[1:0]		DLQ2[1:0]	
7Bh	R/W	Q3	BLQ3[3:0]				FRQ3[1:0]		DLQ3[1:0]	
7Ch	R/W	Q4	BLQ4[3:0]				FRQ4[1:0]		DLQ4[1:0]	
7Dh	R/W	Q5	BLQ5[3:0]				FRQ5[1:0]		DLQ5[1:0]	
7Eh	R/W	Q6	BLQ6[3:0]				FRQ6[1:0]		DLQ6[1:0]	
7Fh	R/W	Q7	BLQ7[3:0]				FRQ7[1:0]		DLQ7[1:0]	

Established : 2009-07-23
Revised : 2013-04-01

OPERATION (continued)

3. Register map (1) Detail descriptions

Address 00h to 08h

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
00h RST	Data name	—	—	—	—	—	—	RAMRST	SRST
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : SRST Soft reset control bit
[0] : Reset release state (default)
[1] : Reset control

*After Reset operation, this register returns from “1” to “0” automatically.

D1 : RAMRST RAM reset control bit for address 09h to 7Fh
[0] : RAM reset release state (default)
[1] : RAM reset control

*After Reset operation, this register returns from “1” to “0” automatically.

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
01h POWERCNT	Data name	—	—	—	—	—	—	—	OSCEN
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : OSCEN ON/OFF bit for internal oscillator
[0] : Internal oscillator is off. (default)
[1] : Internal oscillator is on

- The variation width of internal oscillator is 0.96 MHz to 1.44 MHz.
- The variation width of internal clock is 694.4 ns to 1042 ns.

OPERATION (continued)

3. Register map (1) Detail descriptions (continued)

Address 00h to 08h(continued)

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
02h LDOCNT	Data name	—	—	—	—	—	—	—	REG18
	Default	0	0	0	0	0	0	0	1
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : REG18 ON/OFF control for LDO (at LDOCNT = Low)

[0] : LDO OFF

[1] : LDO ON (default)

- LDO turns on regardless of the state of REG18 at LDOCNT = High.
- Set LDOCNT to Low after setting REG18 to "0" to shift to OFF mode.

Sub address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
03h LSITEST	Data name	—	—	—	—	—	—	—	—
	Default	0	0	0	0	0	0	0	1
	mode	R	R	R	R	R	R	R	R

D7-0 : Register for LSI Test

- Access is prohibited

Established : 2009-07-23
Revised : 2013-04-01