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Panasonic

AN32180A

http://www.semicon.panasonic.co.jp/en/

4 x 4 Dots Matrix LED Driver LSI

FEATURES

- 4 × 4 LED Matrix Driver (Total LED that can be driven = 16)
- LED Selectable Maximum Current
- LED Music Synchronizing Function
- I^2C interface (Standard Mode, Fast Mode and Fast Mode Plus) (4 Slave address selectable)
- 16 pin Plastic Quad Flat Non-leaded Package (QFN Type)

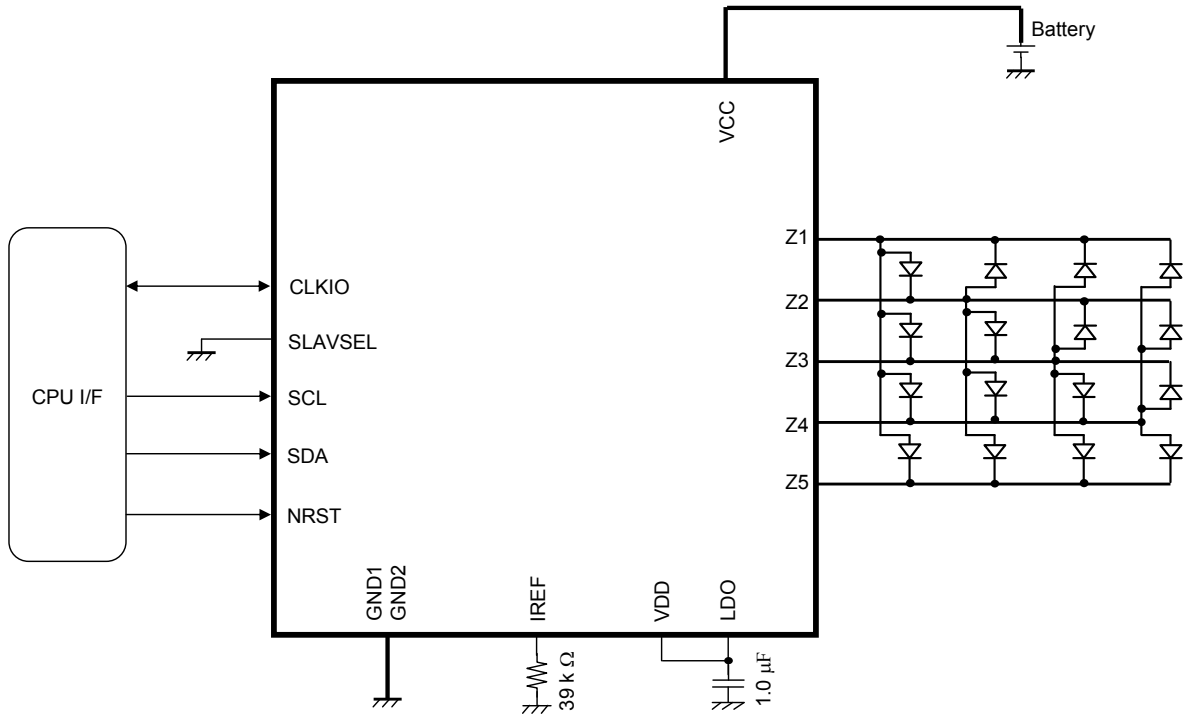
DESCRIPTION

AN32180A is a 16 Dots Matrix LED Driver.
It can drive up to 4 channels of RGB LEDs.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note)
This application circuit is an example. The operation of the mass production set is not guaranteed. Customers shall perform enough evaluation and verification on the design of mass production set. Customers shall be fully responsible for the incorporation of the above application circuit and information in the design of the equipment.

Established : 2011-07-29
Revised : 2013-03-22

CONTENTS

Established : 2011-07-29
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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VCC_{MAX}	6.0	V	*1
	VDD_{MAX}	6.0	V	*1
Operating ambience temperature	T_{opr}	– 30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	SLAVSEL, SCL, SDA, CLKIO, NRST	– 0.3 to 6.0	V	—
Output Voltage Range	IREF, LDO, CLKIO, Z1, Z2, Z3, Z4, Z5	– 0.3 to 6.0	V	—
ESD	HBM	2.0	kV	—

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1: VCC_{MAX} = VCC, VDD_{MAX} = VDD.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for operating ambient temperature, operating junction temperature and storage temperature, all ratings are for Ta = 25°C.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
16 pin Plastic Quad Flat Non-leaded package (QFN Type)	189.2 °C /W	0.529 W	0.212 W

Note) For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this LSI has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VCC	3.1	5.0	5.5	V	—
	VDD	1.7	5.0	5.5	V	—
Input Voltage Range	SLAVSEL, SCL, SDA, CLKIO	– 0.3	—	VDD + 0.3	V	*1
	NRST	– 0.3	—	VCC + 0.3	V	*1
Output Voltage Range	IREF, LDO, CLKIO, Z1, Z2, Z3, Z4, Z5	– 0.3	—	VCC + 0.3	V	*1

Note) Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for GND.
VCC is voltage for VCC. VDD is voltage for VDD.
Do not apply external currents or voltages to any pin not specifically mentioned.
*1 : (VCC + 0.3) V must not exceed 6 V. (VDD + 0.3) V must not exceed 6 V.

Established : 2011-07-29
Revised : 2013-03-22

ELECTRICAL CHARACTERISTICS

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Circuit Current							
Circuit Current (1) OFF Mode	ICC1	NRST = 0 V	—	0	1	μA	—
Circuit Current (2) OFF Mode	ICC2	NRST = High	—	250	500	μA	—
Internal Oscillator							
Oscillation Frequency	FDC1	VCC = 3.6 V	1.92	2.40	2.88	MHz	—
SCAN Switch							
Switch On Resistance	RSCAN	VCC = 3.6 V $I_{Z1\sim Z4}$ = – 20 mA	—	1.5	3	Ω	—
Constant Voltage Source (LDO)							
Output voltage (1)	VL1	I_{LDO} = – 10 μA	2.75	2.85	2.95	V	—
Output voltage (2)	VL2	I_{LDO} = – 15 mA	2.75	2.85	2.95	V	—
CLKIO							
High Level Input Voltage Range	VIH1	High Level Acknowledged Voltage (At External CLK Input Mode)	0.7 × VDD	—	VDD + 0.3	V	—
Low Level Input Voltage Range	VIL1	Low Level Acknowledged Voltage (At External CLK Input Mode)	– 0.3	—	0.3 × VDD	V	—
High Level Output Voltage	VOH1	I_{CLKIO} = – 1 mA (At Internal CLK Output Mode)	0.8 × VDD	—	VDD + 0.3	V	—
Low Level Output Voltage	VOL1	I_{CLKIO} = 1 mA (At Internal CLK Output Mode)	– 0.3	—	0.2 × VDD	V	—
High Level input Current	IIH1	VCC = 5.5 V V_{CLKIO} = 5.5 V	– 1	0	1	μA	—
Low Level input Current	IIL1	VCC = 5.5 V V_{CLKIO} = 0 V	– 1	0	1	μA	—

Established : 2011-07-29
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ELECTRICAL CHARACTERISTICS (continued)

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Constant Current Source (Matrix LED)							
Output Current (1)	IMX1	LED Current Setting = 20.2 mA IMAX = [011], BRTXX = [1010] $V_{Z1~Z5}$ = 1 V	19.2	20.2	21.2	mA	*1
DAC Current Step	DACSTEP	DAC Constant Current Mode LED Current Setting = 20.2 mA IMAX = [011], BRTXX = [1010] $V_{Z1~Z5}$ = 1 V, IDAC1 = $I_{Z1~Z5}$ LED Current Setting = 22 mA IMAX = [011], BRTXX = [1011] $V_{Z1~Z5}$ = 1 V, IDAC2 = $I_{Z1~Z5}$ DACSTEP = IDAC2 – IDAC1	0	2	4	mA	—
OFF Mode Leak Current1	IMXOFF1	VCC = 5.5 V, VDD = 5.5 V OFF Mode $V_{Z1~Z5}$ = 5.5 V	– 1	—	1	µA	—
OFF Mode Leak Current2	IMXOFF2	VCC = 5.5 V, VDD = 5.5 V OFF Mode $V_{Z1~Z5}$ = 0 V	– 1	—	1	µA	—
Channel Difference	IMXCH	LED Current Setting = 20.2 mA IMAX = [011], BRTXX = [1010] Difference of Z1 to 5 current from the average current value	– 5	—	5	%	—
Voltage at which LED driver can keep constant current value							
LED Driver Voltage	VLD2	LED Current Setting = 20.2 mA IMAX = [011], BRTXX = [1010] Voltage at which LED Current change within ± 5 % compared with LED Current of pin voltage = 0.5 V.	0.4	—	—	V	—

Note) * 1: This is allowable value when recommended parts (ERJ2RHD393X) are used for the terminal IREF.

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ELECTRICAL CHARACTERISTICS (continued)

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SLAVSEL							
High Level Input Voltage Range	VIH2	High Level Acknowledged Voltage	0.7 × VDD	—	VDD + 0.3	V	—
Low Level Input Voltage Range	VIL2	Low Level Acknowledged Voltage	– 0.3	—	0.3 × VDD	V	—
High Level Input Current	IIH2	VCC = 5.5 V $V_{SLAVSEL}$ = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	IIL2	VCC = 5.5 V $V_{SLAVSEL}$ = 0 V	– 1	0	1	µA	—
NRST							
High Level Input Voltage Range	VIH3	High Level Acknowledged Voltage	1.5	—	VCC + 0.3	V	—
Low Level Input Voltage Range	VIL3	Low Level Acknowledged Voltage	– 0.3	—	0.6	V	—
High Level Input Current	IIH3	VCC = 5.5 V V_{NRST} = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	IIL3	VCC = 5.5 V V_{NRST} = 0 V	– 1	0	1	µA	—
I²C bus (Internal I/O stage characteristics)							
Low-level input voltage	V_{IL}	Voltage which recognized that SDA and SCL are Low-level	– 0.5	—	0.3 × VDD	V	*2
High-level input voltage	V_{IH}	Voltage which recognized that SDA and SCL are High-level	0.7 × VDD	—	VDD_{MAX} + 0.5	V	*2
Low-level output voltage 1	V_{OL1}	VDD > 2 V I_{SDA} = 3 mA	0	—	0.4	V	—
Low-level output voltage 2	V_{OL2}	VDD < 2 V I_{SDA} = 3 mA	0	—	0.2 × VDD	V	—
Low-level output current	I_{OL}	V_{SDA} = 0.4 V	20	—	—	mA	—
Input current each I/O pin	I_i	VCC = 5.5 V, VDD = 5.5 V V_{SCL}, V_{SDA} = 0.1 VDD_{MAX} to 0.9 VDD_{MAX}	– 10	0	10	µA	—
SCL clock frequency	f_{SCL}	—	0	—	1000	kHz	—

Note) VDD_{max} refers to the maximum operating supply voltage of VDD.

*2 : The input threshold voltage of I²C bus (Vth) is linked to VDD (I²C bus I/O stage supply voltage).
In case the pull-up voltage is not VDD, the threshold voltage (Vth) is fixed to ((VDD / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.
In this case, pay attention to Low-level (max.) value (V_{ILMAX}).
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (VDD).

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ELECTRICAL CHARACTERISTICS (continued)

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
TSD (Thermal shutdown protection circuit)							
Detection temperature	Tdet	Temperature which Constant current circuit, and Matrix SW turn off.	—	150	—	°C	*3 *4
Constant Voltage Source (LDO)							
Ripple rejection ratio (1)	PSL11	VCC = 3.6 V + 0.3 V [p-p] f = 1 kHz I_{LDO} = – 15 mA PSL11 = 20 log (acV_{LDO} / 0.3)	—	– 50	—	dB	*4
Ripple rejection ratio (2)	PSL12	VCC = 3.6 V + 0.3 V[p-p] f = 10 kHz I_{LDO} = – 15 mA PSL12 = 20 log (acV_{LDO} / 0.3)	—	– 40	—	dB	*4
Short-circuit protection current	IPT1	V_{LDO} = 0 V	—	40	—	mA	*4
I²C bus (Internal I/O stage characteristics) (Continued)							
Hysteresis of Schmitt trigger input 1	V_{hys1}	VDD > 2 V, Hysteresis of SDA, SCL	0.05 × VDD	—	—	V	*5 *6
Hysteresis of Schmitt trigger input 2	V_{hys2}	VDD < 2 V, Hysteresis of SDA, SCL	0.1 × VDD	—	—	V	*5 *6
Output fall time from V_{IHmin} to V_{ILmax}	t_{of}	Bus capacitance : 10 pF to 550 pF $I_P \leq 20$ mA (V_{OLmax} = 0.4 V) I_P : Max. sink current	—	—	120	ns	*5 *6
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	—	0	—	50	ns	*5 *6
Capacitance for each I/O pin	C_i	—	—	—	10	pF	*5 *6

Note) *3 : Constant current circuit, and Matrix SW turn off and IC reset when TSD operates.
*4 : Typical Design Value
*5 : The timing of Fast-mode Plus devices in I²C-bus is specified in Page.10. All values referred to V_{IHMIN} and V_{ILMAX} level.
*6 : These are values checked by design but not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Bus line specifications) (Continue)							
Hold time (repeated) START condition	$t_{HD:STA}$	The first clock pulse is generated after $t_{HD:STA.}$	0.26	—	—	µs	*5 *6
Low period of the SCL clock	t_{LOW}	—	0.5	—	—	µs	*5 *6
High period of the SCL clock	t_{HIGH}	—	0.26	—	—	µs	*5 *6
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.26	—	—	µs	*5 *6
Data hold time	$t_{HD:DAT}$	—	0	—	—	µs	*5 *6
Data set-up time	$t_{SU:DAT}$	—	50	—	—	ns	*5 *6
Rise time of both SDA and SCL signals	t_r	—	—	—	120	ns	*5 *6
Fall time of both SDA and SCL signals	t_f	—	—	—	120	ns	*5 *6
Set-up time of STOP condition	$t_{SU:STO}$	—	0.26	—	—	µs	*5 *6
Bus free time between STOP and START condition	t_{BUF}	—	0.5	—	—	µs	*5 *6
Capacitive load for each bus line	C_b	—	—	—	550	pF	*5 *6
Data valid time	$t_{VD:DAT}$	—	—	—	0.45	µs	*5 *6
Data valid acknowledge	$t_{VD:ACK}$	—	—	—	0.45	µs	*5 *6
Noise margin at the Low-level for each connected device	V_{nL}	—	0.1 × VDD	—	—	V	*5 *6
Noise margin at the High-level for each connected device	V_{nH}	—	0.2 × VDD	—	—	V	*5 *6

Note) *5 : The timing of Fast-mode Plus devices in I²C-bus is specified in Page.10. All values referred to V_{IHMIN} and V_{ILMAX} level.
*6 : These are values checked by design but not production tested.

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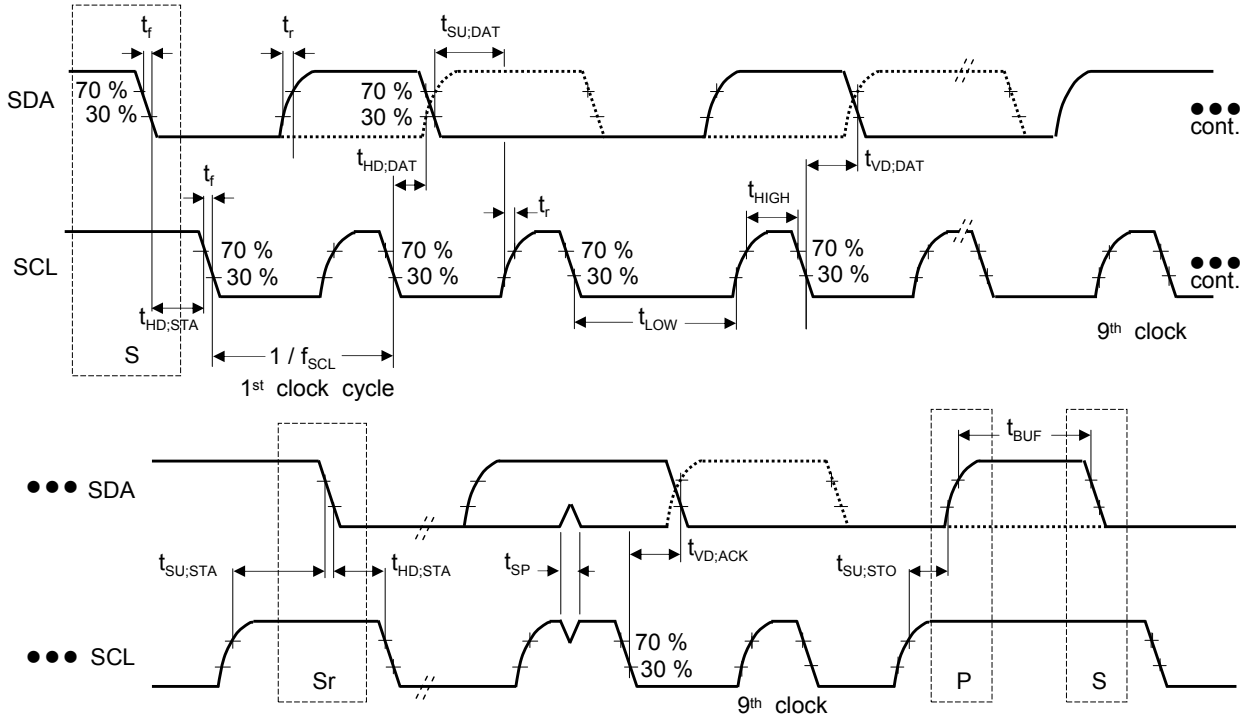
ELECTRICAL CHARACTERISTICS (continued)

VCC = 3.6 V, VDD = 1.85 V

Note) Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned



V_{ILMAX} = 0.3 V_{DD}

V_{IHMIN} = 0.7 V_{DD}

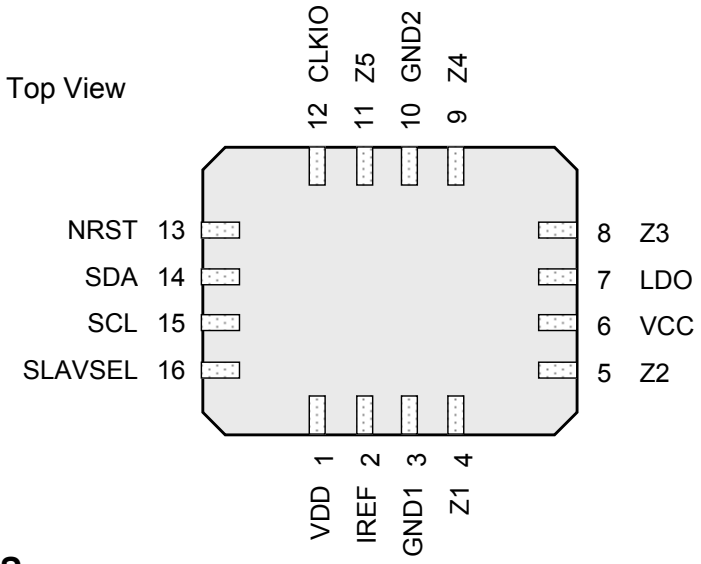
S : START condition

Sr : Repeat START condition

P : STOP condition

Establ ished : 2 0 1-0 7-2 9
Revised : 2 0 1-0 3-2 2

PIN CONFIGURATION



PIN FUNCTIONS

Pin No.	Pin name	Type	Description	Pin processing at unused
1	VDD	Power supply	Power supply pin for I²C interface	(Required pin)
2	IREF	Output	Resistor connection pin for constant current setup	(Required pin)
3 10	GND1 GND2	Ground	Ground pin	(Required pin)
4	Z1	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
5	Z2	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
6	VCC	Power supply	Power supply pin for matrix driver and Internal reference circuit	Battery or External power supply
7	LDO	Output	LDO output pin	(Required pin)
8	Z3	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
9	Z4	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
11	Z5	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
12	CLKIO	Input/Output	Reference clock input output / Music Input pin	Open
13	NRST	Input	Reset input pin	(Required pin)
14	SDA	Input/Output	Data input / output pin for I²C interface	(Required pin)
15	SCL	Input	Clock input pin for I²C interface	(Required pin)
16	SLAVSEL	Input	Slave address selection pin for I²C interface	(Required pin)

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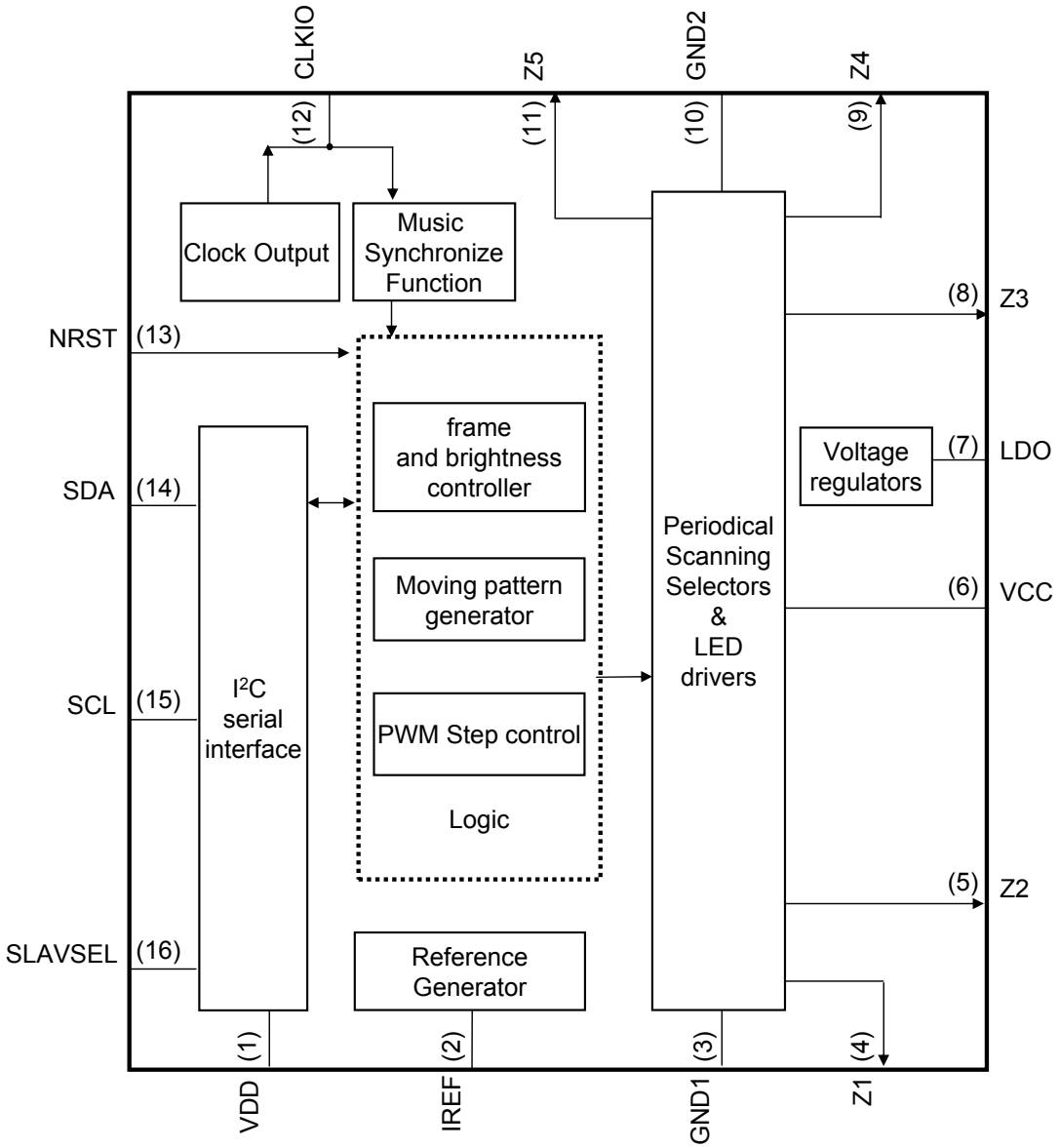
FUNCTIONAL BLOCK DIAGRAM



Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

Established : 2011-07-29
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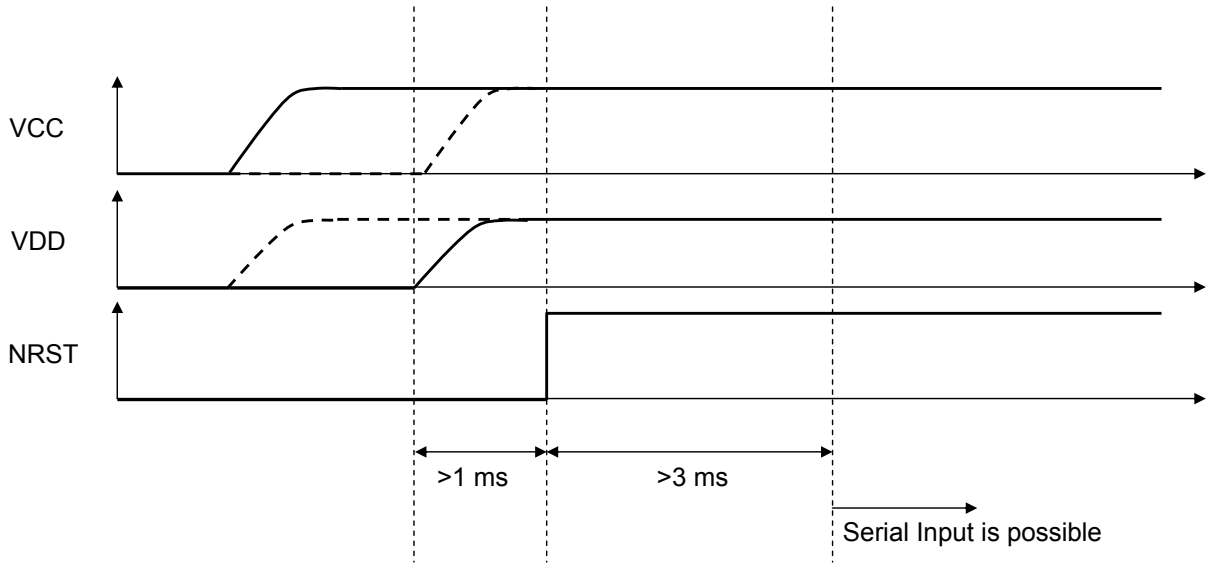
OPERATION

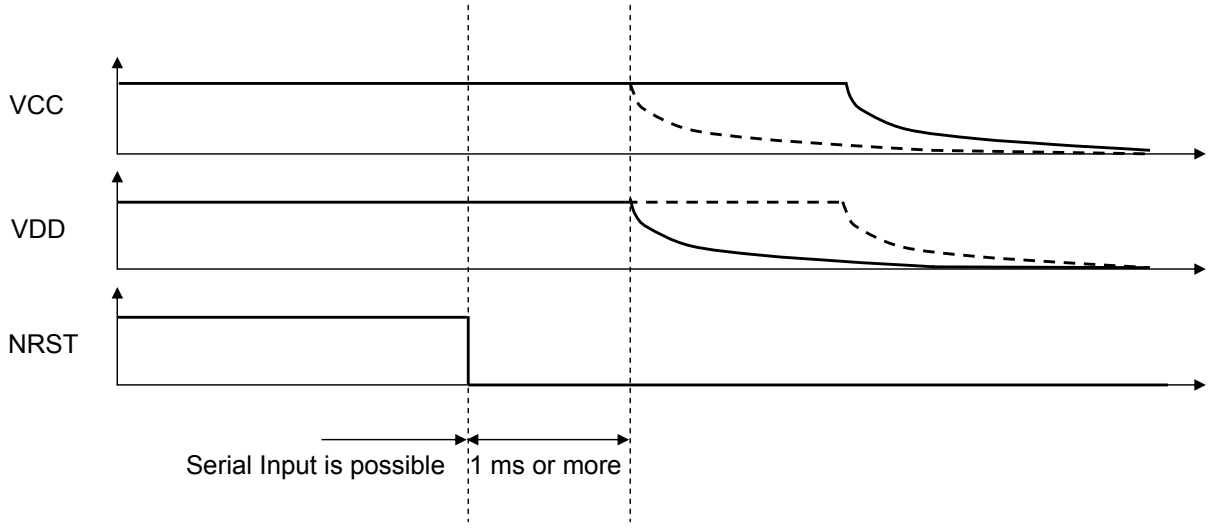
1. Power Supply Sequence

Power ON



Note) For the Startup Timing of VCC and VDD, it is possible to be changed.

Power OFF



Note) For the Shut down Timing of VCC and VDD, it is possible to be changed.

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OPERATION (continued)

2. Register Map

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
01h	RST	00h	R/W	--	--	--	--	--	--	RAMRST	SRST
02h	POWERCNT	00h	R/W		--	--	--	--	--	--	OSCEN
03h	reserved	--	--	--	--	--	--	--	--	--	--
04h	OPTION	00h	R/W	--	--	--	--	ZPDEN	MLDACT	CLKOUT	EXTCLK
05h	MTXON	1Eh	R/W	--	--	--	IMAX Reserved	IMAX[2:0]			MTXON
06h	PWMEN1	00h	R/W	PWMB4	PWMB3	PWMB2	PWMB1	PWMA4	PWMA3	PWMA2	PWMA1
07h	PWMEN2	00h	R/W	PWMD4	PWMD3	PWMD2	PWMD1	PWMC4	PWMC3	PWMC2	PWMC1
08h	MDLEN1	00h	R/W	MLDB4	MLDB3	MLDB2	MLDB1	MLDA4	MLDA3	MLDA2	MLDA1
09h	MDLEN2	00h	R/W	MLDD4	MLDD3	MLDD2	MLDD1	MLDC4	MLDC3	MLDC2	MLDC1
0Ah	MDLMODE2	00h	R/W	--	GRP_ALL	GRP8_1	GRP8_0	GRP4_3	GRP4_2	GRP4_1	GRP4_0
0Bh	MLDCOM	03h	R/W	--	--	--	--	--	MLDCOM[2:0]		
0Ch	THOLD	00h	R/W	THOLD[7:0]							
0Dh	XCONST	00h	R/W	--	--	--	X5	X4	X3	X2	X1
0Eh	YCONST	00h	R/W	Y4	Y3	Y2	Y1	Y4MSK	Y3MSK	Y2MSK	Y1MSK
0Fh	SLPTIME	00h	R/W	--	SCANSET[1:0]		FADTIM	SLOPEEXTL[1:0]		SLOPEEXTH[1:0]	

Note) "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used.
For data bits indicated by "--" in other registers except for "reversed" registers, will return "zero" value if these bits are read.
Writing to these bits will be ignored. IMAX Reserved will give default value [1].

OPERATION (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
10h	DTA1	00h	R/W	DTA1[7:0]							
11h	DTA2	00h	R/W	DTA2[7:0]							
12h	DTA3	00h	R/W	DTA3[7:0]							
13h	DTA4	00h	R/W	DTA4[7:0]							
14h	DTB1	00h	R/W	DTB1[7:0]							
15h	DTB2	00h	R/W	DTB2[7:0]							
16h	DTB3	00h	R/W	DTB3[7:0]							
17h	DTB4	00h	R/W	DTB4[7:0]							
18h	DTC1	00h	R/W	DTC1[7:0]							
19h	DTC2	00h	R/W	DTC2[7:0]							
1Ah	DTC3	00h	R/W	DTC3[7:0]							
1Bh	DTC4	00h	R/W	DTC4[7:0]							
1Ch	DTD1	00h	R/W	DTD1[7:0]							
1Dh	DTD2	00h	R/W	DTD2[7:0]							
1Eh	DTD3	00h	R/W	DTD3[7:0]							
1Fh	DTD4	00h	R/W	DTD4[7:0]							
20h	A1	00h	R/W	BRTA1[3:0]				--	SDTA1[2:0]		
21h	A2	00h	R/W	BRTA2[3:0]				--	SDTA2[2:0]		
22h	A3	00h	R/W	BRTA3[3:0]				--	SDTA3[2:0]		
23h	A4	00h	R/W	BRTA4[3:0]				--	SDTA4[2:0]		
24h	B1	00h	R/W	BRTB1[3:0]				--	SDTB1[2:0]		
25h	B2	00h	R/W	BRTB2[3:0]				--	SDTB2[2:0]		
26h	B3	00h	R/W	BRTB3[3:0]				--	SDTB3[2:0]		
27h	B4	00h	R/W	BRTB4[3:0]				--	SDTB4[2:0]		
28h	C1	00h	R/W	BRTC1[3:0]				--	SDTC1[2:0]		
29h	C2	00h	R/W	BRTC2[3:0]				--	SDTC2[2:0]		
2Ah	C3	00h	R/W	BRTC3[3:0]				--	SDTC3[2:0]		
2Bh	C4	00h	R/W	BRTC4[3:0]				--	SDTC4[2:0]		
2Ch	D1	00h	R/W	BRTD1[3:0]				--	SDTD1[2:0]		
2Dh	D2	00h	R/W	BRTD2[3:0]				--	SDTD2[2:0]		
2Eh	D3	00h	R/W	BRTD3[3:0]				--	SDTD3[2:0]		
2Fh	D4	00h	R/W	BRTD3[3:0]				--	SDTD4[2:0]		

Note) Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
Writing to these bits will be ignored.

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OPERATION (continued)

3. Register map Detailed Explanation

Register Name		RST							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
01h	R/W	--	--	--	--	--	--	RAMRST	SRST
Default	00h	0	0	0	0	0	0	0	0

D1 : RAMRST RAM reset
[0] : RAM can be overwritten (default)
[1] : Clear all PWM duty setting and intensity setting

D0 : SRST Soft reset control
[0] : Reset release state (default)
[1] : Reset reset

• This register will auto-return to zero when written with "High" logic value.

Register Name		POWERCNT							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
02h	R/W	--	--	--	--	--	--	--	OSCEN
Default	00h	0	0	0	0	0	0	0	0

D0 : OSCEN Internal oscillator ON/OFF bit
[0] : Internal oscillator OFF (default)
[1] : Internal oscillator ON

• Oscillator will auto turn ON if any of the LED drivers are enabled (MTXON = 1) even if this bit is [0].

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		OPTION							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
04h	R/W	--	--	--	--	ZPDEN	MLDACT	CLKOUT	EXTCLK
Default	00h	0	0	0	0	0	0	0	0

D3 : ZPDEN Ghost Image Prevention Enable
[0] : Turn off ghost image prevention (default)
[1] : Turn on ghost image prevention

D2 : MLDACT External Melody Input Selection
[0] : Turn off melody mode (default)
[1] : Turn on melody mode

D1 : CLKOUT Internal clock output enable
[0] : Internal clock is not output from CLKOUT (default)
[1] : Internal clock is output from CLKOUT

D0 : EXTCLK Internal/external synchronous clock selection
[0] : Internal clock operation (default)
[1] : External clock operation

- Ghost Image Prevention may not remove the ghost image perfectly. It depends on the LED color combination and LED connection method. Please refer to Page.46 for details.
  Please refer to Page.47 for details especially when this LSI is used for RGB driver.
- For D2, D1 and D0 cannot be set to High at the same time. In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.

Register Name		MTXON							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
05h	R/W	--	--	--	IMAX Reserved	IMAX[2:0]			MTXON
Default	1Eh	0	0	0	1	1	1	1	0

D3-1 : IMAX Maximum current setup selection

[000] : 7.5 mA	[100] : 37.5 mA
[001] : 15 mA	[101] : 45 mA
[010] : 22.5 mA	[110] : 52.5 mA
[011] : 30 mA	[111] : 60 mA (default)

D0 : MTXON LED Matrix Set up ON/OFF control
[0] : OFF (default)
[1] : ON

- For better accuracy, it is advisable to set IMAX at 30 mA (IMAX = 011). The brightness can be adjusted lower by using brightness register (BRT*[3:0] (register #20h to #2Fh)) or PWM register (DT*[7:0] (register #10h to #1Fh)).

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		PWMEN1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
06h	R/W	PWMB4	PWMB3	PWMB2	PWMB1	PWMA4	PWMA3	PWMA2	PWMA1
Default	00h	0	0	0	0	0	0	0	0

D7 : PWMB4 B4 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D6 : PWMB3 B3 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D5 : PWMB2 B2 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D4 : PWMB1 B1 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D3 : PWMA4 A4 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D2 : PWMA3 A3 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D1 : PWMA2 A2 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D0 : PWMA1 A1 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		PWMEN2							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
07h	R/W	PWMD4	PWMD3	PWMD2	PWMD1	PWMC4	PWMC3	PWMC2	PWMC1
Default	00h	0	0	0	0	0	0	0	0

D7 : PWMD4 D4 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D6 : PWMD3 D3 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D5 : PWMD2 D2 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D4 : PWMD1 D1 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D3 : PWMC4 C4 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D2 : PWMC3 C3 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D1 : PWMC2 C2 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

D0 : PWMC1 C1 PWM mode enable
[0] : Not PWM mode (default)
[1] : PWM mode

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MDLEN1							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
08h	R/W	MLDB4	MLDB3	MLDB2	MLDB1	MLDA4	MLDA3	MLDA2	MLDA1
Default	00h	0	0	0	0	0	0	0	0

D7 : MLDB4 B4 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D6 : MLDB3 B3 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D5 : MLDB2 B2 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D4 : MLDB1 B1 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D3 : MLDA4 A4 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D2 : MLDA3 A3 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D1 : MLDA2 A2 Melody mode enable
[0] : Not PWM mode (default)
[1] : Melody mode

D0 : MLDA1 A1 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MDLEN2							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
09h	R/W	MLDD4	MLDD3	MLDD2	MLDD1	MLDC4	MLDC3	MLDC2	MLDC1
Default	00h	0	0	0	0	0	0	0	0

D7 : MLDD4 D4 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D6 : MLDD3 D3 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D5 : MLDD2 D2 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D4 : MLDD1 D1 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D3 : MLDC4 C4 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D2 : MLDC3 C3 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

D1 : MLDC2 C2 Melody mode enable
[0] : Not PWM mode (default)
[1] : Melody mode

D0 : MLDC1 C1 Melody mode enable
[0] : Not Melody mode (default)
[1] : Melody mode

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MDLMODE2							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Ah	R/W	--	GRP_ALL	GRP8_1	GRP8_0	GRP4_3	GRP4_2	GRP4_1	GRP4_0
Default	00h	0	0	0	0	0	0	0	0

D6 : GRP_ALL All LED blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode
(D1→C1→B1→A1→D2→C2→B2→A2→D3→C3→B3→A3→D4→C4→B4→A4)

D5 : GRP8_1 Column 3 and Column 4 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D3→C3→B3→A3→D4→C4→B4→A4)

D4 : GRP8_0 Column 1 and Column 2 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D1→C1→B1→A1→D2→C2→B2→A2)

D3 : GRP4_3 Column 4 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D4→C4→B4→A4)

D2 : GRP4_2 Column 3 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D3→C3→B3→A3)

D1 : GRP4_1 Column 2 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D2→C2→B2→A2)

D0 : GRP4_0 Column 1 blink with external input as a group
[0] : Normal (default)
[1] : Bar meter mode (D1→C1→B1→A1)

A1	A2	A3	A4
B1	B2	B3	B4
C1	C2	C3	C4
D1	D2	D3	D4

GRP_ALL	GRP8_0	GRP4_0	MLDA1	Melody Modes
0	0	0	0	Normal mode
1	x	x	x	Bar meter mode of all LED
0	1	x	x	Bar meter mode of Column 1 and Column 2
0	0	1	x	Bar meter mode of Column 1
0	0	0	1	Melody mode of A1

• During Bar Meter Mode, auto threshold detection should be used. This LSI does not support Bar Meter Mode with fixed threshold setting.

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MLDCOM							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Bh	R/W	--	--	--	--	--	MLDCOM[2:0]		
Default	03h	0	0	0	0	0	0	1	1

D2-0 : MLDCOM LED Turn on time compensation in melody mode

[000] : 0 s
[001] : 0.86 µs
[010] : 1.72 µs
[011] : 2.58 µs (default)
[100] : 3.44 µs
[101] : 4.30 µs
[110] : 5.17 µs
[111] : 6.03 µs

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		THOLD							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Ch	R/W	THOLD[7:0]							
Default	00h	0	0	0	0	0	0	0	0

D7 : THOLD[7] Threshold 8 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 8 is used. (Threshold 8 is about 1.93 V)

D6 : THOLD[6] Threshold 7 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 7 is used. (Threshold 7 is about 1.80 V)

D5 : THOLD[5] Threshold 6 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 6 is used. (Threshold 6 is about 1.67 V)

D4 : THOLD[4] Threshold 5 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 5 is used. (Threshold 5 is about 1.55 V)

D3 : THOLD[3] Threshold 4 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 4 is used. (Threshold 4 is about 1.42 V)

D2 : THOLD[2] Threshold 3 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 3 is used. (Threshold 3 is about 1.30 V)

D1 : THOLD[1] Threshold 2 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 2 is used. (Threshold 2 is about 1.17 V)

D0 : THOLD[0] Threshold 1 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 1 is used. (Threshold 1 is about 1.04 V)

- When all bits are set zero, threshold is in auto-detection mode (default)
- Do not set more than 1 register bit to logic "High" value at the same time.
- If 2 bits are set to "High" at the same time, system will only recognize the first "High" bit threshold that is set.

OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		XCONST							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	R/W	--	--	--	X5	X4	X3	X2	X1
Default	00h	0	0	0	0	0	0	0	0

D4 : X5 Z5 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z5 is fixed as constant current mode. The LED D1's current setting is used.

D3 : X4 Z4 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z4 is fixed as constant current mode. The LED A4's current setting is used.

D2 : X3 Z3 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z3 is fixed as constant current mode. The LED A3's current setting is used.

D1 : X2 Z2 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z2 is fixed as constant current mode. The LED A2's current setting is used.

D0 : X1 Z1 is fixed as constant current mode.
[0] : Normal matrix operation (default)
[1] : Z1 is fixed as constant current mode. The LED A1's current setting is used.

• Please refer to Page.30 for details.

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