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Panasonic

AN32181B

http://www.semicon.panasonic.co.jp/en/

12 x 12 Dots Matrix LED Driver IC

FEATURES

- 12 × 12 LED Matrix Driver
  (Total LED that can be driven = 144)
- LED Selectable Maximum Current
- LED Melody Mode Function
- LED Open/Short Detection
- LED Ghost Image Prevention Function
- SPI Interface
- I²C interface
  (Standard Mode, Fast Mode and Fast Mode Plus)
  (4 Slave address selectable)
- 28 pin Plastic Quad Flat Non-leaded Package
  (QFN Type)

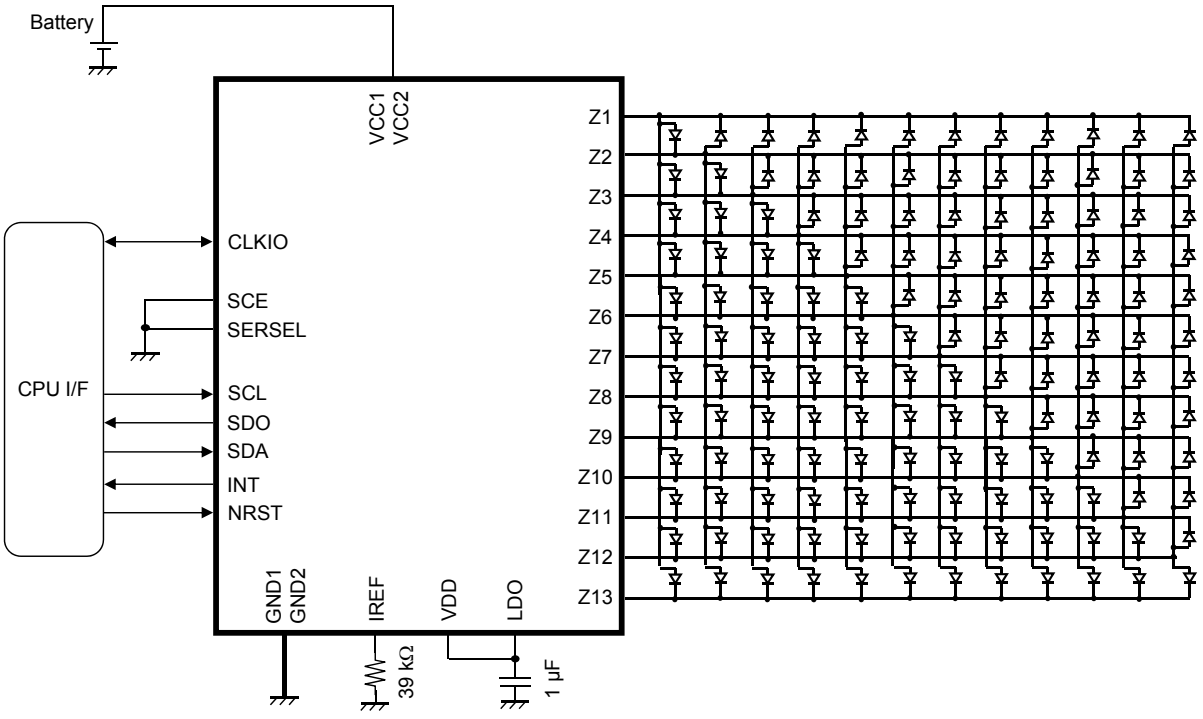
DESCRIPTION

AN32181B is a 144 Dots Matrix LED Driver.
It can drive up to 48 RGB LEDs.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note:
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

Established : 2012-02-07
Revised : 2014-09-01

CONTENTS

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ORDERING INFORMATION

Order Number	Feature	Package	Output Supply
AN32181B-VB	Matrix LED Driver	28 pin QFN	Emboss Taping

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VCC_{MAX}	6.0	V	*1
	VDD_{MAX}	6.0	V	*1
Operating ambience temperature	T_{opr}	– 30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	V_{SERSEL}, V_{SCL}, V_{SDA}, V_{SCE}, V_{CLKIO}, V_{NRST}	– 0.3 to 6.0	V	—
Output Voltage Range	V_{INT}, V_{CLKIO}, V_{SDO}, V_{Z1}, V_{Z2}, V_{Z3}, V_{Z4}, V_{Z5}, V_{Z6}, V_{Z7}, V_{Z8}, V_{Z9}, V_{Z10}, V_{Z11}, V_{Z12}, V_{Z13}	– 0.3 to 6.0	V	—
	V_{LDO}	– 0.3 to 4.0	V	—
ESD	HBM	2.0	kV	—

Note: This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

VCC_{MAX} is voltage for VCC1 and VCC2. VCC1 = VCC2.

VDD_{MAX} is voltage for VDD.

Do not apply external currents or voltages to any pin not specifically mentioned.

*1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for operating ambient temperature, operating junction temperature and storage temperature, all ratings are for Ta = 25°C.

POWER DISSIPATION RATING

Package	θ_{j-a}	P_D (Ta = 25 °C)	P_D (Ta = 85 °C)
28 pin Plastic Quad Flat Non-leaded package (QFN Type)	175.5 °C / W	0.569 W	0.228 W

Note: For the actual usage, please refer to the P_D-Ta characteristics diagram in the Package Standards, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage range	V_{CC}	3.1	3.6	5.5	V	*1
	V_{DD}	1.70	1.85	5.50	V	*1
Input Voltage Range	V_{SCL}, V_{SDA}, V_{SCE}, V_{CLKIO}	– 0.3	—	V_{DD} + 0.3	V	*2
	V_{SERSEL}, V_{NRST}	– 0.3	—	V_{CC} + 0.3	V	*2
Output Voltage Range	V_{INT}, V_{CLKIO}, V_{SDO}	– 0.3	—	V_{DD} + 0.3	V	*2
	V_{Z1}, V_{Z2}, V_{Z3}, V_{Z4}, V_{Z5}, V_{Z6}, V_{Z7}, V_{Z8}, V_{Z9}, V_{Z10}, V_{Z11}, V_{Z12}, V_{Z13}	– 0.3	—	V_{CC} + 0.3	V	*2
	V_{LDO}	– 0.3	—	3.5	V	—

Note: *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for GND1 and GND2.
GND1 = GND2.
V_{CC} is voltage for VCC1 and VCC2. VCC1 = VCC2.
V_{DD} is voltage for VDD.
Do not apply external currents or voltages to any pin not specifically mentioned.
*2: (V_{CC} + 0.3) V must not exceed 6.0 V. (V_{DD} + 0.3) V must not exceed 6.0 V.

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ELECTRICAL CHARACTERISTICS

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Circuit Current							
Circuit Current (1) OFF Mode	I_{CC1}	V_{NRST} = 0 V	—	0	1	μA	—
Circuit Current (2) OFF Mode	I_{CC2}	V_{NRST} = High	—	240	500	μA	—
Internal Oscillator							
Oscillation Frequency	F_{DC1}	—	1.92	2.40	2.88	MHz	—
SCAN Switch							
Switch On Resistance	R_{SCAN}	$I_{Z1\ to\ Z12}$ = – 20 mA	—	1.0	2.5	Ω	—
Constant Voltage Source (LDO)							
Output voltage (1)	V_{L1}	I_{LDO} = – 10 μA	2.75	2.85	2.95	V	—
Output voltage (2)	V_{L2}	I_{LDO} = – 15 mA	2.75	2.85	2.95	V	—
CLKIO							
High Level Input Voltage Range	V_{IH1}	High Level Acknowledged Voltage (At External CLK Input Mode)	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Input Voltage Range	V_{IL1}	Low Level Acknowledged Voltage (At External CLK Input Mode)	– 0.3	—	0.3 × V_{DD}	V	—
High Level Output Voltage	V_{OH1}	I_{CLKIO} = – 1 mA (At Internal CLK Output Mode)	0.8 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Output Voltage	V_{OL1}	I_{CLKIO} = 1 mA (At Internal CLK Output Mode)	– 0.3	—	0.2 × V_{DD}	V	—
High Level input Current	I_{IH1}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{CLKIO} = 5.5 V	– 1	0	1	μA	—
Low Level input Current	I_{IL1}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{CLKIO} = 0 V	– 1	0	1	μA	—

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Constant Current Source (Matrix LED)							
Output Current (1)	I_{MX1}	LED Current Setting = 19.85 mA IMAX = [01010] $V_{Z1\ to\ Z13}$ = 1 V	18.85	19.85	20.85	mA	*1
IMAX Current Step	I_{MXSTEP}	Constant Current Mode LED current setting = 22 mA, IMAX = [01011] $V_{Z1\ to\ Z13}$ = 1 V, ILED1 = $I_{Z1\ to\ Z13}$ LED current setting = 19.85 mA, IMAX = [01010] $V_{Z1\ to\ Z13}$ = 1 V, ILED2 = $I_{Z1\ to\ Z13}$ IMXSTEP = ILED1 – ILED2	0.0	2.0	3.5	mA	—
OFF Mode Leak Current (1)	I_{MXOFF1}	V_{CC} = 5.5 V, V_{DD} = 5.5 V OFF Mode $V_{Z1\ to\ Z13}$ = 5.5 V	– 1	—	1	µA	—
OFF Mode Leak Current (2)	I_{MXOFF2}	V_{CC} = 5.5 V, V_{DD} = 5.5 V OFF Mode $V_{Z1\ to\ Z13}$ = 0 V	– 1	—	1	µA	—
Channel Difference	I_{MXCH}	LED Current Setting = 19.85 mA IMAX = [01010] Difference of Z1 to 13 current from the average current value	– 5	—	5	%	—
Voltage at which LED driver can keep constant current value							
LED Driver Voltage	V_{LD}	LED Current Setting = 19.85 mA IMAX = [01010] Voltage at which LED Current change within ± 5 % compared with LED Current of pin voltage = 0.5 V.	0.4	—	—	V	—

Note: * 1: This is allowable value when recommended parts (ERJ2RHD393X) are used for the terminal IREF.

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SERSEL							
High Level Input Voltage Range	V_{IH2}	High Level Acknowledged Voltage	0.7 × V_{CC}	—	V_{CC} + 0.3	V	—
Low Level Input Voltage Range	V_{IL2}	Low Level Acknowledged Voltage	– 0.3	—	0.3 × V_{CC}	V	—
High Level Input Current	I_{IH2}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{SERSEL} = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	I_{IL2}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{SERSEL} = 0 V	– 1	0	1	µA	—
NRST							
High Level Input Voltage Range	V_{IH3}	High Level Acknowledged Voltage	1.5	—	V_{CC} + 0.3	V	—
Low Level Input Voltage Range	V_{IL3}	Low Level Acknowledged Voltage	– 0.3	—	0.6	V	—
High Level Input Current	I_{IH3}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{NRST} = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	I_{IL3}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{NRST} = 0 V	– 1	0	1	µA	—
INT							
ON Resistance	R_{INTON}	I_{INT} = 5 mA	—	10	50	Ω	—
SDO							
High Level Output Voltage	V_{OH3}	I_{SDO} = – 3 mA	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Output Voltage	V_{OL3}	I_{SDO} = 3 mA	0	—	0.3 × VDD	V	—
SCE							
High-level input voltage range	V_{IH4}	High Level Acknowledged Voltage	V_{DD} × 0.7	—	V_{DD} + 0.5	V	—
Low-level input voltage range	V_{IL4}	Low Level Acknowledged Voltage	– 0.5	—	V_{DD} × 0.3	V	—
High-level input current	I_{IH4}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{SCE} = 5.5 V	– 1	0	1	µA	—
Low-level input current	I_{IL4}	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{SCE} = 0 V	– 1	0	1	µA	—

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Internal I/O stage characteristics) (SCL, SDA)							
Low-level input voltage	V_{IL}	Voltage which recognized that SDA and SCL are Low-level	– 0.5	—	0.3 × V_{DD}	V	*2
High-level input voltage	V_{IH}	Voltage which recognized that SDA and SCL are High-level	0.7 × V_{DD}	—	V_{DDmax} + 0.5	V	*2 *3
Low-level output voltage 1	V_{OL1}	V_{DD} > 2 V I_{SDA}, I_{SCL} = 3 mA	0	—	0.4	V	—
Low-level output voltage 2	V_{OL2}	V_{DD} < 2 V I_{SDA}, I_{SCL} = 3 mA	0	—	0.2 × V_{DD}	V	—
Low-level output current	I_{OL}	V_{SDA} = 0.4 V	20	—	—	mA	—
Input current each I/O pin	I_i	V_{CC} = 5.5 V , V_{DD} = 5.5 V V_{SDA}, V_{SCL} = 0.1 × V_{DDmax} to 0.9 × V_{DDmax}	– 10	0	10	µA	*3
SCL clock frequency	f_{SCL}	—	0	—	1000	kHz	—

Note: *2 : The input threshold voltage of I²C bus (Vth) is linked to V_{DD} (I²C bus I/O stage supply voltage).
In case the pull-up voltage is not V_{DD}, the threshold voltage (Vth) is fixed to ((V_{DD} / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.
In this case, pay attention to Low-level (max.) value (V_{ILmax}).
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (V_{DD}).

*3 : V_{DDmax} refers to the maximum operating supply voltage of V_{DD}.

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
TSD (Thermal shutdown protection circuit)							
Detection temperature	Tdet	Temperature which Constant current circuit, and Matrix SW turn off.	—	150	—	°C	*4 *5
Constant Voltage Source (LDO)							
Ripple rejection ratio (1)	PSL11	V_{CC} = 3.6 V + 0.3 V[p-p] f = 1 kHz I_{LDO} = – 15 mA PSL11 = 20 log(acV_{LDO} / 0.3)	—	– 50	—	dB	*5
Ripple rejection ratio (2)	PSL12	V_{CC} = 3.6 V + 0.3 V[p-p] f = 10 kHz I_{LDO} = – 15 mA PSL12 = 20 log(acV_{LDO} / 0.3)	—	– 40	—	dB	*5
Short-circuit protection current	I_{PT1}	V_{LDO} = 0 V	—	40	—	mA	*5
I²C bus (Internal I/O stage characteristics)							
Hysteresis of Schmitt trigger input (1)	V_{hys1}	V_{DD} > 2 V, Hysteresis of SDA, SCL	0.05 × V_{DD}	—	—	V	*6 *7
Hysteresis of Schmitt trigger input (2)	V_{hys2}	V_{DD} < 2 V, Hysteresis of SDA, SCL	0.1 × V_{DD}	—	—	V	*6 *7
Output fall time from V_{IHmin} to V_{ILmax}	t_{of}	Bus capacitance: 10 pF to 550 pF $I_P \leq$ 20 mA (V_{OLmax} = 0.4 V) I_P : Max. sink current	—	—	120	ns	*6 *7
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	—	0	—	50	ns	*6 *7
Capacitance for each I/O pin	C_i	—	—	—	10	pF	*6 *7

Note: *4 : Constant current circuit, and Matrix SW turn off and IS reset when TSD operates.
*5 : Typical Design Value
*6 : The timing of Fast-mode Plus devices in I²C-bus is specified in page 11. All values referred to V_{IHmin} and V_{ILmax} level.
*7 : These are values checked by design but not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Bus line specifications) (Continue)							
Hold time (repeated) START condition	$t_{HD:STA}$	The first clock pulse is generated after $t_{HD:STA.}$	0.26	—	—	µs	*6 *7
Low period of the SCL clock	t_{LOW}	—	0.5	—	—	µs	*6 *7
High period of the SCL clock	t_{HIGH}	—	0.26	—	—	µs	*6 *7
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.26	—	—	µs	*6 *7
Data hold time	$t_{HD:DAT}$	—	0	—	—	µs	*6 *7
Data set-up time	$t_{SU:DAT}$	—	50	—	—	ns	*6 *7
Rise time of both SDA and SCL signals	t_r	—	—	—	120	ns	*6 *7
Fall time of both SDA and SCL signals	t_f	—	—	—	120	ns	*6 *7
Set-up time of STOP condition	$t_{SU:STO}$	—	0.26	—	—	µs	*6 *7
Bus free time between STOP and START condition	t_{BUF}	—	0.5	—	—	µs	*6 *7
Capacitive load for each bus line	C_b	—	—	—	550	pF	*6 *7
Data valid time	$t_{VD:DAT}$	—	—	—	0.45	µs	*6 *7
Data valid acknowledge	$t_{VD:ACK}$	—	—	—	0.45	µs	*6 *7
Noise margin at the Low-level for each connected device	V_{nL}	—	0.1 × V_{DD}	—	—	V	*6 *7
Noise margin at the High-level for each connected device	V_{nH}	—	0.2 × V_{DD}	—	—	V	*6 *7

Note: *6 : The timing of Fast-mode Plus devices in I²C-bus is specified in page 11. All values referred to V_{IHmin} and V_{ILmax} level.
*7 : These are values checked by design but not production tested.

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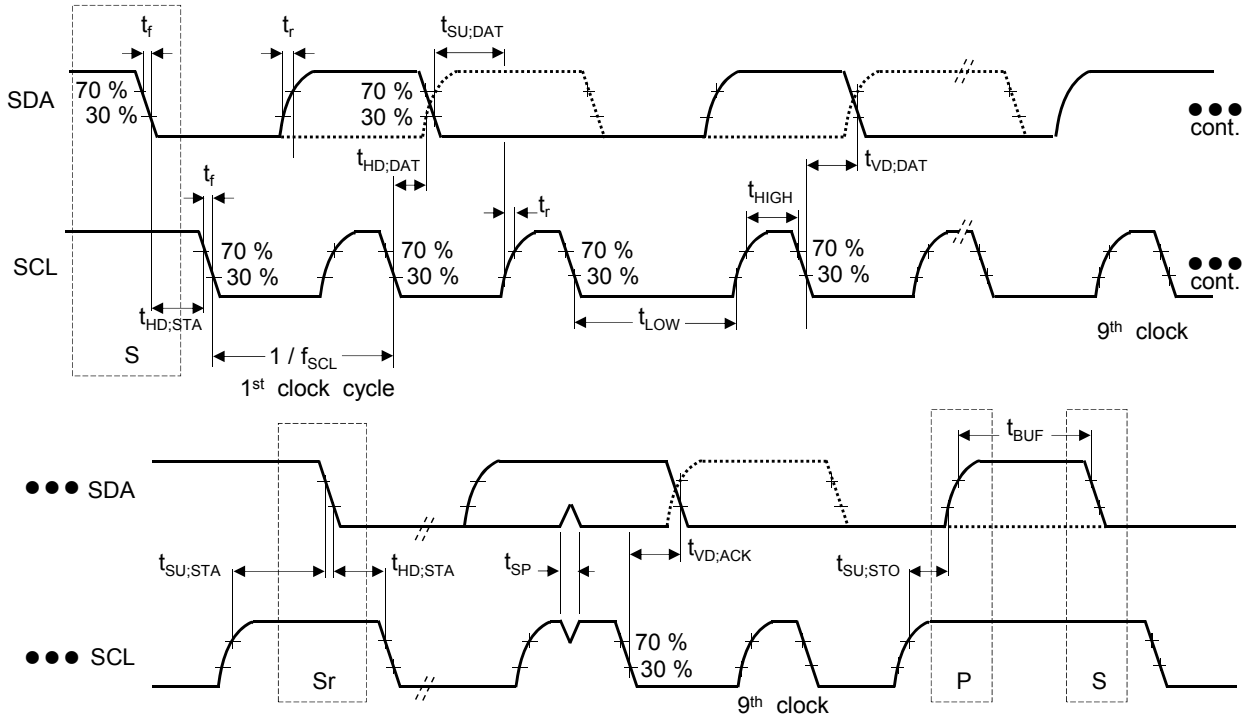
ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned



V_{VILMAX} = 0.3 × V_{DD}

V_{VIHMIN} = 0.7 × V_{DD}

S : START condition

Sr : Repeat START condition

P : STOP condition

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ELECTRICAL CHARACTERISTICS (continued)

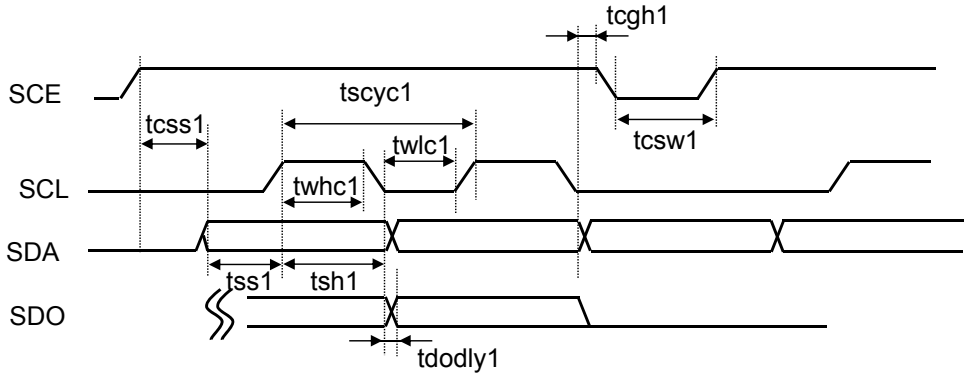
V_{CC} = 3.6 V, V_{DD} = 1.85 V

Note: Operating Ambient Temperature, T_a = 25 °C ± 2 °C, unless specifically mentioned

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI interface characteristics (V_{DD} = 1.85 V ± 3 %) Reception timing							
SCL cycle period	tscyc1	—	—	200	—	ns	*5
SCL cycle period High period	twhc1	—	—	100	—	ns	*5
SCL cycle period Low period	twlc1	—	—	100	—	ns	*5
Serial data setup time	tss1	—	—	142	—	ns	*5
Serial data hold time	tsh1	—	—	142	—	ns	*5
Transceiving interval	tcsw1	—	—	100	—	ns	*5
Chip enable setup time	tcss1	—	—	5	—	ns	*5
Chip enable hold time	tcgh1	—	—	5	—	ns	*5
SPI interface characteristics (V_{DD} = 1.85 V ± 3 %) Transmission timing							
SCL cycle period	tscyc1	—	—	200	—	ns	*5
SCL cycle period High period	twhc1	—	—	100	—	ns	*5
SCL cycle period Low period	twlc1	—	—	100	—	ns	*5
Serial data setup time	tss1	—	—	142	—	ns	*5
Serial data hold time	tsh1	—	—	142	—	ns	*5
Transceiving interval	tcsw1	—	—	100	—	ns	*5
Chip enable setup time	tcss1	—	—	5	—	ns	*5
Chip enable hold time	tcgh1	—	—	5	—	ns	*5
DC delay time	tdodly1	Read mode only	—	30	—	ns	*5

Note: *5 : Typical Design Value

Interface timing chart



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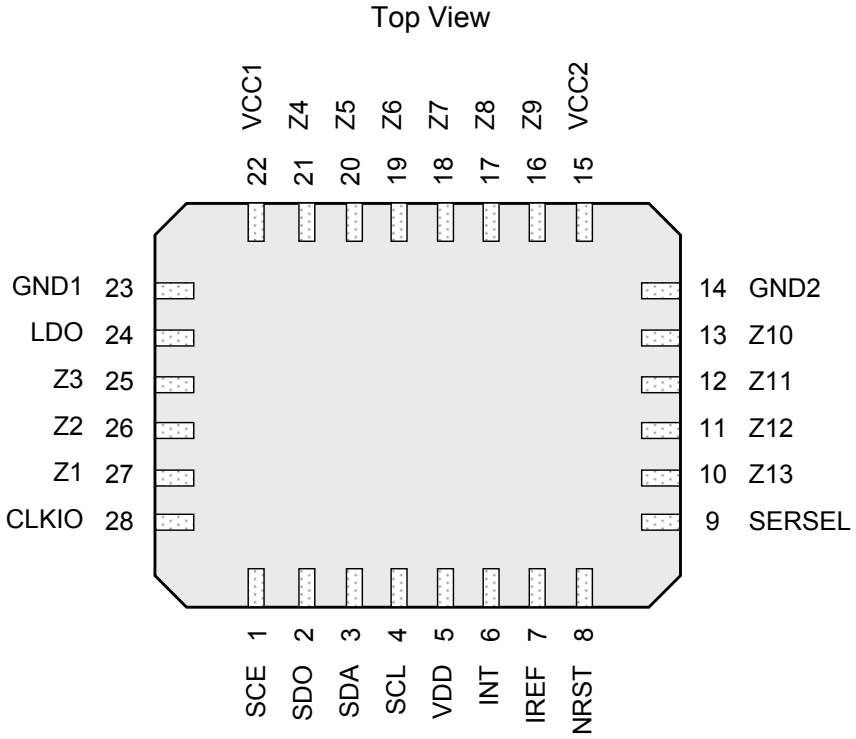
PIN CONFIGURATION



PIN FUNCTIONS

Pin No.	Pin name	Type	Description	Pin processing at unused
1	SCE	Input	Chip enable signal for SPI interface.	SERSEL = High Then GND or V_{CC}
			Slave address selection pin for I²C interface.	SERSEL = Low Then GND or V_{CC} or SCL or SDA
2	SDO	Output	Data output pin for SPI interface	Open
3	SDA	Input/Output	Data input / output pin for SPI or I²C interface	(Required pin)
4	SCL	Input	Clock input pin for SPI or I²C interface	(Required pin)
5	VDD	Power Supply	Power supply for SPI or I²C interface	(Required pin)
6	INT (*1)	Output	Interruption signal output pin / Open drain	Open
7	IREF	Output	Resistor connection pin for constant current setup	(Required pin)
8	NRST	Input	Reset input pin	(Required pin)
9	SERSEL	Input	Serial Interface selection pin / SPI or I²C interface	(Required pin)
10	Z13	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open

Note: *1 : INT pin must be pulled up to V_{DD} when it is in use.

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PIN FUNCTIONS (continued)

Pin No.	Pin name	Type	Description	Pin processing at unused
11	Z12	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
12	Z11	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
13	Z10	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
14 23	GND2 GND1	Ground	Ground pin	(Required pin)
15 22	VCC2 VCC1	Power Supply	Power supply for matrix driver, Internal reference circuit	Battery or External power supply
16	Z9	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
17	Z8	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
18	Z7	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
19	Z6	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
20	Z5	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
21	Z4	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
24	LDO	Output	LDO output pin	(Required pin)
25	Z3	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
26	Z2	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
27	Z1	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
28	CLKIO	Input/Output	Reference clock input/output, LED control input pin	Open

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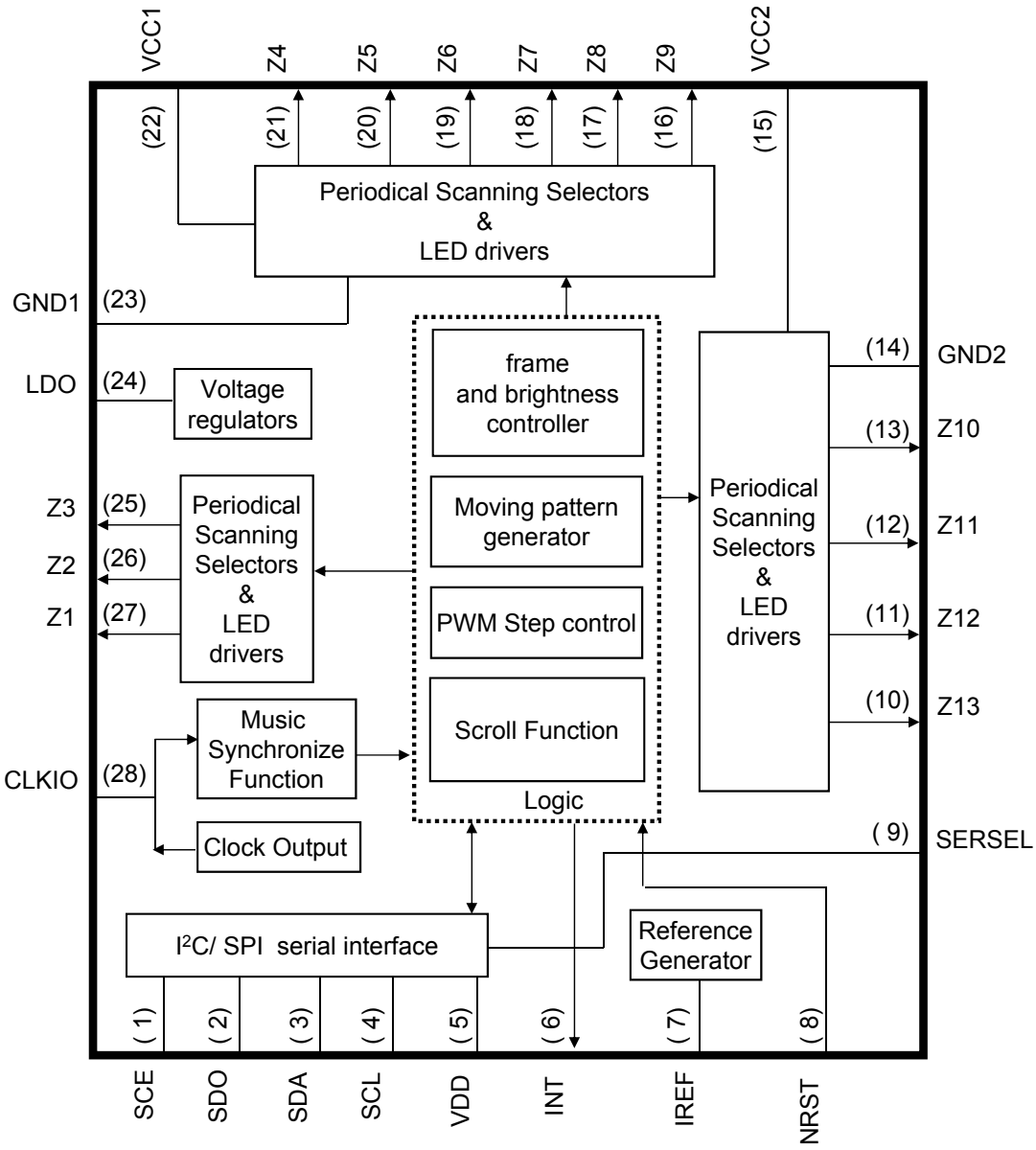
Revised : 2014-09-01

FUNCTIONAL BLOCK DIAGRAM



Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

Established : 2012-02-07
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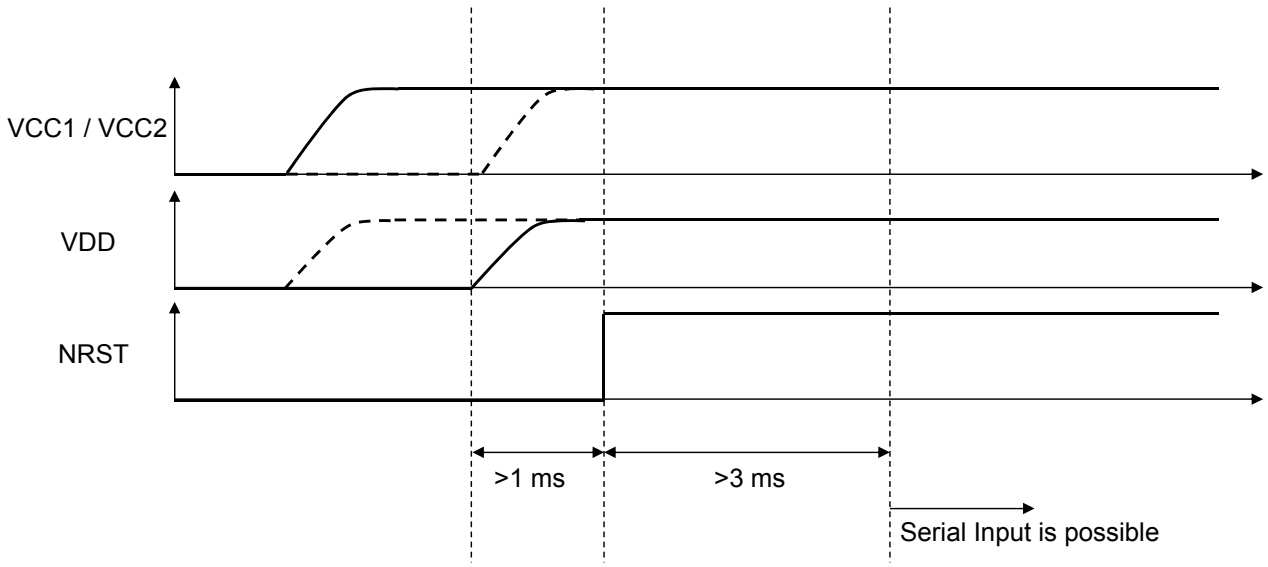
OPERATION

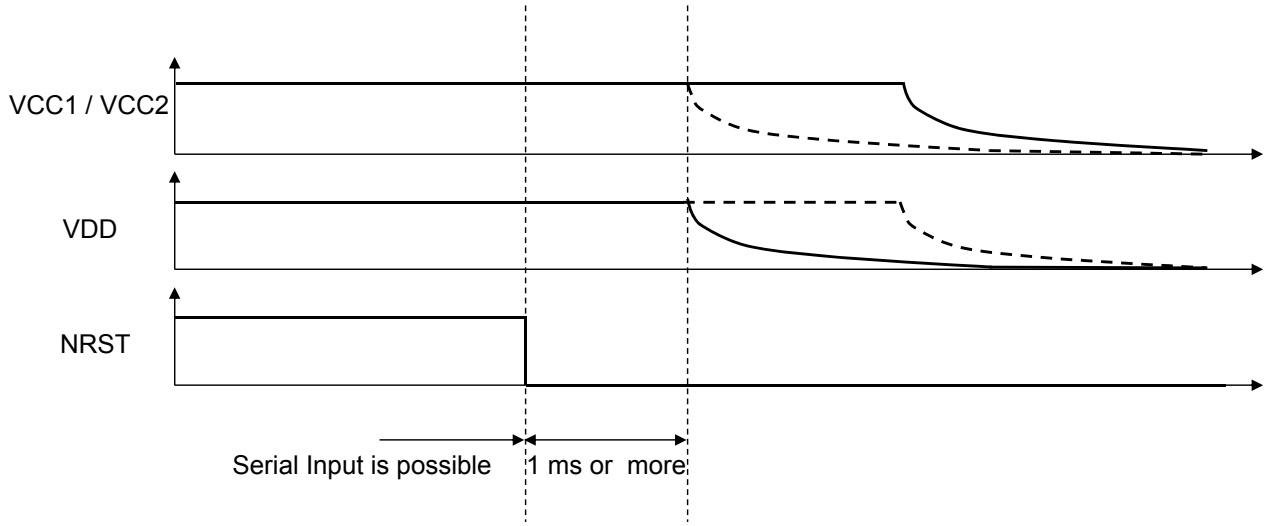
1. Power Supply Sequence

Power ON



Note: For the Startup Timing of VCC1 / VCC2 and VDD, it is possible to be changed.

Power OFF



Note: For the Shut down Timing of VCC1 / VCC2 and VDD, it is possible to be changed.

Established : 2012-02-07
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OPERATION (continued)

2. Register Map

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
00h	RST	00h	R/W	--	--	--	--	--	RAM2RST	RAM1RST	SRST
01h	reserved	--	--	--	--	--	--	--	--	--	--
02h	reserved	--	--	--	--	--	--	--	--	--	--
03h	CLKCTL	78h	R/W	IMAX[4:0]					OSCEN	CLKOUT	EXTCLK
04h	MTXON	00h	R/W	--	--	--	--	ZPDEN	MTXMODE[1:0]		MTXON
05h	FRMSEL	00h	R/W	--	--	--	--	--	--	--	FRMSEL
06h	MTXON1	00h	R/W	A8ON	A7ON	A6ON	A5ON	A4ON	A3ON	A2ON	A1ON
07h	MTXON2	00h	R/W	B4ON	B3ON	B2ON	B1ON	A12ON	A11ON	A10ON	A9ON
08h	MTXON3	00h	R/W	B12ON	B11ON	B10ON	B9ON	B8ON	B7ON	B6ON	B5ON
09h	MTXON4	00h	R/W	C8ON	C7ON	C6ON	C5ON	C4ON	C3ON	C2ON	C1ON
0Ah	MTXON5	00h	R/W	D4ON	D3ON	D2ON	D1ON	C12ON	C11ON	C10ON	C9ON
0Bh	MTXON6	00h	R/W	D12ON	D11ON	D10ON	D9ON	D8ON	D7ON	D6ON	D5ON
0Ch	MTXON7	00h	R/W	E8ON	E7ON	E6ON	E5ON	E4ON	E3ON	E2ON	E1ON
0Dh	MTXON8	00h	R/W	F4ON	F3ON	F2ON	F1ON	E12ON	E11ON	E10ON	E9ON
0Eh	MTXON9	00h	R/W	F12ON	F11ON	F10ON	F9ON	F8ON	F7ON	F6ON	F5ON
0Fh	MTXON10	00h	R/W	G8ON	G7ON	G6ON	G5ON	G4ON	G3ON	G2ON	G1ON
10h	MTXON11	00h	R/W	H4ON	H3ON	H2ON	H1ON	G12ON	G11ON	G10ON	G9ON
11h	MTXON12	00h	R/W	H12ON	H11ON	H10ON	H9ON	H8ON	H7ON	H6ON	H5ON
12h	MTXON13	00h	R/W	I8ON	I7ON	I6ON	I5ON	I4ON	I3ON	I2ON	I1ON
13h	MTXON14	00h	R/W	J4ON	J3ON	J2ON	J1ON	I12ON	I11ON	I10ON	I9ON
14h	MTXON15	00h	R/W	J12ON	J11ON	J10ON	J9ON	J8ON	J7ON	J6ON	J5ON
15h	MTXON16	00h	R/W	K8ON	K7ON	K6ON	K5ON	K4ON	K3ON	K2ON	K1ON
16h	MTXON17	00h	R/W	L4ON	L3ON	L2ON	L1ON	K12ON	K11ON	K10ON	K9ON
17h	MTXON18	00h	R/W	L12ON	L11ON	L10ON	L9ON	L8ON	L7ON	L6ON	L5ON
18h	THOLD	00h	R/W	THOLD[7:0]							
19h	MELODY	00h	R/W	--	MLDCOM[2:0]			GRP4	GRP3	GRP2	GRP1
1Ah	INTREG	00h	R/W	--	--	--	--	TSTEND	OPEN	SHORT	FRMINT
1Bh	INTMSK	0Fh	R/W	--	--	--	--	TSTMSK	OPMSK	SHMSK	FRMMSK
1Ch	DETECT	00h	W	--	--	--	--	--	--	--	DETECT
1Dh	LEDON	00h	R/W	FADTIM	LED7ON	LED6ON	LED5ON	LED4ON	LED3ON	LED2ON	LED1ON

Note: "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used.
For data bits indicated by "--" in other registers except from "reversed" registers, will return "zero" value if these bits are read. Writing to these bits will be ignored.

OPERATION (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
1Eh	PWM1CTL	00h	R/W	--	PWM1EN	LED1DT[5:0]					
1Fh	PWM2CTL	00h	R/W	--	PWM2EN	LED2DT[5:0]					
20h	PWM3CTL	00h	R/W	--	PWM3EN	LED3DT[5:0]					
21h	PWM4CTL	00h	R/W	--	PWM4EN	LED4DT[5:0]					
22h	PWM5CTL	00h	R/W	--	PWM5EN	LED5DT[5:0]					
23h	PWM6CTL	00h	R/W	--	PWM6EN	LED6DT[5:0]					
24h	PWM7CTL	00h	R/W	--	PWM7EN	LED7DT[5:0]					
25h	LED0	00h	R/W	SDTH[1:0]		SDTL[1:0]		BRT0[3:0]			
26h	LED1	00h	R/W	--	SDT1[2:0]			BRT1[3:0]			
27h	LED2	00h	R/W	--	SDT2[2:0]			BRT2[3:0]			
28h	LED3	00h	R/W	--	SDT3[2:0]			BRT3[3:0]			
29h	LED4	00h	R/W	--	SDT4[2:0]			BRT4[3:0]			
2Ah	LED5	00h	R/W	--	SDT5[2:0]			BRT5[3:0]			
2Bh	LED6	00h	R/W	--	SDT6[2:0]			BRT6[3:0]			
2Ch	LED7	00h	R/W	--	SDT7[2:0]			BRT7[3:0]			
2Dh	LEDSEL1	00h	R/W	--	A2SEL[2:0]			--	A1SEL[2:0]		
2Eh	LEDSEL2	00h	R/W	--	A4SEL[2:0]			--	A3SEL[2:0]		
2Fh	LEDSEL3	00h	R/W	--	A6SEL[2:0]			--	A5SEL[2:0]		
30h	LEDSEL4	00h	R/W	--	A8SEL[2:0]			--	A7SEL[2:0]		
31h	LEDSEL5	00h	R/W	--	A10SEL[2:0]			--	A9SEL[2:0]		
32h	LEDSEL6	00h	R/W	--	A12SEL[2:0]			--	A11SEL[2:0]		
33h	LEDSEL7	00h	R/W	--	B2SEL[2:0]			--	B1SEL[2:0]		
34h	LEDSEL8	00h	R/W	--	B4SEL[2:0]			--	B3SEL[2:0]		
35h	LEDSEL9	00h	R/W	--	B6SEL[2:0]			--	B5SEL[2:0]		
36h	LEDSEL10	00h	R/W	--	B8SEL[2:0]			--	B7SEL[2:0]		
37h	LEDSEL11	00h	R/W	--	B10SEL[2:0]			--	B9SEL[2:0]		
38h	LEDSEL12	00h	R/W	--	B12SEL[2:0]			--	B11SEL[2:0]		
39h	LEDSEL13	00h	R/W	--	C2SEL[2:0]			--	C1SEL[2:0]		
3Ah	LEDSEL14	00h	R/W	--	C4SEL[2:0]			--	C3SEL[2:0]		
3Bh	LEDSEL15	00h	R/W	--	C6SEL[2:0]			--	C5SEL[2:0]		
3Ch	LEDSEL16	00h	R/W	--	C8SEL[2:0]			--	C7SEL[2:0]		
3Dh	LEDSEL17	00h	R/W	--	C10SEL[2:0]			--	C9SEL[2:0]		
3Eh	LEDSEL18	00h	R/W	--	C12SEL[2:0]			--	C11SEL[2:0]		
3Fh	LEDSEL19	00h	R/W	--	D2SEL[2:0]			--	D1SEL[2:0]		

Note: Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
Writing to these bits will be ignored.

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OPERATION (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
40h	LEDSEL20	00h	R/W	--	D4SEL[2:0]			--	D3SEL[2:0]		
41h	LEDSEL21	00h	R/W	--	D6SEL[2:0]			--	D5SEL[2:0]		
42h	LEDSEL22	00h	R/W	--	D8SEL[2:0]			--	D7SEL[2:0]		
43h	LEDSEL23	00h	R/W	--	D10SEL[2:0]			--	D9SEL[2:0]		
44h	LEDSEL24	00h	R/W	--	D12SEL[2:0]			--	D11SEL[2:0]		
45h	LEDSEL25	00h	R/W	--	E2SEL[2:0]			--	E1SEL[2:0]		
46h	LEDSEL26	00h	R/W	--	E4SEL[2:0]			--	E3SEL[2:0]		
47h	LEDSEL27	00h	R/W	--	E6SEL[2:0]			--	E5SEL[2:0]		
48h	LEDSEL28	00h	R/W	--	E8SEL[2:0]			--	E7SEL[2:0]		
49h	LEDSEL29	00h	R/W	--	E10SEL[2:0]			--	E9SEL[2:0]		
4Ah	LEDSEL30	00h	R/W	--	E12SEL[2:0]			--	E11SEL[2:0]		
4Bh	LEDSEL31	00h	R/W	--	F2SEL[2:0]			--	F1SEL[2:0]		
4Ch	LEDSEL32	00h	R/W	--	F4SEL[2:0]			--	F3SEL[2:0]		
4Dh	LEDSEL33	00h	R/W	--	F6SEL[2:0]			--	F5SEL[2:0]		
4Eh	LEDSEL34	00h	R/W	--	F8SEL[2:0]			--	F7SEL[2:0]		
4Fh	LEDSEL35	00h	R/W	--	F10SEL[2:0]			--	F9SEL[2:0]		
50h	LEDSEL36	00h	R/W	--	F12SEL[2:0]			--	F11SEL[2:0]		
51h	LEDSEL37	00h	R/W	--	G2SEL[2:0]			--	G1SEL[2:0]		
52h	LEDSEL38	00h	R/W	--	G4SEL[2:0]			--	G3SEL[2:0]		
53h	LEDSEL39	00h	R/W	--	G6SEL[2:0]			--	G5SEL[2:0]		
54h	LEDSEL40	00h	R/W	--	G8SEL[2:0]			--	G7SEL[2:0]		
55h	LEDSEL41	00h	R/W	--	G10SEL[2:0]			--	G9SEL[2:0]		
56h	LEDSEL42	00h	R/W	--	G12SEL[2:0]			--	G11SEL[2:0]		
57h	LEDSEL43	00h	R/W	--	H2SEL[2:0]			--	H1SEL[2:0]		
58h	LEDSEL44	00h	R/W	--	H4SEL[2:0]			--	H3SEL[2:0]		
59h	LEDSEL45	00h	R/W	--	H6SEL[2:0]			--	H5SEL[2:0]		
5Ah	LEDSEL46	00h	R/W	--	H8SEL[2:0]			--	H7SEL[2:0]		
5Bh	LEDSEL47	00h	R/W	--	H10SEL[2:0]			--	H9SEL[2:0]		
5Ch	LEDSEL48	00h	R/W	--	H12SEL[2:0]			--	H11SEL[2:0]		
5Dh	LEDSEL49	00h	R/W	--	I2SEL[2:0]			--	I1SEL[2:0]		
5Eh	LEDSEL50	00h	R/W	--	I4SEL[2:0]			--	I3SEL[2:0]		
5Fh	LEDSEL51	00h	R/W	--	I6SEL[2:0]			--	I5SEL[2:0]		

Note: Data bits indicated by "--" cannot be accessed. It will return "zero" value if these bits are read.
Writing to these bits will be ignored.

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OPERATION (continued)

2. Register Map (continued)

ADDR	Register Name	Default	R/W	DATA							
				D7	D6	D5	D4	D3	D2	D1	D0
60h	LEDSEL52	00h	R/W	--	I8SEL[2:0]			--	I7SEL[2:0]		
61h	LEDSEL53	00h	R/W	--	I10SEL[2:0]			--	I9SEL[2:0]		
62h	LEDSEL54	00h	R/W	--	I12SEL[2:0]			--	I11SEL[2:0]		
63h	LEDSEL55	00h	R/W	--	J2SEL[2:0]			--	J1SEL[2:0]		
64h	LEDSEL56	00h	R/W	--	J4SEL[2:0]			--	J3SEL[2:0]		
65h	LEDSEL57	00h	R/W	--	J6SEL[2:0]			--	J5SEL[2:0]		
66h	LEDSEL58	00h	R/W	--	J8SEL[2:0]			--	J7SEL[2:0]		
67h	LEDSEL59	00h	R/W	--	J10SEL[2:0]			--	J9SEL[2:0]		
68h	LEDSEL60	00h	R/W	--	J12SEL[2:0]			--	J11SEL[2:0]		
69h	LEDSEL61	00h	R/W	--	K2SEL[2:0]			--	K1SEL[2:0]		
6Ah	LEDSEL62	00h	R/W	--	K4SEL[2:0]			--	K3SEL[2:0]		
6Bh	LEDSEL63	00h	R/W	--	K6SEL[2:0]			--	K5SEL[2:0]		
6Ch	LEDSEL64	00h	R/W	--	K8SEL[2:0]			--	K7SEL[2:0]		
6Dh	LEDSEL65	00h	R/W	--	K10SEL[2:0]			--	K9SEL[2:0]		
6Eh	LEDSEL66	00h	R/W	--	K12SEL[2:0]			--	K11SEL[2:0]		
6Fh	LEDSEL67	00h	R/W	--	L2SEL[2:0]			--	L1SEL[2:0]		
70h	LEDSEL68	00h	R/W	--	L4SEL[2:0]			--	L3SEL[2:0]		
71h	LEDSEL69	00h	R/W	--	L6SEL[2:0]			--	L5SEL[2:0]		
72h	LEDSEL70	00h	R/W	--	L8SEL[2:0]			--	L7SEL[2:0]		
73h	LEDSEL71	00h	R/W	--	L10SEL[2:0]			--	L9SEL[2:0]		
74h	LEDSEL72	00h	R/W	--	L12SEL[2:0]			--	L11SEL[2:0]		
75h	SCROLL1	00h	R/W	--	E_STOP	D_STOP	C_STOP	B_STOP	A_STOP	UP	LEFT
76h	SCROLL2	00h	R/W	--	--	--	--	--	SCLTIME[2:0]		
77h	XCONST1	00h	R/W	X8CONST	X7CONST	X6CONST	X5CONST	X4CONST	X3CONST	X2CONST	X1CONST
78h	XCONST2	00h	R/W	--	--	--	X13 CONST	X12 CONST	X11 CONST	X10 CONST	X9 CONST
79h	YMSK1	00h	R/W	Y8MSK	Y7MSK	Y6MSK	Y5MSK	Y4MSK	Y3MSK	Y2MSK	Y1MSK
7Ah	YMSK2	00h	R/W	--	--	--	YMSKVAL	Y12MSK	Y11MSK	Y10MSK	Y9MSK
7Bh	reserved	--	--	--	--	--	--	--	--	--	--
7Ch	reserved	--	--	--	--	--	--	--	--	--	--
7Dh	reserved	--	--	--	--	--	--	--	--	--	--
7Eh	SCANSET	0Bh	R/W	--	--	--	--	SCANSET[3:0]			
7Fh	reserved	--	--	--	--	--	--	--	--	--	--

Note) "Reserved" registers and data bits indicated by "--" cannot be accessed. "Reserved" registers are not used.
For data bits indicated by "--" in other registers except from "reversed" registers, will return "zero" value if these bits are read.
Writing to these bits will be ignored.

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OPERATION (continued)

3. Register map Detailed Explanation

Register Name		RST							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
00h	W	--	--	--	--	--	RAM2RST	RAM1RST	SRST
Default	00h	0	0	0	0	0	0	0	0

D2 : RAM2RST Frame 2 reset control
[0] : No operation (default)
[1] : Frame 2 data is cleared

D1 : RAM1RST Frame 1 reset control
[0] : No operation (default)
[1] : Frame1 data is reset

D0 : SRST Soft reset control
[0] : No operation (default)
[1] : System reset

• This register will auto-return to [0] when written with [1] logic value.

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		CLKCTL							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
03h	R/W	IMAX[4:0]					OSCEN	CLKOUT	EXTCLK
Default	78h	0	1	1	1	1	0	0	0

D7 : IMAX Maximum current selection
[0] : 30 mA (default)
[1] : 60 mA

D6-3 : IMAX Maximum current setup selection
[0000] : 0 mA / 0 mA
[0001] : 2 mA / 4 mA
.....
[1110] : 28 mA / 56 mA
[1111] : 30 mA (Default) / 60 mA

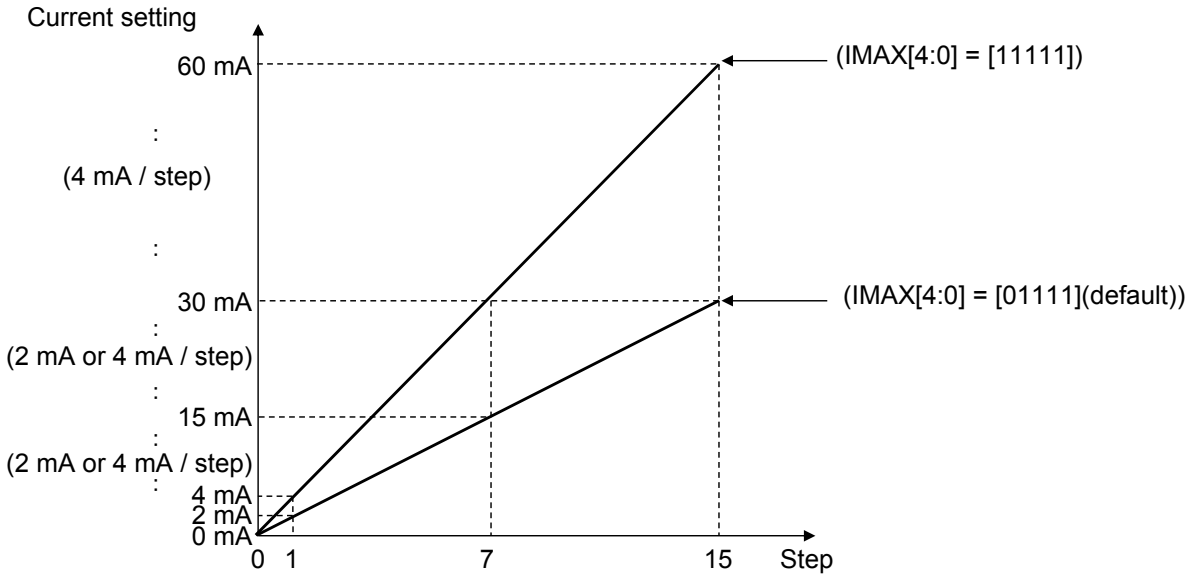
D2 : OSCEN Internal oscillator ON / OFF control
[0] : Internal oscillator OFF (default)
[1] : Internal oscillator ON

• Oscillator will auto turn ON if any of the LED drivers are enabled (MTXON = [1]) even if this bit is [0].

D1 : CLKOUT Internal clock output enable
[0] : Internal clock is not output from CLKIO (default)
[1] : Internal clock is output from CLKIO

D0 : EXTCLK Internal / external clock select
[0] : 2.4 MHz Internal clock is used in operation (default)
[1] : External clock is used in operation

• Please do not set MTXMODE = [10] (Melody Mode), EXTCLK = [1] and CLKOUT = [1] at the same time. In such case, the priority of operation will be EXTCLK then CLKOUT and then Melody Mode will have the least priority.



Established : 2012-02-07
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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MTXON							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
04h	R/W	--	--	--	--	ZPDEN	MTXMODE[1:0]		MTXON
Default	00h	0	0	0	0	0	0	0	0

D3 : ZPDEN Ghost image prevention function enable
[0] : Turn off ghost image prevention (default)
[1] : Turn on ghost image prevention

D2-1 : MTXMODE Matrix mode of operation select
[00] : Display Matrix frame 1 character (default)
[01] : Display Matrix frame 2 character
[10] : Melody Mode
[11] : Scroll Mode

D0 : MTXON Matrix ON / OFF setting
[0] : OFF (default)
[1] : ON

- Ghost Image Prevention may not remove the ghost image perfectly. It depends on the LED color combination and LED connection method. Please refer to Page.59 for details.
- Please refer to Page.60 for details especially when this IC is used for RGB driver.

Register Name		FRMSEL							
Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
05h	R/W	--	--	--	--	--	--	--	FRMSEL
Default	00h	0	0	0	0	0	0	0	0

D0 : FRMSEL

(1) Normal Modes :
[0] : Matrix Frame 1 is selected for character write (default).
[1] : Matrix Frame 2 is selected for character write.

(2) Melody Mode :
[0] : Matrix Frame 1 is selected for character write (default).
[1] : Matrix Frame 2 is selected for melody enable for each LED.

- During scroll mode, FRMSEL need not be set. Frame to be written is automatically selected whichever is free.

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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		MTXON1							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
06h	W	A8ON	A7ON	A6ON	A5ON	A4ON	A3ON	A2ON	A1ON
Default	00h	0	0	0	0	0	0	0	0

D7 : A8ON

(1) Normal Mode : LED A8 of Matrix ON / OFF control
[0] : OFF (default)
[1] : ON

(2) Melody Mode & FRMSEL = [1] : LED A8 of Matrix Melody Mode ON / OFF control
[0] : LED A8 Melody Mode OFF (default)
[1] : LED A8 Melody Mode ON

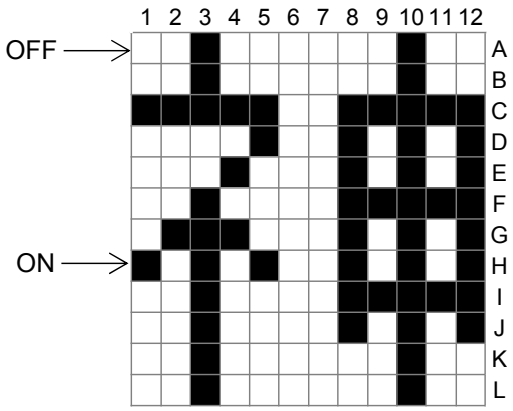
...

D0 : A1ON

(1) Normal Mode : LED A1 of Matrix ON / OFF control
[0] : OFF (default)
[1] : ON

(2) Melody Mode & FRMSEL = [1] : LED A1 of Matrix Melody Mode ON / OFF control
[0] : LED A1 Melody Mode OFF (default)
[1] : LED A1 Melody Mode ON

- The definition for register addresses 07h to 17h is the same as address 06h.
- Collectively, these register addresses are used to create frame character (*see figure*).
- If FRMSEL = [0], the data written to these group of registers will be for Matrix frame 1 character.
- If FRMSEL = [1], the data written to these group of registers will be for Matrix frame 2 character.
- During Melody Mode, the data written on these group of registers when FRMSEL = [1] will be designated as melody enable for each LED in matrix. The character to be display is determined by the data written when FRMSEL = [0].



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OPERATION (continued)

3. Register map Detailed Explanation (continued)

Register Name		THOLD							
Address	**R/W**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18h	R/W	THOLD[7:0]							
Default	00h	0	0	0	0	0	0	0	0

D7 : THOLD[7] Threshold 8 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 8 is used. (Threshold 8 is about 1.93 V)

D6 : THOLD[6] Threshold 7 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 7 is used. (Threshold 7 is about 1.80 V)

D5 : THOLD[5] Threshold 6 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 6 is used. (Threshold 6 is about 1.67 V)

D4 : THOLD[4] Threshold 5 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 5 is used. (Threshold 5 is about 1.55 V)

D3 : THOLD[3] Threshold 4 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 4 is used. (Threshold 4 is about 1.42 V)

D2 : THOLD[2] Threshold 3 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 3 is used. (Threshold 3 is about 1.30 V)

D1 : THOLD[1] Threshold 2 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 2 is used. (Threshold 2 is about 1.17 V)

D0 : THOLD[0] Threshold 1 is used as voltage detection.
[0] : Others (default)
[1] : Threshold 1 is used. (Threshold 1 is about 1.04 V)

- When all bits are set [0], threshold is in auto-detection mode (default)
- Do not set more than 1 register bit to logic [1] value at the same time.
- If 2 bits are set to [1] at the same time, system will only recognize the first [1] bit threshold that is set.