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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Panasonic

AN44067A

37V/2.5A Microstepping Motor Driver

FEATURES

- Built-in decoder for micro steps

  (2 phase excitation, half-step, 1-2 phase excitation, W1-2 phase excitation and 2W1-2 phase excitation)

  Stepping motor can be driven by only external clock signal.
- PMW can be driven by built-in CR (3-value can be selected during PWM OFF period.)

  Selection during PWM OFF period enables the best PWM drive.
- Mix Decay compatible (4-value for Fast Decay ratio can be selected.)

  Mix Decay control can improve accuracy of motor current wave form.
- Built -in low voltage detection

  If supply voltage lowers less than the range of operating supply voltage, low voltage detection operates and all phases of motor drive output are turned OFF.
- Built-in thermal protection

  If chip junction temperature rises and reaches setup temperature, all phases of motor drive output are turned OFF.
- 1 power supply with built-in 5 V power supply (accuracy ±5%)

  Motor can be driven by only 1 power supply because of built-in 5 V power supply.
- Built-in standby function

  Operation of standby function can lower current consumption of LSI.
- Built-in Home Position function

  Home Position function can detect the position of a motor.
- 34 pin Plastic Small Outline Package With Heat Sink (SOP Type)

DESCRIPTION

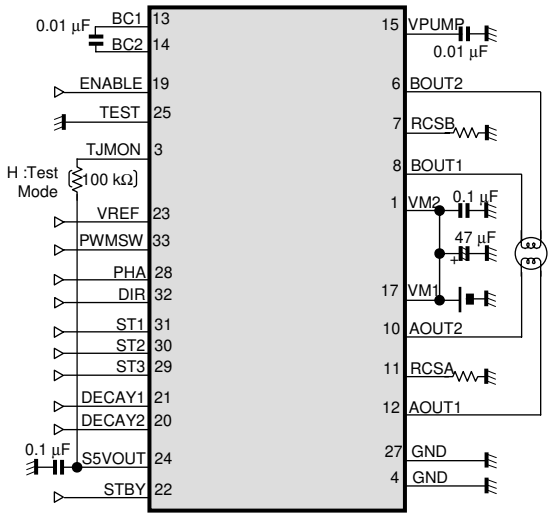
AN44067A is a two channel H-bridge driver LSI. Bipolar stepping motor can be controlled by a single driver LSI.

2 phase excitation, half- step, 1-2 phase excitation, W1-2 phase excitation and 2W1-2 phase excitation can be selected.

APPLICATIONS

- LSI for stepping motor drives

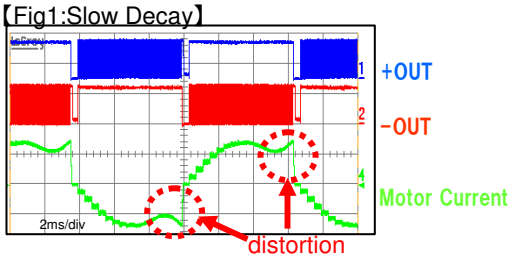
SIMPLIFIED APPLICATION



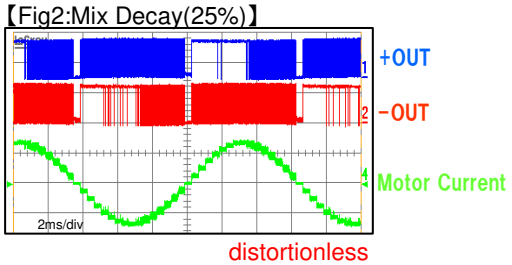
Notes)
This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

Mix Decay effect for Motor current

【Fig1:Slow Decay】



【Fig2:Mix Decay(25%)】



Condition:
excitation mode :2W1-2 phase drive
fig1 DECAY1=L DECAY2=L
fig2 DECAY1=L DECAY2=H

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_M	37	V	*1
Power dissipation	P_D	0.466	W	*2
Operating ambient temperature	T_{opr}	–20 to +70	°C	*3
Operating junction temperature	T_j	–20 to +150	°C	*3
Storage temperature	T_{stg}	–55 to +150	°C	*3
Output pin voltage (Pin 6, 8, 10, 12)	V_{OUT}	37	V	*4
Motor drive current (Pin 6, 8, 10, 12)	I_{OUT}	±2.5	A	*5,*6
Flywheel diode current (Pin 6, 8, 10, 12)	I_f	2.5	A	*5,*6
Input Voltage Range	V_{RCSA},V_{RCSB}	2.5	V	—
	V_{BC2}	(VM-1) to 43	V	*7
	V_{VPUMP}	(VM-2) to 43	V	*7
	V_{ENABLE}	-0.3 to 6	V	—
	V_{DECAY1},V_{DECAY2}	-0.3 to 6	V	—
	V_{STBY}	-0.3 to 6	V	—
	V_{VREF}	-0.3 to 6	V	—
	V_{TEST}	-0.3 to 6	V	—
	V_{PHA}	-0.3 to 6	V	—
	V_{ST1},V_{ST2},V_{ST3}	-0.3 to 6	V	—
	V_{DIR}	-0.3 to 6	V	—
	V_{PWMSW}	-0.3 to 6	V	—
	I_{TJMON}	1	mA	*8
	I_{S5VOUT}	-7 to 0	mA	—
ESD	HBM (Human Body Model)	± 2	kV	—
	CDM (Charge Device Model)	± 1	kV	—

Notes). This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at Ta = 70° C for the independent (unmounted) LSI package without a heat sink. When using this LSI, refer to the PD-Ta diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25° C.

*4 : This is output voltage rating and do not apply input voltage from outside to these pins. Set not to exceed allowable range at any time.

*5 : Do not apply external currents to any pin specially mentioned. For circuit currents, (+) denotes current flowing into the LSI and (–) denotes current flowing out of the LSI.

*6 : Rating when cooling fin on the back side of the LSI is connected to the GND pattern of the glass epoxy 4-layer board. (GND area : 2nd-layer or 3rd-layer : more than 1500 mm²) In case of no cooling fin on the back side of the LSI, rating current is 1.5 A on the glass epoxy 2-layer board.

*7 : These are pins not applied voltage from outside. Set so that the rating must not be exceeded transiently.

*8 : In case of TEST = High-level input, TJMON voltage is only Low-level.

POWER DISSIPATION RATING

Condition	θ_{JA}	PD (Ta=25 °C)	PD (Ta=70 °C)
Mount on PWB *1	86.0 °C/W	1453mW	930mW
Without PWB	171.6 °C/W	728mW	466mW

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, supply voltage, load and ambient temperature conditions to ensure that there is enough margin follow the power and the thermal design does not exceed the allowable value.

*1: Glass-Epoxy: 50×50×0.8 (mm) , heat dissipation fin: Dai-pad , the state where it does not mount.

CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VM1,VM2	10	24	34	V	*1
Input Voltage Range	V_{ENABLE}	0	-	5.5	V	—
	V_{DECAY1},V_{DECAY2}	0	-	5.5	V	—
	V_{STBY}	0	-	5.5	V	—
	V_{VREF}	0	-	5	V	—
	V_{TEST}	0	-	5.5	V	—
	V_{PHA}	0	-	5.5	V	—
	V_{ST1},V_{ST2},V_{ST3}	0	-	5.5	V	—
	V_{DIR}	0	-	5.5	V	—
	V_{PWMSW}	0	-	5.5	V	—
External Constants	C_{BC}	-	0.01	-	µF	—
	C_{VPUMP}	-	0.01	-	µF	—
	C_{S5VOUT}	-	0.1	-	µF	—
Operating ambient temperature	Ta^{opr}	-20	-	70	°C	—
Operating junction temperature	Tj^{opr}	-	-	120	°C	—

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

ELECRTRICAL CHARACTERISTICS

VM=24V, T_a = 25°C±2°C unless otherwise noted.

*1 : Typical Value checked by design.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Output Drivers							
High-level output saturation voltage	V_{OH}	I = –1.2 A	V_M – 0.75	V_M – 0.42	—	V	—
Low-level output saturation voltage	V_{OL}	I = 1.2 A	—	0.54	0.825	V	—
Flywheel diode forward voltage	V_{DI}	I = 1.2 A	0.5	1.0	1.5	V	—
Output leakage current	I_{LEAK}	V_M = 37 V, V_{RCS} = 0 V	—	10	20	µA	—
Supply current (Active)	I_M	ENABLE = High, STBY = High	—	5.5	10	mA	—
Supply current (STBY)	I_{MSTBY}	STBY = Low	—	25	50	µA	—
Output slew rate 1	VT_r	Output voltage rise	—	220	—	V/µs	*1
Output slew rate 2	VT_f	Output voltage fall	—	200	—	V/µs	*1
Dead time	T_D	—	—	0.8	—	µs	*1
I/O Block							
High-level STBY input voltage	V_{STBYH}	—	2.1	—	5.5	V	—
Low-level STBY input voltage	V_{STBYL}	—	0	—	0.6	V	—
High-level STBY input current	I_{STBYH}	STBY = 5 V	25	50	100	µA	—
Low-level STBY input current	I_{STBYL}	STBY = 0 V	–2	—	2	µA	—
High-level PHA input voltage	V_{PHAH}	—	2.1	—	5.5	V	—
Low-level PHA input voltage	V_{PHAL}	—	0	—	0.6	V	—
High-level PHA input current	I_{PHAH}	PHA = 5 V	25	50	100	µA	—
Low-level PHA input current	I_{PHAL}	PHA = 0 V	–2	—	2	µA	—
Highest-level PHA input frequency	f_{PHA}	—	—	—	100	kHz	—
High-level ENABLE input voltage	$V_{ENABLEH}$	—	2.1	—	5.5	V	—
Low-level ENABLE input voltage	$V_{ENABLEL}$	—	0	—	0.6	V	—
High-level ENABLE input current	$I_{ENABLEH}$	ENABLE = 5 V	25	50	100	µA	—
Low-level ENABLE input current	$I_{ENABLEL}$	ENABLE = 0 V	–2	—	2	µA	—
High-level PWMSW input voltage	V_{PWMSWH}	—	2.3	—	5.5	V	—
Middle-level PWMSW input voltage	V_{PWMSWM}	—	1.3	—	1.7	V	—
Low-level PWMSW input voltage	V_{PWMSWL}	—	0	—	0.6	V	—
High-level PWMSW input current	I_{PWMSWH}	PWMSW = 5 V	40	83	150	µA	—
Low-level PWMSW input current	I_{PWMSWL}	PWMSW = 0 V	–70	–36	–18	µA	—

ELECRTRICAL CHARACTERISTICS (continued)

VM=24V, T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I/O Block (Continued)							
PWMSW voltage at open	V_{PWMSWO}	—	1.3	1.5	1.7	V	—
High-level DECAY input voltage	V_{DECAYH}	—	2.1	—	5.5	V	—
Low-level DECAY input voltage	V_{DECAYL}	—	0	—	0.6	V	—
High-level DECAY input current	I_{DECAYH}	DECAY1 = DECAY2 = 5 V	25	50	100	µA	—
Low-level DECAY input current	I_{DECAYL}	DECAY1 = DECAY2 = 0 V	–2	—	2	µA	—
High-level DIR input voltage	V_{DIRH}	—	2.1	—	5.5	V	—
Low-level DIR input voltage	V_{DIRL}	—	0	—	0.6	V	—
High-level DIR input current	I_{DIRH}	DIR = 5 V	25	50	100	µA	—
Low-level DIR input current	I_{DIRL}	DIR = 0 V	–2	—	2	µA	—
High-level ST input voltage	V_{STH}	—	2.1	—	5.5	V	—
Low-level ST input voltage	V_{STL}	—	0	—	0.6	V	—
High-level ST input current	I_{STH}	ST1 = ST2 = ST3 = 5 V	25	50	100	µA	—
Low-level ST input current	I_{STL}	ST1 = ST2 = ST3 = 0 V	–2	—	2	µA	—
High-level TEST input voltage	V_{TESTH}	—	4.0	—	5.5	V	—
Middle-level TEST input voltage	V_{TESTM}	—	2.3	—	2.7	V	—
Low-level Test input voltage	V_{TESTL}	—	0	—	0.6	V	—
High-level TEST input current	I_{TESTH}	TEST = 5 V	25	50	100	µA	—
Low-level TEST input current	I_{TESTL}	TEST = 0 V	–2	—	2	µA	—
Torque Control Block							
Input bias current 1	I_{REFH}	V_{REF} = 5 V	–15	—	5	µA	—
Input bias current 2	I_{REFL}	V_{REF} = 0 V	–2	—	2	µA	—
PWM OFF time 1	T_{OFF1}	PWMSW = Low	16.8	28	39.2	µs	—
PWM OFF time 2	T_{OFF2}	PWMSW = Middle	9.1	15.2	21.3	µs	—
PWM OFF time 3	T_{OFF3}	PWMSW = High	4.9	8.1	11.3	µs	—
Pulse blanking time	T_B	V_{REF} = 0 V	0.4	0.7	1.0	µs	—
Comp threshold	VT_{CMP}	V_{REF} = 5 V	475	500	525	mV	—
Reference Voltage Block							
Reference voltage	V_{S5VOUT}	I_{S5VOUT} = 0 mA	4.75	5.0	5.25	V	—
Output impedance	Z_{S5VOUT}	I_{S5VOUT} = –7 mA	—	—	10	Ω	—

ELECRTRICAL CHARACTERISTICS (continued)

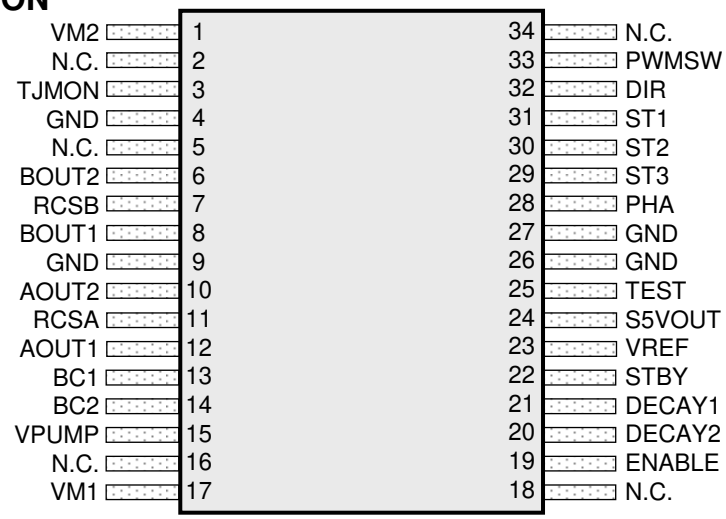
VM=24V, T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Home Position Block							
At TEST High-level input TJMON output Low-level voltage	V_{TJL}	Pull up TJMON pin to 5 V with 100 kΩ.	—	0.1	0.3	V	—
At TEST High-level input TJMON output leakage current	$I_{TJ(leak)}$	V_{TJMON} = 5 V	—	—	5	µA	—
Thermal Protection							
Thermal protection operating temperature	TSD_{on}	—	—	150	—	°C	*1
Thermal protection hysteresis width	ΔTSD	—	—	40	—	°C	*1
Low voltage Protection							
Protection operating voltage	V_{UVLO1}	—	—	7.9	—	V	*1
Protection releasing voltage	V_{UVLO2}	—	—	8.7	—	V	*1

*1 : Typical Value checked by design.

PIN CONFIGURATION

Top View

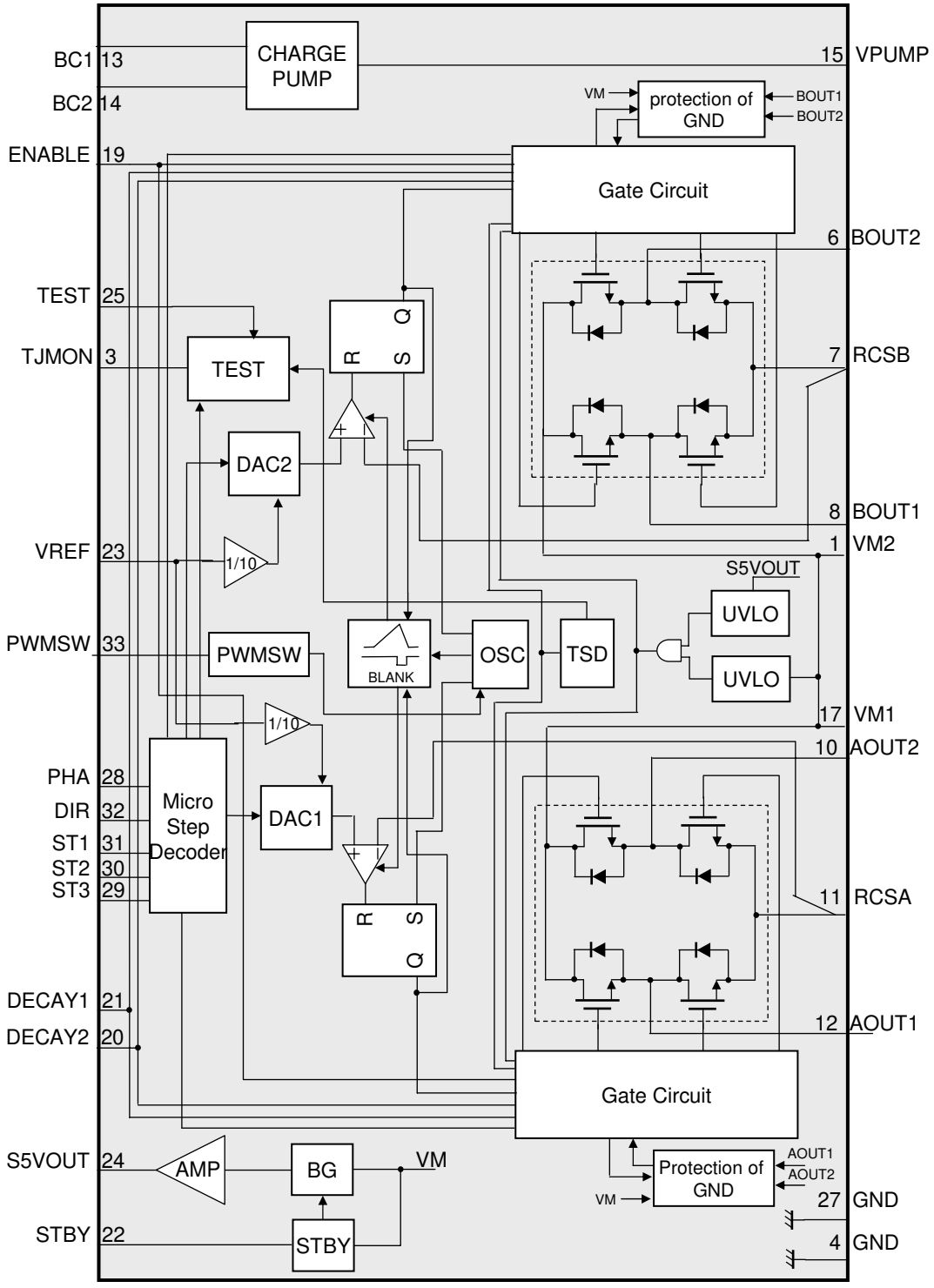


PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	VM2	Power supply	Motor power supply 2
2, 5, 16,18,34	N.C.	—	No Connection
3	TJMON	Output	VBE monitor / Test output / Home Position output
4, 9, 26, 27	GND	Ground	ground
6	BOUT2	Output	Phase B motor drive output 2
7	RCSB	Input / Output	Phase B current detection
8	BOUT1	Output	Phase B motor drive output 1
10	AOUT2	Output	Phase A motor drive output 2
11	RCSA	Input / Output	Phase A current detection
12	AOUT1	Output	Phase A motor drive output 1
13	BC1	Output	Charge pump capacitor connection 1
14	BC2	Output	Charge pump capacitor connection 2
15	VPUMP	Output	Charge pump circuit output
17	VM1	Power supply	Motor power supply 1
19	ENABLE	Input	Enable / disable CTL
20	DECAY2	Input	Mix Decay setup 2
21	DECAY1	Input	Mix Decay setup 1
22	STBY	Input	Standby
23	VREF	Input	Torque reference voltage input
24	S5VOUT	Output	Internal reference voltage (output 5 V)
25	TEST	Input	Test mode
28	PHA	Input	Clock input
29	ST3	Input	Step select 3
30	ST2	Input	Step select 2
31	ST1	Input	Step select 1
32	DIR	Input	Rotation direction
33	PWMSW	Input	PWM OFF period selection input

Note) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

FUNCTIONAL BLOCK DIAGRAM



Note) This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

1. Control mode

1) Truth table (Step select)

ENABLE	DIR	ST1	ST2	ST3	Output excitation mode (Phase B 90° delay : to Phase A)
High	—	—	—	—	Output OFF
Low	Low	Low	Low	Low	2 phase excitation drive (4-step sequence)
Low	Low	Low	High	Low	Half-step drive (8-step sequence)
Low	Low	High	Low	Low	1-2 phase excitation drive (8-step sequence)
Low	Low	High	High	Low	W1-2 phase excitation drive (16-step sequence)
Low	Low	—	—	High	2W1-2 phase excitation drive (32-step sequence)

ENABLE	DIR	ST1	ST2	ST3	Output excitation mode (Phase B 90° advance : to Phase A)
High	—	—	—	—	Output OFF
Low	High	Low	Low	Low	2 phase excitation drive (4-step sequence)
Low	High	Low	High	Low	Half-step drive (8-step sequence)
Low	High	High	Low	Low	1-2 phase excitation drive (8-step sequence)
Low	High	High	High	Low	W1-2 phase drive (16-step sequence)
Low	High	—	—	High	2W1-2 phase drive (32-step sequence)

2) Truth table (Control/Charge pump circuit)

STBY	ENABLE	Control /Charge pump circuit	Output transistor
Low	—	OFF	OFF
High	High	ON	OFF
High	Low	ON	ON

3) Truth table (PWM OFF period selection)

PWMSW	PWM OFF period
Low	28.0 µs
Middle	15.2 µs
High	8.1 µs

4) Truth table (Decay selection)

DECAY1	DECAY2	Decay control
Low	Low	Slow Decay
Low	High	25%
High	Low	50%
High	High	100%

5) Truth table (Test mode)

TEST	TJMON
Low	VBE monitor
Middle	Test output (Output transistor : OFF)
High	Home Position output

Note) For each PWM OFF period, Fast Decay is applied according to the above table.

OPERATION (continued)

2. Each phase current value

1) 1-2 phase, W1-2 phase, 2W1-2 phase DIR = Low

Note) The definition of Phase A and B current "100%" : (VREF × 0.1) / Current detection resistance

1-2 phase (8 Step)	W1-2 phase (16 Step)	2W1-2 phase (32 Step)	Phase A current (%)	Phase B current (%)
		1	19.5	–98.1
	1	2	38.3	–92.4
		3	55.6	–83.2
1	2	4	70.7	–70.7
		5	83.2	–55.6
	3	6	92.4	–38.3
		7	98.1	–19.5
2	4	8	100	0
		9	98.1	19.5
	5	10	92.4	38.3
		11	83.2	55.6
3	6	12	70.7	70.7
		13	55.6	83.2
	7	14	38.3	92.4
		15	19.5	98.1
4	8	16	0	100
		17	–19.5	98.1
	9	18	–38.3	92.4
		19	–55.6	83.2
5	10	20	–70.7	70.7
		21	–83.2	55.6
	11	22	–92.4	38.3
		23	–98.1	19.5
6	12	24	–100	0
		25	–98.1	–19.5
	13	26	–92.4	–38.3
		27	–83.2	–55.6
7	14	28	–70.7	–70.7
		29	–55.6	–83.2
	15	30	–38.3	–92.4
		31	–19.5	–98.1
8	16	32	0	–100

OPERATION (continued)

2. Each phase current value (continued)

2) 1-2 phase, W1-2 phase, 2W1-2 phase DIR = High

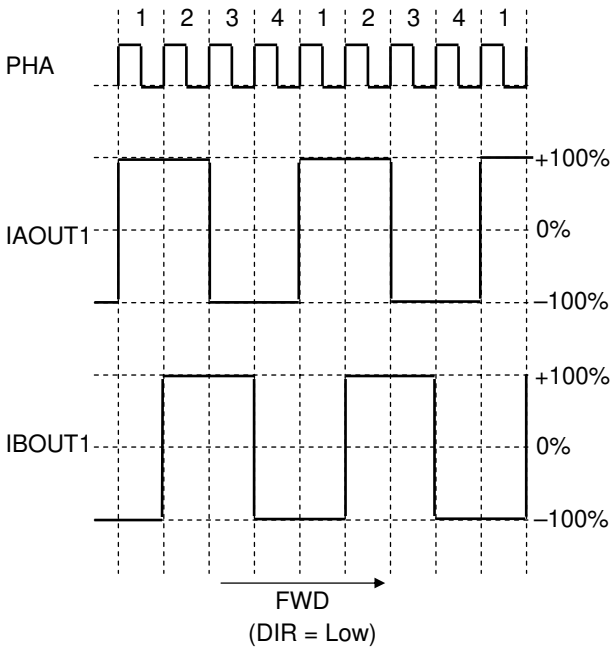
Note) The definition of Phase A and B current "100%" : (VREF × 0.1) / Current detection resistance

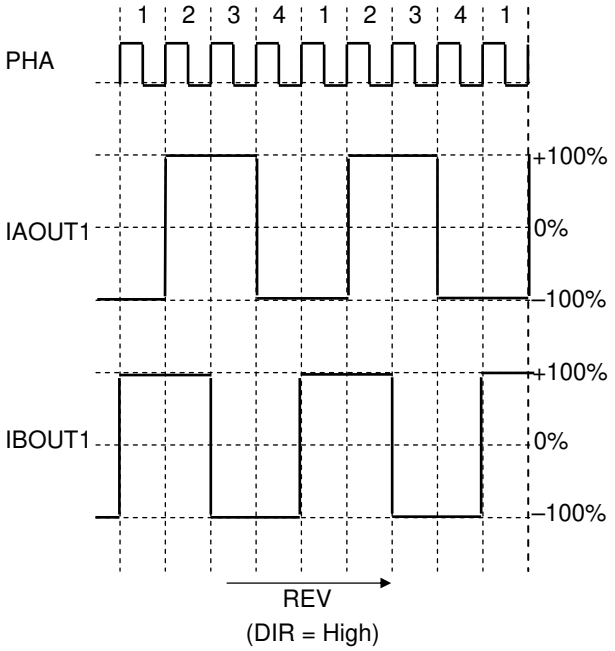
1-2 phase (8 Step)	W1-2 phase (16 Step)	2W1-2 phase (32 Step)	Phase A current (%)	Phase B current (%)
		1	–19.5	–98.1
	1	2	–38.3	–92.4
		3	–55.6	–83.2
1	2	4	–70.7	–70.7
		5	–83.2	–55.6
	3	6	–92.4	–38.3
		7	–98.1	–19.5
2	4	8	–100	0
		9	–98.1	19.5
	5	10	–92.4	38.3
		11	–83.2	55.6
3	6	12	–70.7	70.7
		13	–55.6	83.2
	7	14	–38.3	92.4
		15	–19.5	98.1
4	8	16	0	100
		17	19.5	98.1
	9	18	38.3	92.4
		19	55.6	83.2
5	10	20	70.7	70.7
		21	83.2	55.6
	11	22	92.4	38.3
		23	98.1	19.5
6	12	24	100	0
		25	98.1	–19.5
	13	26	92.4	–38.3
		27	83.2	–55.6
7	14	28	70.7	–70.7
		29	55.6	–83.2
	15	30	38.3	–92.4
		31	19.5	–98.1
8	16	32	0	–100

OPERATION (continued)

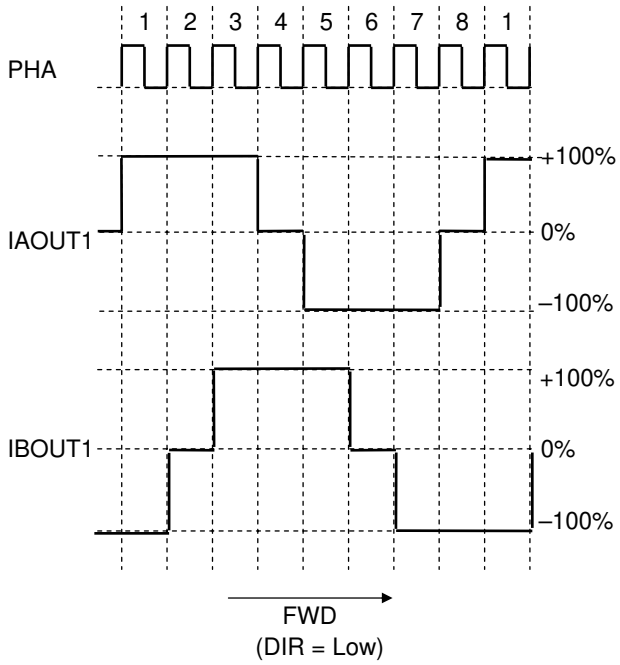
3. Each phase current (Timing chart)

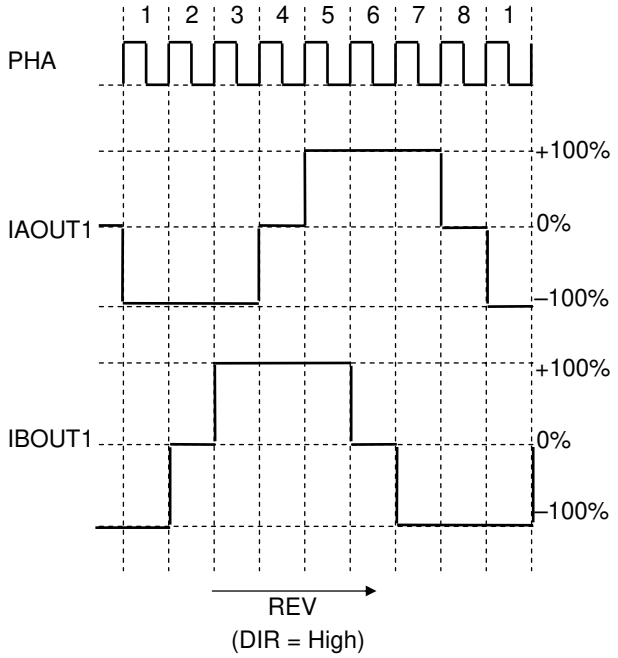
1) 2 phase excitation drive (4-step sequence)
(ST1 = Low, ST2 = Low, ST3 = Low)





2) Half-step drive (8-step sequence)
(ST1 = Low, ST2 = High, ST3 = Low)

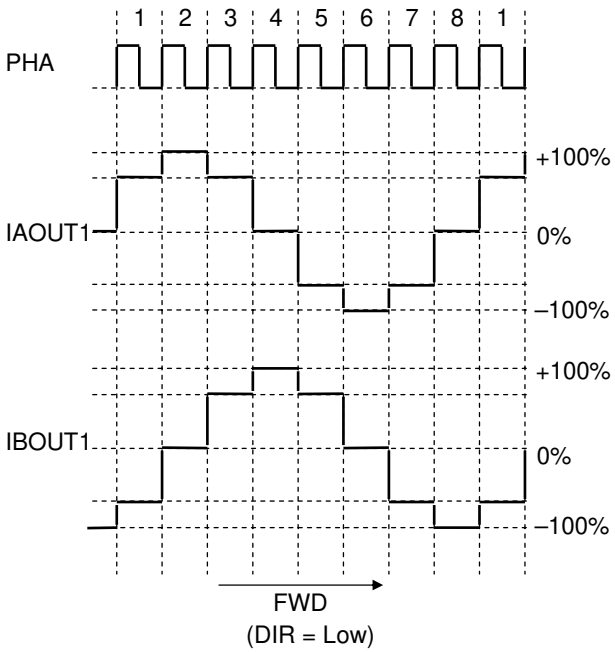


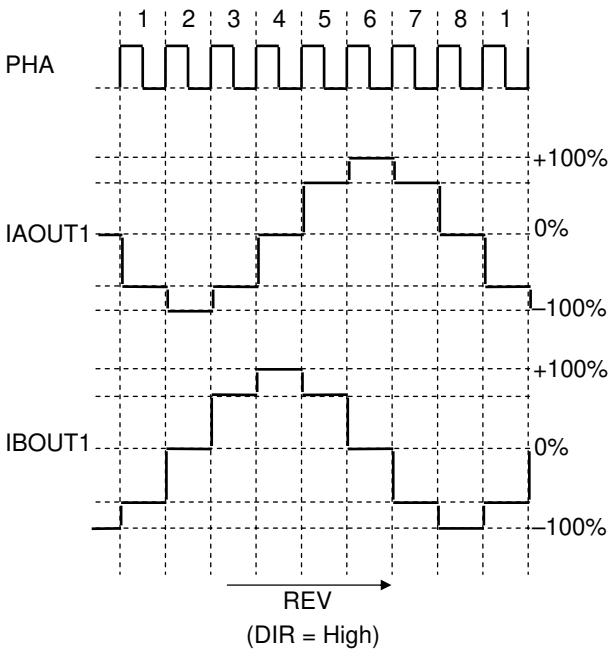


OPERATION (continued)

3.Each phase current (Timing chart) (continued)

3) 1-2 phase excitation (8-step sequence)
(ST1 = High, ST2 = Low, ST3 = Low)

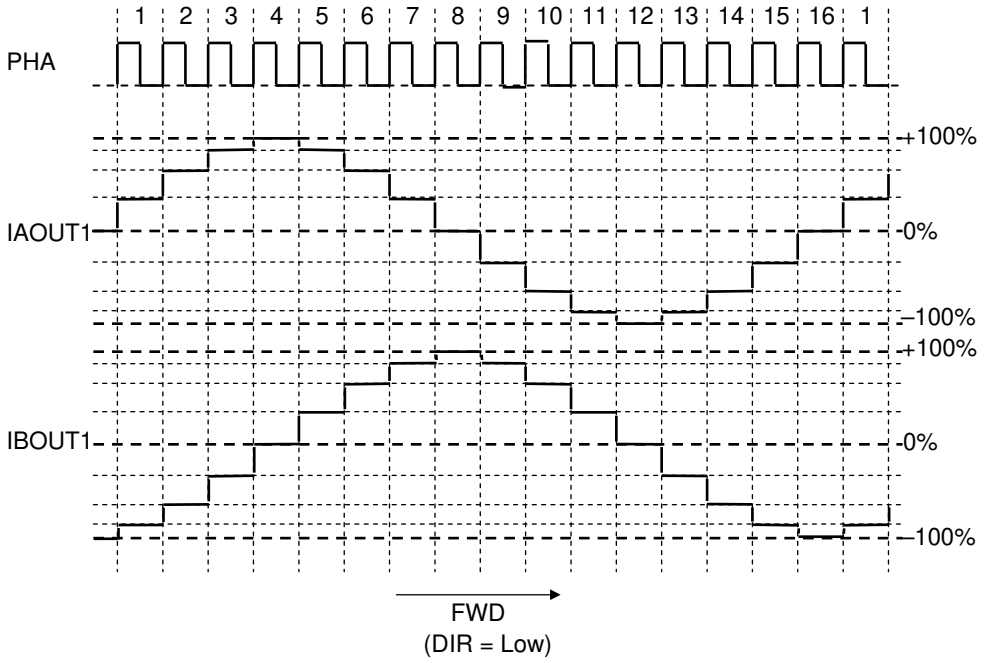


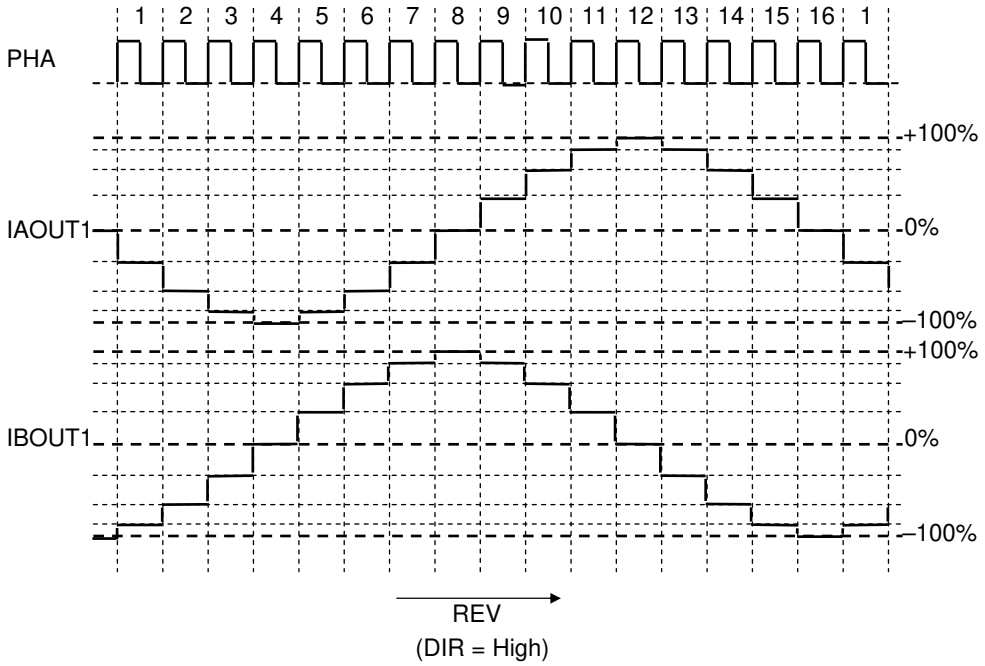


OPERATION (continued)

3.Each phase current (Timing chart) (continued)

4) W1-2 phase excitation (16-step sequence)
(ST1 = High, ST2 = High, ST3 = Low)

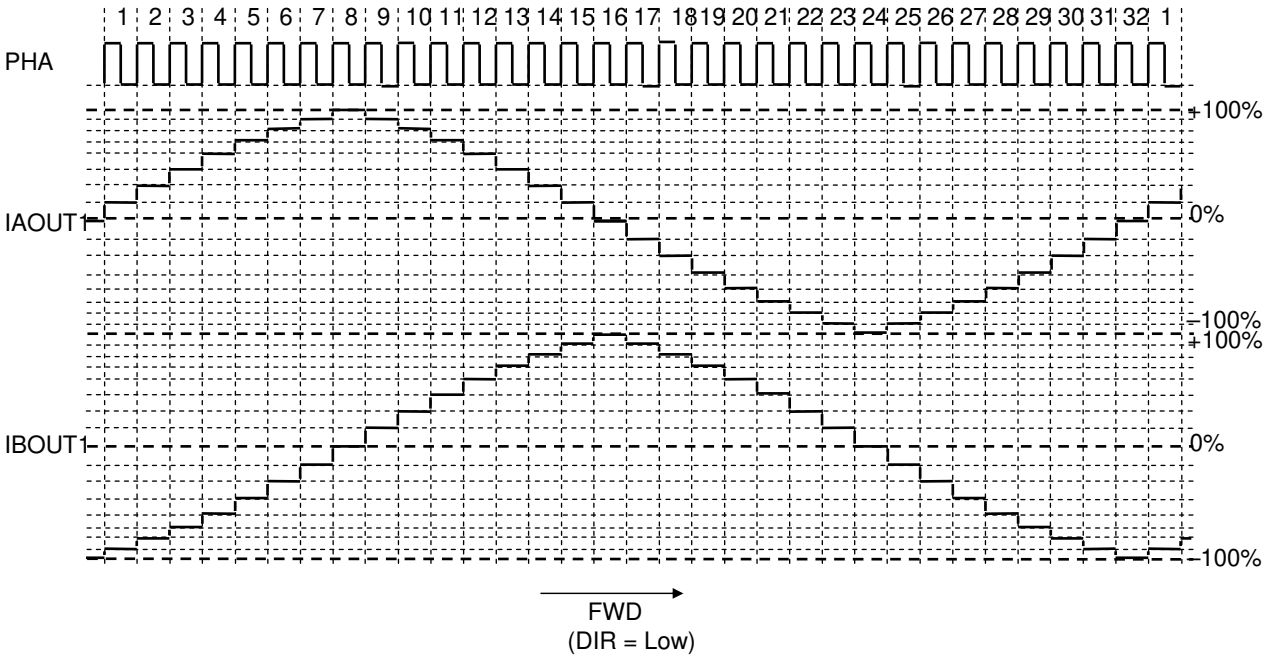


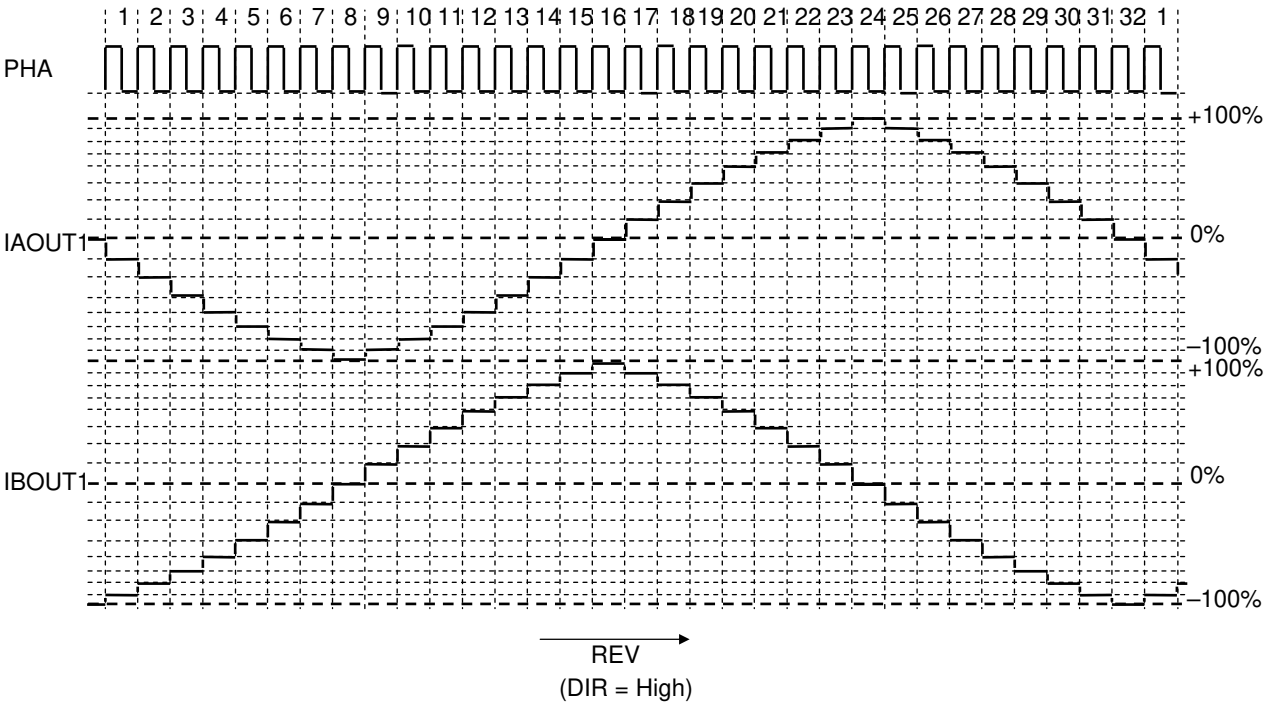


OPERATION (continued)

3.Each phase current (Timing chart) (continued)

5) 2W1-2 phase excitation (32-step sequence)
(ST3 = High)

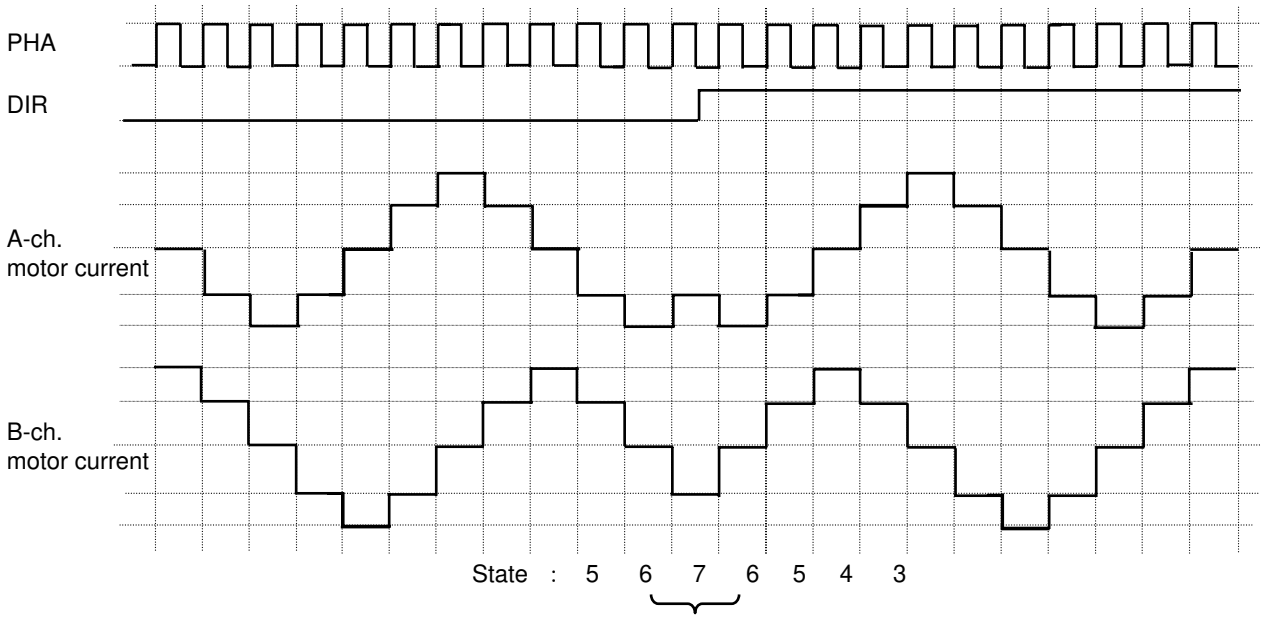




OPERATION (continued)

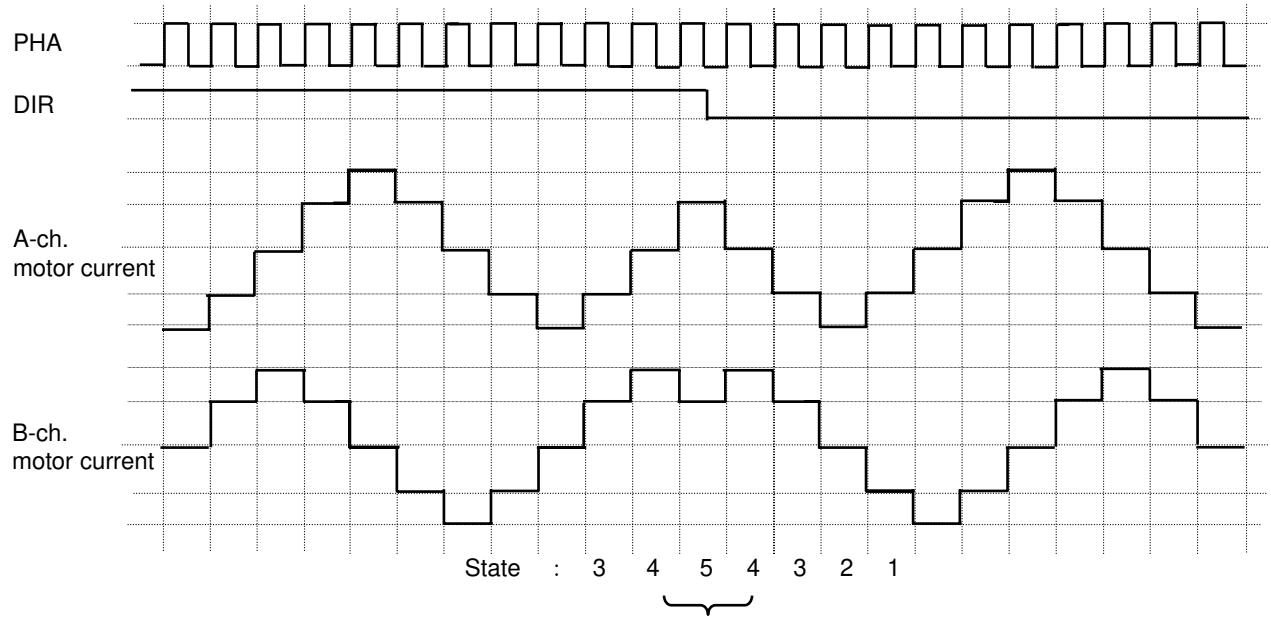
4.Timing chart at change of DIR

(Ex.1) Timing chart at 1-2 phase excitation (DIR : Low → High)



At change of DIR, the state before the change is held and the operation is continued.

(Ex.2) Timing chart at 1-2 phase excitation (DIR : High → Low)



At change of DIR, the state before the change is held and the operation is continued.

OPERATION (continued)

5.Home Position function

This LSI has built-in Home Position function to reduce the displacement of motor current state at change of excitation mode while a motor is driving.

Home Position function , following as the below chart, outputs Low-level voltage to TJMON pin at the timing when the displacement of motor current state is minimum at change of excitation mode in case of TEST = High-level input.

At other timing, Home Position function outputs High-level voltage (in case the pull-up resister (recommendation : 100 kΩ to 5 V) is connected because TJMON pin is made with open drain) at TJMON pin.

1) Home Position output timing chart (DIR = Low)

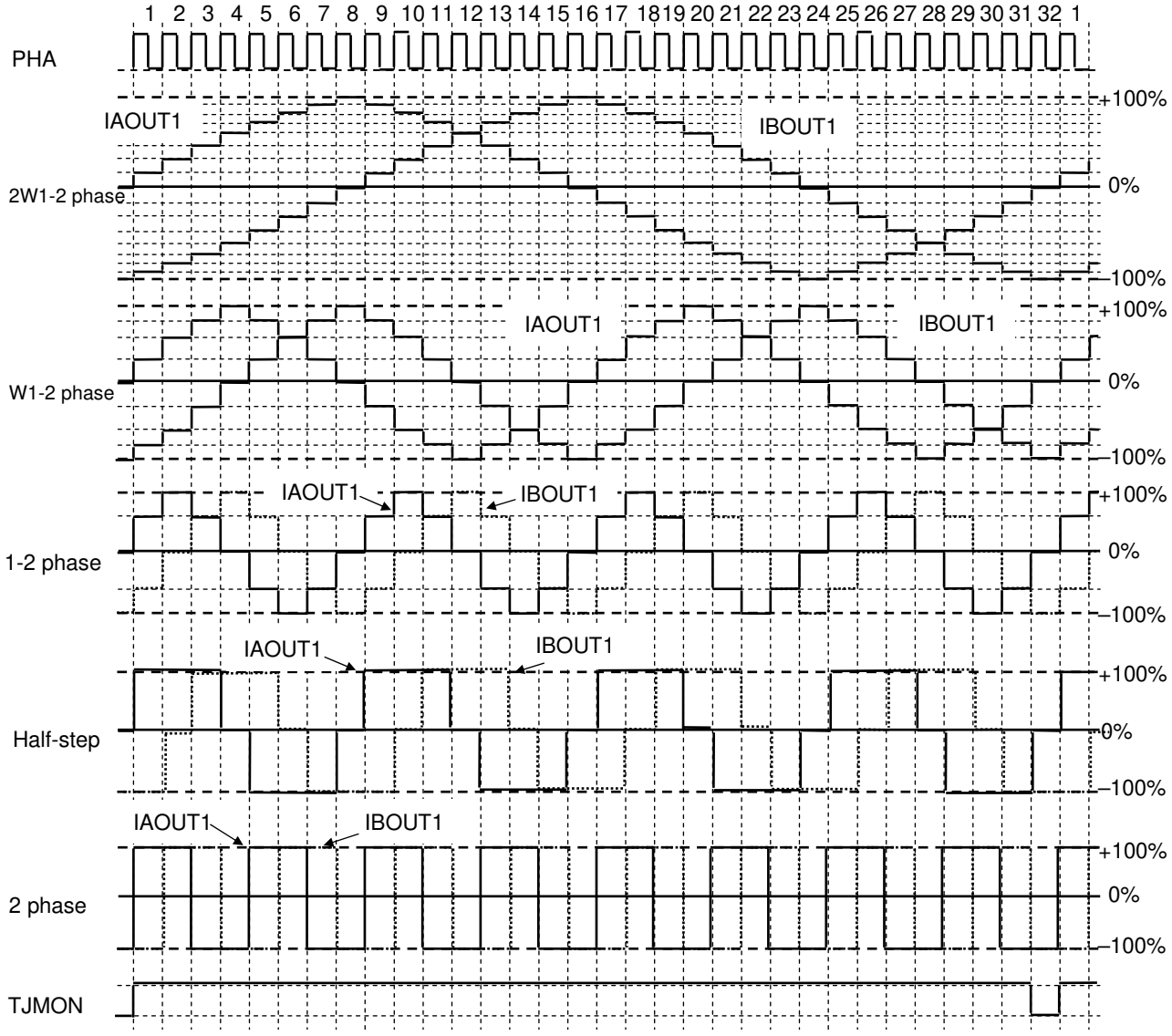


Table Output current of each excitation mode at Home Position = Low (DIR = Low)

	2 phase excitation	Half-step	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation
Phase A current	–100%	0%	0%	0%	0%
Phase B current	–100%	–100%	–100%	–100%	–100%

OPERATION (continued)

5.Home Position function（continued）

2) Home Position output timing chart (DIR = High)

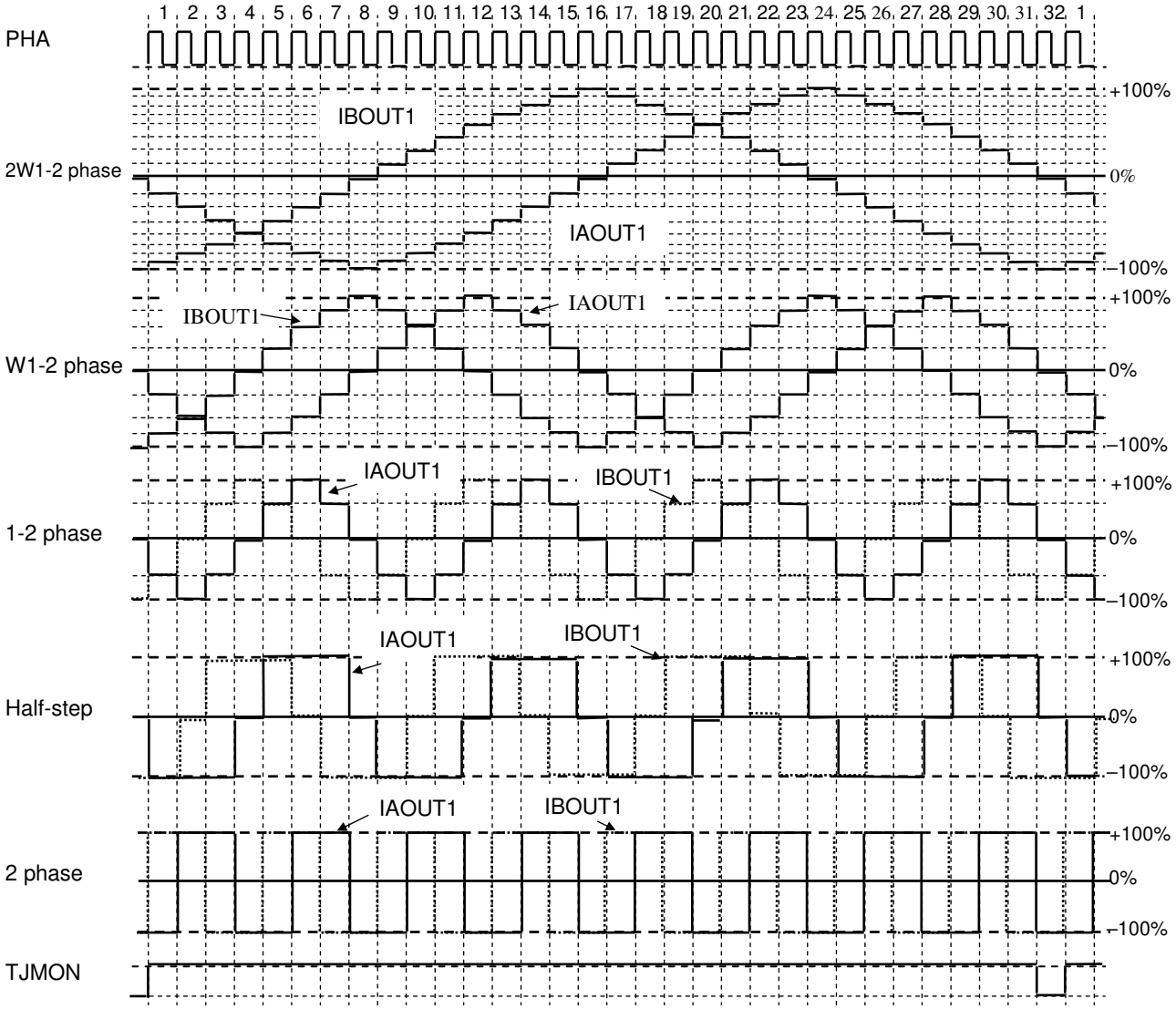


Table Output current of each excitation mode at Home Position = Low (DIR = High)

	2 phase excitation	Half-step	1-2 phase excitation	W1-2 phase excitation	2W1-2 phase excitation
Phase A current	–100%	0%	0%	0%	0%
Phase B current	–100%	–100%	–100%	–100%	–100%

APPLICATIONS INFORMATION

1. Notes

1) Pulse blanking time
This LSI has pulse blanking time (0.7 µs/Typ. value) to prevent erroroneous current detection caused by noise. Therefore, the motor current value will not be less than current determined by pulse blanking time. Pay attention at the time of minimum current control.
The relation between pulse blanking time and minimum current value is shown as Chart 1.
In addition, increase-decrease of motor current value is determined by L value, wire wound resistance, induced voltage and PWM on Duty inside a motor.

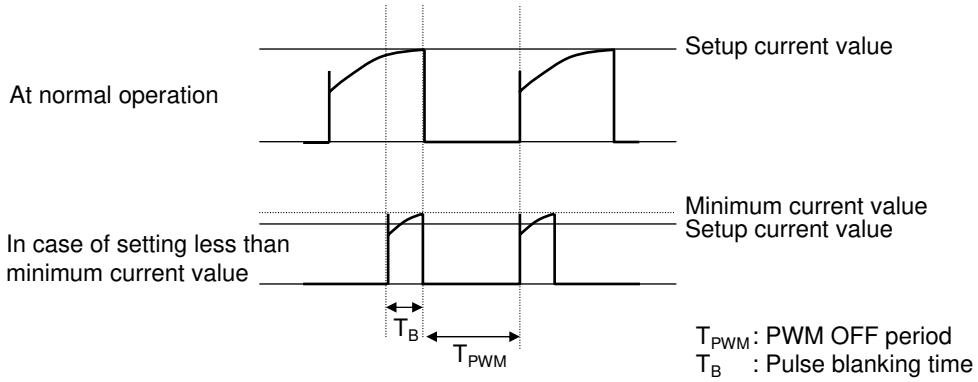


Chart 1. RCS current waveform

2) VREF voltage
When VREF voltage is set to Low-level, erroroneous detection of current might be caused by noise because threshold of motor current detection comparator becomes low (= VREF/10 × motor current ratio [%]).
Use this LSI after confirming no misdetection with setup REF voltage.

3) Notes on interface
Absolute maximum of Pin 19 to Pin 23 and Pin 28 to Pin 33 is –0.3 V to 6 V. When the setup current for a motor is large and lead line of GND is long, GND pin potential might rise. Take notice that interface pin potential is negative to difference in potential between GND pin reference and interface pin in spite of inputting 0 V to the interface pin. At that time, pay attention allowable voltage range must not be exceeded.

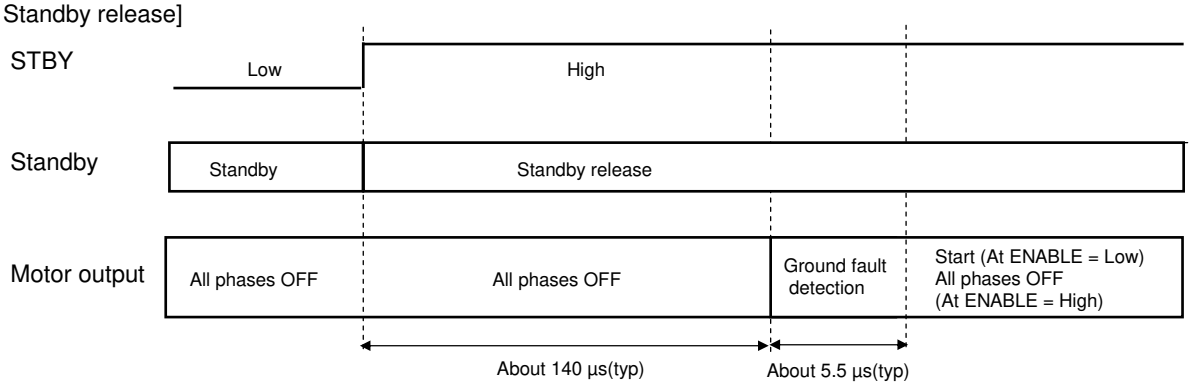
4) Notes on test mode
When inputting voltage of above 0.6 V and below 4.0 V to TEST (Pin 25), this LSI might become test mode. When disturbance noise etc. makes this LSI test mode, motor output pin might be Hi-Z. Therefore, use this LSI on condition that TEST pin is shorted to GND or S5VOUT at normal motor operation.

APPLICATIONS INFORMATION (continued)

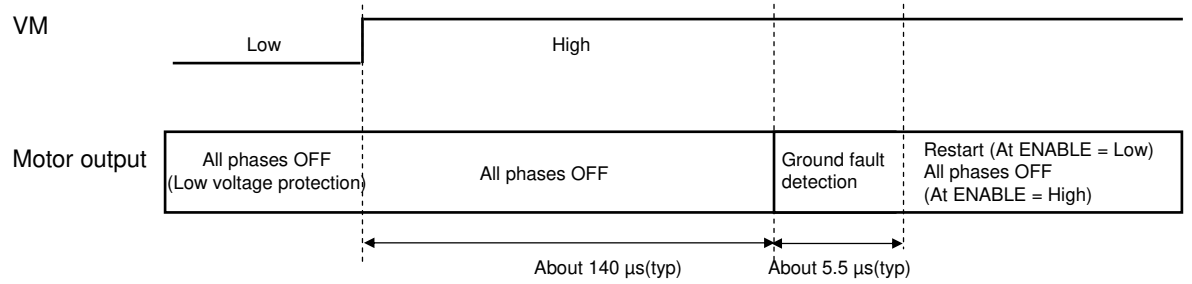
1. Notes (continued)

5) Notes on Standby mode release / Low voltage protection release
This LSI has all phases OFF period of about 140 µs (typ) owing to release of Standby and Low voltage protection (Refer to the below figure).
This is why restart from Standby and Low voltage protection is performed after booster voltage rises sufficiently because booster operation stops at Standby and Low voltage protection.
When the booster voltage does not rise sufficiently during all phases OFF period due to that capacitance voltage between VPUMP and GND becomes large etc., the LSI might overheat. In this case, release Standby and Low voltage protection at ENABLE = High-level, and restart at ENABLE = Low-level after the booster voltage rises sufficiently.
Moreover, take notice that state of motor current becomes default position at Standby and Low voltage protection operation following as 1. Notes No.8.

[At Standby release]



[At Low voltage protection release]



6) Ground fault protection function
This LSI has built-in ground fault protection function to detect ground fault of motor output pin at board mounting.
As the above figure, ground fault detection function will operate after release of Low voltage protection and Standby, and check ground fault of motor output pins. If ground fault is detected, this function makes motor output all phases OFF and motor operation stop.
If ground fault is not detected, this function makes motor start. However, take notice that LSI might be destroyed before ground fault protection function operates in case that ASO (Area of Safe Operation) of device or maximum rating are exceeded in a moment.
In addition, this function might not detect ground fault when starting VM at STBY = High-level. It is recommended that VM is started at STBY = Low-level.
In case of release of ground fault detection, restart LSI after inputting low voltage to STBY pin or making VM voltage OFF.

7) Notes on release of thermal protection
The release of thermal protection operation will restart after all phases OFF of about 140 µs and ground fault detection operation as 1. Notes No.5, 6.
Moreover, take notice that the state of motor current will become default position after release of thermal protection operation as 1. Notes No.8

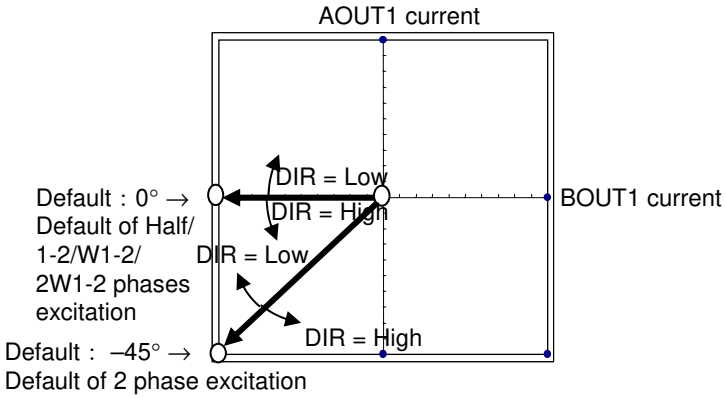
APPLICATIONS INFORMATION (continued)

1. Notes (continued)

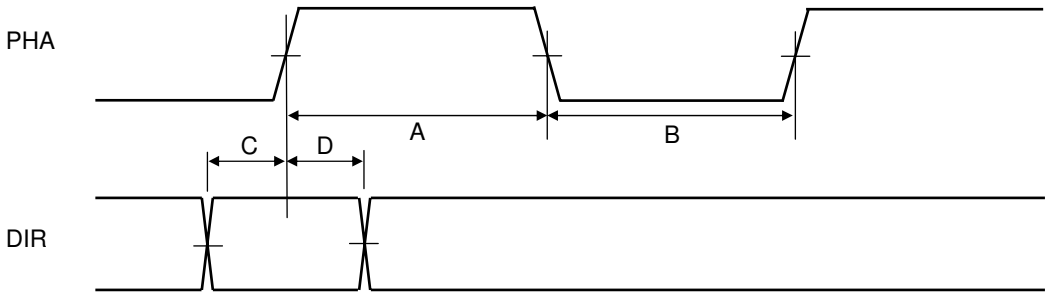
8) Default of motor current state
Default of motor current follows as the below figure after release of Low voltage protection, Standby and thermal protection on each excitation mode.

Table default position of each excitation mode

Excitation mode	Default electrical angle
2 phase excitation (4 step)	– 45°
Half-step (8 step)	0°
1-2 phase excitation (8 step)	0°
W1-2 phase excitation (16 step)	0°
2W1-2 phase excitation (32 step)	0°



9) PHA input signal and DIR input signal
The set/hold time of PHA and DIR input signals, PHA input minimum pulse width (High/Low) are shown as the below figure.
Input signals after securing set/hold time.



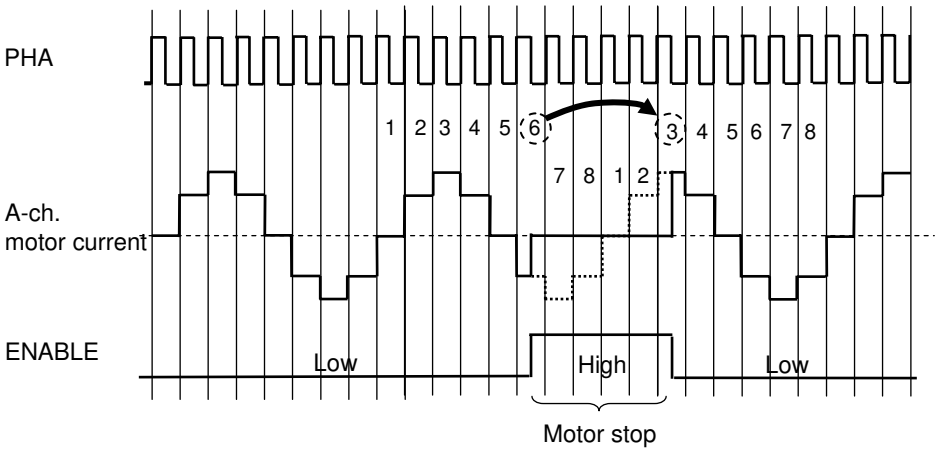
Period	Contents	Time
A	PHA input minimum pulse width (High)	5 µs or more
B	PHA input minimum pulse width (Low)	5 µs or more
C	DIR set time	2 µs or more
D	DIR hold time	2 µs or more

APPLICATIONS INFORMATION (continued)

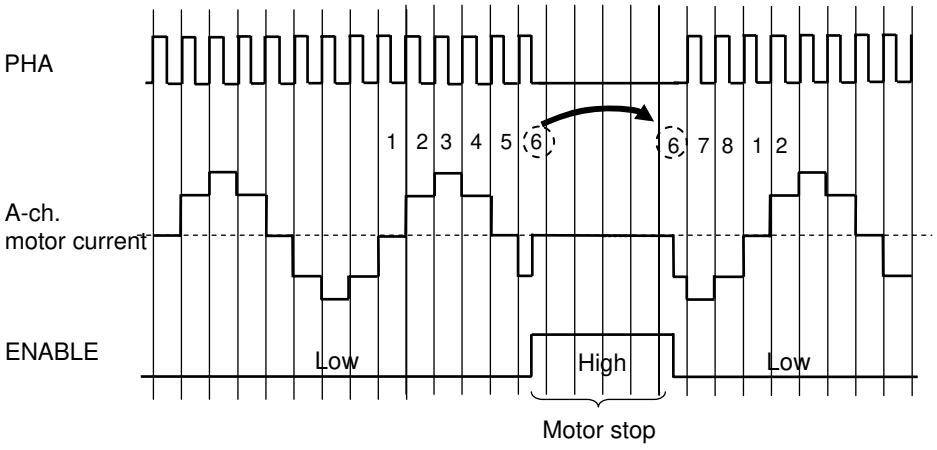
1.Notes (continued)

10) PHA input at ENABLE = High
As the below figure (Ex. 1-2 phase excitation), when inputting PHA at the time of motor stop and ENABLE = High (All phases are OFF → Motor current = 0 A), the setup value of motor current will proceed at PHA input. Therefore, in case of restart at ENABLE = Low, take notice that the position of restart is where the current state just before motor stop gains PHA input.

Ex.) 1-2 phase excitation



In spite of stop at state[6] , because PHA is input at ENABLE = High, the motor will restart after ENABLE = Low at state [3].

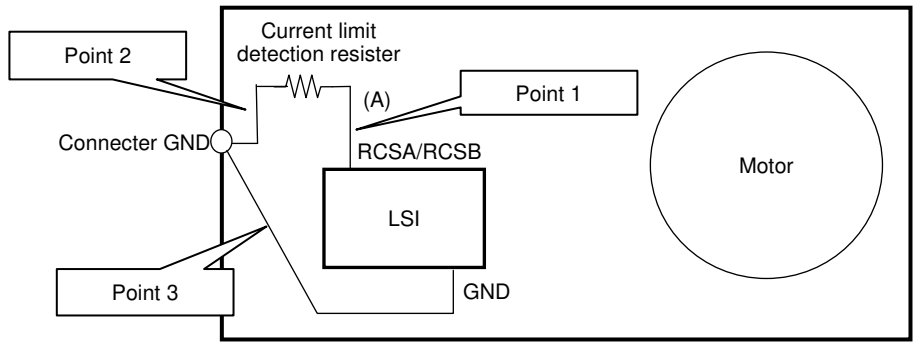


In spite of stop at state [6] , because PHA is not input at ENABLE = High, the motor will restart after ENABLE = Low at state [6] just before stop.

APPLICATIONS INFORMATION (continued)

1. Notes (continued)

11) Notes on RCS line
Take consideration in the below figure and the points and design PCB pattern.
(1) Point 1
Design so that the wiring to the current detection pin (RCSA/RCSB pin) of this LSI is thick and short to lower impedance. This is why current can not be detected correctly owing to wiring impedance and current might not be supplied to a motor sufficiently.
(2) Point 2
Design so that the wiring between current detection resister and connecter GND (the below figure Point 2) is thick and short to lower impedance. As the same as Point 1, sufficient current might not be supplied due to wiring impedance. In addition, if there is a common impedance on the side of GND of RASA and RCSB, peak detection might be erroroneous detection. Therefore, install the wiring on the side of GND of RCSA and RCSB independently.
(3) Point 3
Connect GND pin of this LSI to the connecter on PCB independently. Separate the wiring removed current detection resister of large current line (Point 2) from GND wiring and make these wirings one-point shorted at the connecter as the below figure. That can make fluctuation of GND minimum.



12) A high current flows into the LSI. Therefore, the common impedance of PCB can not be ignored. Take the following points into consideration and design the PCB pattern for a motor. Because the wiring connecting to VM1 (Pin 17) and VM2 (Pin 1)of this LSI is high-current, it is easy to generate noise at time of switching by wiring L. That might cause malfunction and destruction (Figure 2). As Figure 3, the escape way of the noise is secured by connecting a capacitor to the connector close to the VM pin of the LSI. This makes it possible to suppress the fluctuation of direct VM pin voltage of the LSI. Make the setting as shown in Figure 3 as much as possible.

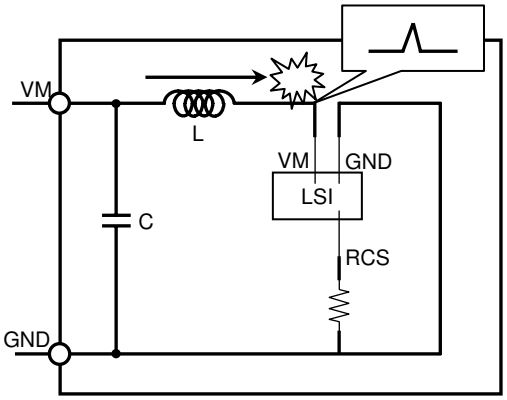


Figure 2. No recommended pattern

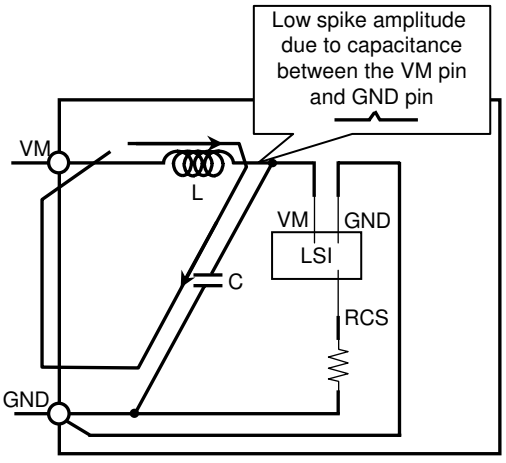


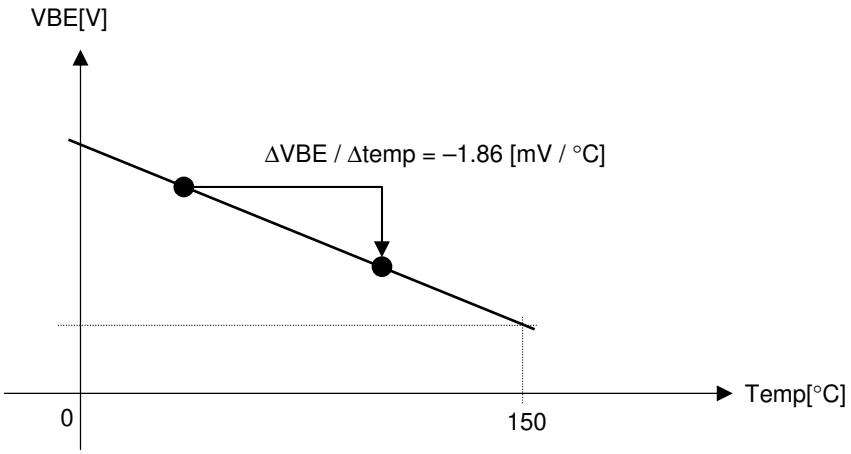
Figure 3. Recommended pattern

APPLICATIONS INFORMATION (continued)

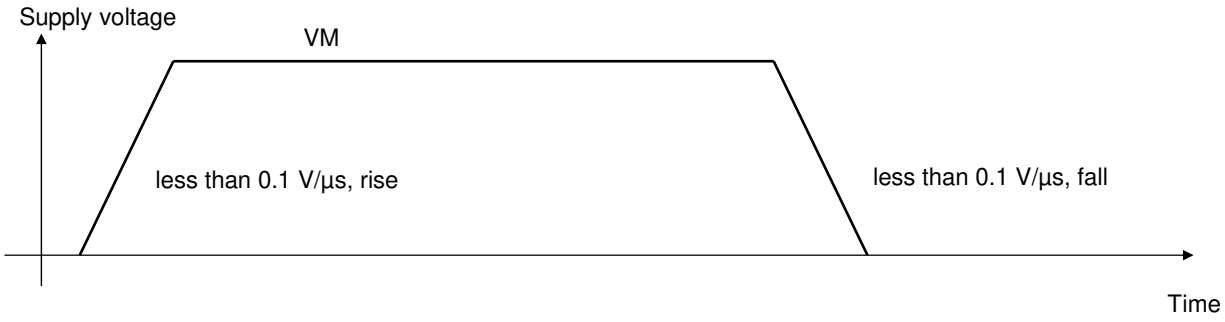
1. Notes (continued)

13) LSI junction temperature
In case of measuring chip temperature of this LSI, measure the voltage of TJMON pin (Pin 3) and estimate the chip temperature from the data below. However, because this data is technical reference data, conduct a sufficient reliability test of the LSI and evaluate the product with the LSI incorporated.

TJMON pin temperature characteristics

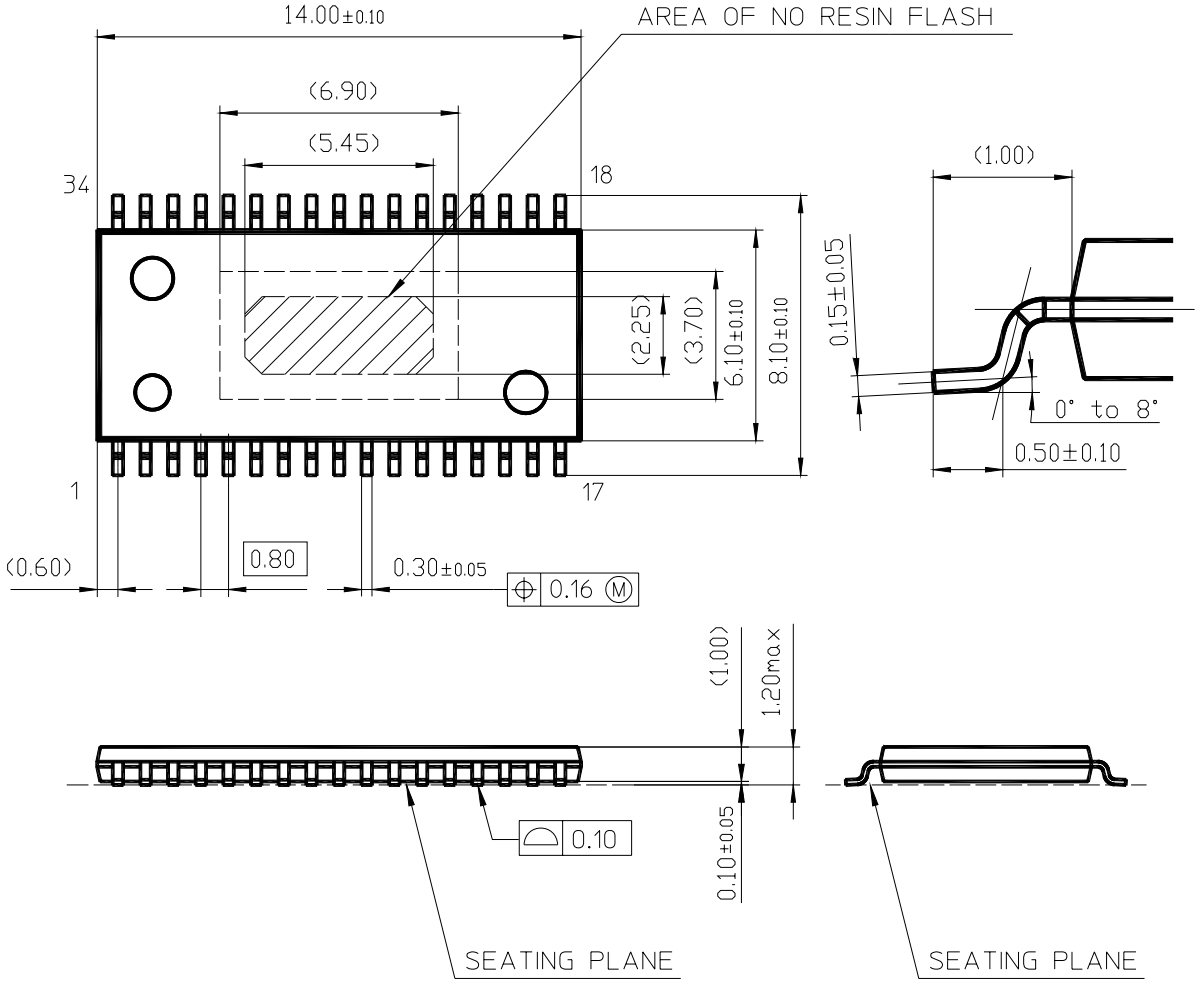


14) Speed of supply and cut of power
When supplying to VM pin (Pin 1, 17) , set the rise speed of VM voltage to less than 0.1 V/µs and fall speed to less than 0.1 V/µs. If the speed of rise and fall of power supply is too rapid, that might cause malfunction and destruction of the LSI. In this case, conduct a sufficient reliability test and also check a sufficient evaluation for a product.



PACKAGE INFORMATION (Reference Data)

Package Code:HSOP034-P-0300A unit:mm



Body Material	:	Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	Pd Plating